Laboratoire des Systèmes Intégrés (Integrated Systems Laboratory)

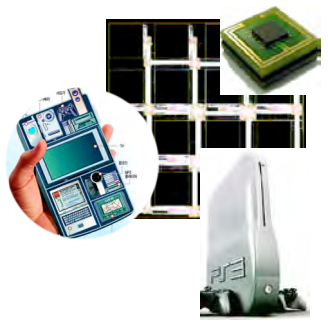
Research Activities

Dr. David Atienza
Prof. Giovanni De Micheli

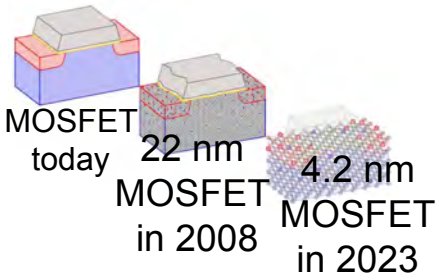
RWTH Aachen – EPFL Joint Research Meeting

Research Projects (1/2)

- System-on-Chip Consumer Electronics
  - Networks-on-Chip (NoC) interconnects
  - Thermal modeling SoCs

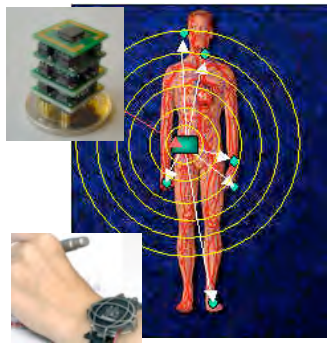


- Reliable Nano-Scale Circuits
  - Efficient addressing schemes (micro/nano)
  - Circuit-level defect modeling and reliable CAD tools

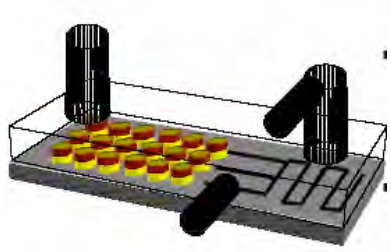


Research Projects (2/2)

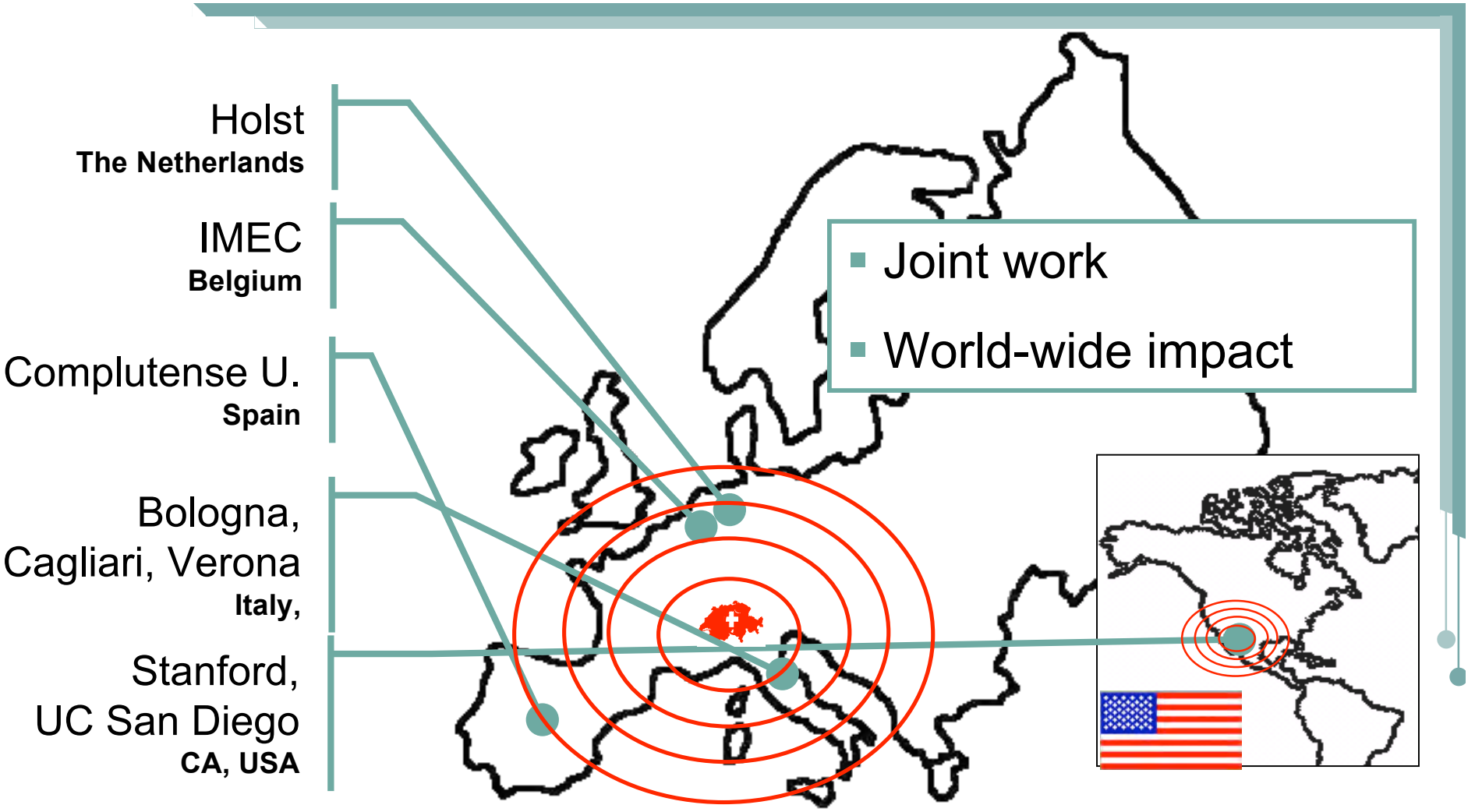
- Wireless Sensor Networks (WSNs)
  - Power-efficient communication protocols
  - Modeling of working conditions of nodes
  - Self-maintained (scavenging mechanisms)



- Lab-on-Chip
  - Integration of bio-electro- mechano- opto-systems
  - *Point of care* medical devices
  - Implanted health monitoring devices



World-Wide Partners and Influence



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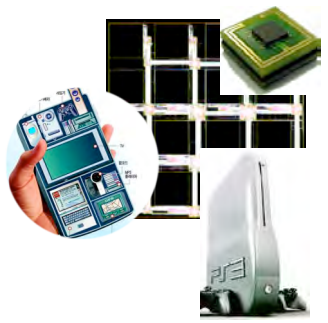

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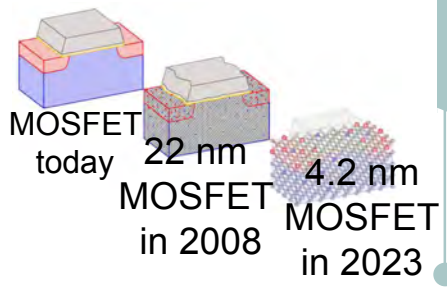
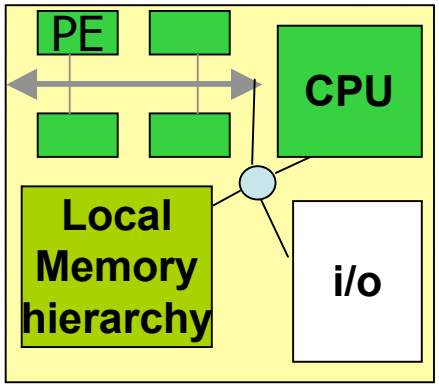
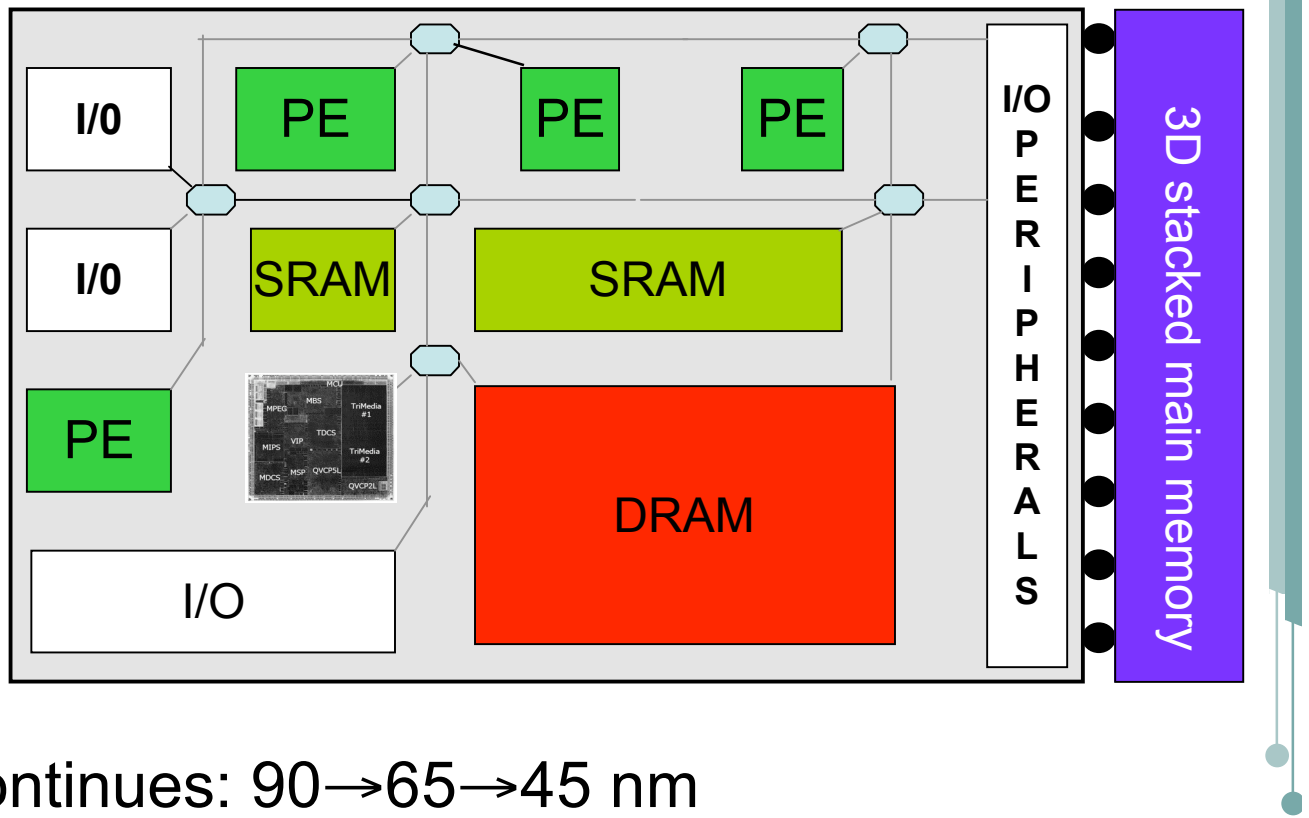


Consumer SoCs: Architecture Evolution

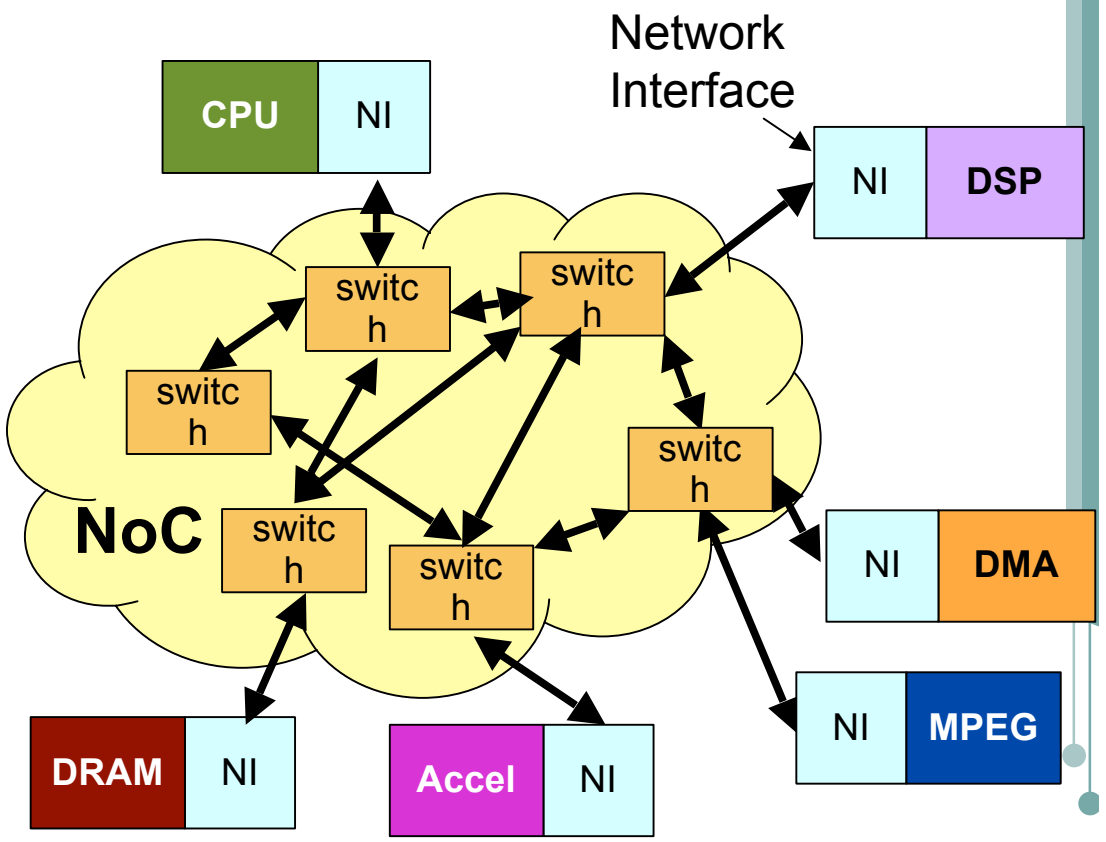




- Roadmap continues: 90→65→45 nm
- “Traditional” Bus-based SoCs fit in one tile !!
- Communication demands: unevenly distributed, because of architectural heterogeneity

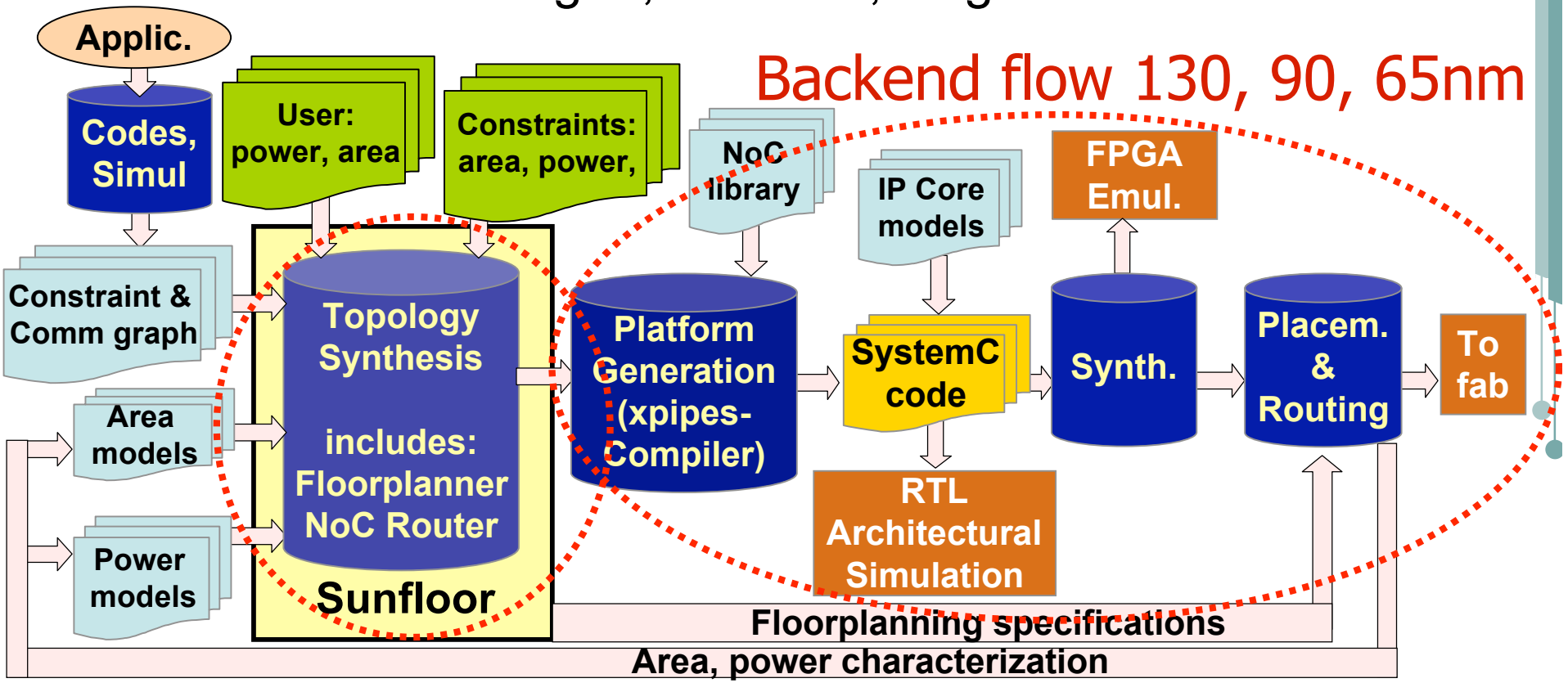
Networks-on-Chip (NoC) Interconnects

- Clean separation at session layer
  - Cores issue end-to-end transactions
  - NI deals with transport, network, link, physical
- Modularity at HW level: only 2 building blocks
  - Network interface
  - Switch (router)
- Physical design aware (floorplan global routing)

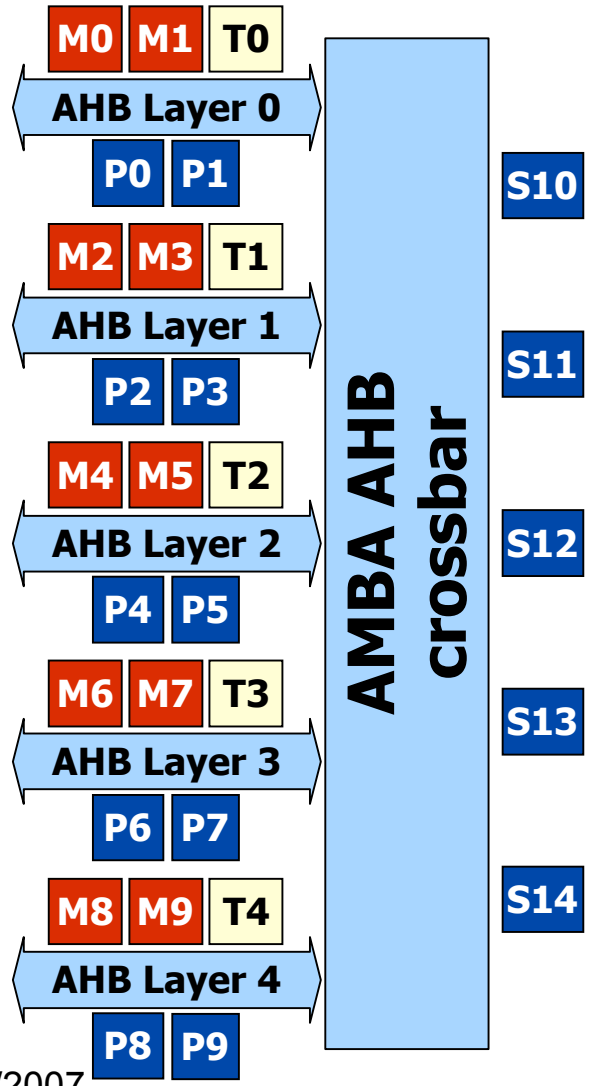


Complete NoC-Based EDA Flow

- Participants:
  - F. Angiolini, A. Pulini, Dr. S. Murali, Dr. D. Atienza, Prof. L. Benini, Prof. G. de Micheli
- Partners: Bologna, Stanford, Cagliari.

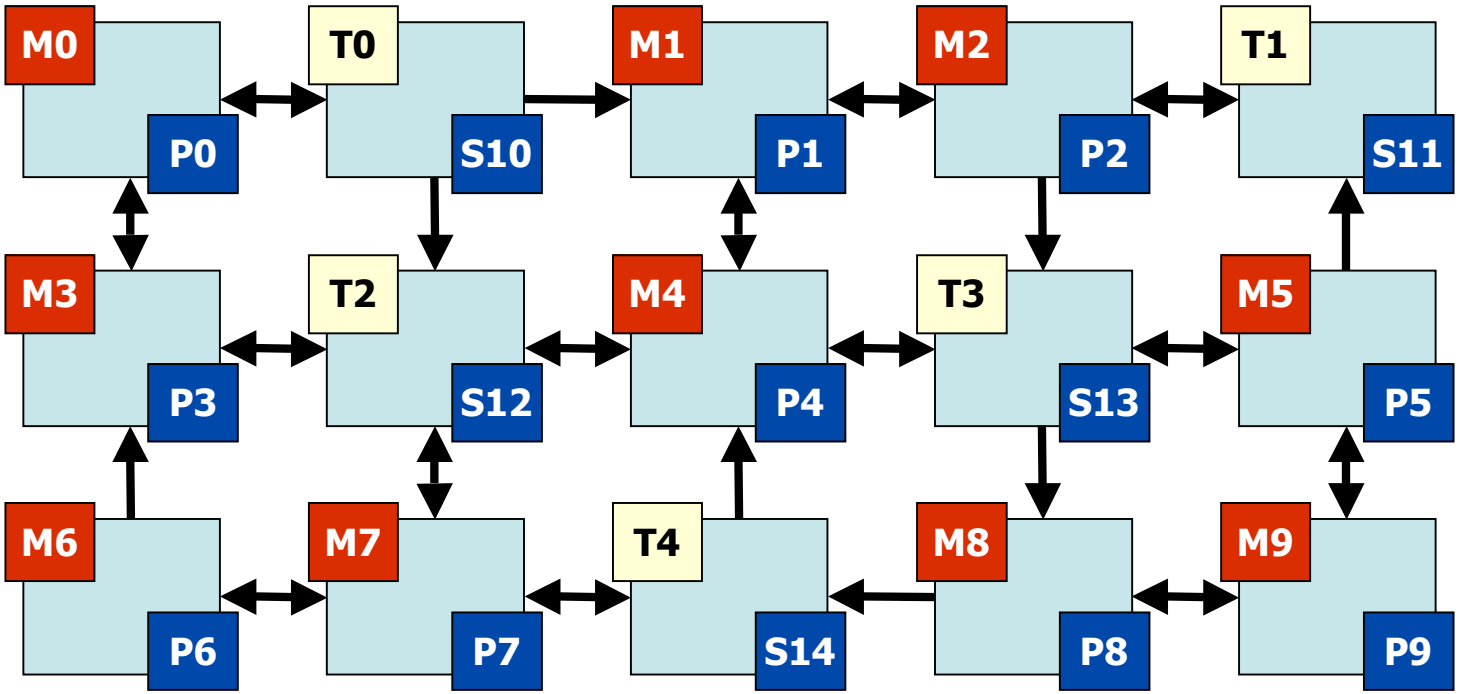


Case study 130nm: AMBA AHB Multilayer



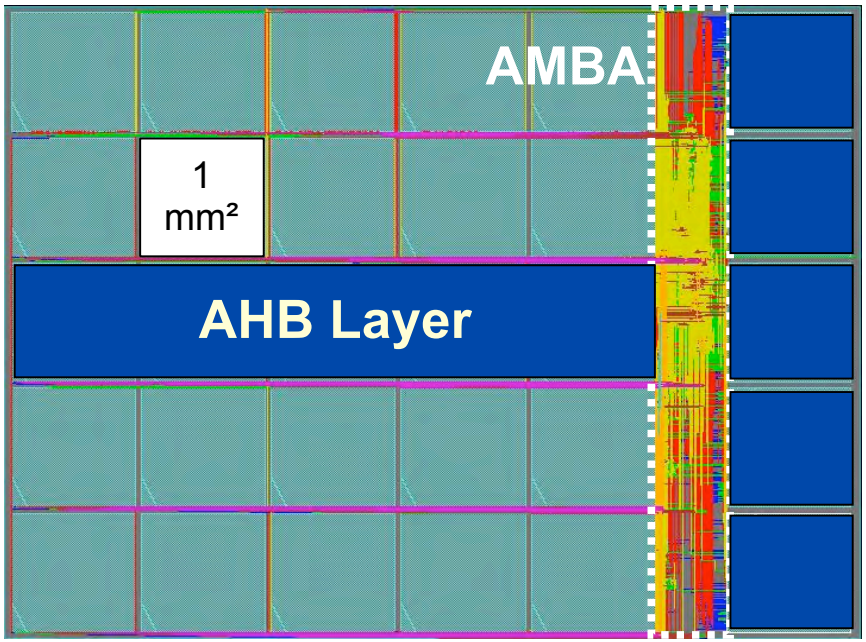
- Realistic 130nm SoC (10 cores, 5 accelerators, 15 mem. slaves)
- Shared bus fully saturated!
- Multilayer solution required for performance:
  - Intra-cluster traffic to private slaves (P0-P9) is bound within each layer, reducing congestion
  - Shared slaves (S10-S14) can be accessed in parallel
- Representative 5x5 Multilayer configuration (up to 8x8)
- Synthesized for max frequency

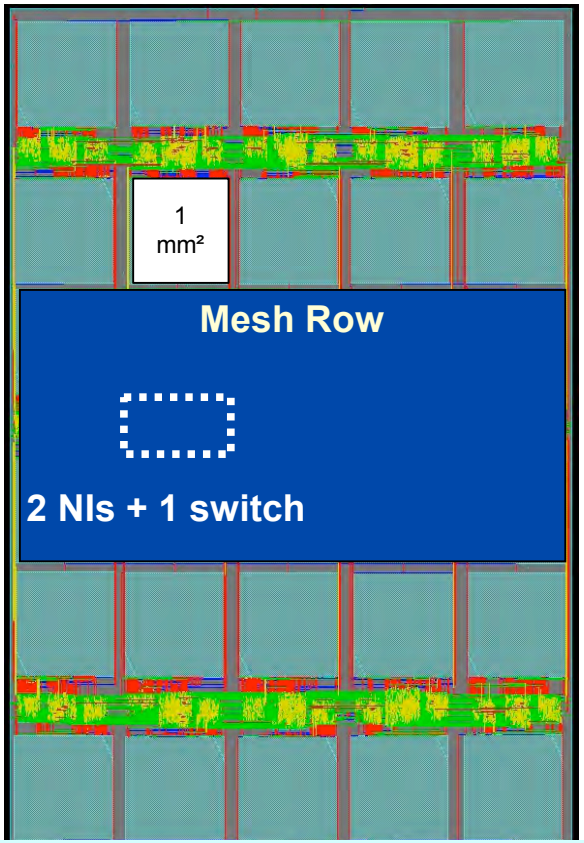
NoC solution: Quasi-Mesh



- Uni- Bi-directional links: balanced, no bottlenecks
- Custom, but almost regular topology: easy to floorplan
- Optimally placed private slaves, scattered shared slaves
- Only 4 hours specification to layout thanks to EDA flow

AMBA vs NoC: Results in 130 nm





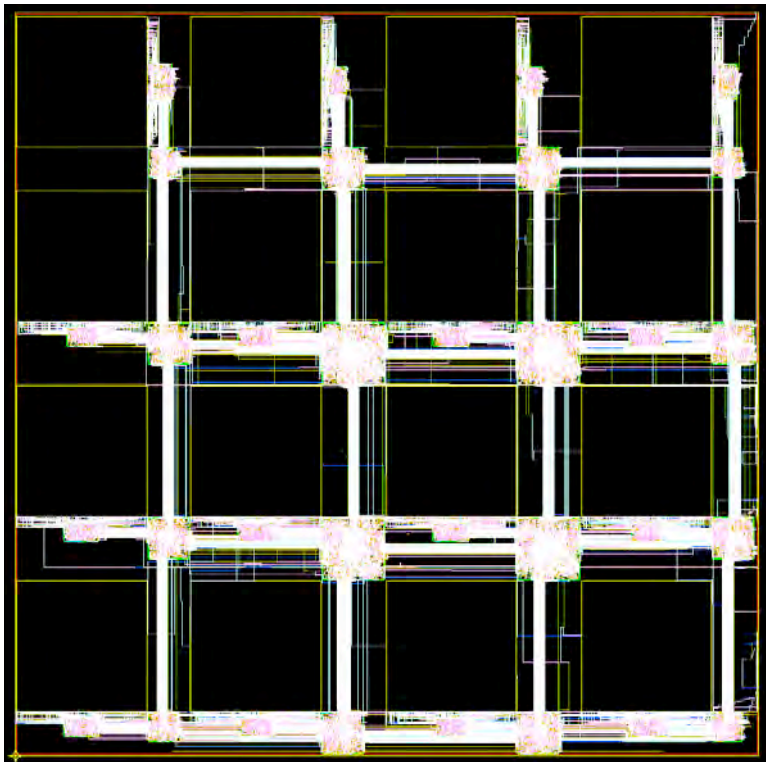
- IPs: 1mm² obstructions (ARM cores, 32kB SRAM)
- Wire routing over the cores was forbidden
- Minimum delay synthesis

Application specific NoC competitive with state-of-the-art interconnect even in 130nm using proposed EDA flow

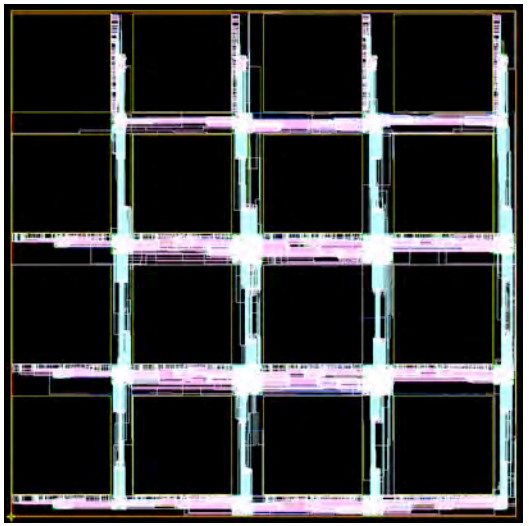
- Clock frequency 795 vs. 370 MHz post P&R → **Much faster**
- **15% avg application speedup** (longer latency, more effective bandwidth)

NoC Technology Scaling

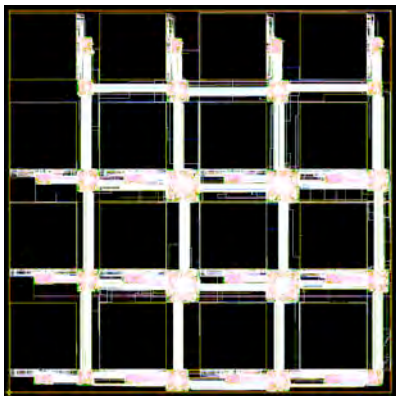
- Three designs for max frequency:



90 nm, 1 mm^2 cores



65 nm, 1 mm^2 cores



65 nm, 0.4 mm^2 cores

NoC Results in 90 and 65nm

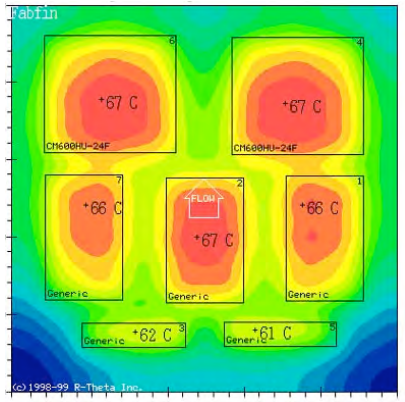
Max Frequency (38-bit links)	Max Freq.	NoC Cell Area	Power	Bandwidth
90 nm, 1 mm^2	1 GHz	1.31 mm^2	784.6 mW	228 GB/s
65 nm, 1 mm^2	1.25 GHz	0.64 mm^2	520.1 mW	285 GB/s
65 nm, .4 mm^2	1.25 GHz	0.63 mm^2	495.3 mW	285 GB/s

- Power shifting from switches/NIs to links (buffering)
  - Links always short (<1.2 mm) → **non-pipelined**
  - Power figures:
    - 90 nm 1 mm^2: 3.1 mW
    - **65 nm 1 mm^2: 3.6 mW (tightest fit → more buffering)**
    - 65 nm 0.4 mm^2: 2.2 mW

Thermal Modeling Multi-Processor SoC

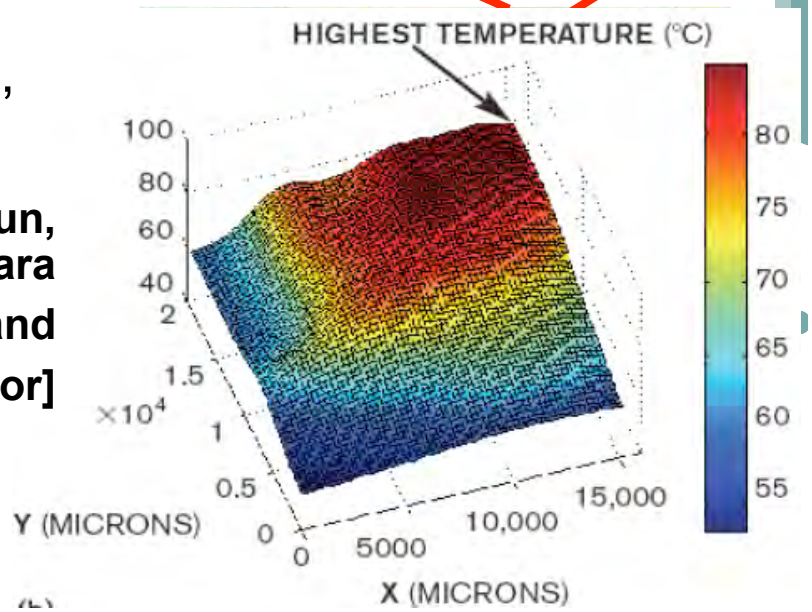
- Complex SoCs, increase power density
- Non-uniform hot-spots
- Spatial gradients: large part of chip with slower performance & leaking

[Sun, 1.8 GHz Sparc v9 Microproc]



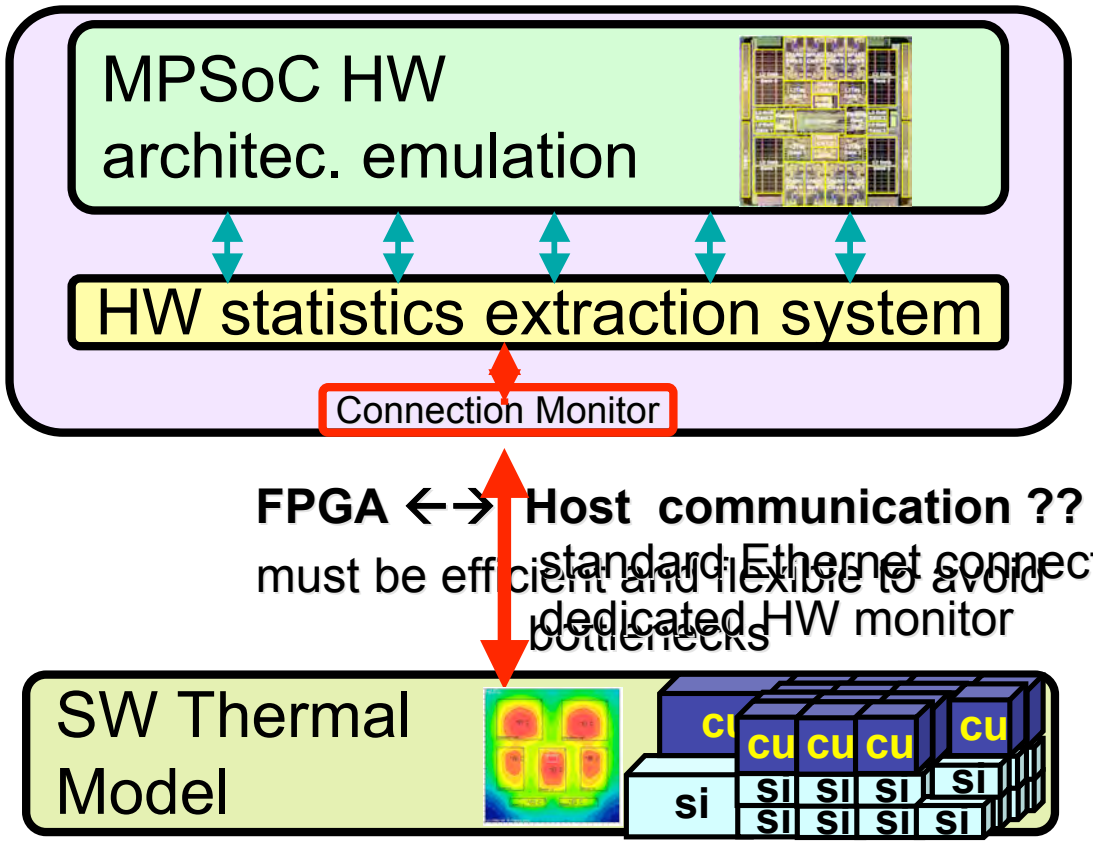
- Participants:
  - F. Mulas, M. Buttu, M. Pittau, P. Valle, Prof. S. Carta, Prof. A. Acquaviva, Dr. D. Atienza, Prof. L. Benini, Prof. G. de Micheli
- Partners: UCM, Cagliari, Verona, Bologna.

[Sun, Niagara Broadband Processor]



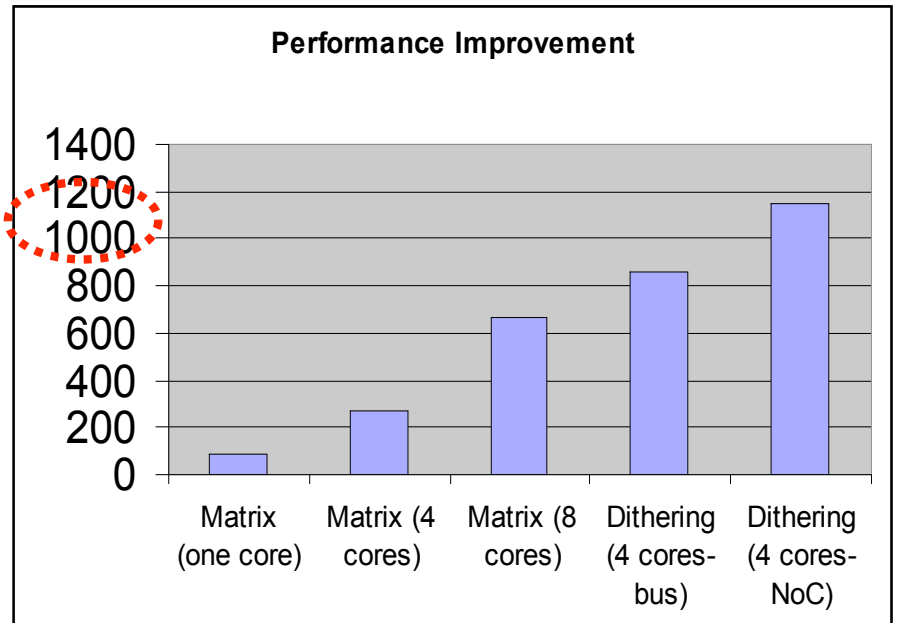
HW/SW Emulation Framework for MPSoC

- Integration FPGA SoC-NoC emul with SW thermal libraries



Comparisons with State-of-the-art Simulators

- HW emulation does not lag with large number of processors (100 MHz) or signal management (NoC)



	MPARM SW sim.	HW/SW Emulator
Matrix (one core)	106 sec	1.2 sec (88x)
Matrix (4 cores)	5’ 23 sec	1.2 sec (269x)
Matrix (8 cores)	13’ 17 sec	1.2 sec (664x)
Multimedia pipeline (4 cores-bus)	2’ 35 sec	0.18 sec (861x)
Multimedia pipeline	3’ 15 sec	0.17 sec

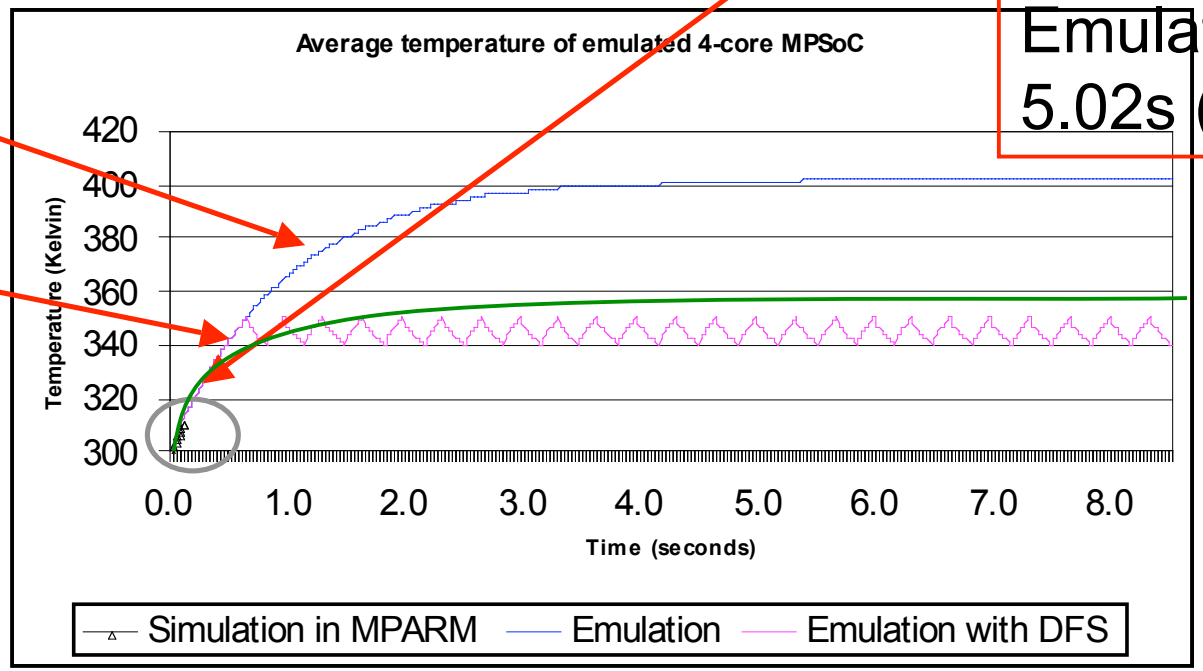
Speed-ups of 3 orders of magnitude with cycle-accurate MPSoC simulators

Long Thermal Studies

- SW sim. very slow with “high” accuracy (<12 cells)
- Long simulations are unaffordable: 2 days for 0.18 real sec

DFS OFF: 500 MHz.

DFS ON: 100 MHz.



Emulation time 5.02s (26 cells)!

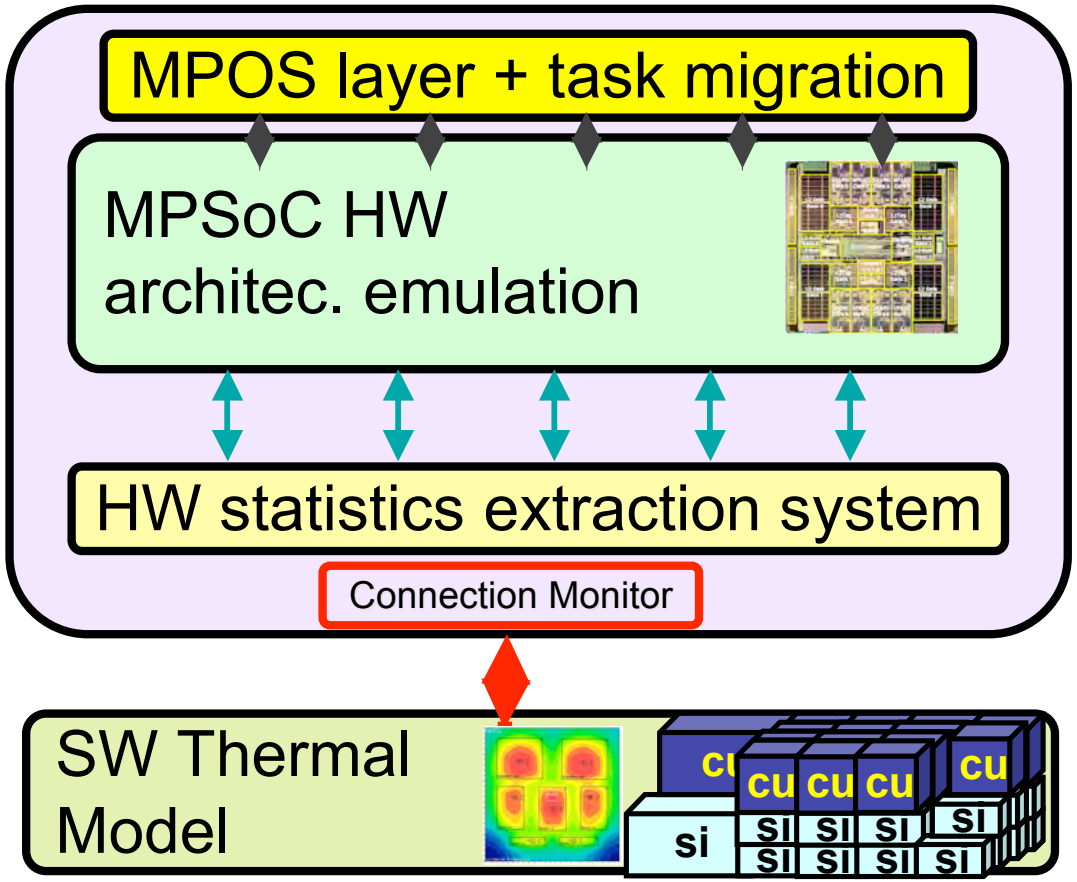
500 MHz.

100 MHz.

Validation run-time thermal management in real-life systems

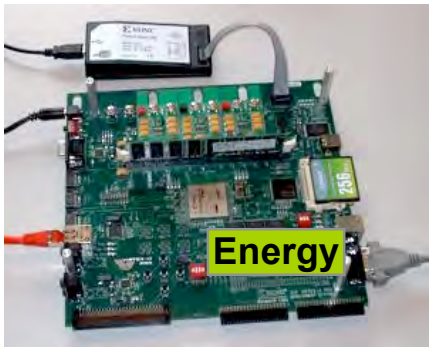
OS-Based Thermal Management Framework

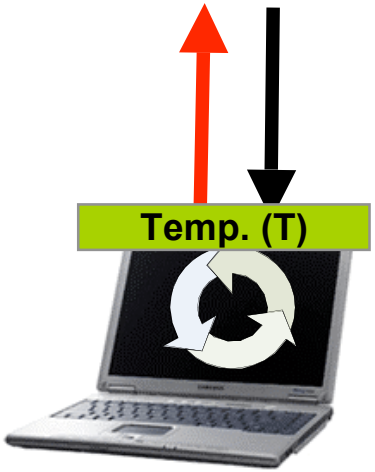
- uCLinux extended with task migration support



FPGA

Xilinx

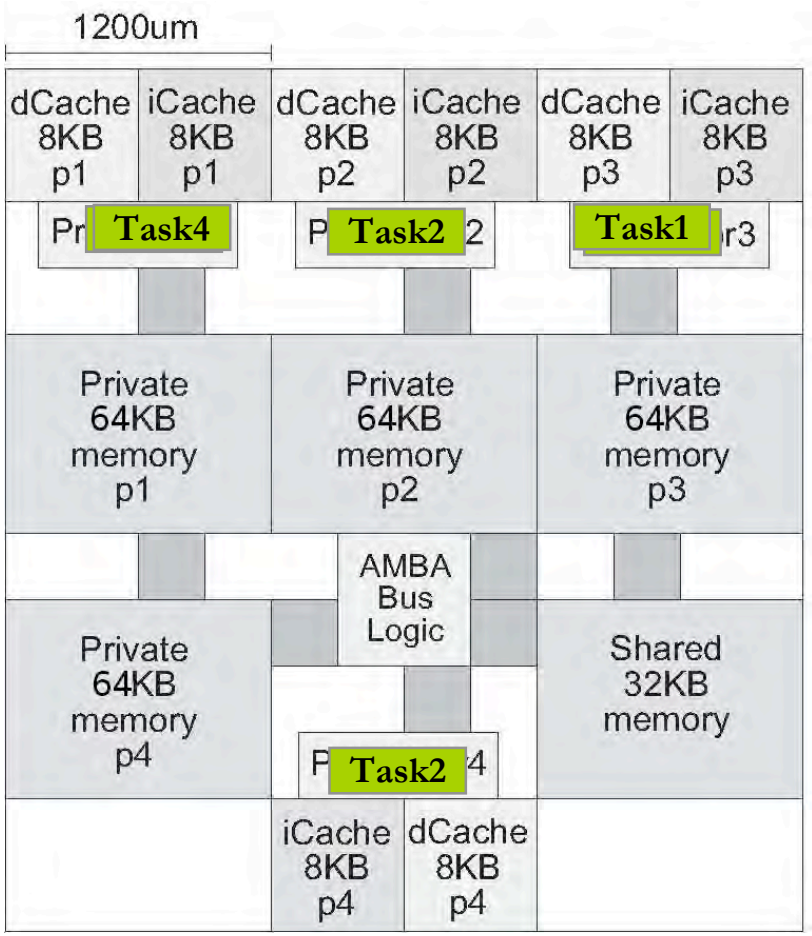




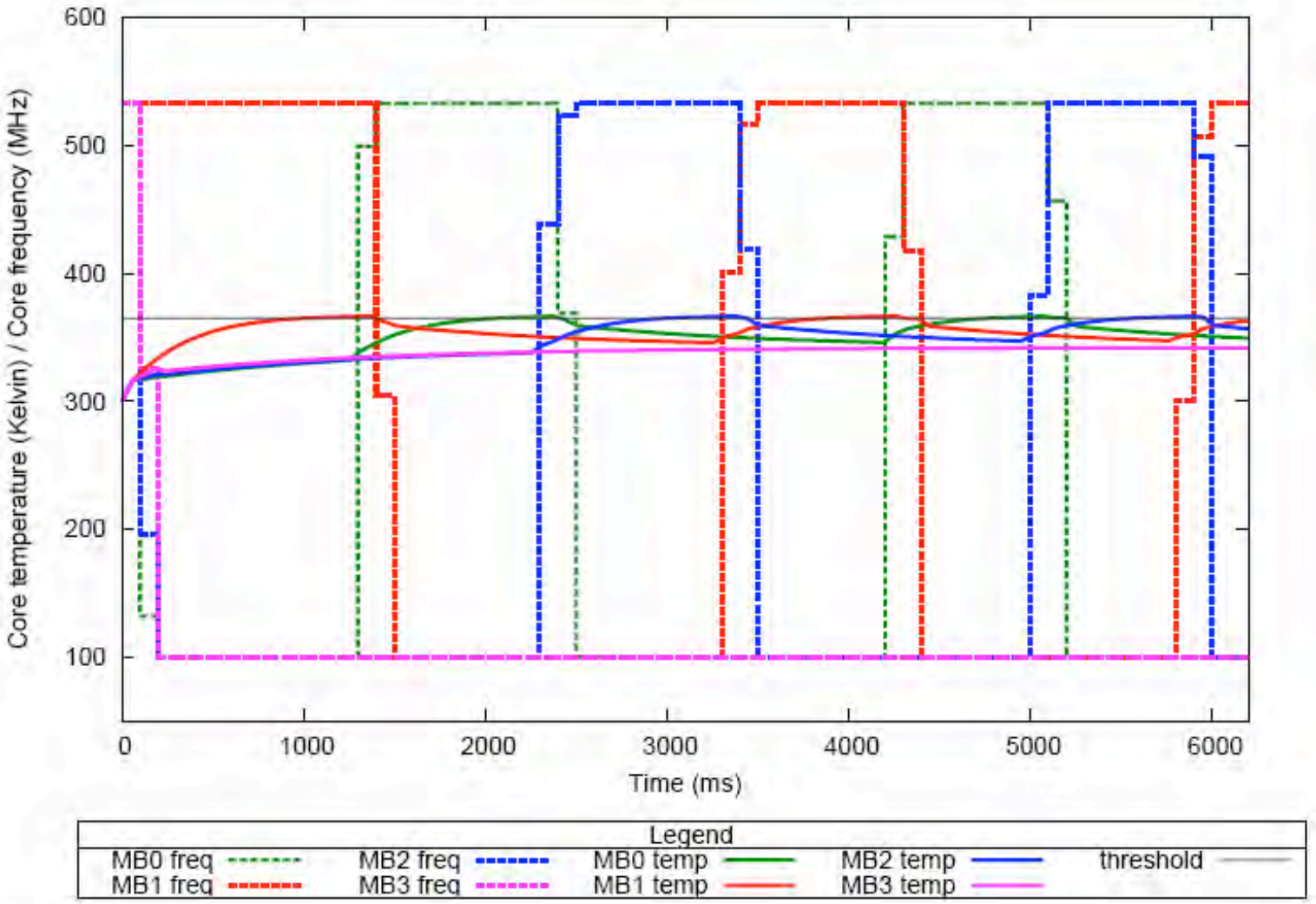
Host PC

Case Study: OS-Based Thermal Policies

- Working conditions
  - 3 cores start processing
  - 1 core remains idle for cooling
- Task migration policy
  - Treshold-Based Policy:
    - Upper bound: 360º K
  - Migration to coolest processor
- DFS Policy
  - 10 Emulated freq: 100-512 MHz
  - Linear decrease applied if deadline met



Results: Thermal Evaluation



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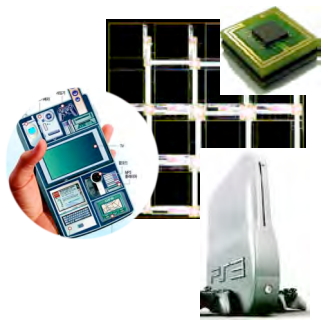

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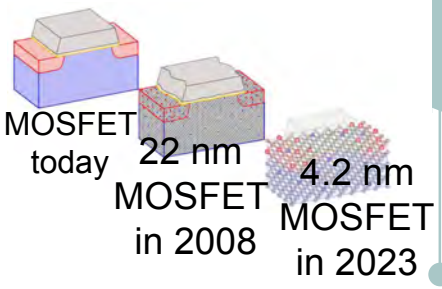
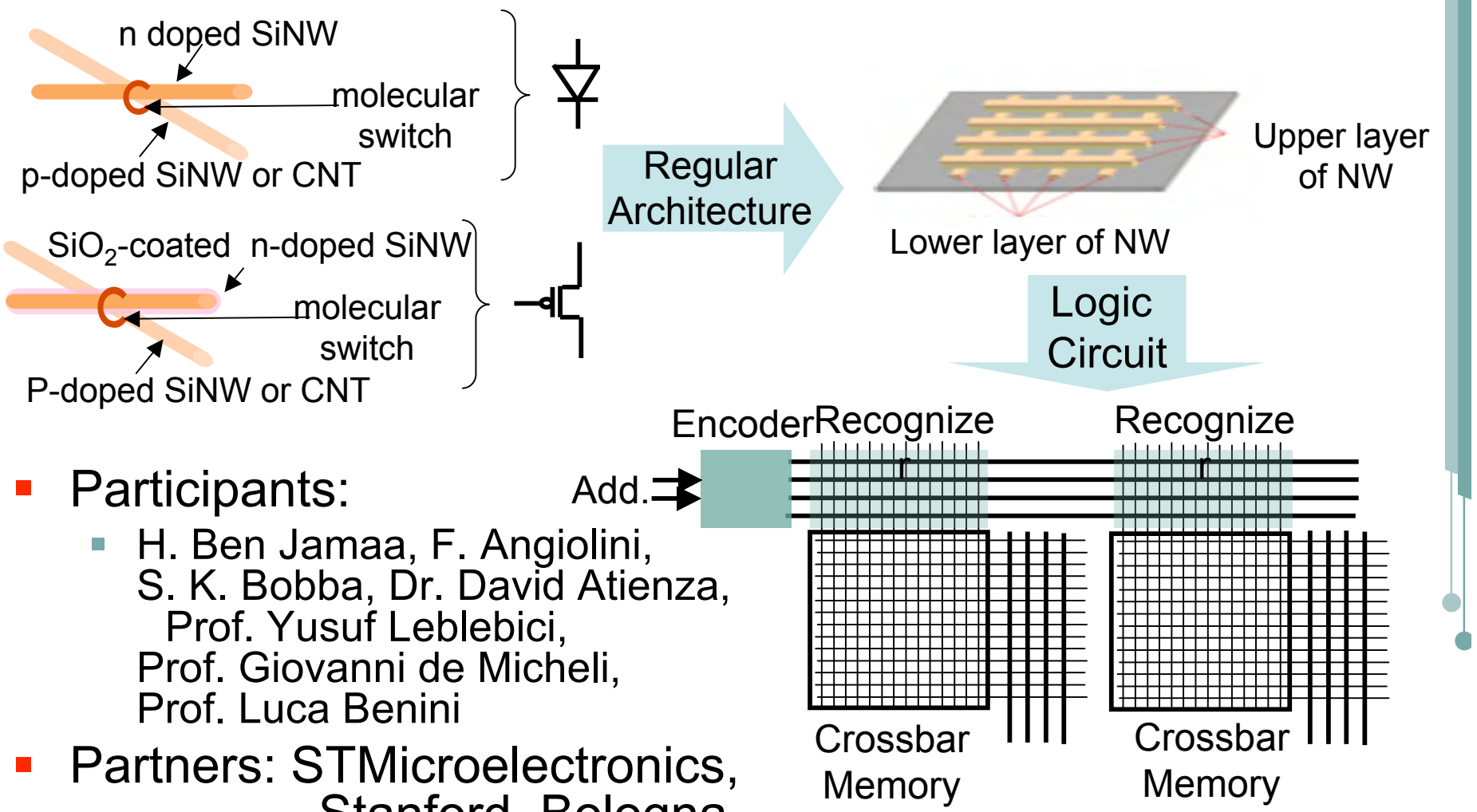
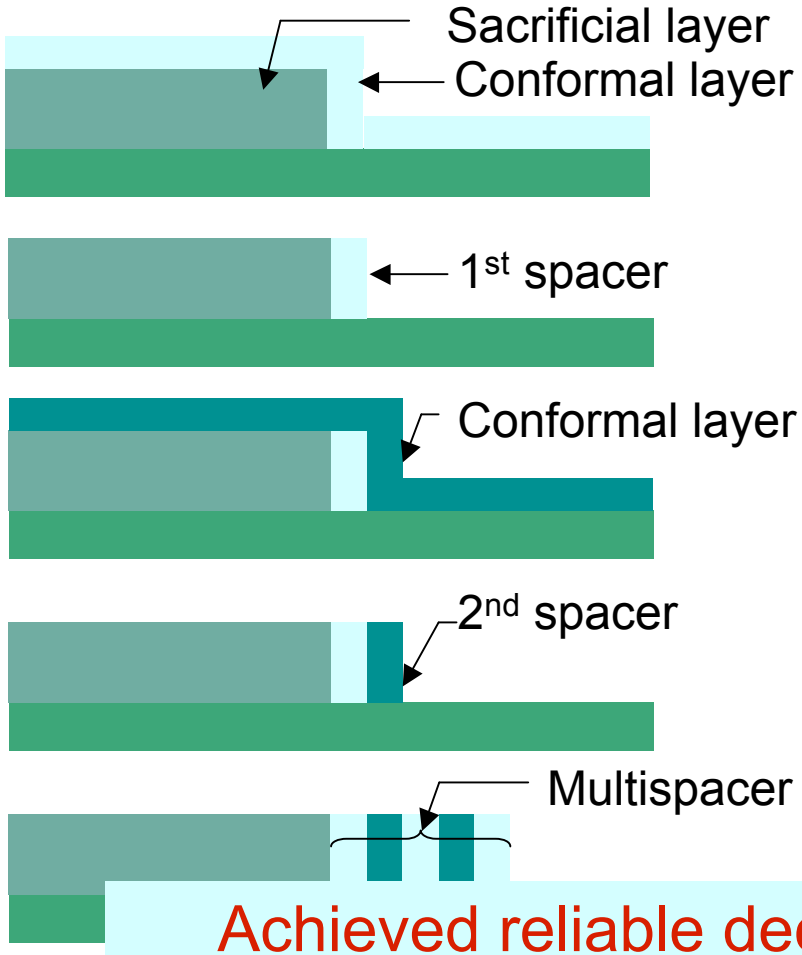


Nanoscale Hybrid Crossbar Memory

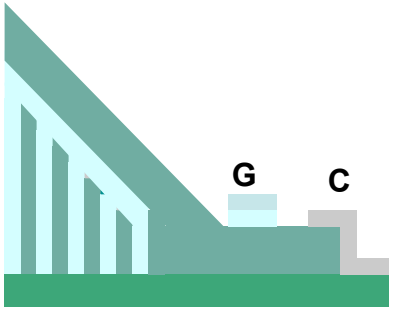


- Participants:
  - H. Ben Jamaa, F. Angiolini, S. K. Bobba, Dr. David Atienza, Prof. Yusuf Leblebici, Prof. Giovanni de Micheli, Prof. Luca Benini
- Partners: STMicroelectronics, Stanford, Bologna

Project Major Research Questions



- **Integration Issue:** micro-to-nano interface within hybridized standard CMOS



Nanowire differentiation

- **Reliability Issues:**
  - Switch defects
  - Nanowire breakage
  - Nanowire shorts

- Defect-aware addressing
- Defect-aware information encoding
- Redundancy at

Achieved reliable decoding schemes for multi-Vt SiNW memory architectures

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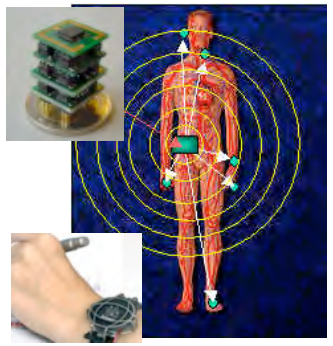

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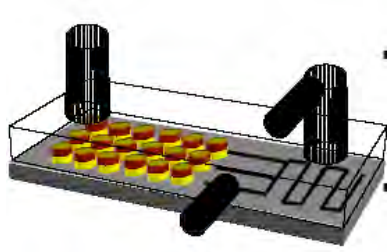
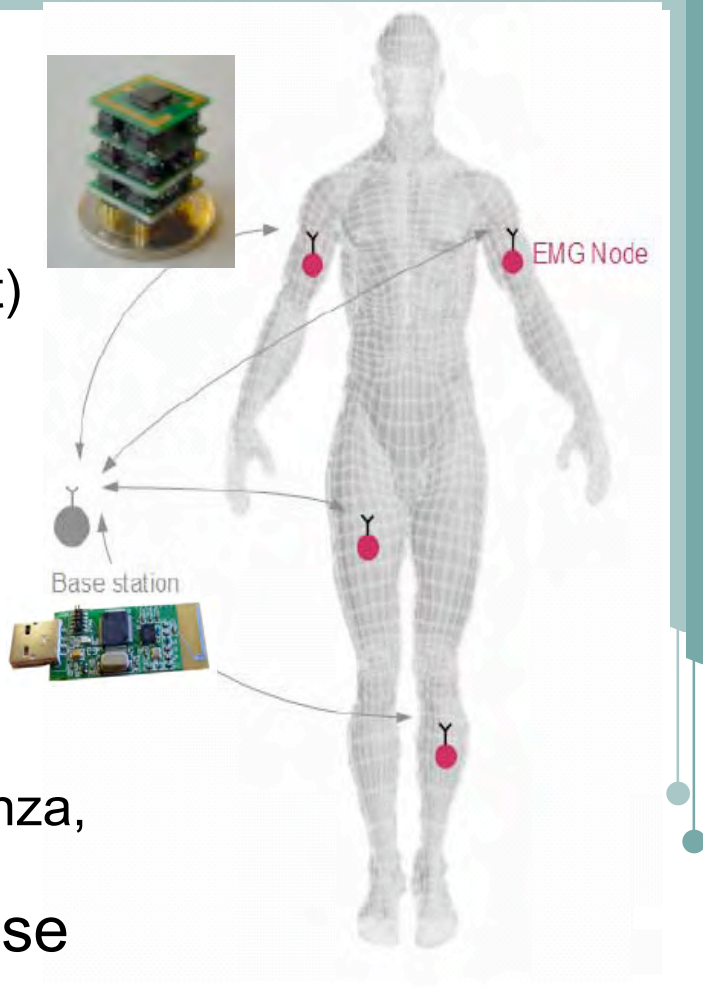


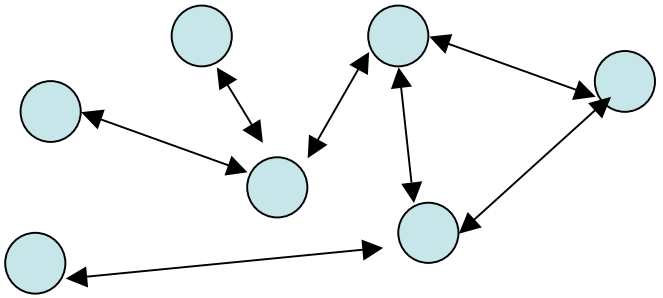
Wireless Sensor Networks (WSN) Projects

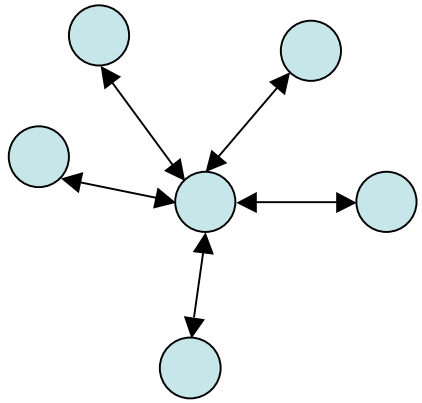
- Optimization of communication protocols for WSN nodes
  - Nodes: SensorCubes (IMEC/Holst)
  - Basestation: USB Stick-MSP 430 (Holst)
  - Tiny OS
- Modeling of scavenging devices
  - Model checking-based simulator
- Participants:
  - A. Susu, F. Rincon, Dr. N. Khaled, Prof. Andrea Acquaviva, Dr. David Atienza, Prof. Giovanni de Micheli
- Partner: IMEC-NL/Holst, Complutense Univ. Madrid



MAC Protocols Exploration

- Contention based/random access
  - Mesh network. Dynamic topology, no rigid structure
  - Allows multihoping, energy optimization, mesh topology
  - Applications: spread networks, alarms o events transmission
  - B-MAC, S-MAC, Aloha protocol.
- TDMA Based dynamic/static
  - Star topology.
  - Optimal under known/static conditions
  - Appls: real time or continuos





Working 5/10-node WSN for biomedical applications monitoring (ECG, EEG, EMG, etc.)

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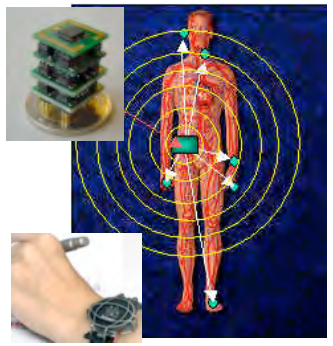

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  - Integration of bio-electro- mechano- opto-systems
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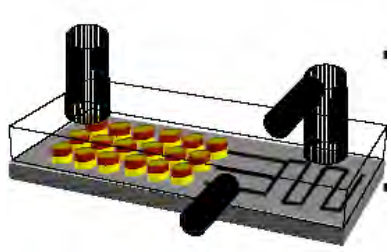
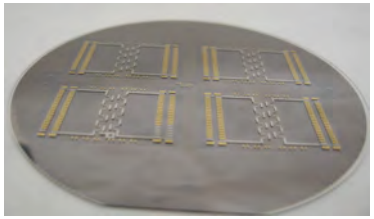
  - Implanted health monitoring devices



Lab-on-Chip Projects

- Cancer research
  - Why incidence of cancer rises exponentially with age?
  - Deterioration in genomic stability due to age creates higher incidence of cancer

- Capacitive DNA sensor chip
  - Aims for cheap label-free detection of DNA
  - Passive sensors realized on glass substrates
  - 4th generation of chips underway



- Participants:
  - Dr. Frank K. Guerkaynak, Dr. Carlotta Guiducci, Prof. Y. Leblebici
  - Dr. Diego Barrettino, Prof. Martin Gijs
  - Prof. Luca Benini, Prof. Giovanni de Micheli
- Partner: Institut Suisse de Recherche Expérimentale sur le Cancer (ISREC), Lab NanoPhysics Paris, Bologna

Moving Forward

- Design better circuits with current technology
  - NoC based design and EDA tools with new tech nodes
  - Thermal studies in multi-FPGA context
  - Relation thermal vs long-term reliability
- Design working circuits with future technologies
  - Interconnect nano wires with micro wires
  - Reliable decoding models of underlying faults and defects
  - Scavenger-based wireless sensor networks
- Extend design and data analysis techniques to integrated non-conventional systems
  - Medical diagnosis and studies of cancer-age relations
  - Capacitive DNA sensor

QUESTIONS ?