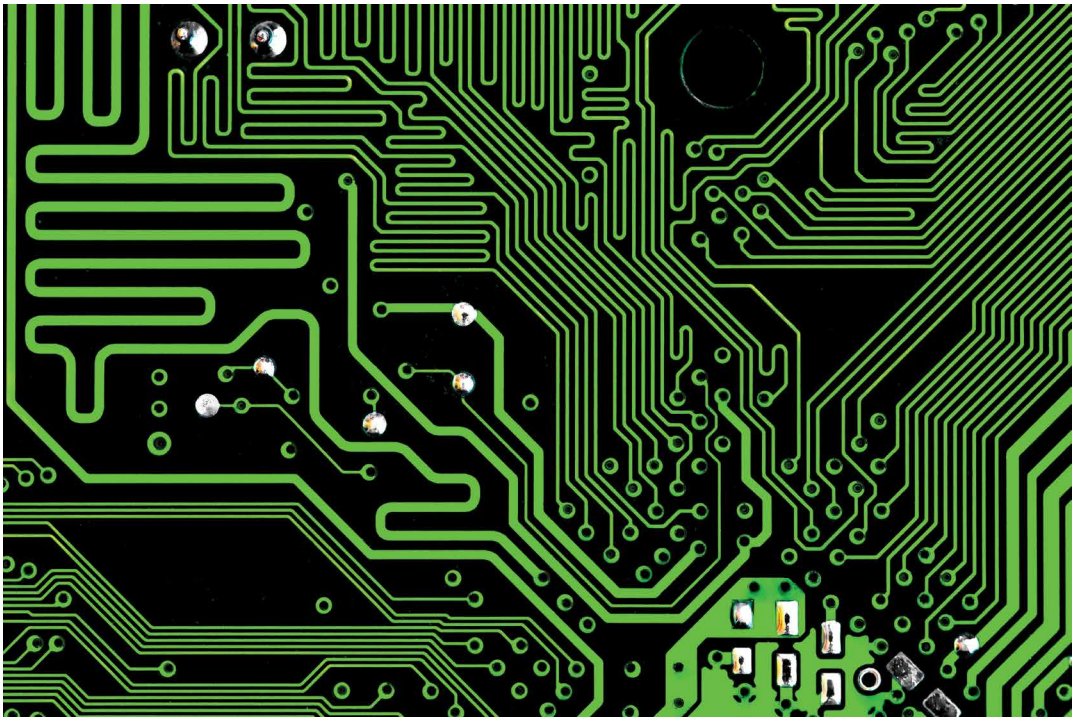

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Superconductive Electronics: A 25-Year Review

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Abstract

The challenges of conventional semiconducting electronics, such as dark silicon, memory wall, and stagnant clock frequency motivate the search for alternative computing technologies. Superconductive electronics (SCE) represents one of the most advanced beyond-CMOS technologies, with the potential of revolutionizing high-performance computing. In this review, the advancements of SCE over the past 25 years are presented. Novel logic families, circuit design techniques, and electronic design automation tools for SCE circuits are described. Eventually, future advancements in SCE are discussed from circuit and system design perspective.

Index Terms—Superconducting electronics, superconducting devices, single-flux-quantum, adiabatic quantum-flux-parametron, reciprocal quantum logic, emerging technologies, Josephson junction, Josephson effect, energy-efficient computing, quantum computing, electronic design automation.

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I. Introduction

Around the time of the invention of the first semiconductor *integrated circuit* (IC), the earliest superconductive IC – the cryotronic memory array — emerged as a viable competitor to transistor-based arrays [1]. The relatively simple physical structure and more reliable fabrication technology made these *superconductive electronic* (SCE) devices a viable alternative [2]. In the seventies there was a major effort led by IBM to design and fabricate computers using superconducting devices. This was paralleled by a similar effort by the major Japanese computer manufacturing companies. Nevertheless, SCE circuits were weakened by the so-called *latching problem* [3] that slows down signal transitions and thus limits the frequency of operation. At the

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same time, the CMOS technology entered its boom age, boosted by the "happy" scaling of design rules and by the rapid increase in performance at each technology node. In the mid-eighties IBM abandoned the pursuit of practical superconducting computers; a few years later, similar efforts were abandoned in Japan.

The rapid technological advances and commercialization of semiconductors diverted mainstream attention towards transistor-based electronics. Over the decades, however, a number of issues have hampered the growth of CMOS systems, such as stagnating clock frequency, limited power density (e.g., dark silicon), and difficulty in scaling the dimensions and threshold voltage of the devices. As we are seeing now the sunset of CMOS technology downscaling on the horizon, a renewed interest is drawn towards emerging technologies for computing. In particular, SCE can outperform established technologies in two metrics:

- *Low Operating Power*. Similar to the power wall of the bipolar electronics being overcome by CMOS [4], superconductive systems can overcome the CMOS power wall [5]. With minimal noise at cryogenic temperatures, the operating voltage of a typical SCE system is on the order of millivolts, dissipating minuscule power.
- *High Speed*. Even at cryogenic temperatures, the frequency of a typical CMOS system cannot exceed 5 GHz, due to, primarily, prohibitive power density. In contrast, SCE systems are consistently demonstrated to operate at frequencies of tens or hundreds of gigahertz [6], [7], [8].

As a result, SCE circuits are prime candidates to support the growth of high-performance computing and in particular the design of the hardware support for *artificial intelligence* (AI) and *machine learning* (ML) applications. The high performance and energy-efficiency of SCE are particularly important for *cloud computing*, since the global data centers currently account for 1–1.5% of global power consumption and keep rapidly increasing [9]. Enabling VLSI-complexity SCE systems will therefore have massive environmental implications by reducing the global cloud computing energy.

Moreover, superconducting technology finds applications in various domains besides computing, and specifically in areas that support data acquisition, computation and transmission. Namely:

- *Sensors*. *Superconducting quantum interference device (SQUID), the fundamental block of SCE devices, is capable of detecting magnetic signals at femtotesla levels.* These advantages are widely utilized in medical and scientific measurements [10], [11], geology [12], [13], and military applications [14].
- *Wireless Communications*. Modern communications systems require efficient signal processing to deliver high data rates and low *signal-to-noise ratio* (SNR). Due to the highly efficient pulse-based architecture, contemporary SCE technology (i.e., RSFQ described in Section III-A) can efficiently realize the high-performance wireless communication system, including *analog-to-digital* (ADC) and *digital-to-analog* (DAC) converters and *digital signal processing* (DSP) circuitry [15], [16].
- *Quantum Computing*. Currently, most advanced *quantum computers* (QCs) are realized using superconductive qubits that can be efficiently interfaced with SCE technologies [17], [18], [19]. Thus SCE circuits can provide an efficient means of communication between the QC chip and the host computer.

Despite the successful applications in the aforementioned areas, the impact of SCE technology is still small as compared to its potential benefits. Indeed, SCE shows a great promise of becoming the next high-performance computing technology and supports seamlessly data acquisition and communication. Still, creating a processor capable of competing with the state-of-the-art CMOS processors remains an elusive task, as well as the realization of a practical SCE computing and communication system. Nonetheless, we think that this ambitious goal will be reached in the next decade, based on the tremendous growth in the complexity of the SCE integrated circuits in the last 25 years. Indeed, the complexity of the SCE systems has been evolving from relatively small prototypes to *large-scale integration* (LSI) functional units [20], [21] and experimental processors [22], [23].

The objective of this review is to track the tremendous growth of SCE technology, covering the most important milestones related to digital circuit design. After SCE devices are described in Section II, features of each major SCE technology are briefly described in Section III. As the complexity of the SCE systems increases, large-scale IC design methodologies are being gradually adopted. Advancements in electronic design automation (EDA) for circuit, logic, and physical design of SCE systems are outlined in Section IV. Remaining challenges and promising future research directions are discussed in Section V, followed by the conclusions in Section VI.

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II. Background

A. Josephson Junction

Consider two superconducting electrodes separated by a narrow barrier, as depicted in Fig. 1(a). The barrier, or a weak link, can be in a form of a vacuum, insulator, or a regular (non-superconducting) metal. Despite no direct connection, the Cooper pairs (i.e., two coupled electrons [24]) can tunnel through the barrier with no voltage drop, producing tunneling supercurrent. This effect is called *Josephson effect*, named after B. D. Josephson who first explained this phenomenon in 1962, and was subsequently awarded the 1973 Nobel Prize in Physics [25]. A *Josephson junction* (JJ) is a superconducting device exhibiting Josephson effect, the primary building block of the superconductive digital electronic systems.

JJs exhibit several crucial properties enabling their use in superconductive electronic systems.

1) Critical Current: The magnitude of the tunneling supercurrent is limited by a value J_c called *Josephson critical current density*. If the current density through the barrier exceeds J_c, the superconductive mode is disrupted and tunneling becomes resistive, as depicted in Fig. 1(b). The magnitude of the critical current density is determined primarily by the material properties of the JJ. In addition to physical parameters, the critical current of a JJ can be reduced by increasing the temperature and applying external magnetic field [26].

Most superconductive IC fabrication technologies are characterized by the critical current density [27].

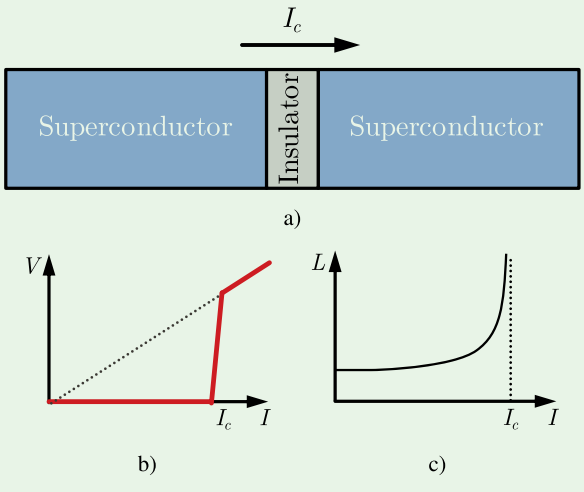

Figure 1. (a) A Josephson junction (JJ) consists of two superconducting electrodes separated by a weak link (typically insulator in SCE). (b) Idealized voltage-current characteristic of a JJ. The voltage drop is zero below the critical current. Beyond the critical current, the JJ exits superconductive mode and behaves as a resistor. (c) Josephson inductance increases with current, particularly close to critical current.

The *critical current* I_c is the maximum current that can be sustained by a JJ with a given area. For example, 25 years ago, state-of-the-art JJ fabrication processes achieved critical current density of 1 kA/cm^2 [28]. In contrast, the modern MITLL SFQ5ee process [27] supports 10 kA/cm^2, enabling the use of JJs with smaller area.

2) Nonlinear Inductance: A JJ behaves as a nonlinear inductor, controlled by the current I flowing through the JJ [2],

$$L = \frac{\Phi_0}{2\pi\sqrt{I_c^2 - I^2}}, \tag{1}$$

where

$$\Phi_0 = \frac{h}{2e} \approx 2.07 \times 10^{-15}\ Wb \tag{2}$$

is the magnetic flux quantum. The relationship between the current and inductance is shown in Fig. 1(c). Note that as current I approaches the critical current, the inductance of the JJ rapidly increases, reflecting the transition of the device to resistive mode.

B. Magnetic Flux Quantization

Consider a circuit depicted in Fig. 2(a). Suppose the circuit operates in non-superconducting mode. The current I_b is equally split between the two sides of the loop due to its symmetry. Suppose a small constant external magnetic field is applied, producing magnetic flux Φ_{ext} within the loop. Such magnetic field produces no changes in the electrical behavior of the loop.

A similar superconducting loop is illustrated in Fig. 2(b). Analogous to the previous case, a small constant magnetic flux $\Phi_{\text{ext}} < \frac{\Phi_0}{2}$ is applied across this loop. In this case, however, the loop responds by inducing additional *screening current* I_s [26], as illustrated in Fig. 2(c). The induced current produces the magnetic flux $\Phi_{\text{int}} = -\Phi_{\text{ext}}$, canceling the external magnetic field. Suppose, the magnetic flux through the superconducting loop is increased, such that $\frac{\Phi_0}{2} < \Phi_{\text{ext}} < \Phi_0$. The screening current changes the direction to produce flux $\Phi_{\text{int}} = \Phi_0 - \Phi_{\text{ext}}$, yielding the total flux of Φ_0. By further increasing the magnetic flux, a similar pattern repeats – the screening current induces magnetic flux to bring the total magnetic flux to the nearest integer multiple of Φ_0, i.e.

$$\Phi_{\text{int}} + \Phi_{\text{ext}} = n\Phi_0,\ n \in \mathbb{Z} \tag{3}$$

This phenomenon is called *quantization* of magnetic flux.

Quantization of the magnetic flux implies the existence of energetically stable loop currents, producing magnetic fluxes 0, $\pm\Phi_0$, etc. To illustrate this effect,

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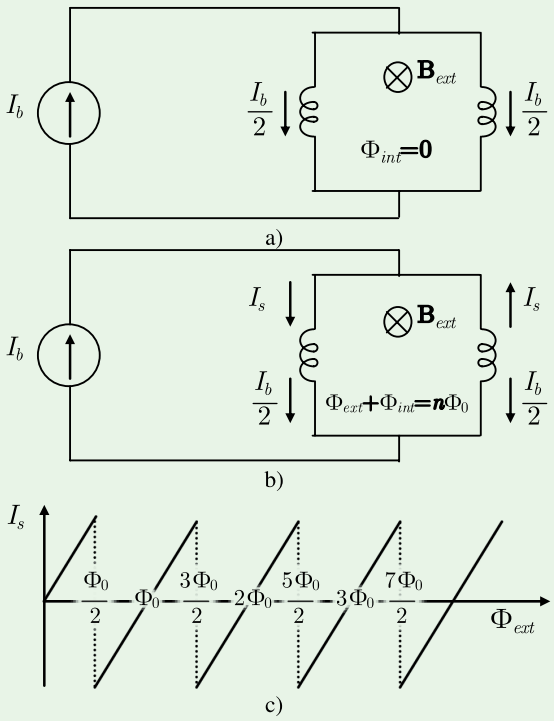

Figure 2. Comparison of magnetic flux within the loops. (a) Normal metal loop. External flux does not affect electrical behavior of the loop. (b) Superconductive loop. Screening current I_s is induced to bring the total flux through the loop towards the nearest integer multiple of Φ_0. c) Screening current as a function of external flux.

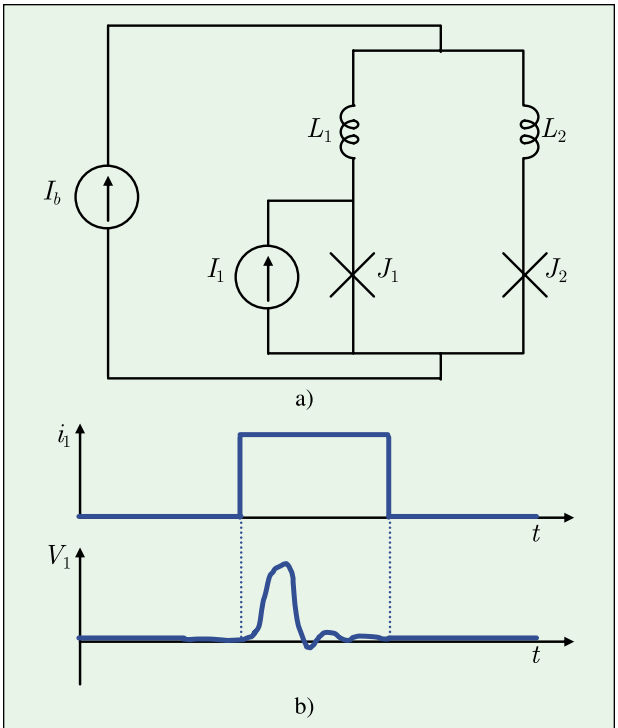

Figure 3. Superconducting storage loop. (a) Circuit topology. (b) External current and voltage across junction J_1.

consider the circuit illustrated in Fig. 3(a) [29]. The bias current I_b is evenly split between the junctions, producing no magnetic flux. A small current pulse I_1 is next injected into the circuit next to the inductor L_1. The increased current causes J_1 to switch to the resistive mode, causing the bias current to redirect towards the junction J_2. Since the bias current is redirected towards J_2, the current through junction J_1 is reduced and the device exits the resistive mode. In this new state, the loop emits the magnetic flux, equal to Φ_0, i.e., the loop stores a *single flux-quantum* (SFQ). Fig. 3(b) depicts the voltage across the junction J_1. After the injection of current I_1, the voltage across J_1 rapidly increases. As the bias current is redirected towards J_2, the J_1 returns to superconductive mode and the voltage reduces to zero. Interestingly, the area under the voltage curve is equal to $\Phi_0 \approx 2.07\ \text{mV} \times ps$. The voltage pulse produced by J_1 is called a *single flux-quantum pulse* (SFQ pulse).

III. SCE Technologies

Superconductive digital technologies have been under active development since 1970's. The early SCE technologies developed in the late 1970's – early 1980's however suffered from the *latching problem*. Transitions from logic `1` to logic `0` were very slow compared to the `0`→`1` transitions. This issue limited the operating frequency of SCE to a few gigahertz, comparable to the fastest non-cryogenic semiconductor circuits of the time. In the late 1980's, the difficulties presented by the *latching problem* in SCE were overcome by using pulse-based signaling. Starting from the first technology of this kind [3], called *Rapid Single-Flux Quantum* (RSFQ)[1], several enhancements were proposed, including low-voltage SFQ, ERSFQ, and eSFQ; along with completely novel SCE technologies, namely AQFP and RQL. Typical characteristics of these technologies are described in Table 1. In this section, the evolution of these technologies is briefly described. The list of these technologies is not exhaustive, but sufficient to give a glimpse of the evolution of SCE.

A. Rapid Single-Flux Quantum (RSFQ)

The early superconductive digital technologies primarily focused on magnetic coupling to induce the control currents within the circuits [34], [35]. This mechanism however was relatively slow, limiting the operating speed of the SCE systems, rendering the

[1]Originally, Resistive Single-Flux Quantum.

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Table 1.
Typical characteristics of major SCE technologies as compared to CMOS [30], [31], [32], [33].

	Clock freq. [GHz]	Bit energy ($I_c\Phi_0$)	Critical current [mA]	EDP [aJ ps]
CMOS	4	—	—	$\sim 10^5$
RSFQ	50	19	150	120
LV-RSFQ	20	3.5	150	54
ERSFQ/eSFQ	20	0.8	150	12
RQL	10	0.33	150	10
AQFP	5	0.0083	50	0.086
Quantum limit				5.3×10^{-5}

cryogenic SCE uncompetitive with the room-temperature CMOS. The Rapid Single-Flux Quantum (RSFQ) technology developed in the late 1980's by Likharev and Semenov [3], addresses this issue by using SFQ pulses to control the currents within the systems. A fundamental RSFQ storage loop is depicted in Fig. 4. Initially, the bias current I_b flows towards J_0, indicating the storage of logic `0`. The magnitude of I_b is adjusted to bring J_0 close to critical current. A voltage pulse at input *D* injects additional current towards the loop, most of which flows through J_0. This injection increases the current through J_0 beyond the critical value, bringing J_0 into the resistive mode. The bias current is redirected towards J_1, indicating the storage of logic `1`.

To determine the state of the storage loop, an additional JJ J_c is connected to the junction J_1. The critical current of J_c is adjusted to be smaller than the critical current of J_1. If logic `0` is stored within the loop, injecting the current at node `clk` would trigger J_c to switch, with no effect on J_1. If the loop stores the logic `1`, the injected current will switch J_1, producing the voltage pulse at node `Q`. The bias current redirects back towards J_0 during this process, resetting the loop state to `0`. This structure is called RSFQ D-flip-flop (DFF).

Observe the similarity of the RSFQ storage loop with Fig. 3(a). Technologies preceding RSFQ utilized magnetic current injection mechanisms. The key innovation of RSFQ is the use of SFQ pulses, enabling operating frequencies of tens to hundreds of gigahertz.

Due to its small size, a single SFQ pulse cannot be reliably transferred to multiple paths. To produce multiple fanout, the **splitter** gate is used, as depicted in Fig. 5. The input junction J_0 generates a SFQ pulse that is distributed to two output junctions, J_A and J_B biased close to critical current. Upon arrival of the input pulse, J_A and J_B both produce a SFQ pulse, thereby copying the input signal.

Merger, often referred to as **confluence buffer** (CB), directs signals from multiple (typically two) input branches into one output branch, as shown in Fig. 6. A pulse arriving from either of the input branches

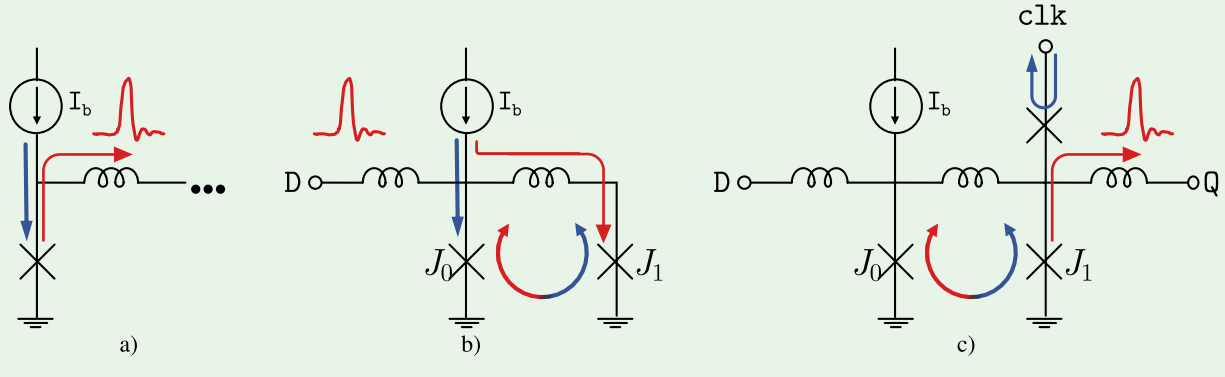

Figure 4. Basic SCE structures. (a) Josephson junction (JJ). If the bias current `Ib` through the junction is small, no voltage drop across the junction occurs. Increasing `Ib` over critical value `Ic` causes JJ to *switch*, producing a SFQ pulse opposing the bias current. (b) Storage loop. Initially, the bias current flows through J_0, denoting the logical `0`. A SFQ pulse at input `D` switches J_0 and redirects the bias current towards J_1, storing logical `1`. (c) The D flip-flop operates similar to storage loop. An incoming `clk` pulse will switch J_c if the loop state is `0`. If the state is `1`, J_1 switches and produces a SFQ pulse at `Q`.

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switches the junction J_x, triggering the release of SFQ pulse towards the output. A CB therefore effectively performs a logical OR function. The merger produces two output pulses, if the pulses are temporally separated, or a single pulse, if the signals arrive simultaneously. By increasing the size and reducing the bias current flowing through J_x, the current necessary for switching J_x can be increased. Under these conditions, the SFQ pulses need to arrive at both inputs simultaneously to increase current through J_x beyond the critical value, producing an **AND** gate. In standard RSFQ technology, simultaneity is achieved by placing DFFs before the merger. The synchronization can however be achieved using clocked gates, a technique called gate compounding [36].

By connecting the storage loop as illustrated in Fig. 7(a), a NOT gate is produced. The arrival of the data signal changes the loop state to 1. If the loop state is 1, junction J_1 switches and resets the loop state to 0. Otherwise, the bottom junction switches, producing a pulse at the output. Note that the inverter requires the clock input.

The **exclusive-or** (**XOR**) gate, illustrated in Fig. 7(b), hosts two quantizing storage loops. A single input pulse arriving to branch A (B) gate reverses the persistent current within the loop J_{a1}-J_{a2}-J_{q1}-J_{q2} (J_{b1}-J_{b2}-J_{q1}-J_{q2}). A data pulse arriving at the opposite branch B (A) before the clock signal increases the persistent current beyond the critical current of junction J_{q1} removing the flux from the loop and resetting both loops to the initial state. The clock pulse reads the state of the loop via the comparator J_{clk}-J_{q2}.

Operating speeds of up to hundreds of gigahertz are consistently achieved in RSFQ systems [6], [7], [8]. Due to this high speed, the RSFQ technology gained significant attention as a potential enabler of petascale [37], [38] and, later, exascale computing [39]. For example, in 2023, a RSFQ floating-point adder and multiplier unit was shown to operate at 56 GHz delivering throughput of 56 GFLOPS [40]. Most RSFQ logic gates require a clock signal to operate correctly, necessitating gate-level pipelining [36]. The gate-level pipelining however significantly complicates the logic synthesis, as described in Section IV-C.

The operating power of RSFQ is two to three orders of magnitude smaller than CMOS. Despite this tremendous energy efficiency, the static power dominates the power dissipated in RSFQ systems, limiting the scalability of the technology and its applicability to heat-sensitive applications [41]. In RSFQ, the bias current is distributed via resistive bias network, as illustrated in Fig. 8 (red), accounting for more than 90% of the dissipated power [42]. Several techniques have been proposed to mitigate this issue.

1) Low-Voltage RSFQ (LV-RSFQ): The primary purpose of large resistance of the bias network is minimization of the current fluctuations during the switching process. Given sufficient design margins, however, it is possible to reduce the voltage and resistance of the bias network, as observed in [42] and [43]. In 2013, this technique was developed into a LV-RSFQ technology [44]. Small resistance of the bias network, however, makes the LV-RSFQ systems more susceptible to crosstalk noise between the RSFQ gates. In addition, the maximum operating

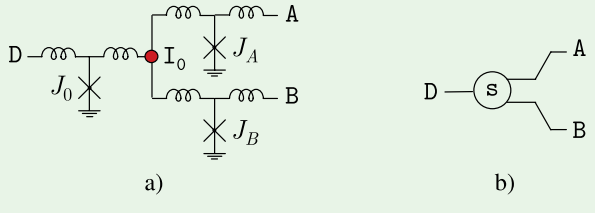

Figure 5. (a) Splitter gate. The red dot I_0 denotes the bias current. (b) Symbol for splitter used in this article.

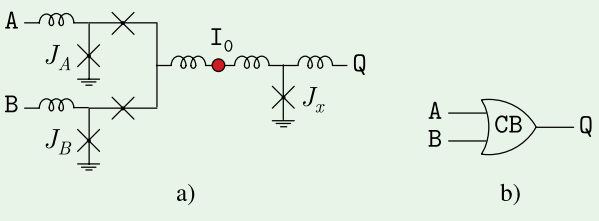

Figure 6. (a) Merger (confluence buffer) gate and (b) equivalent symbol.

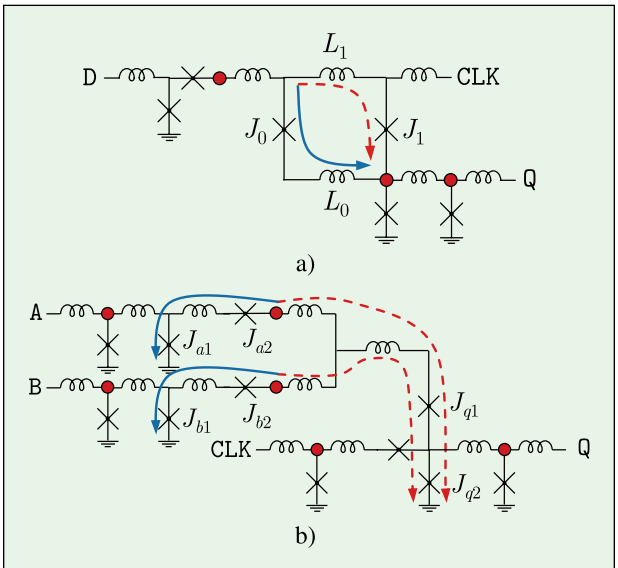

Figure 7. RSFQ clocked gates. (a) Inverter and (b) exclusive-or (XOR).

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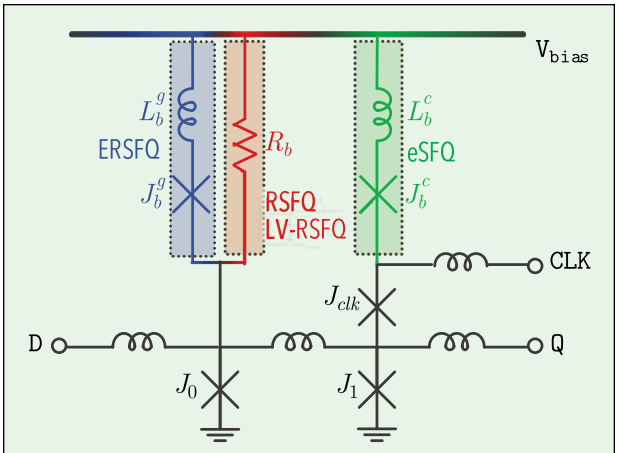

Figure 8. Comparison of bias networks in RSFQ and its derivatives. In conventional RSFQ, the bias current is delivered via the resistive network. In LV-RSFQ, the bias voltage $\mathrm{v_{bias}}$ and bias network resistance R_b are reduced. In ERSFQ, the resistive network is replaced by the inductive network terminated with a feeding JJ J_b^g. In eSFQ, the gate is biased at the clock input J_b^c. Due to the natural load balancing, $L_b^c < L_b^g$.

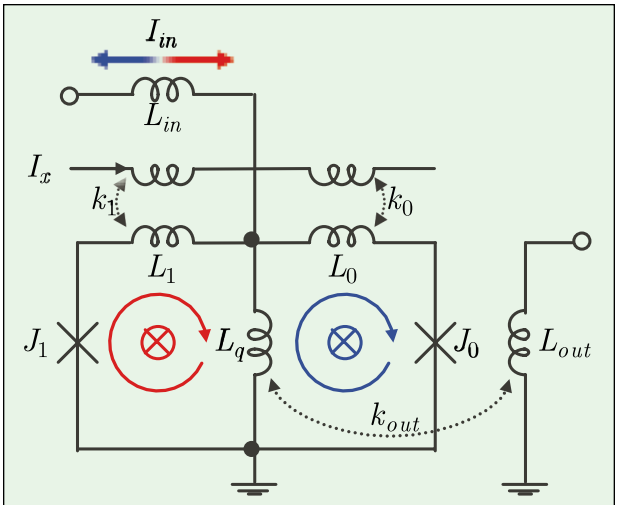

Figure 9. AQFP buffer. The AC current I_x energizes the loop J_1-L_1-L_0-J_0. The input current I_{in} induces a flux quantum to be stored in the left loop (logical 1) or right loop (logical 0). The large current is produced through L_q with the same direction as I_{in} and is inductively coupled to output inductor.

frequency of the gates is reduced due to slower switching [44], as described in Table 1.

2) Energy Efficient SFQ (ERSFQ): One approach to eliminating the static power is superconducting bias distribution network, completely eliminating resistive power dissipation. Similar to LV-RSFQ, this change makes the SFQ systems more sensitive to the switching process. In energy-efficient RSFQ (ERSFQ), described by Kirichenko et al. [45] in 2010, this issue is mitigated by increasing the inductance of the bias distribution network and adding the current-limiting *bias* JJs to the inductive bias network, as illustrated in Fig. 8 (blue). As the gate voltage reduces during the switching process, the bias current towards the gates is increased, switching the current-limiting junction. Switching the bias JJs increases the effective inductance, compensating for the fluctuations caused by the gate switching. Using this technique, zero static power of the ERSFQ circuits has been demonstrated [45].

To completely eliminate the voltage fluctuations, both gate and bias JJs should switch simultaneously. Practically, however, the bias JJ is switched after a delay. To minimize the residual noise, the inductors within the bias network should be enlarged, necessitating additional on-chip resources.

3) Efficient SFQ (eSFQ): The efficient-SFQ (eSFQ) technique, proposed by Mukhanov [46], is based on the observation that the bias limiting JJs within the clock network never switch during the circuit operation. Each time the clock signal delivered to a gate, a switching process occurs at the balanced comparator, regardless of its state. Assuming negligible clock skew, all balanced comparators at the clock network terminals switch simultaneously, maintaining constant voltage within the clock network. This natural balancing is exploited in eSFQ, where the logic gates are biased only via the balanced comparators, as illustrated in Fig. 8 (green). Since the constant voltage within the bias network is naturally maintained, the large bias distribution inductors are no longer necessary, significantly reducing the circuit area [31], [47].

Due to this drastic change in the bias network, eSFQ requires a significantly more complex system design. The logic cells require modification of the bias lines; some of the cells, such as TFF, are not trivial to modify [46], unlike ERSFQ, where only the bias network is replaced [21], [48].

B. Adiabatic Quantum-Flux Parametron

Adiabatic quantum-flux parametron (AQFP) technology proposed by Yoshikawa et al. [49] in 2011 addresses the issue of RSFQ static power by adopting an adiabatic operating scheme [50]. AQFP is based on the fundamental parametron device invented in 1954 by Goto [51] and subsequently realized as a quantum-flux parametron (QFP) in 1987 by Hosoya et al. [52]. The AQFP buffer consists of two superconductive loops shunted by a common inductor, as depicted in Fig. 9. The loop is periodically excited using the adiabatic power-clock I_x. During excitation, a flux-quantum is induced in either left or right loop, depending on the direction of the input data current I_{in}. The location of a flux-quantum determines

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the logical state of the AQFP device. Large current is produced at the inductor L_q in the direction of I_{in}. Note that the magnitude of I_{in} generally does not affect the magnitude of I_{out} [49].

The current through L_q is transferred to the next buffer by inductive coupling. By coupling an odd number of buffers to a common output inductor (e.g., $\{L_{q1}, L_{q2}, L_{q3}\} \rightarrow L_{out}$), the direction of the current through L_{out} will depend on the most prevalent current direction, thereby realizing the majority function [53], [54], enabling highly expressive arithmetic circuits [55]. By inverting the coupling coefficients, the signals can be efficiently inverted.

Multiple fanout in AQFP circuits can be achieved by coupling the output inductor L_q to multiple output inductors. Coupling a single buffer to multiple gates produces weaker input current at the fanouts. Using such a weak fanout in a subsequent gate may produce a data hazard. To ensure the equal current of each fanin, an additional buffer stage called *splitter* is used to amplify the signals.

The primary strength of the AQFP technology is energy efficiency. The JJs within the AQFP SQUID are used as amplifiers rather than switches, converting the small input current into strong output signal [56]. The AQFP systems have been shown to dissipate at least 1,000 times smaller power than CMOS while operating at 5–15 GHz speeds [57], [58], [59]. The reversible AQFP full-adder has been demonstrated to operate below the Landauer bound, dissipating 5.80×10^{-23} J per operation [60], [61]. Similar to RSFQ and its derivatives, however, all AQFP logic gates require synchronization. Numerous works to mitigate this issue during the logic synthesis have been proposed, as described in Section IV-C.

C. Reciprocal Quantum Logic (RQL)

Reciprocal Quantum Logic (RQL) proposed in 2011 by Herr et al. [32] is an energy-efficient adiabatic logic. The DC bias network of RSFQ is replaced by two sinusoidal clock signals shifted in phase by 90 degrees and inductively coupled to the functional gates (see Fig. 10). These signals periodically bias the corresponding parts of the circuit. Due to the adiabatic clocking, incompatible with RSFQ, the RQL data encoding differs from RSFQ. In RQL, presence (absence) of a *pair* of positive and negative (reciprocal) SFQ pulses indicates logical 1 (0). The data propagates through a circuit in four phases spanned by the two clocks, as illustrated in Fig. 10. The RQL technology employs special logic gates, such as *AndOr* and *AnotB* [62]. Unlike the aforementioned technologies, RQL circuits can accommodate multiple gates within the same phase [62], alleviating the complexity of gate-level pipelining.

The adiabatic clocking allows the gates to be biased serially, greatly reducing the bias current requirement and simplifying the design process [63]. Inductive bias distribution eliminates the static power consumption, leaving the JJ switching as the only source of power dissipation [62]. Due to this feature, the power dissipation of RQL logic is similar to eSFQ, on the order of 0.1 aJ per bit [41], [64]. The limitations of RQL are similar to AQFP. RQL circuits require transformers that scale down poorly [2]. Furthermore, the complexity of distributing multiphase clock limits the practically achievable clock frequency to approximately 10 GHz [64].

IV. Evolution of the Design Automation Tools

Over the last 25 years, the SCE technologies gradually increased the integration density, necessitating the use of *electronic design automation* (EDA) tools to produce large-scale systems. However, due to the fundamental differences between SCE and CMOS, most standard CMOS tools are not compatible with SCE. Placement and routing tools offer the easiest adaptation, due to primarily considering geometric features of the target technology, such as cell dimensions and wire width [65]. In contrast, the tools in other domains, such as logic synthesis and circuit analysis, require a complete overhaul. In this section, the development of EDA tools across different domains is described.

A. Placement and Routing (P&R)

The *Josephson transmission lines* (JTL) are drastically different from the standard wires used in CMOS, behaving as active components. Therefore, conventional *place and route* (P&R) algorithms can only consider *passive transmission lines* (PTL) for RSFQ and its derivatives [66]. Early cell libraries, such as CONNECT [67], did not consider this limitation and are therefore not easily compatible with conventional P&R tools. In contrast, modern libraries include PTL drivers and receivers into the standard cell [66], [68], [69].

With PTL interface included in the cell, the conventional P&R methods become applicable to SFQ wire routing. In qGDR [70], for example, the standard global/detailed routing approach is adapted to route an 8-bit integer divider while complying with the MITLL SFQ5ee design rules. A similar technique is applied in [71] to design a 16-bit Sklansky adder.

The VLSI EDA industry offers robust P&R tools, such as Synopsys ICC2 [72] and Cadence Innovus [73]. In addition, several specialized tools have been recently proposed, including qPlace [74] and JRouter [75] that consider such SCE-specific features such as splitter insertion and wirelength matching. Using these tools

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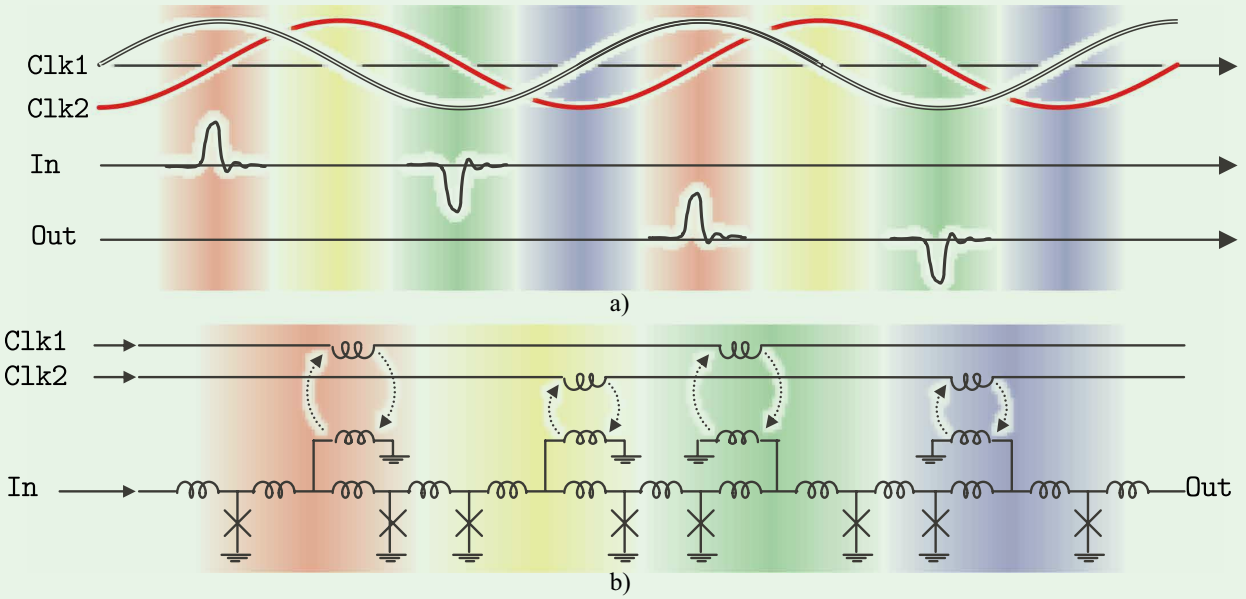

Figure 10. RQL four-phase transmission line. (a) The data is encoded as pair of reciprocal SFQ pulses with the π-phase shift. (b) The data propagates through the transmission line that is alternately coupled to two AC clock signals.

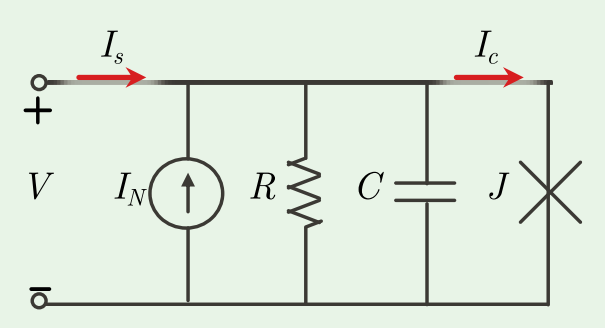

Figure 11. Resistively and capacitively shunted junction (RCSJ) model of a JJ.

however requires compatible cell libraries and design rules. Since these design tools are adapted to grid-based P&R, the standard cells in modern SCE libraries are adjusted to fit into a grid of specific dimensions. In [76] and [77], for example, the asynchronous cells developed for the MITLL SFQ5ee process [78] are adjusted to have dimensions as integer multiples of 32 μm.

A typical CMOS clock network occupies primarily metal layers, which are less critical as compared to device layers [79]. In RSFQ, distributing the clock signal towards N gates requires a splitter tree of $N-1$ gates, occupying significant area at the device layer [80]. A recent study demonstrated that the clock routing and logic placement should be performed simultaneously, achieving 9% reduction in wirelength after adjusting the placement of the logic cells [81].

B. Circuit Analysis

SPICE, the core circuit simulation tool for most conventional electronic systems, offers limited support for JJs [82]. Since the inception of SCE, a number of specialized circuit simulation tools have been developed, including JSIM [83], PSCAN [84], [85], and WRspice [82]. In recent years, a Josephson Simulator JoSIM has been released showing superior performance as compared to JSIM [86].

Sophisticated circuit models are necessary to describe the complex behavior of the JJs. One of the earliest and most commonly used models is the *resistively and capacitively shunted junction* (RCSJ), described independently in 1968 by Stewart [87] and McCumber [88]. The model consists of an idealized JJ, shunted by a parasitic capacitance C, and exhibiting dissipative current during switching R, as described in Fig. 11. The model often includes the current source I_N representing the current due to thermal noise.

Computational efficiency and good accuracy made the RCSJ model widely supported in most circuit simulators, including PSCAN, WRspice, JSIM, and JoSIM. A major limitation of the RCSJ model is the purely macroscopic nature of the model, not grounded in quantum-mechanical principles of Cooper pair tunneling [89]. A series of works in the mid-1960's developed a more accurate model of the JJ behavior [90], [93], subsequently termed a Tunneling Junction Model (TJM, also known as microscopic model, or Werthamer model).

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Due to the relative computational complexity of TJM, most circuit simulation tools are based on RCSJ model. In past technologies with critical current density below 4.5 kA/cm^2, the difference between the TJM and RCSJ models was negligible [89]. Negligible difference combined with larger runtime therefore justified the use of RCSJ model, particularly in digital applications. In the modern SFQ5ee fabrication technology with critical currents of 10 kA/cm^2, an average of 5% difference between the RCSJ and TJM models is observed [89].

An algorithm to accelerate the evaluation of the TJM was proposed in 1987 by Odintsov et al. [94]. This algorithm is the basis of the Microscopic Tunneling Model for Josephson Contacts (MiTMoJCo) package developed by Gulevich [95] in 2018, currently used in WRspice to accurately simulate the JJ using TJM.

An important parameter affecting the behavior of a SCE system is *operating margins*, describing the maximum tolerable parameter variations. Therefore, several SCE simulation tools incorporated the margin analysis functionality. JoSIM, PSCAN, and WRspice can all match the behavioral description of the circuit with the simulation to determine the sensitivity of the circuit to selected parameters. These tools can also optimize the circuit parameters to improve the margins. A more recent JoSIM can additionally estimate the yield of the circuit based on user-specified parameter variations [86]. Several methods have recently been proposed to further accelerate and improve the quality of the multidimensional margin optimization [96], [97], [98].

Layout-versus-schematic (LVS) is a powerful method to evaluate the effect of the layout parameters on the circuit. This process requires accurate parameter extraction. The inductance extraction tool *InductEx* developed by Fourie [99] in 2012 shows superior accuracy as compared to the predecessors, such as Lmeter [100]. Building on top of FastHenry [101], InductEx accurately analyzes the 3D layout structures while supporting specific SCE effects as kinetic inductance. Integration of InductEx within the LVS flow is described in [102] and [103].

C. Logic Synthesis

Since mid-1990's, numerous works proposed novel methods for logic synthesis of RSFQ circuits. In [104] and [105], for example, the RSFQ networks are created directly from binary decision diagrams using the RSFQ demultiplexer [106]. In [107] and [108], semiconductor logic synthesis tools, such as Berkeley SIS and Synopsys Design Analyzer, are adapted to handle RSFQ logic. However, the lack of compatibility between semiconductor and superconductor EDA was soon exposed [109]. Due to the different encoding based on pulses (RSFQ and RQL) and excitation currents (AQFP), SCE circuits require *path balancing* – equalization of logic levels of each gate fanins [100]. In addition, SCE networks require insertion of splitters that are asynchronous in RSFQ and RQL, and clocked in AQFP [111]. The buffer and splitter insertion required for path balancing incurs a significant overhead, often dominating the layout area [111], [112], [113], [114], [115]. Thus, different approaches have been proposed in the literature to tackle this fundamental issue.

1) Path Balancing in RSFQ Circuits: To illustrate the issue of path balancing, consider the logic network illustrated in Fig. 12(a). To ensure this circuit functions correctly in RSFQ, four path balancing DFFs and one splitter are inserted, as shown in Fig. 12(b). Given a fixed logic circuit topology, the polynomial-time retiming algorithms for area minimization [116], [117] can be applied to achieve path balancing with minimum number of DFFs [118]. Further reductions are however possible by combining logic synthesis with path balancing. One of the earliest works in this area is PBMap [119], where the cost of path balancing is estimated during the optimization process. Superior area and delay are however achieved by depth-oriented logic synthesis followed by minimum-area retiming [120]. This approach is adopted in the industrial RTL-to-GDSII Flow for RSFQ and ERSFQ circuits proposed in [121].

Several techniques have been proposed to enable clockless operation of RSFQ circuits. In *dynamic SFQ (DSFQ)*, the gates reset to the initial state after a controlled period of time [122]. The design of DSFQ circuits is therefore similar to CMOS circuits where large combinational blocks can be synchronized using relatively few synchronous elements [2]. Based on similar principle, the *xSFQ* technique is proposed in [123] where combinational logic is realized using dynamic `AND` and `OR` gates and is synchronized using regular DFFs.

Alternative set-reset schemes have been explored in the literature. In [6], the clockless logic gates are created using the nondestructive readout (NDRO) flip-flop. By controlling the arrival time of the data signals, the gates evaluate a function and reset within a single clock cycle, enabling clockless operation. A similar principle is explored in [124], where the clockless operation is achieved by delay-based encoding of the data.

In *dual clocking method (DCM)* [125], [126], a logic circuit is partitioned into separate clocking domains, relaxing path balancing requirements. The gates within a single domain are clocked at high frequency, while cross-domain transfer occurs at low frequency. Since the circuit throughput is determined by the slow clock, the DCM technique trades the throughput for area. Additional circuitry, such as pulse repeaters are however necessary to ensure correct operation of the system employing DCM [126].

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2) AQFP Buffer and Splitter (B/S) Insertion: Compared to RSFQ, AQFP logic synthesis is further complicated by the clocked nature of the splitters. An example of the AQFP system utilizing two buffers and three splitters is depicted in Fig. 12(c). The insertion of one (or more) splitters requires path re-balancing and thus the splitter insertion and path balancing problems are intertwined, requiring a different set of algorithms as compared to those used in RSFQ. The earliest algorithms for AQFP logic synthesis were based on Yosys [127] combined with a custom script to insert the splitters, and to remove the explicit inverter gates [128]. An heuristic algorithm for B/S insertion is proposed in [114]. A more comprehensive strategy for B/S insertion can be achieved by viewing it as a scheduling problem, by introducing a minimal number of splitters through an irredundant splitter insertion algorithm [129], and thus achieving an optimum solution for a given schedule. This scheduling problem can be solved in polynomial time. Further improvement can be achieved via *chunk movement* of parts of the circuit [129] and retiming [117], thus trading off various solutions corresponding to different schedules [111].

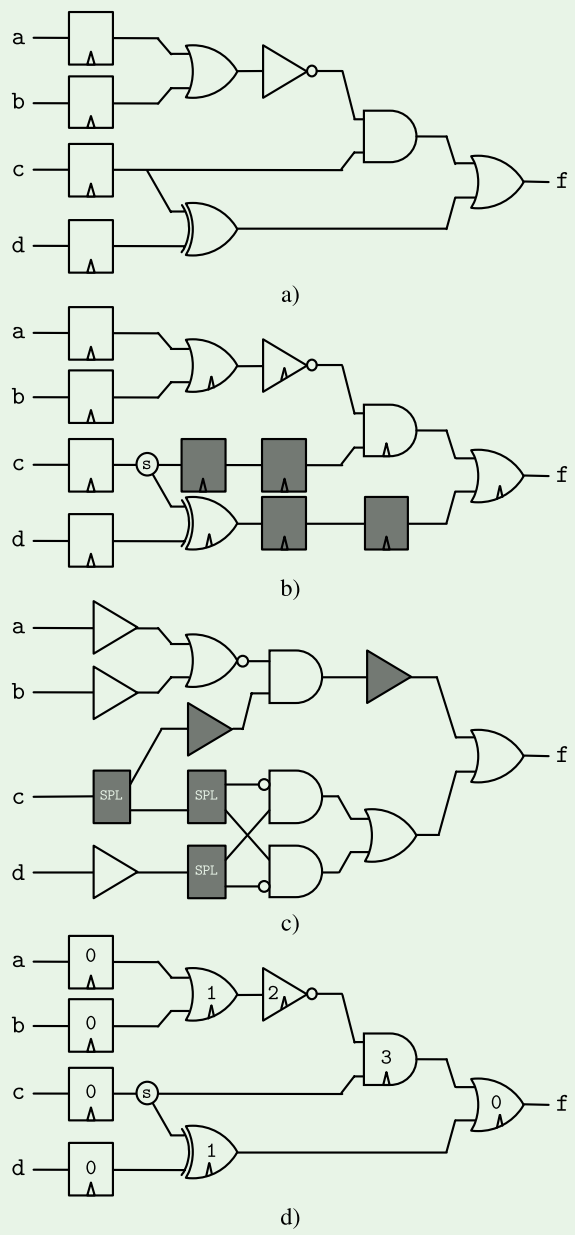

Figure 12. (a) An example of a CMOS circuit. (b) Equivalent RSFQ circuit with a splitter and four path balancing DFFs. (c) Equivalent AQFP circuit with three splitters and two buffers. (d) A four-phase SFQ realization with no path balancing DFFs. The numbers indicate the phase corresponding to each clocked gate.

The native gate in AQFP technology implements a majority function. For this reason, models and algorithms for majority-based logic synthesis are directly applicable to AQFP design. In particular, the *majority-inverter graph* (MIG) [130], [131] and the related algebraic and Boolean optimization algorithms were adopted for AQFP logic synthesis [54], [113], [115], [132], [133]. Fanout-bounded logic synthesis for AQFP circuits aims at structuring logic with limited fanout and hence lower splitter requirements. A key contribution of [134] is observation that by duplicating logic gates, fewer buffers and splitters can be required, thereby achieving superior area and delay. Fanout-bounded logic synthesis has then been formalized as an ILP, and solved exactly and heuristically [135].

V. Future Directions

Over the past decades, robust foundations in fabrication, circuit design, and EDA for SCE have been created. These foundations provide a fertile ground for further innovations. In addition, the computing landscape has significantly evolved in the past 25 years. A multitude of new computing domains has emerged, many of which are well-aligned with SCE. In this section, we survey those recent developments that we believe have the potential to shape the landscape of SCE in the near future.

A. Challenges

Despite the tremendous advancements in SCE circuit design and electronic design automation, SCE technology requires overcoming technological challenges before the widespread adoption can be achieved.

1) Fabrication Density: The state-of-the-art JJ fabrication process has the minimum feature size of 350 nm [136], accommodating approximately 6,000 JJs per mm^2 [137]. The circuit density produced using this technology is approximately two to three orders of magnitude smaller as compared to the modern semiconductor technology

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nodes. Overcoming this issue is critical to ensure VLSI-complexity SCE systems can be manufactured.

The SCE manufacturing technology has been developing at a rate slower than that of semiconductor electronics [138]. Over the past three decades, the number of JJs accommodated within a single circuit has been doubling every 4.5 years. This rate is significantly slower than the rate of CMOS scaling, doubling the transistor count every 1.5–2 years. Nonetheless, novel SCE applications, such as cloud and quantum computing, may attract the necessary investments towards achieving higher integration density.

2) Memory Density: A major advantage of semiconductor technologies over SCE is the large variety of available high-density memory technologies, including static, dynamic, resistive, and magnetic random access memory, as well as phase-change and racetrack memory, to name a few. The SCE however lacks comparably compact memory technology [139]. The nondestructive readout memory cells, for example, store information in the form of inductor current and are not amenable to scaling. Neither can SCE take advantage of the compact semiconductor-based memory technologies. The reading and writing energy in these technologies is approximately 100 times larger than the energy of the SFQ pulse, necessitating sophisticated amplification techniques. A similar issue is observed in hybrid superconductive memories utilizing memristors or magnetic tunnel junctions [139]. Furthermore, excessive read/write energy may produce significant heat, disrupting the superconductive operating mode [140].

B. Multiphase Clocking

Conventional VLSI systems utilize a single clock signal. This synchronization paradigm combined with gate-level pipelining enables SCE systems to achieve very high throughputs. However, the path balancing required by the deep pipelines produces prohibitive area overhead and potentially degrades the manufacturing yield.

Recently, multiphase clocking has been proposed as an effective method for reducing the path balancing overhead [141]. In multiphase clocking, the circuit is synchronized by several clock signals with equal frequency and different phase. By adjusting the phase of each gate, the datapaths can be balanced with fewer DFFs, as illustrated in Fig. 12(d). In [142], using two phases yielded a 25% reduction in total area as compared to the state-of-the-art single-phase methods. Increasing the number of phases to six brings area savings to 50%. Similar approach for AQFP B/S insertion is proposed in [143]. By adjusting the number of phases in AQFP circuits, the length of buffer chains can be significantly reduced.

The major advantage of multiphase clocking is the reduction in circuit area. In RSFQ, multiphase clocking facilitates timing closure, since only a low-frequency clock signal is distributed. Unlike DCM [126], no signal repeaters are necessary in multiphase systems. Similar to DCM, however, the throughput in an n-phase system is reduced by a factor of n, indicating the tradeoff between the area and the throughput.

Due to significant advantages in area and timing closure, multiphase clocking can become the mainstream technology for SCE VLSI systems. Nevertheless, no mainstream EDA tool currently supports multiphase clocking. Therefore, the EDA tools for timing analysis, clock skew scheduling, and clock network synthesis will have to be adapted to support the development of future multiphase SCE systems.

C. Gate Compounding Technique

Asynchronous RSFQ logic gates present an opportunity to realize a logic function without increasing the logic depth of the network. Conventional RSFQ technology, however, only contains two asynchronous gates, namely splitter and merger, as described in Section III-A. Recently, the gate compounding technique has been proposed in [36] and [118]. This technique exploits the synchronization mechanisms of the RSFQ gates, maximizing the functionality achievable within a single clock cycle, because of the extended functionality of compound gates. The key innovation of this technique is identification of three types of logic gates, namely AA, AS, and SA, where the first letter denotes whether input signals should arrive (a)synchronously, while the second letter indicates whether the output is released (a)synchronously. AA elements (merger and splitter) process the inputs immediately upon arrival and the output is released without a synchronizing signal (clock). AS elements (DFF, `NOT`, `XOR`) process the input information immediately upon arrival and release the output synchronously after the arrival of the clock signal. SA elements (`AND`, `OR`) require the inputs to arrive simultaneously. The result of the computation is released immediately after processing.

Based on these synchronization mechanisms, a generic compound gate structure is proposed in [36] and is illustrated in Fig. 13. Based on this structure, any SA gate should be preceded by an AS gate to operate correctly. In conventional RSFQ, this constraint is satisfied by DFFs. However, with gate compounding, other gates, such as `NOT` and `XOR`, can precede the SA gates, greatly enriching the logic functionality achievable within a single clock cycle. For example, single-cycle `XNOR` and `NIMPLY` gates can be realized using compound gates. Due to higher expressive power and smaller logic depth,

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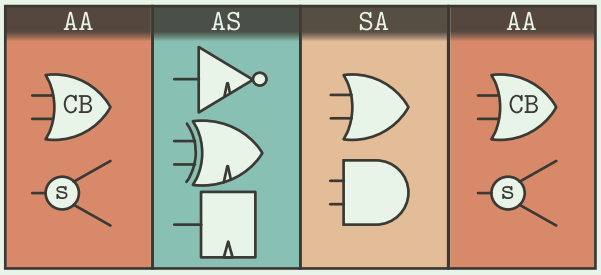

Figure 13. Generic compound gate structure.

circuits with compound gates achieve up to 55% smaller area as compared to conventional RSFQ circuits [118].

To fully realize the benefits of this technique, the conventional RSFQ cell library has to be extended to support the compound gates. In particular, standard cells for SA gates preceded by AS gates are needed to analyze their circuit level behavior. In addition, physical limitations of this technique need to be explored, such as the effects of interconnect delays or clock jitter.

D. All-JJ Circuits

As discussed in Section III, the most common issue in SCE is the reliance on inductors and magnetic fields. RSFQ systems, for example, require inductors to reliably store the flux quanta. These inductors are the primary obstacle to downscaling the RSFQ systems to densities competitive with conventional VLSI systems [27], [144]. While a valiant effort has been made to reduce the size of inductors [145], the novel inductor-free technologies may greatly reduce the need for inductors, further improving the integration density.

The behavior of a JJ is typically described using a special parameter φ called *Josephson phase*. The current flowing through a JJ is described by the RCSJ model as [146]

$$\frac{i(\varphi)}{I_c} = A\sin(\varphi) + B\sin(2\varphi) + \alpha\frac{d\varphi}{dt} + \frac{d^2\varphi}{dt^2}, \tag{4}$$

where φ is the *Josephson phase*, I_c is the critical current of the reference junction, and A and B are the coefficients of the first and second harmonics of the current-phase relationship. The JJs used in the standard RSFQ technology have negligible second-harmonic coefficient, i.e., $B \approx 0$. Such JJ has a single stable energy state at $\varphi = 0$, as illustrated in Fig. 14(a). Such JJs are therefore often called a 0-JJ [147].

Coefficients A and B can however be adjusted to realize different types of JJs. For example, the π-JJs, often realized as superconductor-ferromagnet-superconductor

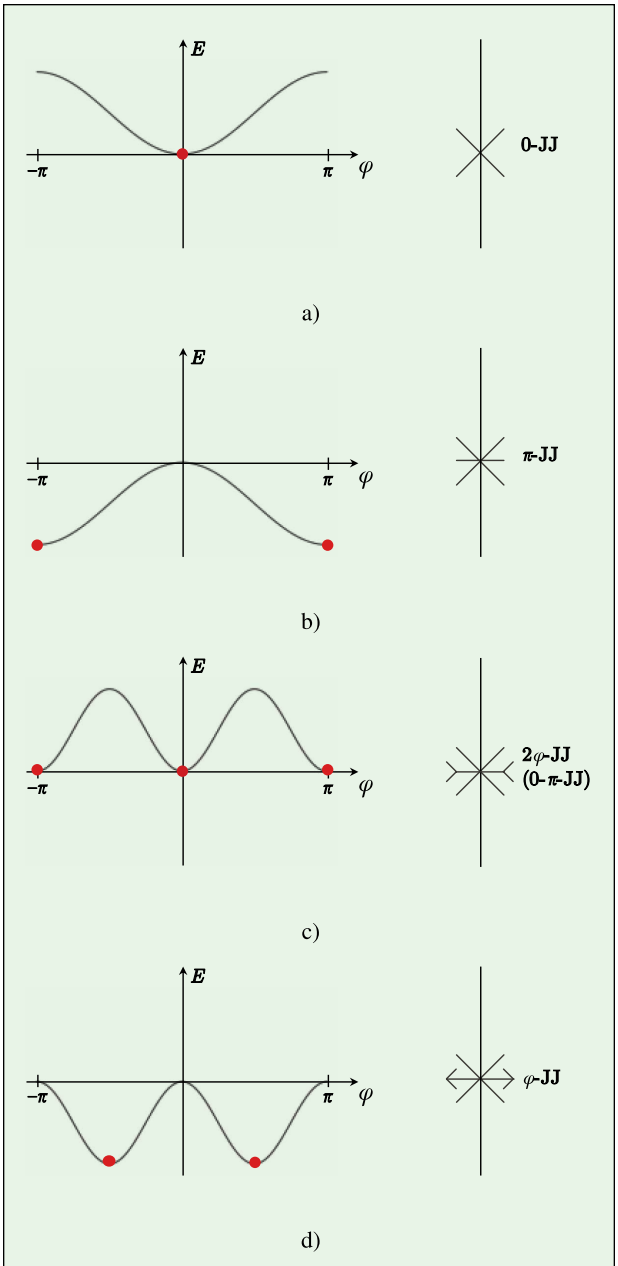

Figure 14. Energy-phase relationships and symbols of different versions of JJ [146]. (a) Regular 0-JJ. (b) π-JJ. (c) 2ϕ-JJ (0-π-JJ). (d) ϕ-JJ.

(SFS) junctions [148], exhibit a stable state at $\varphi = \pi$, as shown in Fig. 14(b). By introducing the π-JJs, the inductance required by a storage loop can be greatly reduced or even eliminated, enabling area-efficient storage loops [146], [147], [149], AQFP buffers [150], and logic gates [151], [152].

By eliminating the first harmonic coefficient (i.e., $A \approx 0$), the second harmonic dominates the current-phase relationship, producing two stable states. Setting coefficient $B > 0$ produces the 0-π-JJ (also referred to as

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Cryogenic operation and low power dissipation of SCE systems may bring the qubit control circuitry closer to the quantum IC, increasing communication bandwidth and reducing cooling requirements.

2φ-JJ) with two stable states at $\varphi = 0$ and $\varphi = \pi$, as illustrated in Fig. 14(c). A negative second-harmonic coefficient $B < 0$ produces a φ-JJ with two stable states at $\varphi = \pm\frac{\pi}{2}$, as illustrated in Fig. 14(d). The novel logic families based on bistable JJs have been recently proposed [146], [153], [154], exhibiting smaller area and power than the conventional RSFQ. Furthermore, high-speed superconductive memory based on 0-π-JJ has been proposed in [155].

Fabrication presents the primary difficulty in realizing the VLSI circuits with the bistable and π-JJs. The logic families utilizing unconventional JJs have only been demonstrated using numerical simulations, while only a few primitive prototypes have been fabricated [150], [156], [157]. In addition, the fabrication technology of the bistable and π-junctions is relatively immature as compared to the conventional 0-JJs. Currently, the area of a ferromagnetic bistable JJ is at least 2.5 times larger than the area of the 0-JJ in SFQ5ee process [158]. The demonstrated area of π-junctions is even larger, indicating the potential future scaling challenges [159].

E. Optimizations in Quantum-Flux Parametron Technology

Several optimizations in AQFP technology have been recently proposed, bringing significant improvements in the latency, density, and operating power. Similar to other SCE technologies, the primary issue of the AQFP scaling is large inductance due to the magnetic excitation and data transfer mechanisms. To alleviate this issue, *Directly-coupled Quantum-Flux Parametron* (DQFP) technology is proposed in [160] and [161], where the data transfer is realized electrically. Coupling inductors are however not completely eliminated due to the magnetic excitation mechanism. This mechanism reduces the size of the QFP logic gates by only 20%.

Further optimizations are achieved by adopting novel AQFP gates with large fanin and fanout. For example, the AQFP *Kogge-Stone-Adder* (KSA) built using the 5-input majority gate has recently been demonstrated in [162], achieving smaller area and latency. The majority function, fundamental to AQFP technology, is relatively inefficient for realizing two-input functions, such as `AND`, due to the additional buffer producing the constant `0` or `1`. By offsetting the excitation current, two-input gates can be realized by using only two input buffers [163].

F. Quantum Computing

Quantum computing is a rapidly developing domain of computing capable of achieving exponential speedup in such applications as quantum simulations [164], [165], linear systems of equations [166], and combinatorial optimization [167]. Currently, most advanced quantum computers are realized using superconductive qubits [168]. Maintaining precise control over these superconducting qubits, while ensuring they remain within the tight bounds of their low-temperature operational environment, is a complex and critical aspect of quantum computer development. Present quantum computing systems are constructed by linking cryogenic quantum chips with qubit control and classical measurement electronics at room temperature through long coaxial cables [169]. This method poses significant scaling challenges due to increasing heat load, latency, and noise as more devices are connected.

SCE is a promising direction for the development of large-scale quantum computing systems. Cryogenic operation and low power dissipation of SCE systems may bring the qubit control circuitry closer to the quantum IC, increasing communication bandwidth and reducing cooling requirements [170]. The use of SCE (particularly RSFQ) for interfacing with quantum ICs has been discussed in the literature since mid-2000's [171], [172], [173]. Many components of the quantum computing systems have been realized in SCE technologies [41]. For example, qubit control using SFQ pulse trains is proposed in [174], [175], and [176]. An integrated system for generating microwave qubit control signals using RSFQ technology is fabricated in [177], dissipating 51.7 microwatt, with potential reductions by adopting ERSFQ or eSFQ. High-speed SFQ-based multiplexers, demultiplexers, digital-to-analog and analog-to-digital converters have been demonstrated in [178] and [181].

To date, however, no integrated SCE co-processor system has been demonstrated, primarily, due to the limited integration density of the modern SCE ICs [41]. However, further developments in integration density [27], combined with the novel inductor-free logic families may pave the way for practical SCE-based quantum interfaces.

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VI. Conclusion

Over the last 25 years, superconductive electronics experienced a tremendous growth from a niche technology to one of the front runners of beyond-CMOS computing. In this article, we introduced the major SCE technologies, their strengths and limitations, as well as their development and prospects. The past 25 years brought us novel ultra-low-power superconductive digital technologies, namely ERSFQ, eSFQ, AQFP, and RQL. The complexity of SCE circuits increased 20-fold, bringing SCE into the domain of large-scale integration. Specialized SCE EDA tools are being developed to support this rapid growth. A multitude of novel algorithms tackle SCE-specific design issues, such as path balancing, buffer and splitter insertion, JJ modeling, and clock tree synthesis.

The achievements of the past decades position SCE as one of the most promising beyond-CMOS technologies. SCE computing is well positioned to address the future challenges brought by AI/ML applications as well as by data-intensive processing required to solve formidable problems in security, chemistry and climate modeling, just to mention a few. Moreover, the integration of SCE computing with sensing and communication makes this technology applicable to complex system design, such as those required for navigation and environmental defense. Overall, we have witnessed the tip of the iceberg emerging from the ocean of discoveries in physics and engineering of SCE, and we will soon be able to apply a more massive body of results and realizations for our digital future.

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