Devices and Circuits using Novel 2-Dimensional Materials: a Perspective for Future VLSI Systems

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***Abstract*—Here, we review the most recent developments in the field of 2D electronics. We focus first on the synthesis of 2D-materials, discussing the different growth techniques currently available and assessing their strengths and weaknesses. Moreover, we describe a possible roadmap to enable CMOS compatible integration of 2D materials. We then shift our attention to 2D devices and circuits, and review the state-of-the-art. Amongst the plethora of device concepts we look closely at 2D tunnel FETs (TFETs) and negative capacitance FETs (NC-FETs) for low power applications. We also put particular emphasis on doping-free polarity-controllable systems, that use electrostatic doping to eliminate the need for physical or chemical doping. We conclude with an analysis of simulations of scaled devices and discuss the possibilities enabled at circuit level by 2D electronics.**

***Index Terms*—2D materials, TMDCs, Beyond CMOS, integration, Growth, Transfer, Low power, polarity-control, doping-free, scaling.**

I. Introduction

RESEARCH on 2-dimensional (2D) materials has experienced remarkable growth in the last decade. Major semiconductor companies are looking with interest at this novel class of materials, in the hope of addressing the shortcomings that are making scaling of silicon-based electronic devices increasingly difficult.

Despite the diversity in conduction properties and atomic composition, all 2D materials are composed by covalently-bonded in-plane layers that are held together by weak Van-der-Waals interactions to form a 3D crystal. Each layer has a uniform thickness ranging from 0.3 to 0.7 nm, depending on its atomic structure (*e.g.* graphene is composed by a single layer of carbon atoms, while in general a transition metal dichalcogenide (TMDC) layer with a general formula of MX_2 is composed by a transition metal (M), sandwiched between two chalcogen atoms (X)) [1], [2]. The weak Van-der-Waals interaction are present in the out-of-plane direction thanks to the pristine surface of each layer, *i.e.* no presence of dangling bonds. This peculiar layered structure, together with certain optical and electrical properties, had already been discovered in 1947 for graphite [1] and in 1969 for TMDCs [2]. It wasn't however until the pioneering work of Novoselov *et al.* in 2004, that a graphite monolayer (now commonly know as graphene) was isolated and studied [3], effectively marking the beginning of 2D electronics. However, the semi-metallic nature of graphene prevents it to be used as the primary vehicle for novel digital transistors and circuits. Amongst TMDC materials, the most studied are the ones formed by group IV (zirconium (Zr) and hafnium (Hf)) and group VI metals (molybdenum (Mo) and tungsten (W)), however other materials formed by different metals, such as platinum (Pt), rhenium (Re) and tin (Sn) are currently gaining interest. These materials show a semiconducting behaviour and have exhibited excellent electrical properties [4]–[6], that will be further analyzed in Sec. IV. The presence of a sizeable bandgap (1-2 eV) makes TMDC materials appealing for electronics applications, as it allows us to realize devices with low leakage level and high ON/OFF current ratios [7]–[10]. Amongst the other remarkable features of TMDCs, their layered structure provides 2D films of controllable uniform thickness with dangling-bond free interfaces. Moreover, their extreme thinness and low in-plane dielectric constant alleviate short-channel effects (SCE) and drain-induced-barrier-lowering (DIBL) [11], [12], which are detrimental to device performance. The high effective mass of charge carriers (especially with respect to III-V materials) helps reducing direct source-to-drain tunneling at ultra-scaled dimensions [13], [14] providing a better control of the device OFF-state by the gate terminals. 2D materials are appealing for future VLSI systems and there are several areas in which they could bring novel functionality in electronic systems. However, several challenges still remain for high quality growth and successful integration, and experimental demonstrations are still far from simulated devices performances.

This review is organized as follows. In Sec. II, we focus on the synthesis of 2D-materials. We highlight the different approaches that are considered for growth of 2D materials on existing CMOS logic, back-end-of-the-line (BEOL) integration, and discuss the need for the development of an efficient transfer technique. We also focus on the possibility of synthesizing lateral and vertical heterostructures, which are appealing for TFETs applications. In Sec. III, we describe a possible roadmap to enable CMOS compatible integration of 2D materials, highlighting the main challenges that still have to be overcome. In Sec. IV, we shift our attention to 2D devices and circuits, and review the state-of-the-art. Amongst the plethora of device concepts, in Sec. V we look more closely

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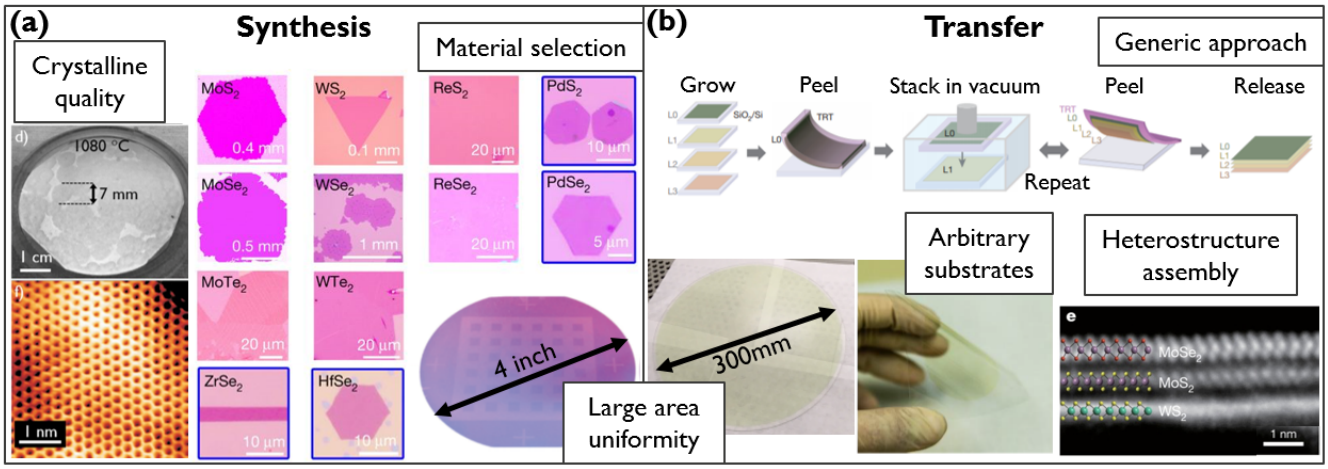

Fig. 1. Relevant metrics for synthesis and transfer of 2D materials, with notable examples. Crystalline quality and wide material selection are important to allow high performance devices. Transfer is a generic approach to allow integration in arbitrary substrates or assembly of heterostructures. Large area uniformity is essential to both synthesis and transfer, to allow low variability in material properties over wafer scales. Adapted with permission from [15]–[20].

at 2D tunnel FETs (TFETs) and negative capacitance FETs (NC-FETs) for low power applications. Sec. VI is dedicated to doping-free polarity-controllable systems, that use electrostatic doping to eliminate the need for physical or chemical doping on 2D materials. Finally, in Sec. VII, we look at scaling opportunities for different types of 2D devices and evaluate their projected performances.

II. Synthesis and Transfer of 2D Materials

The first works with monolayer (1L) and multilayer (ML) 2D materials were all done on exfoliated flakes, from the pioneering work on graphene [3], which led to a Nobel Prize in physics, to several demonstrations with transition metal dichalcogenides (TMDCs) [7], [21]–[23]. Exfoliation results in high crystalline quality flakes which are used to understand the fundamental properties of 2D materials, and pave the way for future applications. The non-deterministic nature of mechanical exfoliation, however, leads to fluctuations in flake thickness, lateral size and shape, all of which make it non-scalable to industrial integration. Logic circuits have been demonstrated on such exfoliated flakes [8], [24]–[27], but most reports involve a small number of devices and low level of integration. If 2D materials are to be considered for CMOS integration, large-area, uniform and high quality synthesis becomes a critical aspect to realize their full potential for future electronic circuits. Fig. 1(a) presents relevant metrics for the synthesis of 2D materials, namely the crystalline quality (*e.g.* grain size) of the grown layers, the possibility of growing a number of different materials and the large area uniformity of the synthetic layer. Two main synthesis approaches exist: growth directly on the device wafer, as often done for TMDCs [15], [17], [28], or growth on an optimized substrate, with a subsequent transfer step [18], [29] for integration. The optimal growth substrate changes with respect to the 2D material grown, with metal films being used for graphene [16], [30] and crystalline hexagonal-Boron Nitride (h-BN) [31], while the best results for TMDCs have been obtained with sapphire [32], [33] or silicon dioxide (SiO_2) [34]. Direct growth is limited by the maximum temperature allowed at different process steps, especially when 2D materials are co-integrated with a standard silicon CMOS technology. This poses as a challenge, since heterogeneous co-integration is an attractive route to enhance the speed or functionality of silicon chips by employing 2D materials alongside current architectures. Examples include using graphene boosting for interconnects [35], where the presence of a graphene layer leads to a resistivity reduction in the metal line, and 2D TMDC transistors at the back-end-of-the-line (BEOL) [36], which can provide further functionalities in the framework of 3D scaling. However, if growth is limited to 450° C, for BEOL integration, the resulting material, in particular 2D TMDCs, is highly defective [37], [38]. Besides prohibitive temperatures, the growth environment (corrosive or metal-containing gases) can also result in lower reliability of the dielectric where the 2D material is grown. When using a dedicated growth substrate, the temperature limitations are lifted, which allows this approach to achieve high crystalline quality [30], [32]. The growth substrate can be carefully selected and tailored to achieve the best possible synthesis, where layer-by-layer growth has been demonstrated with precise atomic control and reduction of strain and doping effects [39]. This temperature flexibility comes at the expense of an additional transfer step, which decouples the growth parameters from the device integration.

Transfer allows high quality 2D materials to be integrated onto arbitrary substrates, which ranges from standard CMOS wafers (either in the front-end-of-the-line (FEOL) or BEOL) to flexible substrates [18]. It is, in principle, a generic approach, which allows the manipulation of different 2D materials with the same method [20]. In the context of logic devices, uniform transfer of large area 2D materials is a key challenge. Transfer relies on interface interactions between the original substrate, 2D material, and the target wafer, and is normally done using water or acid assisted intercalation [18], [29], [40], [41], which can introduce additional contamination or material

modifications [42]–[44]. Understanding those interactions and being able to develop an all-dry process is critical to achieve uniform and repeatable transfer which has minimal impact on the 2D material. By allying 300 mm growth capabilities with standard wafer bonding tools, a uniform 300 mm dry transfer was recently reported [19]. Fig. 1(b) illustrates the transfer process, with notable examples of each of these metrics. Besides transferring the 2D materials onto arbitrary substrates, understanding the interactions present after transfer and the impact of different substrates is also necessary. During this integration step, the 2D material is transferred onto a wafer surface, which may have a series of non-idealities such as roughness, topography, surface chemistry, contamination, among others. Due to the atomically thin nature of the 2D material, it is highly sensitive to the surrounding environment, and these non-idealities can cause unintentional doping, strain and increased defectivity. This surface must be carefully engineered in order to result in stable and reliable transistor operation. Current understanding is that other 2D materials are the ideal substrates for both graphene and TMDC devices [45]–[47].

In the context of transistor fabrication, heterostructures are inherently required, either between TMDCs and conventional metals and oxides, or more exotic TMDCs/graphene, TMDC/hBN or TMDC/TMDC heterostructures [48], [49]. Those can be relized by the two techniques discussed above, either *in situ* growth or assembly *ex situ* through transfer. Growth of vertical (WSe_2/SnS_2, MoS_2/WSe_2, WS_2/MoS_2, graphene/h-BN, *etc.*) [50]–[53] and lateral (WS_2/WSe_2, WSe_2/MoS_2, WS_2/MoS_2, *etc.*) [51], [54] heterostructures presents encouraging results. The main figure of merit in terms of heterostructures are atomically abrupt interfaces, be them vertical or lateral, since this is an important requirement for applications such as tunnel FETs (as will be discussed in Sec. V-A). This is why, *in situ* growth of the heterostructure – as opposed to assembly *ex situ* – is an appealing technique, where the presence of contamination at the interfaces is drastically reduced. In vertical heterostructures atomically-sharp junctions are easier to be obtained, since the layered nature of 2D materials can be exploited, but achievements in terms of growth techniques also allows atomic stitching of lateral heterostructures [54], [55]. Nonetheless, high quality, large-area heterostructure assembly has also been demonstrated either by sequential transfers of different 2D materials one on top of the other [56], or by using a 2D material to pick-up a different one [20], [57]. Beyond their use in established transistor architectures, heterostructures also present interesting physical phenomena, such as tightly bound excitons [58], [59] and plasmonic effects [60], [61], which can lead to exciting new device concepts in the future. These considerations in terms of growth and transfer of 2D materials lead us to the discussion of what are the required milestones to be achieved for their integration with current CMOS technology.

III. Roadmap for CMOS integration of 2D materials

When evaluating the integration of 2D materials on future consumer and industrial applications, several different aspects should be taken into account. Their atomically thin nature and high mechanical strength make them perfect candidates for high-performance flexible electronics [25], [63]. Their electronic structure, featuring an indirect-to-direct band gap transition, makes them promising for opto-electronics [64]. Their large surface-to-volume ratio results in great potential for both energy storage [65] and sensing [66] applications. While other roadmaps include these aspects [67], [68], we will primarily focus on the potential of 2D materials as speed and functionality boosters alongside standard CMOS technology. 2D materials are excellent candidates for this application due to their ultra-thin and self-passivated nature, and for featuring high mobilities even at the atomic thickness limit.

For that to turn into reality, the 2017 IEEE IRDS roadmap [69] mentions several requirements which have to be fulfilled, which are listed below. The list combines requirements for graphene (●), TMDCs (○), and shared requirements (◐). We would like to add that some of the aspects IRDS mentions only for graphene, are also challenges for TMDCs, and are added as shared requirements in the list below:

- ● Band gap formation with high mobility and ON/OFF ratio greater than 10^4
- ● Armchair/zigzag nanoribbon formation
- ○ Improvement of contact resistance
- ◐ Large-area synthesis with low defect density
- ◐ Growth or transfer at controlled locations
- ◐ Growth or transfer of high quality material at low temperature
- ◐ Thickness control
- ◐ Defect-free contacts
- ◐ Techniques for doping
- ◐ Characterization and imaging of nano-scale structures and composition

Fig. 2 outlines the core steps of technology development for 2D material integration in the CMOS process flow. With hundreds of 2D materials currently being isolated or synthesized, selecting a few materials from this growing library becomes an important integration decision. Material selection can be done by benchmarking against current silicon technology, as proposed by Agarwal *et al.* [70], or can be done based on application-specific requirements, with tunnel FETs being the most attractive example [71]–[73]. Another integration option is to select based on stability of the material in ambient and process availability of high quality large area materials. Irrespective of how to select them, a few materials have already attracted special attention, such as graphene, MoS_2, WS_2,WSe_2, hBN and black phosphorus (BP).

Modelling and simulation are key elements for device and circuit design and fabrication, and will be the focus of Sec. VII. Modelling is essential to understand device functionality, especially the impact of contact barriers, non-idealities and possible defects on the transistor functionality [62], [74]–[78]. Important advances are being made in terms of fundamental material and device understanding [79]–[81]. Besides the important design guidelines it generates, simulation tools are

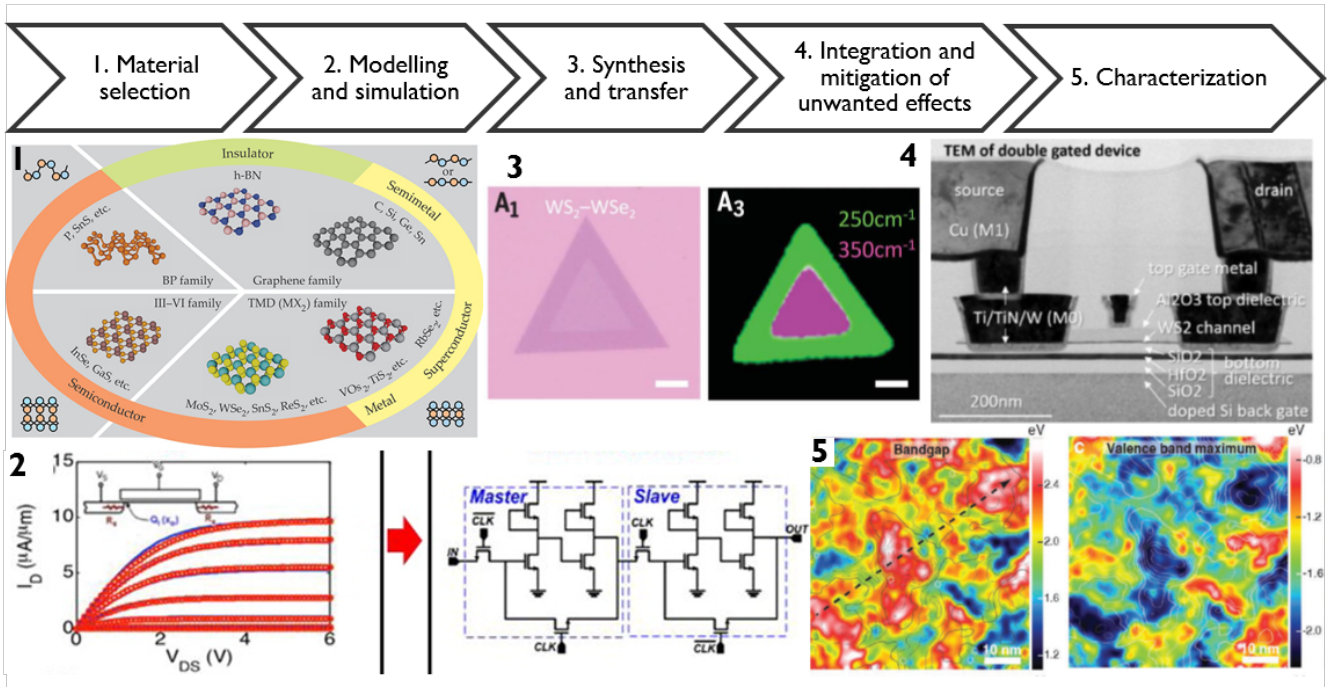

Fig. 2. Roadmap for Integration. Required steps for 2D material to reach product stage. Adapted with permission from [19], [46], [54], [62].

also essential ingredients if widespread circuit design with 2D materials is the objective.

Synthesis and transfer, as discussed in detail in Sec. II are challenging steps which aim to achieve materials with high crystalline quality, controlled thickness at the atomic scale, and integration with arbitrary substrates. Encouraging results from growth of large single crystals and precise heterostructures [54] were demonstrated. When 300 mm integration is the goal, two main routes for transfer emerge: wafer-to-wafer transfer on complete 300 mm blankets [19], or die-to-wafer positioning of small crystals [82].

The integration core step includes upscaling successful lab-scale processes to industry-compatible 300mm platforms, but also mitigating of unwanted effects arising from substrates, encapsulating materials or device processing. Some works have explored mitigation of unintentional doping and strain for both graphene and TMDCs [44]–[46]. Linked to integration is also the precise modulation of the electrical properties of the devices, such as threshold voltage (V_{TH}) and polarity. The precise control of V_{TH} of different devices is critical for correct circuit operation, and while great efforts have been made in the direction of doping, a standard is yet to emerge [83]–[86]. Furthermore, while some materials present either *n*-type or *p*-type conduction, others combine both, opening interesting routes for doping-free devices and optimized circuit design, as will be discussed in depth in Sec. VI [27], [87], [88].

For most processing steps, characterization techniques are essential to assure yield and reliability. While current 2D material characterization allows probing several properties, wafer scale characterization techniques are still not mature. The core techniques used to probe 2D material quality are Raman spectroscopy, photoluminescence and atomic force microscopy [89]–[91] . Techniques to understand interface properties are not fully developed and are essential for achieving reliable and stable transistors [46], [92], [93]. In-line metrology will surely need additional techniques in order to fully probe the reduced dimensions and specific properties of 2D materials. Importantly, the development of a standardized characterization toolkit capable of measuring from material quality to electrical characteristics, including interface properties, is still pending.

In conclusion, in order to realize the full potential of 2D materials as boosters in VLSI systems, several technological developments are still necessary spanning from better quality of the grown material, to the development of an efficient transfer technique to the upscaling of processes to 300mm platforms. However, the recent progresses shown in the understanding of the properties of 2D materials and the demonstration of novel devices keep the research field vibrant and appealing to industries and universities. We now review the state-of-the-art for 2D electronics based on TMDCs and graphene providing insights on the most recent developments in the field.

IV. State of the Art for Experimental Devices and Circuits

Since the first demonstration of a monolayer (1L) MoS_2 transistor with high mobility and high ON/OFF current ratios in 2011 by Radisavljevic *et al.* [7], the field of two-dimensional electronics has gained worldwide traction with a constant increase in the number of publications and a growing interest of the research community. Among the several semiconducting

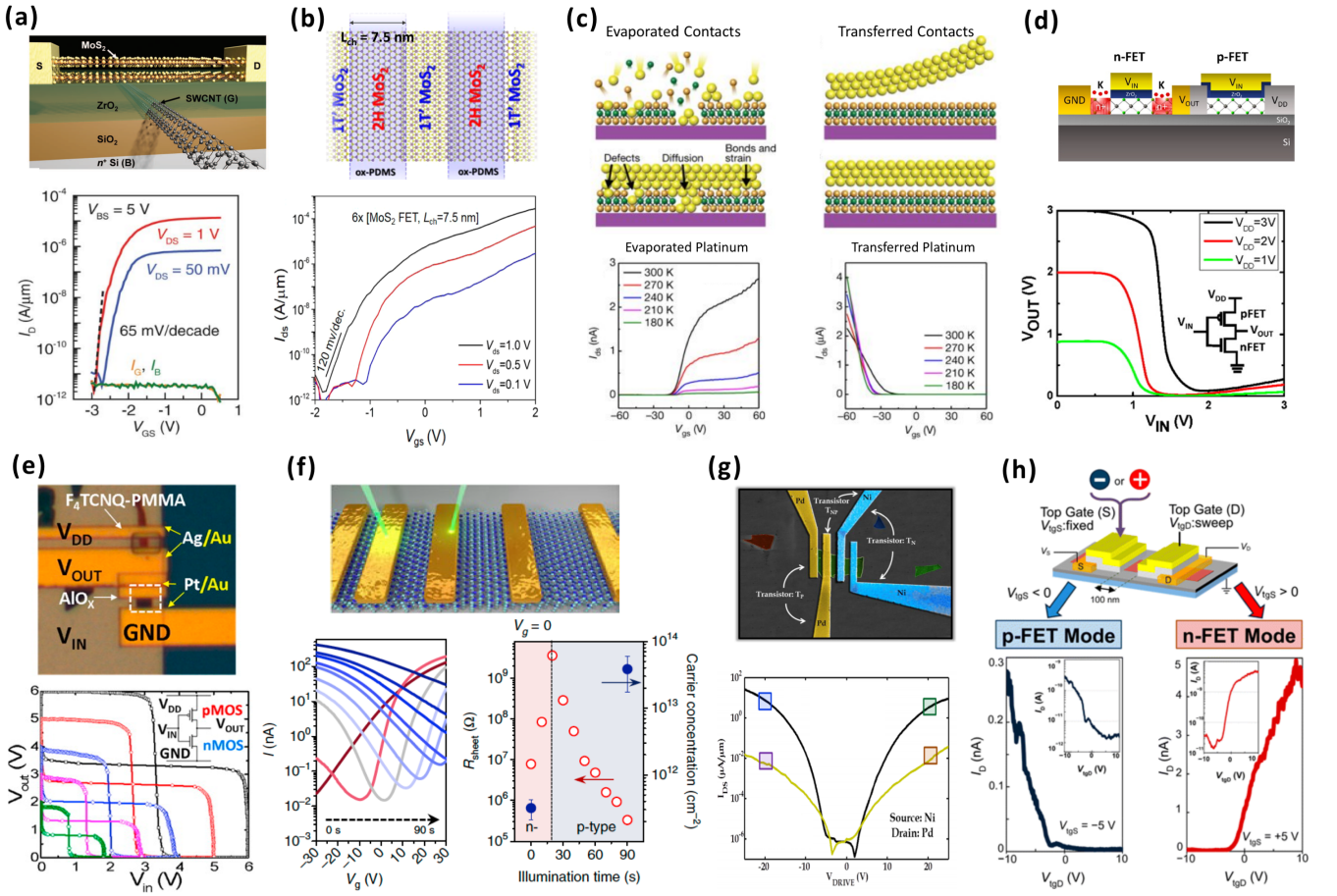

Fig. 3. 2D-TMDCs electronics. (a) Schematic depiction and transfer characteristics of a MoS_2 device gated by a single carbon nanotube. Adapted with permission from [94]. (b) Ultra-scaled MoS_2 devices fabricated with lithium induced change to the metallic phase. Adapted with permission from [95]. (c) Comparison between the transfer characteristics of a MoS_2 device with evaporated and transferred platinum contacts. It is shown how *p*-type condcution can be achieved on MoS_2. Adapted with permission from [96]. (d) Demonstartion of a high-gain complementary inverted realized with chemically doped WSe_2. Adapted with permission from [10]. (e) Chemical doping and different metal contacts, to provide better carrier injection for electrons and holes, are used to demonstrate logic gates on WSe_2. Adapted with permission from [9] (f) Ligh-induced defects on $MoTe_2$ cause *p*-type doping of the 2D semiconductor, allowing for the development of complementary logic. Adapted with permission from [97]. (g) Ambipolar characteristics of WSe_2 device. Adapted with permission from [98]. (h) Ambipolarity and polarity-control demonstarted on exfoliated $MoTe_2$. Adapted with permission from [99].

materials belonging to the TMDCs family, and introduced in Sec. II the most appealing for electronic application have been Molybdenum (MoS_2, $MoTe_2$ and $MoSe_2$) and Tungsten compounds (WSe_2 and WS_2). These semiconducting materials are stable in air, even in their monolayer form, are easily exfoliated from commercially available bulk-crystal and are also grown with high-quality in large-area, as shown in Sec. II. Several major results presented in the following sections have been achieved using mechanical exfoliation, which despite being a non-scalable approach, provides high-quality flakes that are used to gain insights on the properties of these materials and assess their potential for electronic applications. Fig. 3 summarizes few of the most noticeable experimental results of the last years.

The most known TMDC material, MoS_2, has proven to be a viable solution for the realization of *n*-MOS transistors [7], [8], [24], [100], [101] and ultra-scaled devices have been recently demonstrated [94], [95], [102] (see Fig. 3(a,b)). In Fig. 3(a), a single carbon nanotube was used to gate a transistor with MoS_2 semiconducting channel, proving the superior electrostatic control achievable thanks to the ultra-thin MoS_2 [94]. In Fig. 3(b), devices with gate length below 10 nm were realized by inducing a change to the metallic phase of the MoS_2, with a lithium solution. This process also allows for a reduced contact resistance thanks to the metallic MoS_2 forming a seamless contact scheme with the 3D metal [103]. To date, the largest circuit reported on 2D MoS_2 is a 1 bit microprocessor composed of 115 transistors [104], and other small circuits have also been previously demonstrated [8], [24], [105]. However, due to considerable difficulties in achieving *p*-type behavior in MoS_2 [106], these circuits all adopt a non-complementary *n*-MOS logic, that is not power-efficient. It has recently been demonstrated how *p*-type conduction can be achieved on MoS_2 by transferring metal contacts on top of the 2D material, rather than evaporating it [96] (see Fig. 3(c)). Using this innovative technique, it has been possible to show an almost linear relationship between the work function of the contact metal and the height of the Schottky barrier created, and *p*-type conduction has been achieved with high work function metals (such as Gold and

Platinum). Being able to develop both *n*- and *p*-type devices on the same semiconducting material is extremely important in order to achieve complementary operation of logic gates and circuits. Conventional CMOS uses ion implantation to physically dope silicon creating low-resistance ohmic contacts and irreversibly setting the polarity of the fabricated device (*n*- or *p*-type) according to the dopant atoms used (Arsenic (As) for electron and Phosphorus (P) for hole doping). Since a reliable physical doping technique for 2D materials is still lacking, chemical doping techniques have been explored to both reduce contact resistance (thus achieving higher ON-current) and to achieve complementary behavior [9], [10], [107]–[110]. These techniques are often tailored to the specific material used, in order to dope it against its natural carrier concentration (i.e. *n*-doping for WSe_2 and *p*-type doping for MoS_2 and WS_2). The growth conditions also determine the natural carrier concentration of the materials, and it is important to develop techniques that allow the growth of high-quality, intrinsic materials in order to precisely tune specific doping processes. Using WSe_2 as semiconducting material, complementary operations of inverters and other small logic gates has been recently shown (see Fig. 3(d,e)) [9], [10]. However, chemical doping is often non-scalable, non-stable and non-compatible with conventional CMOS fabrication. An innovative doping strategy has recently been proposed where a strong light source is used to locally create defects in $MoTe_2$ semiconducting channels, that upon oxidation induce *p*-type doping [97] (see Fig. 3(f)). This technique has allowed the realization of photovoltaic cells and bipolar-junction-transistor (BJT) arrays [97]. The possibility of using two different 2D semiconductors to separately develop *n*- and *p*-type transistors has been explored using MoS_2 to fabricate *n*-MOS device and monolithically integrate WSe_2 *p*-type devices on top, demonstrating complementary logic gates [26]. This work shows the potential of 2D materials to be used in combination with CMOS for 3D monolithic integration. An alternative to the use of either chemical or physical doping is the exploitation of the ambipolar behavior, which refers to the capability of a semiconductor to conduct both charge carriers, and has been shown on several 2D semiconductors such as WSe_2, $MoTe_2$, WS_2 and $MoSe_2$ [98], [111]–[114] (see Fig. 3(f,g)). A more comprehensive discussion on the opportunity to use the ambipolar behavior to realize doping-free and poalrity-controllable devices is presented in Sec. VI. Other 2D materials that are being explored include members of the TMDCs family such as $HfSe_2$ and $ZrSe_2$ that are appealing since their native oxides HfO_2 and ZrO_2 are CMOS compatible [115], and also black phosphurus (BP). BP in particular has recently drawn considerable interest thanks to its high carrier mobility, ambipolar nature and lower semiconducting bandgap compared to TMDCs [25], [87], [116]–[118]. However, BP is non-stable in ambient condition and only few minutes of air exposure results in a complete oxidation of the semiconducting layer, making it challenging to integrate in a conventional VLSI fabrication flow [119]. While TMDCs and BP have been extensively studied for the fabrication of novel electronic devices, graphene, due to its semi-metallic nature and high carrier mobility [120], is mainly considered to be integrated in VLSI systems for interconnect scaling [121], [122]. Monolayer graphene is explored as diffusion barrier and capping layer to extend scaling of conventional Copper (Cu) interconnects [121], [123], while multilayer graphene, in the form of nanoribbons, is looked at for entirely replacing Cu interconnects [121], [124]. One of the major challenges is the development of a technique that would allow to grow high-quality graphene at BEOL-compatible temperatures (*i.e.*, 450° C). Recently, a low-temperature process to grow graphene has been demonstrated and upon doping with $FeCl_3$ graphene nanoribbons of 20nm width have shown lower resistivity than copper. It is expected that by improving the fabrication process and the doping technique, multilayer graphene interconnects could provide at least 4× smaller circuits delay compared to conventional Cu interconnects [124]. Graphene-based interconnects are also considered for future fully 2D systems [125] and flexible electronics [126]–[128].

Following this general overview, we focus on the experimental results of two classes of devices: tunnel-FETs (TFETs) and negative capacitance FETs (NC-FETs) for low power applications and polarity-controllable FETs for doping-free circuits.

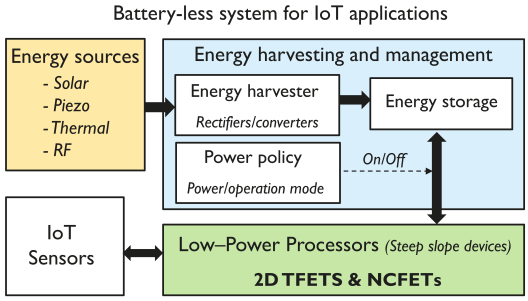

Fig. 4. Overview of Self-sustainable energy harvesting system using low power device alternatives. Adapted with permission from [129]

V. Devices for Low-Power Applications

In order to scale the supply voltage in future technology nodes, and provide more energy-efficient systems, several alternatives based on low power devices are currently being explored. These devices are targeted to reduce the supply voltage to less than 0.5 V by reducing the subthreshold swing (SS) below 60 mV/dec. Besides the benefit in power consumption for VLSI systems, low power devices could enable the realization of power-efficient processors powered by energy harvesters for internet-of-things (IoT) applications [130]–[132] as well as low-voltage static-random-access memories (SRAMs) [131]. Fig. 4 shows a schematic of a self-sustainable (battery-less) energy harvesting system which uses an ambient energy source such as solar, piezo or thermal to power a processors based on 2D tunnel-FETs (TFETs) or ferroelectric FETs, also know as negative-capacitance FETs (NCFETs) [129]. NC-FETs are also being explored for energy-efficient non-volatile computing which is attractive for IoT applications [132]–[134]. This section focuses on TFETs and NCFETs, as several promising demonstration of these classes of devices have been shown using 2D-materials.

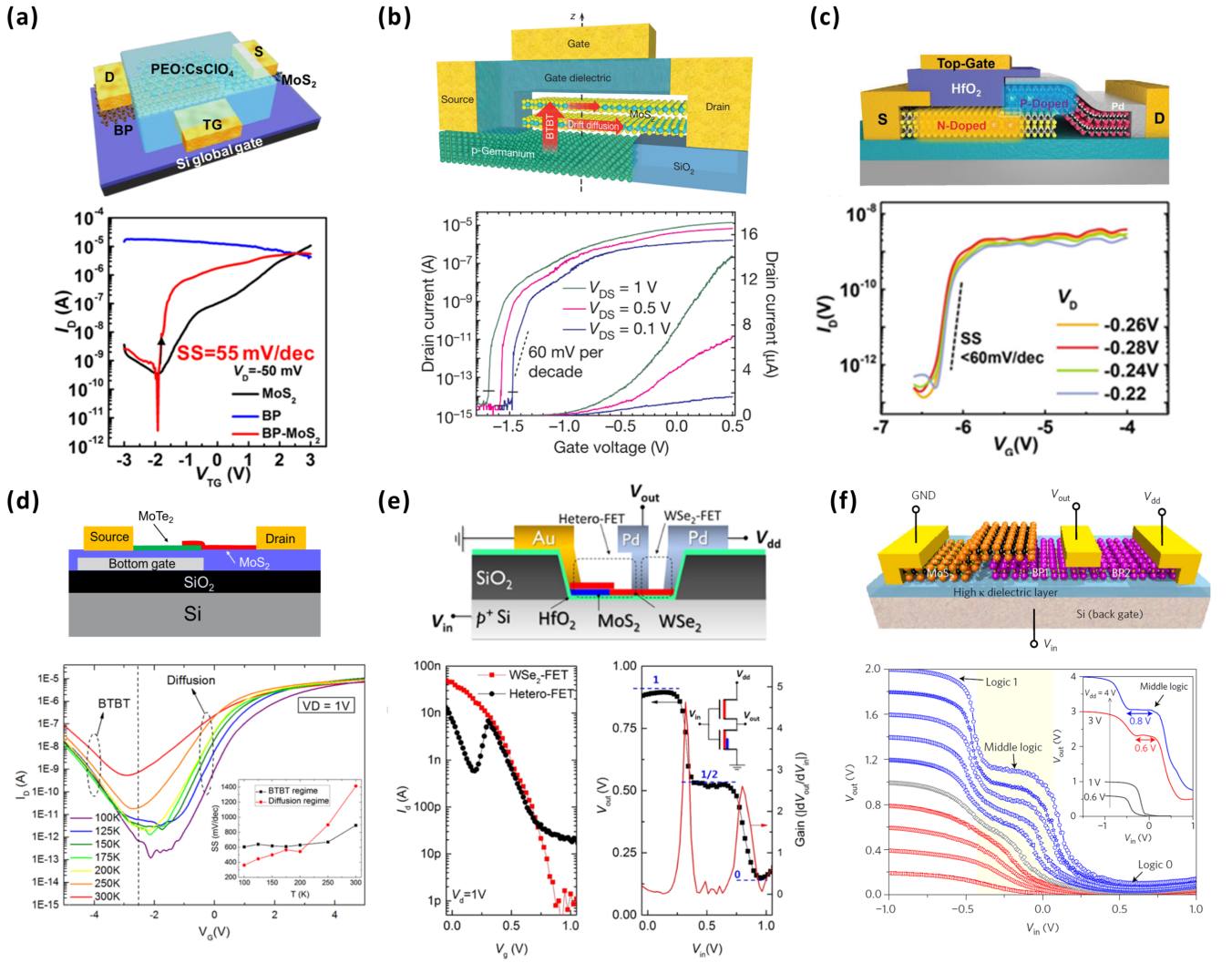

Fig. 5. Experimental results of 2D TFETs. (a) Device schematic and $I_D - V_G$ curve of a MoS_2-BP TFET with electrolyte gating. Adapted with permission from [135] (b) Device schematic and transfer characteristics of a Ge-MoS_2 TFET with electrolyte gating. Adapted with permission from [136]. (c) Schematic cross section and $I_D - V_G$ of a MoS_2-WSe_2 TFET with an isolated gate device. Adapted with permission from [137]. (d) Schematic cross-section and transfer characteristics of MoS_2-$MoTe_2$ with an isolated bottom gate. Adapted with permission from [138]. (e) Device cross-section and $I_D - V_G$ curve of a MoS_2-WSe_2 heterostructure FET showing negative-differential-transconductance (NDT) and multi-valued-logic (MVL) operation. Adapted with permission from [139]. (f) Device schematic and transfer characteristics of a MoS_2-BP heterostructure FET showing NDT behavior for MVL applications. Adapted with permission from [140].

A. Tunnel FETs

TFETs are one of the candidates to replace conventional CMOS for future technology nodes due to their low supply voltage (V_{DD}) requirement and steep sub-threshold slope (SS) at room temperature. The capability to achieve an SS lower than the thermionic limit of 60 mV/dec is enabled by the different conduction mechanism used in these devices. In fact, current flows in a TFET thanks to quantum mechanical tunneling of carriers from the valence band maximum of one material to the conduction band minimum of the other material, while in conventional MOSFETs conduction is dominated by drift-diffusion mechanisms [141]. In recent years, much research has focused on realizing TFETs with semiconductors from group IV and III-V. It has been shown that materials with a direct band gap, such as III-V compounds, can provide higher ON currents with lower supply voltage compared to indirect bandgap materials. This is because indirect bandgap materials require additional energy to compensate the mismatch in momentum when tunneling from the conduction band to the valence band [142]. Moreover, III-V materials have low bandgaps and high electron mobilities, which are ideal for TFET performances. A good figure of merit to measure the TFET current performance is the I_{60} current, which is the maximum current value up to which the subthreshold slope is less than 60 mV/Dec [143]. In order for TFETs to compete with CMOS technology, the minimum required I_{60} current is 10 μA/μm and an ON current of at least 100 μA/μm [142]. However, experimental demonstrations are still far away in reaching these goals. The main reason being that III-V materials show a high density of trap states both at the dielectric and at the heterojunction interface, due to lattice mismatch, which degrades the band-to-band tunneling (BTBT)

mechanism [144]–[146]. Therefore, monolayer 2D materials appear to be an ideal candidate for the realization of vertical hetero-structures TFET applications, thanks to their atomically thin body, direct bandgap and self-passivating surfaces, that could result in no dangling bonds at the interfaces. The advantage of using monolayer 2D materials is evident from simulation studies [147], [148], however it has not yet been confirmed by the experiments, which often use few-layer semiconductors [135]–[140].

Most experimental demonstrations with 2D materials, aim at achieving BTBT by forming a vertical heterostructure between a 2D *n*-type material such as MoS_2, WS_2, ReS_2, $SnSe_2$ and a 2D *p*-type material like WSe_2, $MoTe_2$, Black Phosphorous (BP), to create a vertical tunneling heterojunction. Heterostructure stacks such as MoS_2-WSe_2 [137], [139], [149], [150], MoS_2-$MoTe_2$ [138], $SnSe_2$-WSe_2 [150], $SnSe_2$-$MoTe_2$, MoS_2-BP [85], [140], [151] have all shown to exhibit BTBT. Fig. 5 displays a summary of the state-of-the-art for 2D TFETs. Fig.5(a) shows a MoS_2-BP heterostructure TFET fabricated using an electrolyte gating with a steep subthreshold of 55 mV/dec as shown in the $I_D - V_G$ characteristics [135]. Fig. 5(b) shows an example of a 3D-2D based tunneling approach where germanium (Ge) is stacked with MoS_2 to form a TFET. The $I_D - V_G$ characteristics of Ge-MoS_2 [136] are shown with an average SS of $\sim$31 mV/dec, using electrolyte gating. This SS is the lowest reported on TFETs to date. The advantage of using a bulk material is that they can be easily doped (not yet possible with 2D materials, as discussed in Sec. IV) to provide a lower band offset. This, combined with a 2D material, can lower scattering and provide improved electrostatics thus leading to more efficient tunneling [152]. However, as previously mentioned, great care needs to be taken when dealing with the 3D-2D interface in order to minimize the trap states at the surface. In Fig. 5(c), a MoS_2-WSe_2 TFET is fabricated with two separate gates enabling the individual modulation of the *n*- (MoS_2) and *p*-type (WSe_2) materials [137]. The device also shows SS less than 60 mV/dec. Fig. 5(d) displays a MoS_2-$MoTe_2$ TFET that also follows the previous approach of having an isolated bottom gate that modulates $MoTe_2$ and not MoS_2. The $I_D - V_G$ characteristics shows a temperature dependent BTBT current which occurs due to the recombination/generation currents present at higher temperatures [138]. The devices in Fig. 5(a) and (b) follow a complete top/bottom gate configuration approach, where both the *n*-type and *p*-type materials are modulated with the same gate potential. However, a major drawback is that this device architecture can hinder the possibility of creating a broken band alignment for tunneling if the materials are not doped enough. Moreover the Schottky contacts are also modulated simultaneously with the heterostructure which can degrade the steep switching in the device [138]. The isolated gate approach shown in devices of Fig. 5(c) and (d) has the advantage of modulating the carrier concentration of the individual *n*- and *p*-type materials when neither of the materials are highly doped. However this configuration is more complicated to fabricate as it requires two gates per transistor, which is not ideal in integration point of view. Fig.5(e) shows a MoS_2-WSe_2 heterostructure FET that shows the phenomena of negative differential transconductance (NDT) in the $I_D - V_G$ characteristics [153]. A similar behavior is also shown by a MoS_2-BP heterostructure FET (see Fig 5(f)). The NDT phenomena can be exploited to create devices that support multi-valued logic (MVL), and MVL inverters have been demonstrated with 2D TFETs [139], [140], [154]. Thanks to the higher number of logic states and higher data storage density, MVL logic is considered to be a promising alternative to traditional binary logic.

Despite the large amount of experimental work on 2D TFETs, not many devices have shown a steep SS of less than 60 mV/Dec. This is possibly due to several factors such as the presence of Schottky contacts at the metal-semiconductor heterojunction [138], [155], the high density of interface traps at the semiconductor-oxide interface and the presence of defects and grain boundaries in the 2D materials. Further experimental work is needed to improve the performances of 2D TFETs and enable their integration in VLSI systems.

B. Negative Capacitance FET

Negative capacitance FETs (NCFET) have recently shown promising performances for steep switching application. Unlike TFETs, that obtain the steep switching through band to band tunneling, NCFETs still use a conventional drift-diffusion conduction mechanism, paired with a ferroelectric gate dielectric. The steep switching is enabled by the phenomena of negative capacitance that arises from the transient response of the ferroelectric dielectric while switching its polarization. A ferroelectric material has two polarized states which can be altered from one state to another with an external applied bias [160]. When the polarization state is switched, the charge to voltage variation becomes negative (*i.e.*, $dQ/dV < 0$). This negative value of dQ/dV corresponds to a negative differential capacitance and when inputted in the equation of SS, results in a subthreshold swing less than 60 mV/dec [161], [162]. The phenomena of negative capacitance could act as a performance booster for any CMOS platform, even conventional silicon FinFETs, by improving both the subthreshold slope and the overdrive voltage [163]. However, 2D materials are attractive for NCFETs because, thanks to their atomically thin body and high mobility, they can respond to a change in polarization more rapidly than a bulk semiconductor.

Several works have focused on the integration of ferroelectric materials in Si MOSFETs and FinFETs to achieve steep slope performance, and CMOS compatible hafnium oxide based ferroelectric materials have been demonstarted by doping hafnium oxide (HfO_2) with materials such as Al, Zr, Si. 2D-based NCFETS using Al and Zr doped HfO_2 and other ferroelectrics have been shown to have steep switching characteristics, as discussed below [166]–[168]. Moreover, there has been considerable interest in the recent demonstration of an NCFET using a 2D semiconductor (MoS_2), as well as a 2D ferroelectric oxide $CuInP_2S_6$ (CIPS) [169]. A considerable and yet unsolved issue with NCFET is the large hysteresis that arises from the ferroelectric material while shifting the polarization state [160]. Hysteresis could be reduced by capacitance matching between the ferroelectric and dielectric layer.

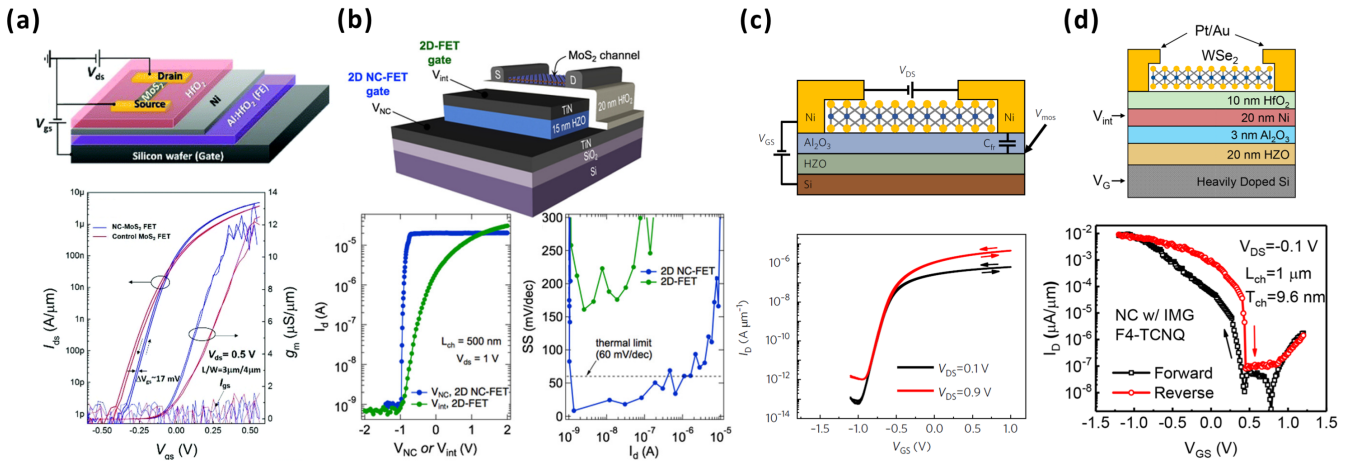

Fig. 6. Experimental researches results on 2D-NCFET based on different 2D materials and ferroelectric gate stacks, respectively. (a) The structure schematic and $I_D - V_G$ curve of the MoS_2-NCFET with ferroelectric Al:HfO_2 layer. adapted with permission from [156]. (b) The structure schematic and $I_D - V_G$ and SS curves of the MoS_2-NCFET with ferroelectric hafnium-zirconium-oxide (HZO) layer. Adapted with permission from [157]. (c) Schematic cross-section and $I_D - V_G$ characteristics of the MoS_2-NCFET with ferroelectric HZO without an IMG layer. Adapted with permission from [158] (d) Schematic cross-section and transfer characteristics of the WSe_2-NCFET with ferroelectric HZO layer. Adapted with permission from [159] .

This complicated process aims at achieving a single energy minimum in the energy landscape of the resulting capacitor, thus reducing or eliminating hysteresis, which originates from the presence of two energy minimum [170], [171]. Design guidelines for NCFETs should thus include specifications for the tolerance range of hysteresis, as addressed in [172]. However, in order to achieve a steeper SS most of the NCFETs reported in literature are fabricated with an internal metal gate (IMG), placed in between the ferroelectric and dielectric layer, that makes capacitance matching impossible to obtain and enhances the histeretic behavior [173].

Fig. 6 displays several 2D NCFETs fabricated with and without an IMG architecture. Fig. 6(a) show a schematic cross-section of a MoS_2 NCFET using Al:HfO_2 dielectric with a Ni IMG layer [156]. The $I_D - V_G$ shows a low hysteresis with a slight improvement in SS of 57mV/dec compared to when only gating it with regular HfO_2. Fig. 6(b) shows a schematic cross-section of a MoS_2 NCFET using hafnium-zirconium oxide (HZO) with a TiN IMG layer [157]. The $I_D - V_G$ displays a very steep SS with a minimum of 6.07 mV/dec when compared to the regular MoS_2 FET. However a very large hysteresis is also observed for this device. Fig. 6(c) shows a MoS_2 NCFET with HZO as ferroelectric without an IMG layer [158]. The $I_D - V_G$ has very small hysteresis, however with the trade-off of a larger SS of 52.3 mV/dec. For this device, the drain ON-current level, I_{ON}, of 510 µA/µm is among the highest values for state-of-the-art steep-slope FETs reported so far [174]. A *p*-type NCFET using WSe_2 was also realized as shown in Fig. 6(d) using HZO ferroelectric with an IMG layer [159]. The device dimensions and their performances in terms of SS and ON-current are summarized in Table I, which also includes other notable examples. The devices are separated into two types, metal ferroelectric metal insulator semiconductor (MFMIS) - the devices that contain an IMG layer and metal ferroelectric insulator semiconductor (MFIS) - devices without an IMG layer. The devices have shown to obtain a steep SS below 60 mV/dec and have shown more promise compared to its TFET counterpart. All the reports used exfoliated flakes with a majority of the work done using MoS_2 and different ferroelectric materials.

Apart from improving performances of CMOS devices, NCFETs have other potential applications such as to realize nonvolatile flip-flops for IoT applications, provided that the polarization of the ferroelectric layer is maintained in the absence of gate voltage [133]. As mentioned earlier, the hysteresis created by the introduction of the ferroelectric material is detrimental for purely logic applications, but if properly controlled could improve the noise margin on SRAMs [132]–[134]. Moreover, the possibility of dynamically tuning the hysteresis to the zero-gate-voltage region will create novel

TABLE I
STATISTICAL TABLE OF EXPERIMENTAL RESULTS ON 2D-NCFETS

No.	2D Material	FE Material	Type	L_{ch}	V_d	I_{60}	I_{ON}	lowest SS	ref
2	MoS_2	HZO	MFMIS	500 nm	1 V	5 µA	5 µA	6.07 mV/dec	[157]
3	MoS_2	Al:HfO2	MFMIS	3 µm	0.5 V	500 pA	13 µA	57 mV/dec	[156]
4	MoS_2	P(VDF-TrFE)	MFIS	80 nm	0.5 V	10 nA	100 µA	24.2 mV/dec	[164]
5	MoS_2	HZO	MFMIS	1 µm	0.5 V	100 pA	10 µA	37.6 mV/dec	[165]
6	MoS_2	HZO	MFIS	2 µm	0.5 V	N/A	510 µA	52.3 mV/dec	[158]
7	WSe_2	HZO	MFMIS	1 µm	0.1 V	200 pA	10 nA	14.4 mV/dec	[159]

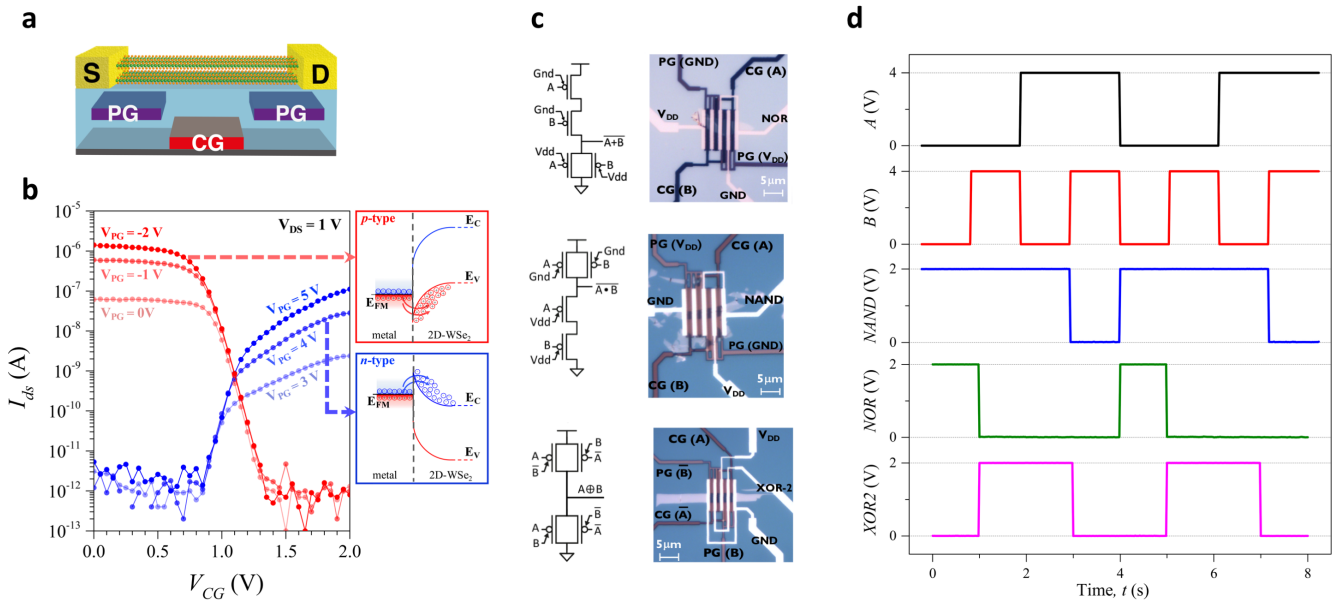

Fig. 7. Polarity-controllable devices and circuits.(a) Schematic cross-section of a single polarity-controllable device, highlighting the presence of the PG acting at the contact interface and the CG placed in the central region of the channel. (b) Transfer characteristics demonstrating polarity-controllable behavior. The insets show a schematic depiction of the band-bending at the contacts for *n*- and *p*-type operation. (c) Optical micrograph and circuit schematic of the fabricated NAND, NOR and 2-input XOR gates. (d) Quasi-static measurements of the doping-free logic gates, demonstrating proper operation. Adapted with permission from [27]

memory-logic interchangeable circuits for energy harvesting processor and in-memory computing [129]. As a final remark, it is worth mentioning that NCFETs offer extensive dynamic voltage frequency scaling (DVFS) with wide range of power-performance options [175], [176]. This feature can be applied to low voltage near-threshold computing, that is an active area of research with attractive energy efficiency [176], [177].

VI. Polarity-Controllable Doping-Free Devices and Logic Gates on WSe_2

Physical doping, through ion-implantation, of 2D material has not proven to be successful due to extreme thinness of the 2D semiconductors, with ions just implanting in the substrate. The possibility of introducing dopant atoms (such as rhenium (Re) or niobium (Nb) for MoS_2) during growth of the 2D material as been reported, but lacks selectivity and does not allow for any control of the doping profile [178]–[182]. Several chemical and molecular doping techniques have been developed, and have been addressed in Sec. IV, but are often non-stable and non CMOS compatible, thus not allowing integration of chemically-doped 2D devices in the BEOL fabrication of VLSI circuits [9], [10], [107]. A device concept that would not rely on any physical doping, and use un-doped materials, would be of great interest in this regard. When no physical or chemical doping is introduced (i.e, an un-doped material is used), contact to a 2D-semiconductor usually results in the creation of a Schottky barrier at the source and drain contacts. The height of the Schottky barrier determines the conduction properties of the device, as un-doped materials are, for the most part, able to conduct both charge carriers (*i.e.*, electrons and holes). However, it is challenging to control the OFF state of a purely ambipolar device when using a standard gate configuration, as we cannot selectively suppress the conduction of a specific type of charge carriers [98] [183]. In order to control the polarity of the transistor and achieve either *n*- or *p*-type behavior a separate gating of different channel regions is introduced, which we refer to as double-independent-gate (DIG) structure [183]. A second gate is added, namely polarity gate (PG), that induces electrostatic doping at the contact interfaces, effectively modulating the height of the Schottky barrier and blocking the injection either of electrons or holes. It is then possible to dynamically reconfigure the device polarity at run time, by reversing the bias applied to the polarity gate. A conventional gate, named control gate, acts in the central region of the channel, and controls the ON/OFF state of the device. The possibility to dynamically flip the polarity at run-time enhances the switching property of the devices enabling a doping-free, highly flexible design for logic circuits [184], [185]. Differently from the TFETs and NCFETs, DIG-FETs do not inherently provide a way to reduce the SS below the limit of 60 mV/dec, although steep switching has been demonstrated on Si FinFETs with a DIG structure by increasing the V_{DS} bias and achieving weak-impact ionization of charge carriers [186]. Moreover the application of ferroelectric oxide to a DIG-FET structure could be foreseen in future research.

As mentioned in Sec. IV, ambipolar behavior has been demonstrated on several 2D materials (such as WSe_2, $MoTe_2$, $MoSe_2$ and BP), with WSe_2 showing high mobility and high current densities for both charge carriers [98], [187]–[190]. Recent progress in the demonstration of 2D polarity-controllable doping-free devices and circuits have been made using WSe_2 and are summarized in Fig. 7 [27]. A schematic cross-section of a single device in presented in Fig. 7(a), highlighting the position of the PG and CG as well as the semi-

conducting channel. The devices are fabricated experimentally on exfoliated WSe_2 and the demonstration of polarity-control is shown in Fig. 7(b). The inset shows a schematic depiction of the band profile at the source contact for two opposite biases of the PG. When the PG is biased at 0 V or below, holes are favorably injected in the channel and the device behaves as a *p*-type transistor. Conversely the transistor is programmed to function as a *n*-type device when the PG is biased at 3 V and above. In both cases, the CG is able to turn ON and OFF the transistor when swept between 0 and 2 V. A standard-cell library has been demonstrated with doping-free polarity-controllable WSe_2 FETs including inverters, NAND, NOR, XOR and MAJ gates (see Fig. 7(c,d)). The DIG structure results in a more expressive switching function of the fabricated devices which act as comparison driven switches (*i.e.*, the device is conducting when both PG and CG are controlled by the same logic value). Thanks to the higher expressivity of the single device, it is possible to realize compact 2-input XOR gates using only 4 transistors (not counting the inverters needed to generate the negate signals), while in CMOS 8 transistors would be necessary. The peculiar switching properties of the devices also enable the fabrication of 3-input XOR and 3-input MAJ using only 4 transistors and replacing the V_{DD} and GND terminals with logic inputs [27], [185]. The possibility of realizing highly compact XOR and MAJ gates has been explored in the synthesis of arithmetic circuits, as will be discussed in Sec. VII. The challenges that need to be addressed to enable the use of polarity-controllable devices in VLSI systems include achieving a symmetric behavior of the *n*- and *p*-branches by tuning the Schottky barrier at contacts, reach *p*-type behavior without the need to apply negative gate voltages (to ensure cascadability) and operate both gate terminals with the same voltage bias.

The experimental results presented in Sec. IV, V and VI show the potential of 2D semicondcutors for several applications, but simulations are essential to better evaluate the strength and weakness of different devices. In the following section we will focus on the most recent simulation results for 2D devices and circuits.

VII. Performances projection at scaled device dimensions

The need for modeling and simulation to assess the performances of devices and circuits at scaled gate dimensions has already been highlighted in Sec. III as one of the critical steps in the roadmap. It is crucial to rely on accurate simulations to understand the scaling possibilities for different classes of devices, compare their performances and assess circuit level metrics. Simulations can also provide guidance and insights to improve the fabrication process (*e.g.* which metal provides the lowest contact resistance or which oxide lowers the phonon scattering). Scaled device characteristics for 2D materials have mainly been studied using *ab-initio* methods, where the band structure extracted from density functional theory (DFT) calculations [195] is used within a non-equilibrium Green functions (NEGF) formalism to derive the current-voltage characteristics of a device [196]. These simulations require a high computational cost, that increases tremendously when several conduction and valence bands are considered in the Hamiltonian and when scattering is introduced in the simulations [197]. They are also only suitable for single scaled-devices simulations. In order to reduce the computational cost and extend the simulations to circuit level several compact models have been proposed that are able to reproduce the results of NEGF simulations or experimental results for both doped-FETs and TFETs [62], [74]–[78], [198]. Using these compact models, circuit simulations have shown that 2D materials could theoretically outperform conventional Si-FinFETs and meet ITRS performance and power-delay requirements [62], [199]–[202]. Fig. 8 summarizes some of the main simulation results both at device and circuit level for the 3 main classes of devices presented in this review (*i.e,* conventional doped 2D-FETs, 2D-TFETs and doping-free 2D-FETs). We excluded considerations on NC-FETs as simulation results on scaled devices and circuit perspectives are still lacking for 2D materials.

1) Doped 2D-FETs: For 2D-doped FETs, it was found that a double-gated structure, as the one presented in Fig. 8(a), provide better electrostatic control on the channel, particularly when using a few-layer 2D material. Work from Cao *et al.* [11] and Szabo *et. al.* [197] have focused on understanding the impact of charge and phonon scattering on the device performances (see Fig. 8(b)) and have shown that even at ultra scaled dimensions (L_G = 8 nm) scattering can reduce the ON-current considerably. As mentioned in Sec. III, material choice can be guided by several factors, such as intrinsic device performances, fabrication simplicity or stability of the 2D materials. In this context, several simulations have been performed to assess which 2D material can provide the best device performances [11], [12], [14], [70], [191], [201] (see Fig. 8(c)). Thanks to the possibility of low-temperature integration (see Sec. II), the performance projection of monolithically integrated 2D-FETs have been studied (see Fig. 8(d)) [70]. Simulations including parasitic capacitances and wire loads have shown how devices based on WS_2 could be able to provide lower energy-delay-product (EDP) than conventional Fin-FETs in future technology nodes [70]. Moreover a 32-bit commercial processor core has been implemented with 5-nm design rules to assess the benefits of 2D transitors on a large-scale design [199]. It was found that 2D-FETs can provide $\sim 2\times$ better energy-delay-product (EDP) with respect to conventional Si Fin-FETs, provided that a contact resistivity $< 6 \times 10^{-8} \Omega \cdot \mu m^2$ can be achieved [199].

2) 2D-TFETs: The schematic structure of a scaled TFET exploiting band-to-band vertical tunneling between a *p*- and *n*-type semiconductor is shown in Fig. 8(e), with a schematic depiction of the band levels and effective masses [148]. As shown in Fig. 8(f), the transfer characteristics of the scaled devices appear promising reaching ON-currents greater than 100 µA/µm, having I_{60} of around 1 µA/µm and operating at V_{DD} = 0.5 V. These simulations, although promising, are purely ballistic and not include any effect arising from scattering, traps and contact resistance. Other works have also investigated different geometries and materials [203]–[206].

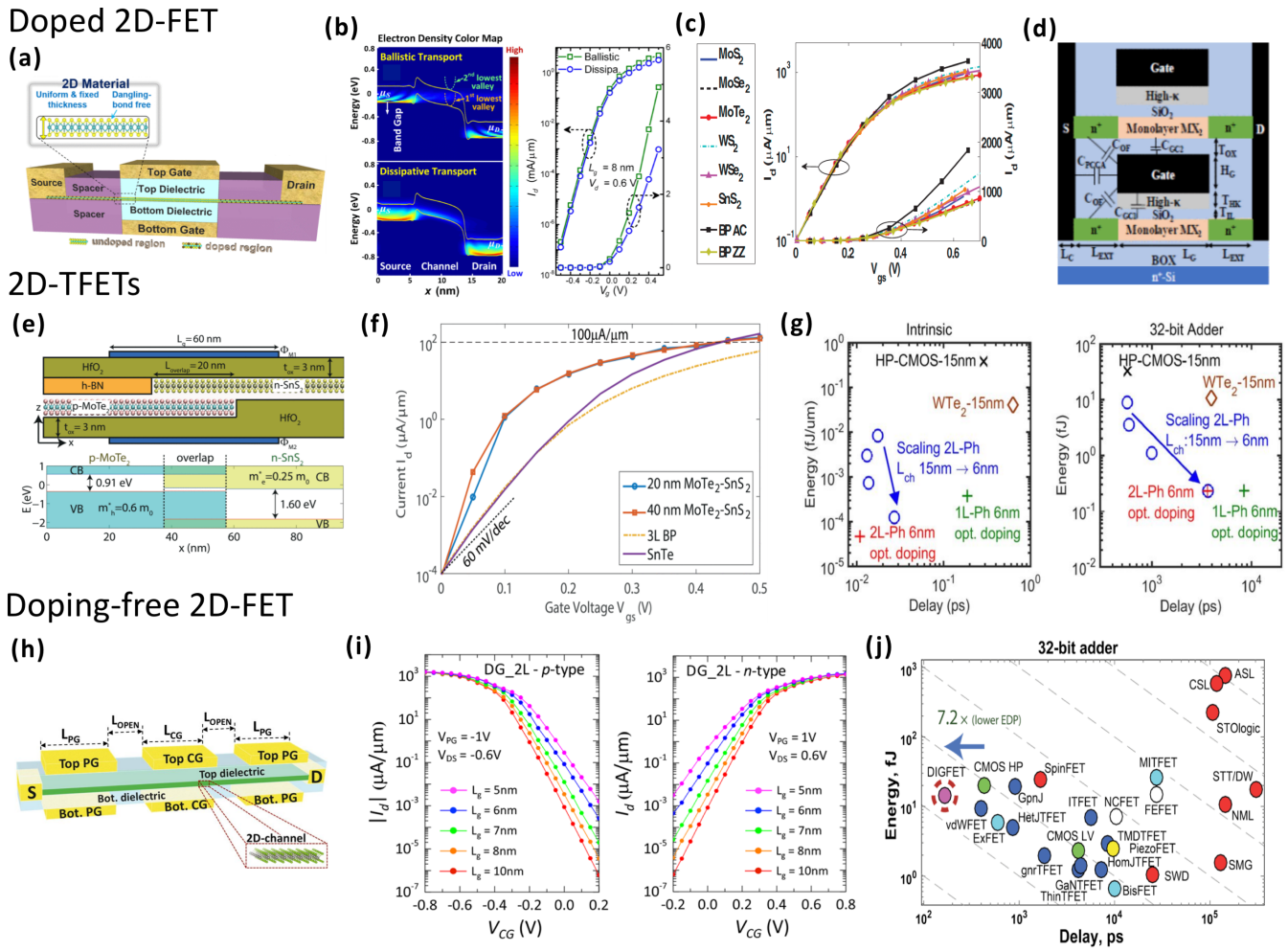

Fig. 8. Device and circuits performances at scaled gate lengths. (a) Schematic depiction of a double-gate FET with doped contacts. Adapted with permission from [11].(b) Electron density color map and transfer characteristics of the scaled device in (a) showing the effect of scattering on the performances of the device. Adapted with permission from [11]. (c) Comparison of transfer characteristics for several 2D TMDCs and BP. Adapted with permission from [191]. (d) Schematic illustration of a monolithically integrated device with MX_2 materials that is bench-marked against conventional Si-FinFETs. Adapted with permission from [70]. (e) Schematic cross section of a scaled TFET device, showing the band alignment between the 2D semiconductors. Adapted with permission from [148]. (f) Transfer characteristics of the device in (e), showing steep-switching and relatively high ON-current. Adapted with permission from [148] (g) Study of EDP improvements both at device and circuit level for ultra-scaled BP-TFETs. Adapted with permission from [192]. (h) 3D schematic illustration of the simulated polarity-controllable FET. (i) Transfer characteristics for the device in (h) showing the feasibility of polarity-control down to 5 nm gate lengths. Scaling of the channel length results in an increased SS, as also demonstrated for conventional doped 2D-FETs in [11]. Adapted with permission from [193]. (j) EDP projection for a doping-free 32-bit adder realized with polarity-controllable 2D-FETs. The use of polarity-controllable 2D-FETs enables a $\sim 7\times$ reduction in EDP compared to scaled high-power CMOS. Adapted with permission from [194].

As mentioned in Sec. V-A BP is a material that has attracted considerable interest for TFETs applications and its performances at scaled gate lengths have been studied [192] and compared to high-performance (HP) CMOS as in the beyond-CMOS benchmark [207]. In this case, no heterostructure is used and the BTBT takes place between the heavily *p*-doped source and the heavily *n*-doped drain through and intrinsic region (*i.e., p-i-n* structure). Fig. 8(g) shows the switching energy *vs* delay, a metric usually referred to as energy-delay product (EDP), for the intrinsic scaled BP device and for a 32-bit adder realized with 2D-BP TFETs. It is demonstrated that thanks to the lower bandgap, 2-layer BP with asymmetric optimized doping provides the most improvement in EDP. However, it can be seen in Fig. 8(g) that the improvements in EDP for the 32-bit adder are not as significant as the ones promised by the intrinsic EDP. This is caused by the presence of interconnects and parasitic capacitances, that in the sub-10nm regime play a critical role.

3) Doping-free 2D-FETs: Using a scaled double-gated structure, see Fig. 8(h), the performances of doping-free polarity-controllable devices have been assessed by Resta *et. al.* in [193], using ballistic NEGF simulations. It is shown how a reduction in the semicondcuting bandgap of the MX_2 material can lead to higher ON-currents (due to improved tunneling at the contacts) while maintaining sufficient electrostatic control over the channel to switch OFF the device (see Fig. 8(i)). For a bandgap energy of 0.8 eV, the I_{ON} can reach 1.5 μA/μm, while keeping I_{OFF} well below 10^{-2} μA/μm down to $L_G = 5$ nm. It should be noted that due to the presence of the additional PG, the device is inherently longer than conventional CMOS, and in the simulations L_G refers to the length of each gated segments, either PG or CG. The simulated

transfer characteristics for the 10 nm devices were used to simulate the behavior of a 32-bit adder, which is compared to other technologies of beyond-CMOS benchmark [194], [207]. Thanks to the design possibilities enabled by polarity-controllable devices at circuit level, *e.g.* compact realization of XOR and MAJ gates, it was shown a $\sim 7\times$ reduction in energy-delay product (EDP) when compared to high-performance scaled CMOS (see Fig. 8(j)) [194].

VIII. Conclusion and Perspective

This paper provided an overview of the recent advances in the field of 2D electronics. We focused on three different aspects that are equally relevant for the evaluation of novel materials and novel devices considering material synthesis, experimental demonstrations and projections of device performances. We looked closely at novel device concepts that have been boosted by the properties of 2D materials such as TFETs and NCFETs and also provided an in-depth discussion on the possibility of realizing doping-free 2D circuits thanks to polarity-controllable devices. For each topic we highlighted the main achievements and evaluated the challenges that remain to be addressed in order to integrate 2D materials into VLSI systems. This integration can be fruitful by using 2D materials alongside conventional silicon CMOS, where we could envison 2D-TMDCs circuits being integrated in the BEOL and graphene nanoribbons used for interconnects. A truly 3-dimensional nanosystem could be enabled by the low-temperature fabrication process required by 2D materials leading to dense 3D monolithic VLSI systems, integrating memory, sensors and electronics on the same chip [208]. Moreover, foldable and flexible electronic system could also greatly benefit from the thinness and large area availability of 2D materials, enabling more compact and portable wearable systems.

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