Designing Robust Systems with Uncertain Information

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System engineers are facing new opportunities and challenges at the beginning of this new century. Silicon technology has progressed even more rapidly than expected, and the increased miniaturization of devices enables monolithic system to realize very complex functions. New emerging technologies have matured, and start being candidates for replacing silicon-based technologies in the coming years. At the same time, the task of system design has become harder, because of the stringent requirements on monolithic systems in terms of performance, reliability and energy consumption. The design challenges are direct consequences of the technological progress, and are due to the extremely *small* nature of electronic devices, the extremely *large* complexity of systems, and the *new*, unchartered territory set by novel technologies.

As miniaturized devices approach the physical limits of operation, the characterization of their parameters becomes an increasingly harder task. The spread of physical parameters complicates design, as traditional, conservative worst-case design approaches may hinder the advantages of using extremely scaled-down devices. New, aggressive design methods may address the problem by using self-calibrating circuits and error-resilient computation and communication. Such methods will be based on a design paradigm shift: electrical level information may happen to be corrupted, yet systems will yield reliable services because means are provided to correct for such errors. At the same time, the amount of effort spent in correcting information may be used to calibrate operational parameters (e.g., voltages) so that error rates fit within desirable bounds.

Digital circuit design will have to cope with increasingly more detailed analog circuit features and varying operational environments. Consequently, the underpinning computational methods for design will migrate from deterministic to stochastic approaches. Indeed it will be more appropriate to characterize circuits and their environments with statistical distributions. Design optimization will relate to minimizing expected values of observable design metrics, such as latency and energy consumption. Nevertheless, it will be increasingly harder to insure worst-case bounds on such metrics, and system architectures will need to cope with this new viewpoint.

As systems become also more complex, their assembly will be made out of complex standard parts, such as processor and controller cores and memory arrays. The major design challenge will be to provide correct and reliable operation of the interconnected components. Also for this reason, new design paradigms will be used. Top-down correct component interconnection will become increasingly harder to succeed, because the interface features of components will also scale-up in complexity. New design methodologies will leverage component self-configuration [1], which support malleable interfaces and the ability of a component to recognize features of its neighbours and adapt to them. Thus, component interconnection will become a bottom-up process.

Reliable on-chip communication will require viewing routing wires as information channels, and systems as *micro-networks* of components. Signal transmission will face an increasingly more noisy environment, where noise abstracts undesirable effects such as timing variations, cross-talk and interference. Techniques borrowed from networking will be applicable at the chip level, to provide reliable communication over unreliable physical channels [2]. At the same time, the increasingly larger amount of on-chip information processing and storage resources will require communication architectures to replace system busses. Information encoding, packetization and routing will provide us with a new facet of design, to support reliable data transfer in a noisy environment [3].

Forthcoming technologies (e.g., carbon nanotubes and nanowires) will enable the design of systems with a much higher density of switching design as compared to scaled-down silicon technologies. On the other hand, monolithic systems constructed with self-assembly techniques will also display a much higher defect density. The unprecedented amount of computational power will be useful only if new design methodologies will be able to insure correct and reliable design on an unreliable physical medium. Again, techniques based on encoding, computation and communication redundancy and reconfiguration will be key to the success of these technologies. In this respect, designing monolithic systems based on nanotechnologies will face challenges similar to those of CMOS scaled-down towards its physical limitations. Indeed, robust large-scale system design, with advanced technologies that push devices towards the physical limits of materials, requires solving system-level information management problems.

REFERENCES

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