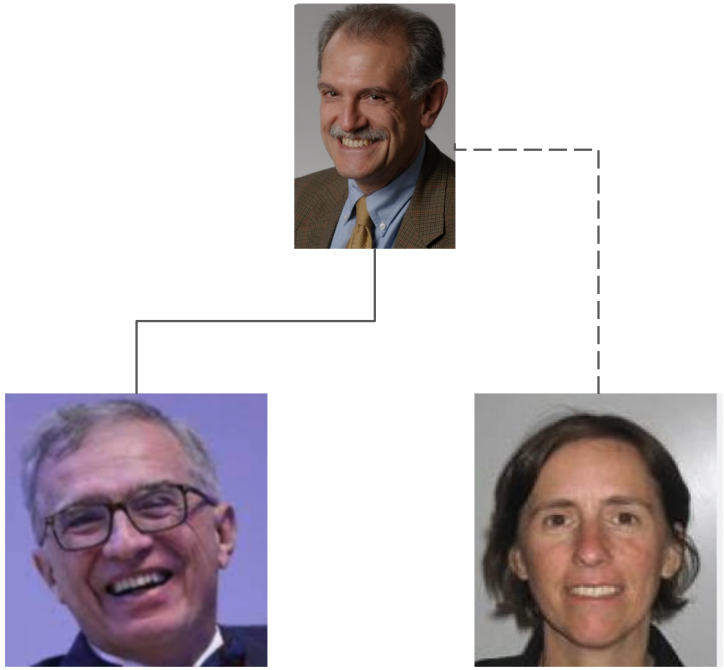
Tour de Career

- Prolog: UCB, HP
- Stage 1: Stanford
- Stage 2: HP Labs, HP Openview, Rainfinity
- Rest Day 1: Travel
- Stage 3: HighWire Press (Stanford)
- Rest Day 2: Duplicate Bridge
- Stage 4: Atypon
- Stage 5: Google

Polly Siegel
June 23, 2024

Prolog: UCB, Hewlett-Packard (1978-1987)



DELIGHT-MIMO: AN INTERACTIVE, OPTIMIZATION-BASED MULTIVARIABLE CONTROL SYSTEM DESIGN PACKAGE. *

by

D. Q. Mayne**, W. T. Nye***, E. Polak***, A. Sangiovanni Vincentelli***, P. Siegel***, A.L. Tits***, and T. Wuu***.

ABSTRACT.

This paper describes an interactive, optimization based-multivariable control system design package which is currently under development at the University of California, Berkeley. The package will combine a number of subroutines from the Imperial College Multivariable Design System and the Kingston Polytechnic SLICE library with DELIGHT, the University of California, Berkeley general purpose interactive, optimization-based CAD system.

Hewlett-Packard: Chipbuster (1985-1987)

CHIPBUSTER ERS

Jim Wilmore Charles McCord
Polly Siegel Mark Hammer
Fred Harder Izumi Suwa
Peter Cheng Dell Lee
Dave Wells

May 21, 1985

Behavioural and Logic Simulation in the ChipBuster Design System - The BEST simulator

Wei-Jin Dai
Polly Siegel

Design Technology Center

Abstract

BEST is an event driven based simulator that performs behavioural and gate level simulation. BEST helps a designer throughout the design process to verify the functionality of the chip, to study the performance, and to ensure the correct circuit implementation. At the behavioural level, models are described in the MADL hardware description language. BEST also provides built-in gate-level primitives. BEST provides models for transport delays and inertial delays (minimum pulse width).

This paper describes the architecture, the algorithms, the delay models, and the capabilities of the BEST simulator (familiarity with behavioural simulation is helpful). Performance comparisons with previous simulators are described. Current status of the simulator and future plans are described as well.

Chipbuster

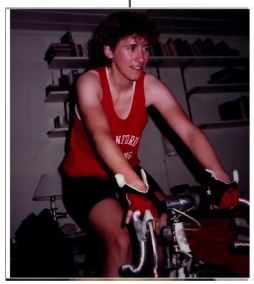
ChipBuster is a UNIX*-based computer-aided design system for custom VLSI design. Key features include a high degree of configurability and integration. Functionally, it includes an art-work/schematic editor and extensive simulation and verification capabilities. A common connectivity database and common user interface provide fast loop time for IC design activities and a powerful script-based environment.

As ChipBuster is a very large project (approximately 600,000 lines of code), there were many challenges in controlling its development. These fell into two chief categories: management and technical. Management's challenge was that it required close coordination between eight R&D teams in three sections in two states to develop core functionality. Additionally, coordination with product marketing, customer support, sales development, software QA, and software manufacturing was required.

To manage this large-scale project, Technical Team Meetings (TTMs) and Product Team Meetings (PTMs) were held regularly and provided forums for the exchange of information about the technical aspects of the project, and the presentation of the information from R&D to the customer.

A central design team was vital in avoiding discrepancies in the user interface design which included how the user interfaced with the system. Although the program is far too large to

Stage 1: Stanford (1987-1994ish)



Automatic Technology Mapping for Generalized Fundamental-Mode Asynchronous Designs *

Polly Siegel Giovanni De Micheli David Dill

Center for Integrated Systems
Stanford University, Stanford CA 94305

Abstract— **We address the problem of technology mapping for generalized fundamental-mode asynchronous designs. In this design style we can separate the combinational portions of the design from the sequential portions, similar to synchronous design styles. We examine each step of algorithmic technology mapping for its influence on the hazard behavior of the modified network. We then present modifications to an existing synchronous technology mapper to work for this asynchronous design style. We present efficient algorithms for hazard analysis that are used during the mapping process. These algorithms have been implemented and incorporated into the program CERES to produce a technology mapper suitable for asynchronous designs.**

1 Introduction

Asynchronous design styles have been increasing in popularity as device sizes shrink and concurrency is exploited to increase system performance. However, asynchronous designs are difficult to design correctly because the presence of hazards (which are of no consequence to synchronous systems) can cause improper circuit operation. Many asynchronous design styles, together with accompanying automated synthesis algorithms, address the issues of design complexity and correctness. Typically, these synthesis systems [1, 2, 3] take a high-level description of an asynchronous system and produce a logic-level description of the resultant design that is hazard-free for transitions of interest. This logic-level description is then manually translated by a designer to a technology-specific implementation. The designer must be careful at this step not to introduce new hazards into the design. The size of designs is limited in part by the inability to safely (and reliably) map the technology-independent description into an implementation.

Automatic technology mapping techniques have been employed for synchronous design styles [4, 5, 6]. These algorithms allow translation of a technology-independent logic description into a technology-dependent implementation. However, these techniques by themselves are not suitable for asynchronous design styles since they do not take hazards into account.

In this paper we look at the problem of technology mapping for asynchronous designs. In particular, we concentrate on the *generalized fundamental-mode* asynchronous design style [1], since we can easily separate the combinational portions of the design from the sequential portions, similar to synchronous design styles. We examine each step of algorithmic technology mapping for its influence on the hazard behavior of the modified network. We then present modifications to an existing synchronous technology mapper, CERES, to adapt it to work for generalized fundamental-mode designs. We present efficient algorithms for hazard analysis that are used during the mapping process. Finally, we present some results of automatic technology mapping for some asynchronous fundamental-mode designs using our modified technology mapper.

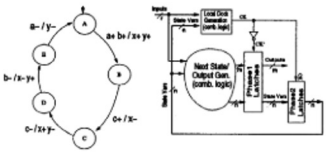


Figure 1: *Burst-mode state description, and corresponding high-level block diagram.*

2 Definitions

2.1 Design Style

Several popular asynchronous design styles extend the single-input change fundamental-mode assumption imposed by Mealy and Moore machines [7] to allow multiple-input change bursts in a particular state. The synthesis methods [1, 2] that incorporate this burst-mode—or *generalized fundamental-mode*—design style produce logic under the assumption that a burst of input changes can occur in any order, and the outputs and feedback variables of the combinational portion will settle before the next set of input changes are applied. As in the case of single-input change fundamental-mode, no hazards can be tolerated during the input bursts. However, in this design style both single-input change hazards and multi-input change hazards must be considered.

Figure 1 shows a simple burst-mode specification, along with the architecture to which it will be mapped by an automatic synthesis method [1]. The job of the technology mapper is then to implement this design using parts from a library of standard cells (for example) such that no hazards are introduced in the combinational logic blocks.

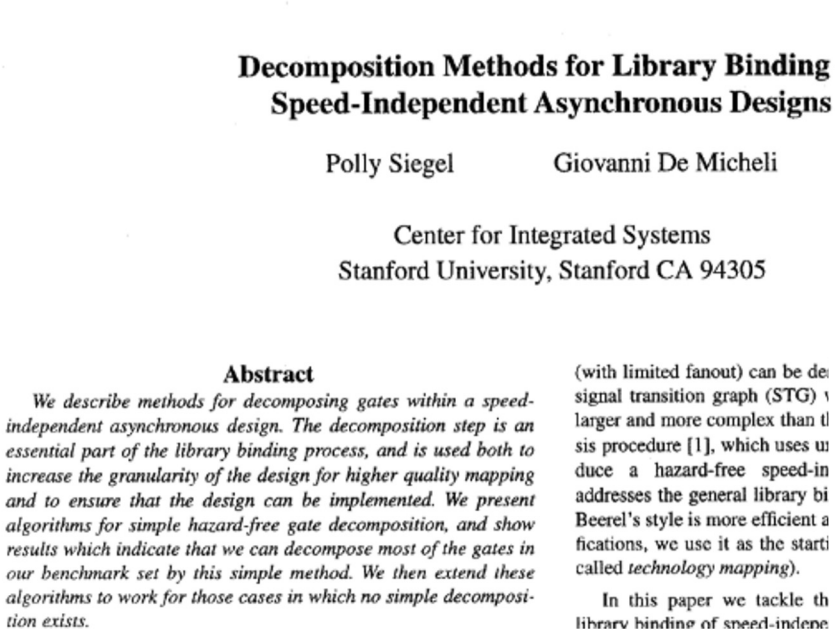
2.2 Hazards

A *hazard*, in the most general sense, is an unwanted output glitch in response to a change in some input or inputs. The

*This work was supported by the Semiconductor Research Corporation, Contract no. 92-DJ-205, and a Stanford CIS trust grant.

30th ACM/IEEE Design Automation Conference®

Stage 1: Stanford – last 60km



Decomposition Methods for Library Binding of Speed-Independent Asynchronous Designs

Polly Siegel Giovanni De Micheli

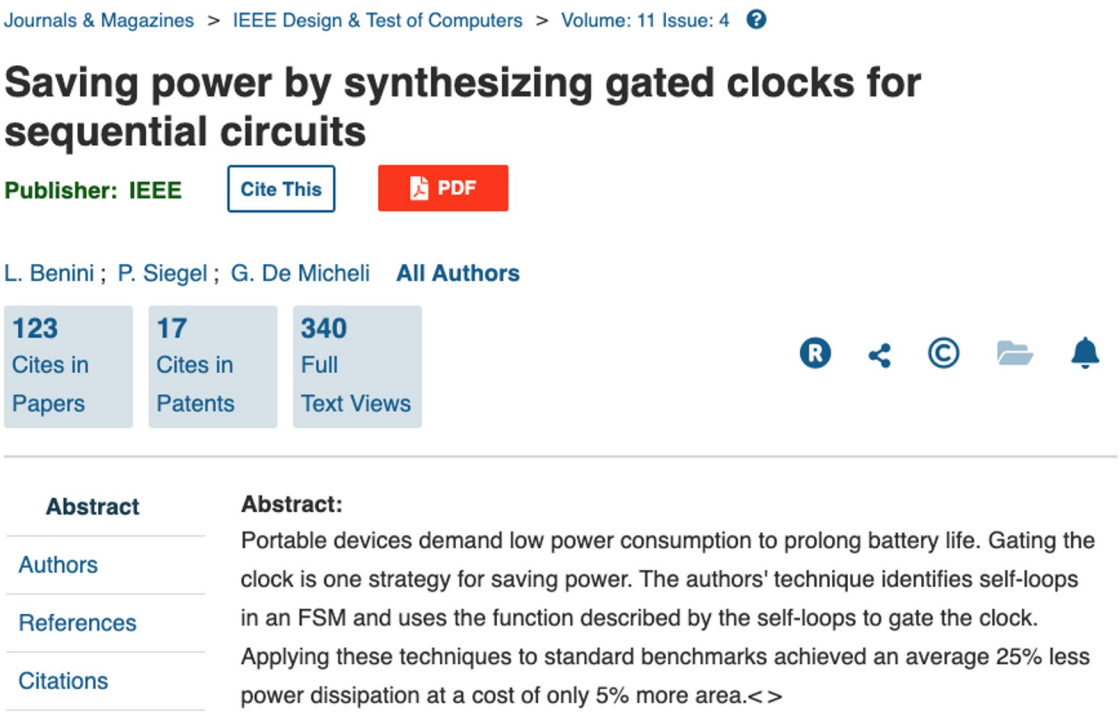
Center for Integrated Systems
Stanford University, Stanford CA 94305

Abstract

We describe methods for decomposing gates within a speed-independent asynchronous design. The decomposition step is an essential part of the library binding process, and is used both to increase the granularity of the design for higher quality mapping and to ensure that the design can be implemented. We present algorithms for simple hazard-free gate decomposition, and show results which indicate that we can decompose most of the gates in our benchmark set by this simple method. We then extend these algorithms to work for those cases in which no simple decomposition exists.

(with limited fanout) can be de
signal transition graph (STG)
larger and more complex than t
sis procedure [1], which uses u
duce a hazard-free speed-in
addresses the general library bi
Beerel's style is more efficient a
fications, we use it as the starti
called *technology mapping*).

In this paper we tackle th
library binding of speed-indepe



Journals & Magazines > IEEE Design & Test of Computers > Volume: 11 Issue: 4

Saving power by synthesizing gated clocks for sequential circuits

Publisher: IEEE Cite This PDF

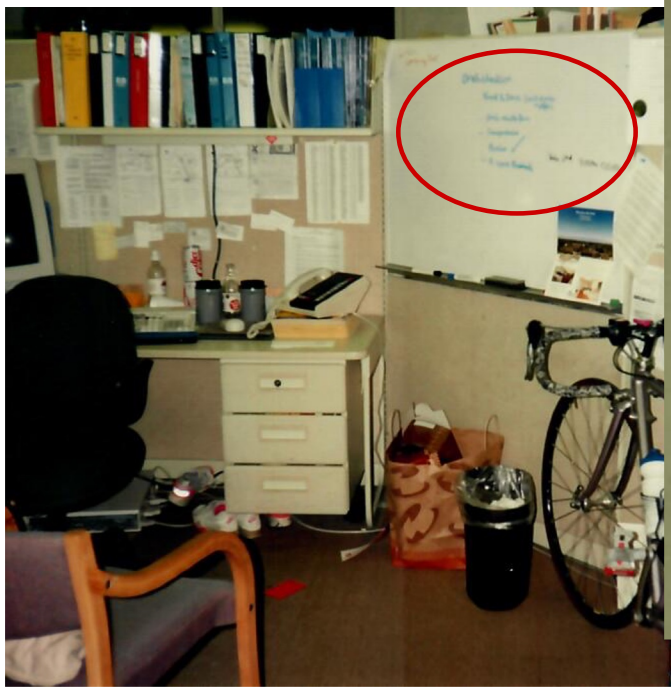
L. Benini ; P. Siegel ; G. De Micheli All Authors

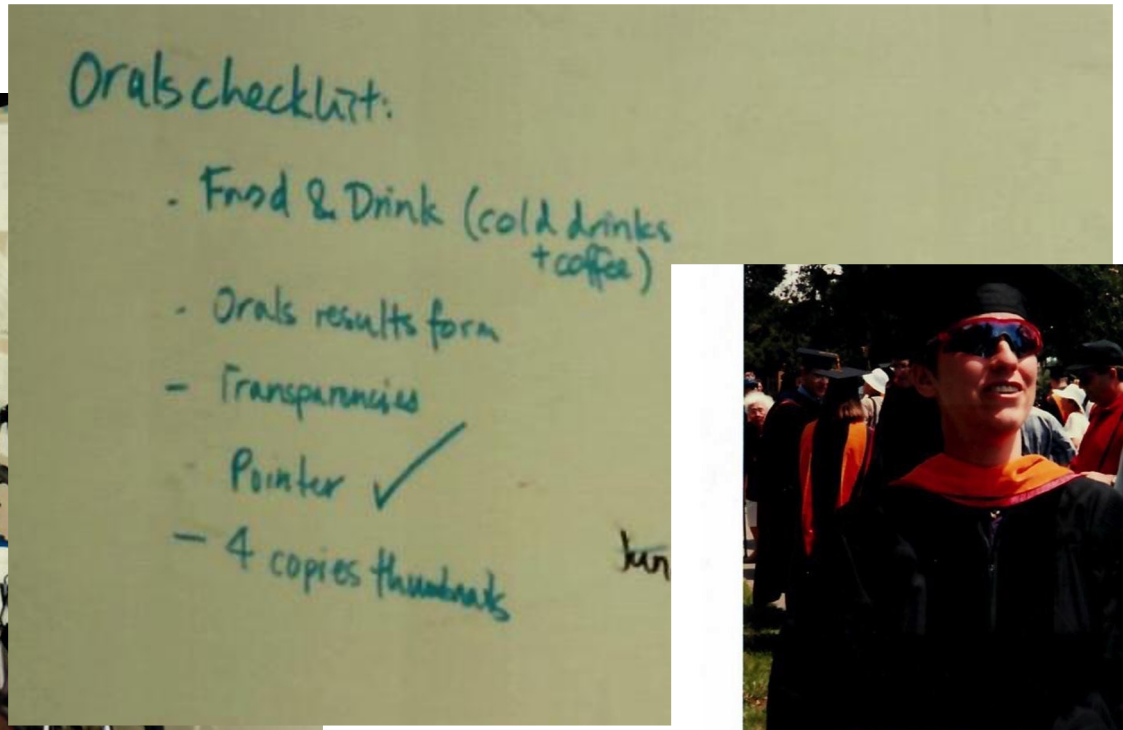
123 Cites in Papers | 17 Cites in Patents | 340 Full Text Views

Abstract
Authors
References
Citations

Abstract:
Portable devices demand low power consumption to prolong battery life. Gating the clock is one strategy for saving power. The authors' technique identifies self-loops in an FSM and uses the function described by the self-loops to gate the clock. Applying these techniques to standard benchmarks achieved an average 25% less power dissipation at a cost of only 5% more area.< >

Stage 1: Stanford – finish line





(Luca)

Stage 2: HP Labs, HP OpenView, Rainfinity (1994-2001)

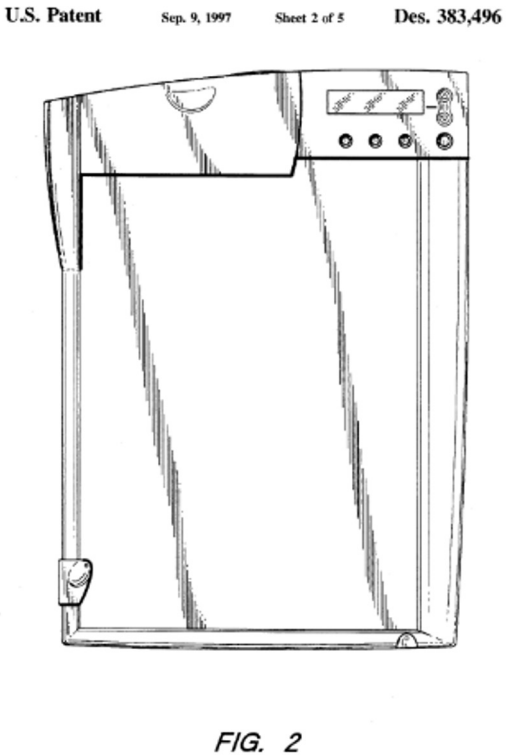


FIG. 2

System for editing graphical data based upon relative time of entry

US6151611A
United States

Download PDF | Find Prior Art | Similar

Inventor: Polly S. K. Siegel

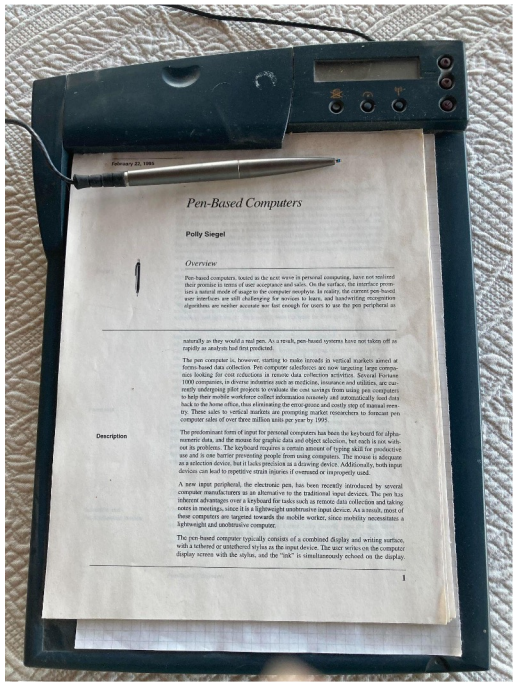
Current Assignee : Hewlett Packard Development Co LP

Worldwide applications

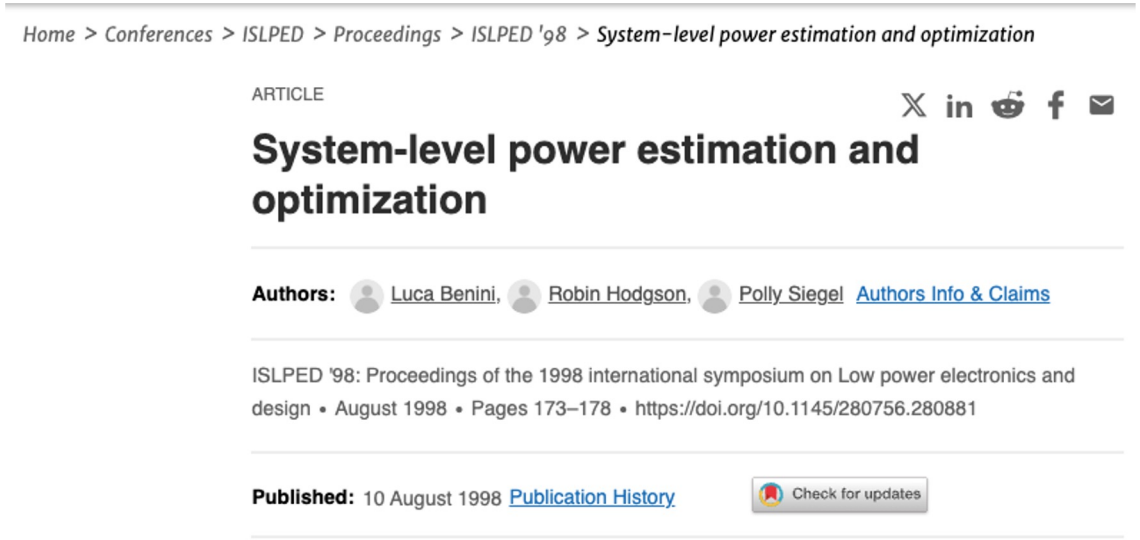
1997 ~~US~~ 1998 EP WO DE JP 2007 JP

Application US08/962,489 events

1997-10-31	Application filed by Hewlett Packard Co
1997-10-31	Priority to US08/962,489
2000-11-21	Publication of US6151611A
2000-11-21	Application granted
2017-10-31	Anticipated expiration
Status	Expired - Lifetime



Stage 2: HP Labs, HP OpenView, Rainfinity (1994-2001)



Home > Conferences > ISLPED > Proceedings > ISLPED '98 > System-level power estimation and optimization

ARTICLE

System-level power estimation and optimization

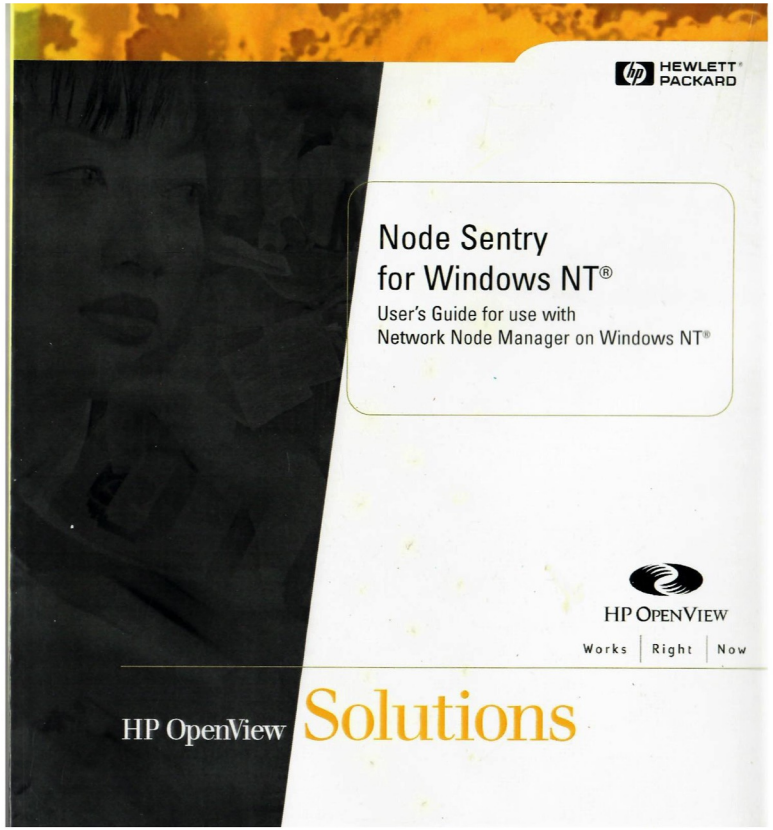
Authors: Luca Benini, Robin Hodgson, Polly Siegel Authors Info & Claims

ISLPED '98: Proceedings of the 1998 international symposium on Low power electronics and design • August 1998 • Pages 173–178 • https://doi.org/10.1145/280756.280881

Published: 10 August 1998 Publication History

Check for updates

Stage 2: HP Labs, HP OpenView, Rainfinity (1998-2000)



Stage 2: HP Labs, HP OpenView, Rainfinity (2000-2001)

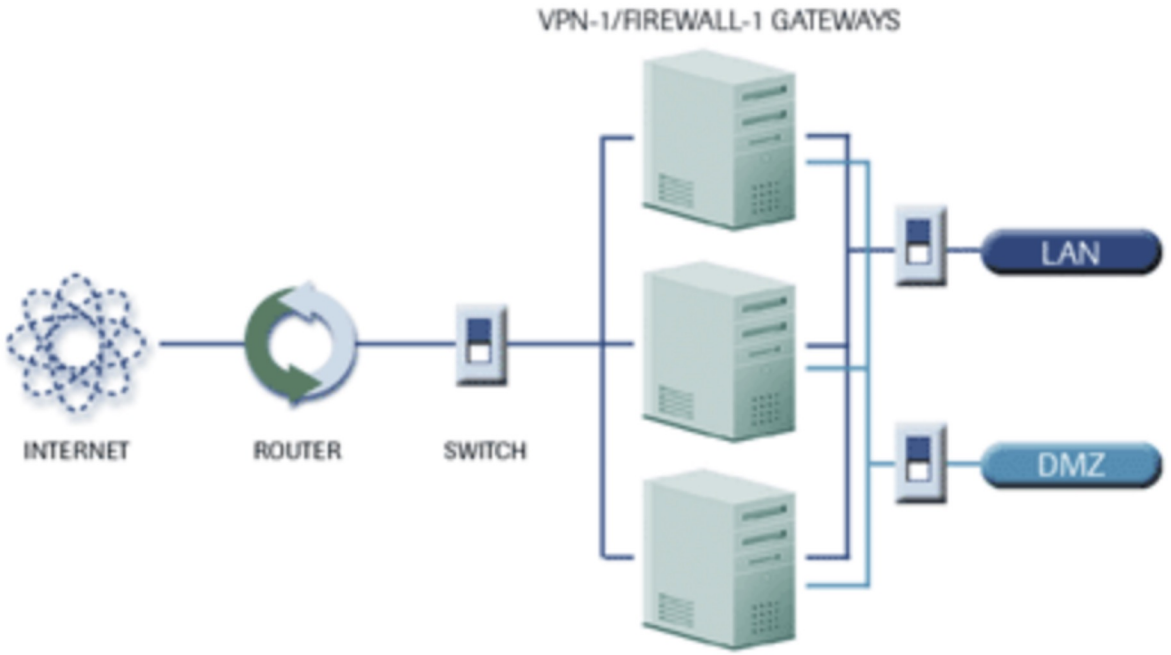
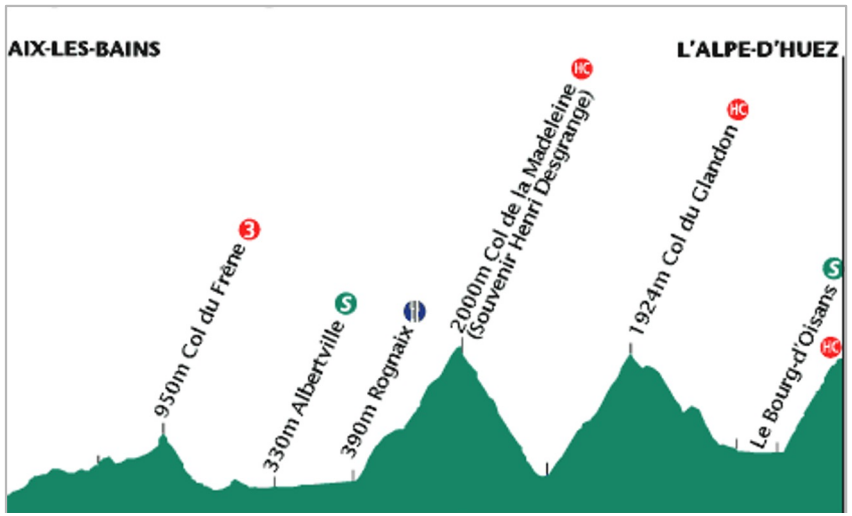
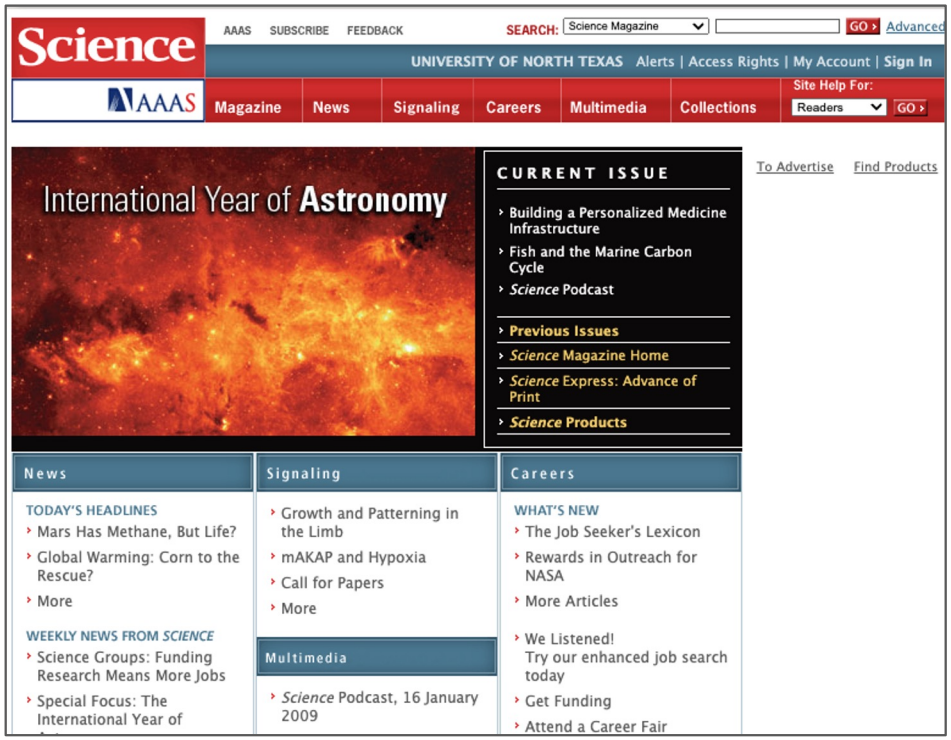


Fig1. Rainwall reduces costs and complexity by installing directly on your existing VPN-1/Firewall-1 servers.

Rest day 1: Italian, cycling (Italy, TdF), soul searching



Stage 3: HighWire Press, Stanford University (2001-2011)



Stage 3: HighWire Press, Stanford University (2001-2011)

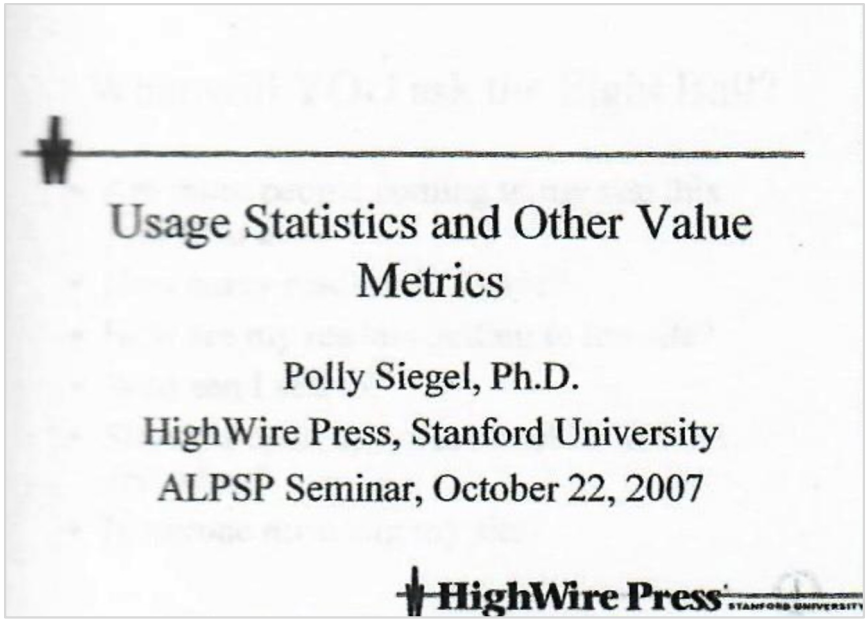
The European Association for Cardio-Thoracic Surgery

Moscow Science Course
Applied Science for Cardio-Thoracic Surgeons

Moscow, 13–14 April, 2009

PROGRAMME

09.30	**Searching the medical literature** Part II: discovering hidden treasure	*P. Siegel*
10.30	**Coffee break**	
11.00	Art of meeting presentation: avoiding common errors	*M. Turina*
11.40	How to write a successful manuscript I	*A. Wechsler*
12.30	**Lunch break**	
13.30	Critical approach to the medical literature: how to spot errors, omissions and mistakes	*P. Sergeant*
14.30	How to write a successful manuscript II	*J. Vaage*

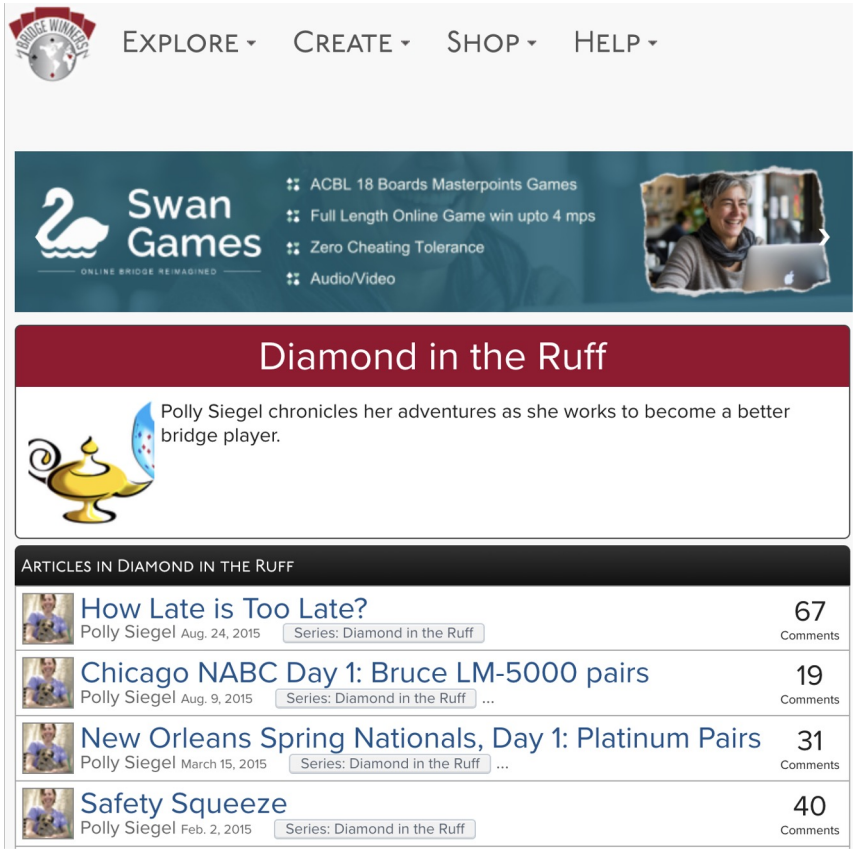


Rest day 2: Bridge (2011-2013)

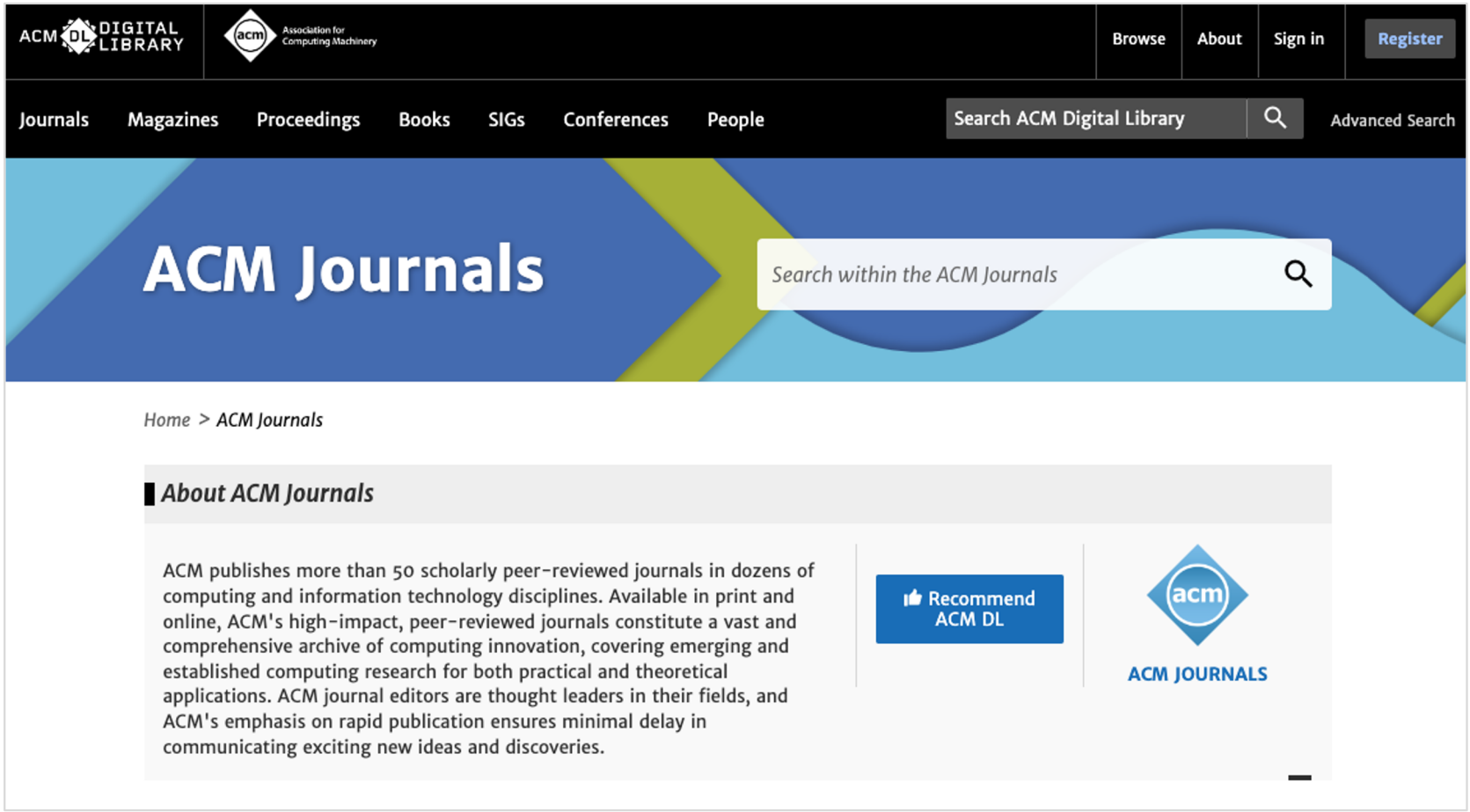
50 to 100 Mini-McKenney Masterpoint Race

Rank	Player	Location	Points
1	Polly Siegel	Los Altos CA	330.98
2	Debra Gay Falcon	Harvey LA	250.25
3	Greg Lagos	Spring Hill FL	247.64

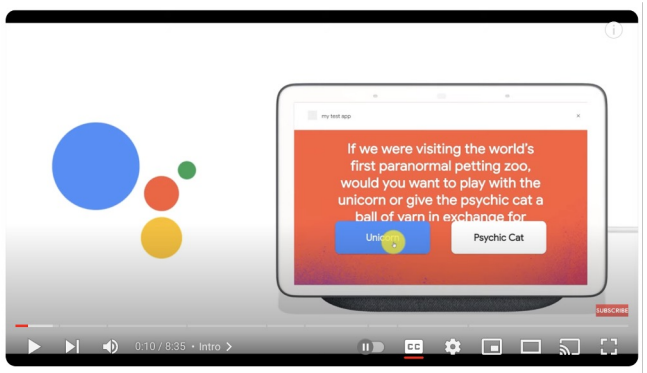
Clickbait



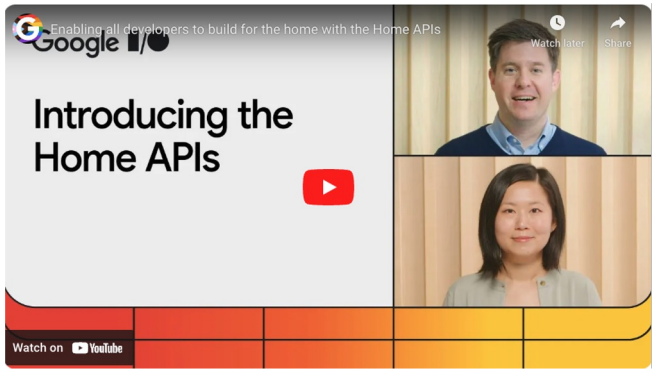
Stage 4: Atypon (2014-2018)

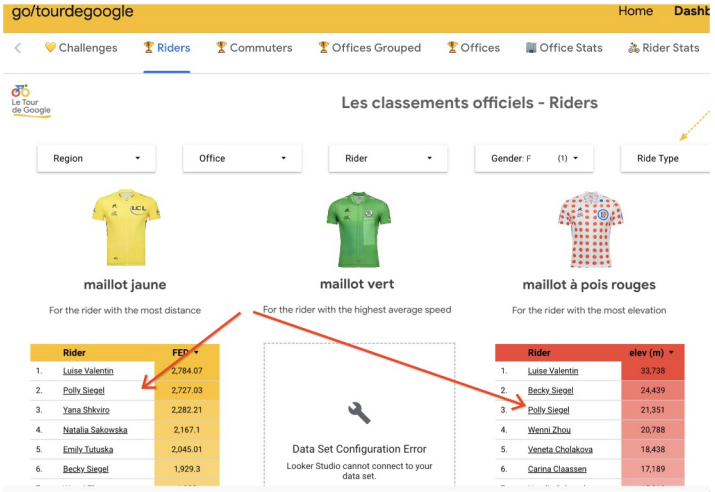


Stage 5: Google (2018 - present)



Create Actions for Google Assistant with no code using Actions Template





Thoughts about getting a Ph.D.

- Professionally, even though I didn’t go into academia, it has opened doors and made it easier to take advantage of certain opportunities (e.g., teaching at medical conferences)
- It’s been super helpful in dealing with the medical profession who are more degree conscious
- As a woman in tech, I’ve discovered that having a Ph.D. gives a certain credibility that would otherwise take a long time to earn