"Synthesis and Optimization" of An EDA Researcher

Cunxi Yu

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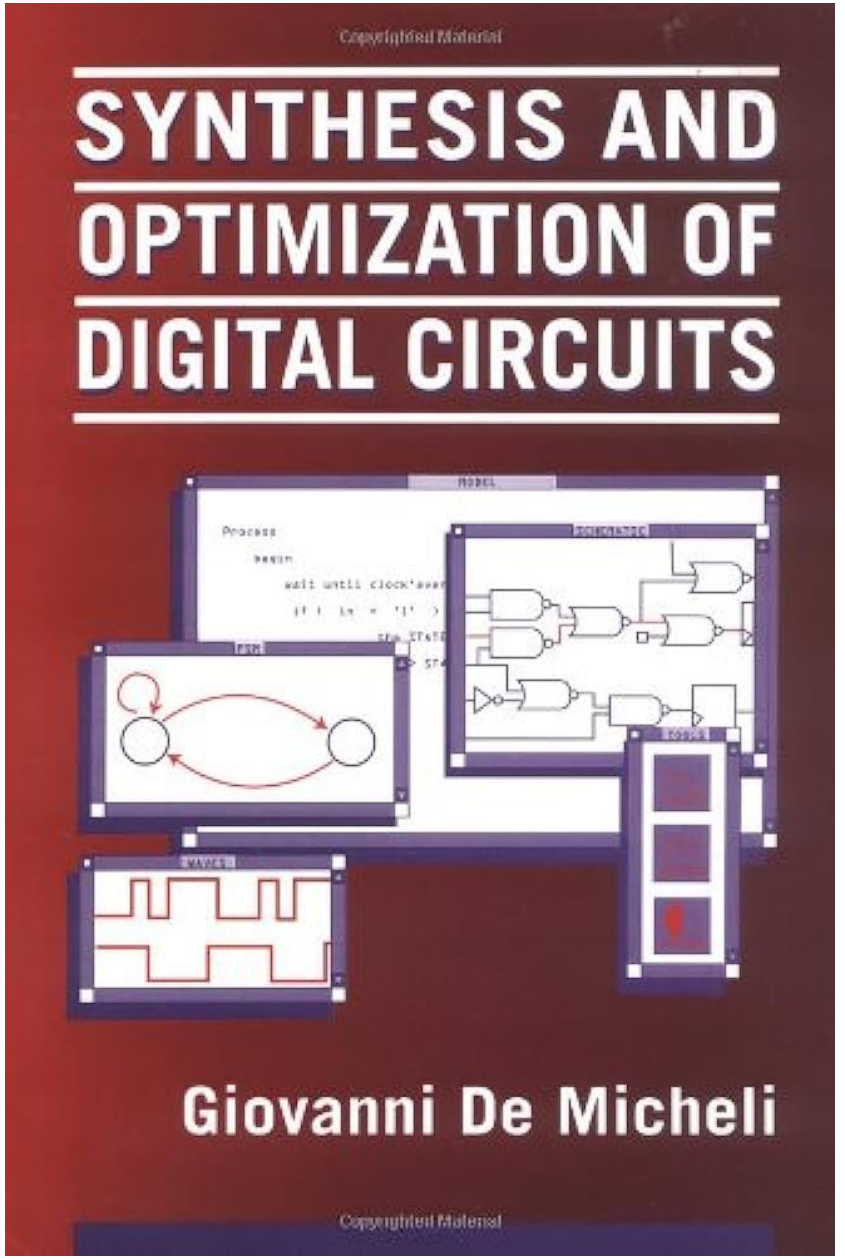
UNIVERSITY OF MARYLAND

My Ticket to the Workshop

- Born and educated in China
- Academic pursuits at UMass Amherst
- The honest thought about ”synthesis” before the Digital CAD class ..

  - Trained in formal verification and synthesis under Prof. Maciej Ciesielski



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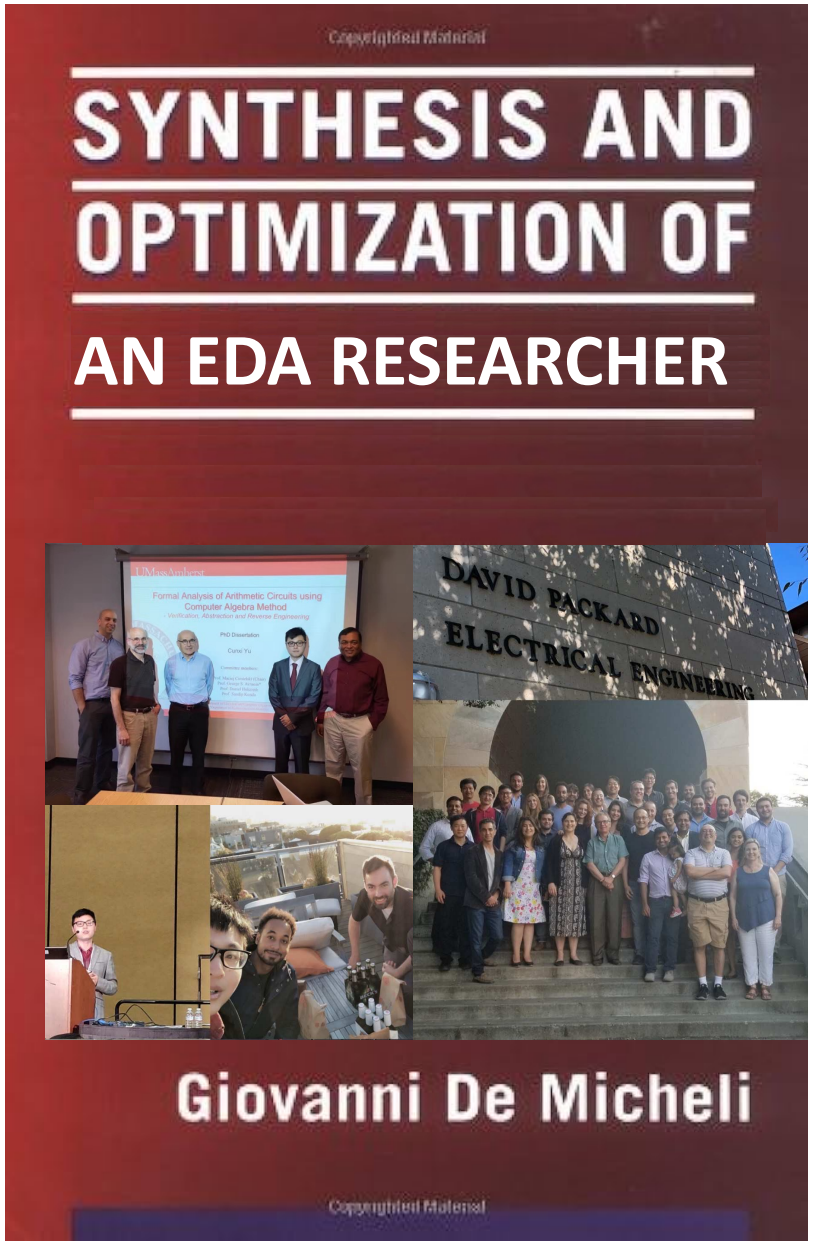
- First job after PhD ☞ PostDoc with Nanni



Stepping Forward to New Direction

- A short-stay: 2017-2018
  - Initiated research into machine learning (ML) and ML for synthesis
- But **lasting influence**
  - ☞ PostDoc with Zhiru Zhang (Cornell)
    - Met Zhiru at IWLS 2018 at EPFL!
  - ☞ Job talk on *ML for EDA* ☞ University of Utah (2019)
    - CAREER on “OneSense: One-Rule-for-All Combinatorial Boolean Synthesis via Reinforcement Learning” (2021)
  - Design Automation Conference (DAC) Best Paper (2023)
    - Graph learning for Boolean Reasoning

Stepping Forward to New Direction

Recap of the EPFL Benchmark Results

- Are were making some progress since 2016?
  - Maybe

Developing Synthesis Flows Without Human Knowledge

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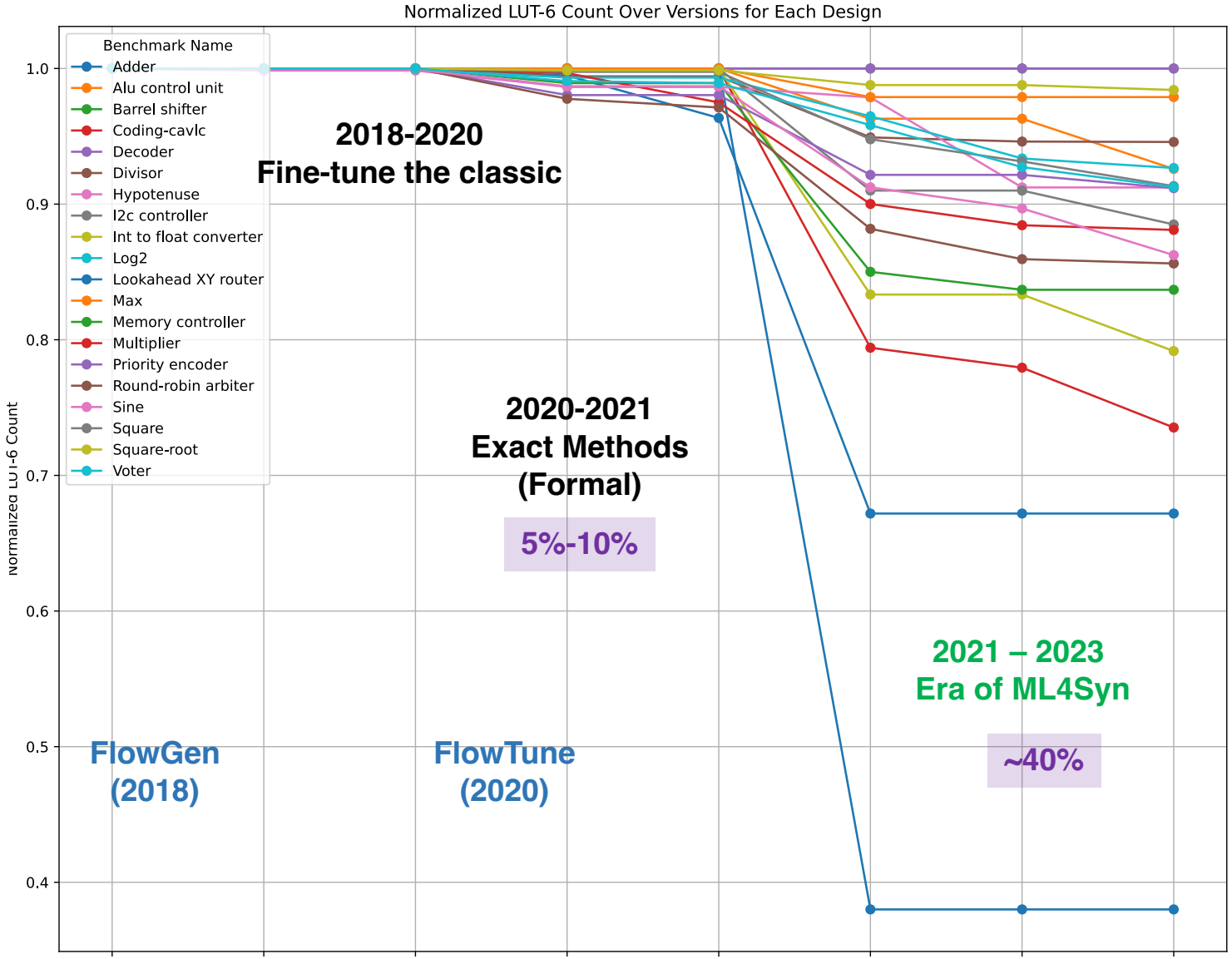
ABSTRACT

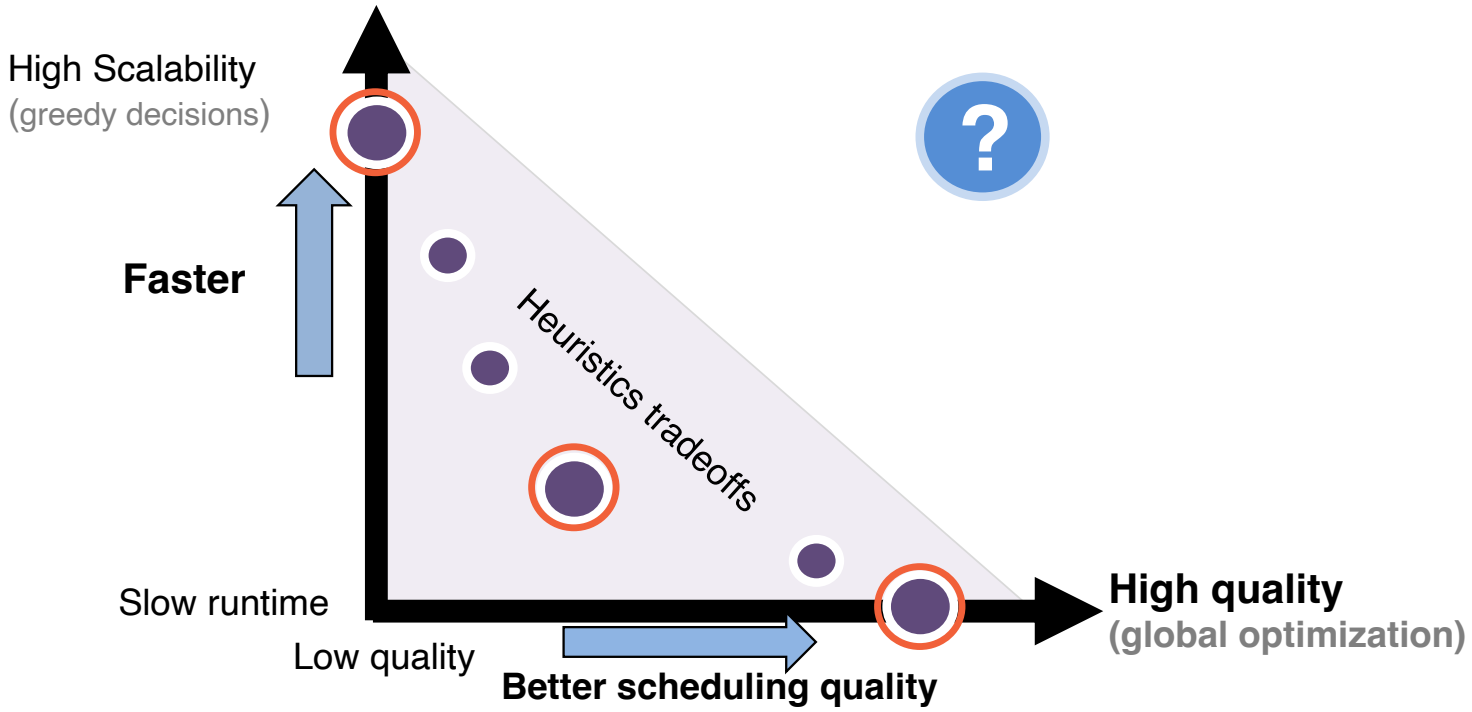
Design flows are the explicit combinations of design transformations, primarily involved in synthesis, placement and routing processes, to accomplish the design of Integrated Circuits (ICs) and System-on-Chip (SoC). Mostly, the flows are developed based on the knowledge of the experts. However, due to the large search space of design flows and the increasing design complexity, developing *Intel-*

search space of general flows is formally defined in Section 2.1. Although the significant efforts spent in providing high-quality design flows, the technique that systematically generates *IP-specific* synthesis flows has been lagging. Similarly, these problems exist in designing System-on-Chip (SoC). In Section 2 (Figure 1), two motivating examples are provided to show the needs of developing such technique.



Amarú, Luca, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. "The EPFL combinational benchmark suite." Proceedings of the 24th International Workshop on Logic & Synthesis (IWLS). 2015.

ML for Combinatorial Optimization



Classic CO Algorithms/R&D	ML for COs
Difficulties of parallelism.	**Natural parallelism in batched processing**
Inefficient utilization of modern computing platforms	**Strong system/HW supports from ML infra & domain-specific accelerators**
Hand-crafted heuristics limited by domain knowledge	**Learning unseen heuristics & intelligent exploration & adaptative to new domain**

Talking about ML…

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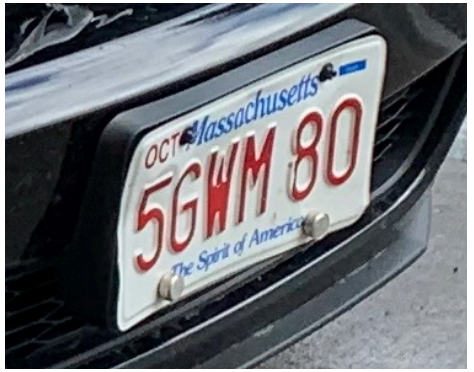

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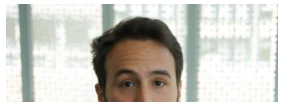
Continuing the Legacy

[TCAD] 

Organizing

Topic Area(s): RTL/Logic Level and High-level Synthesis

Room: 3002, 3rd Floor

Session Chair(s): Giovanni de Micheli, École Polytechnique Fédérale de Lausanne; Cunxi Yu, University of Utah

Organizing IWLS

1:30pm - 3:00pm PDT Research Manuscript Advanced Logic Synthesis - Improving Runtime and Quality

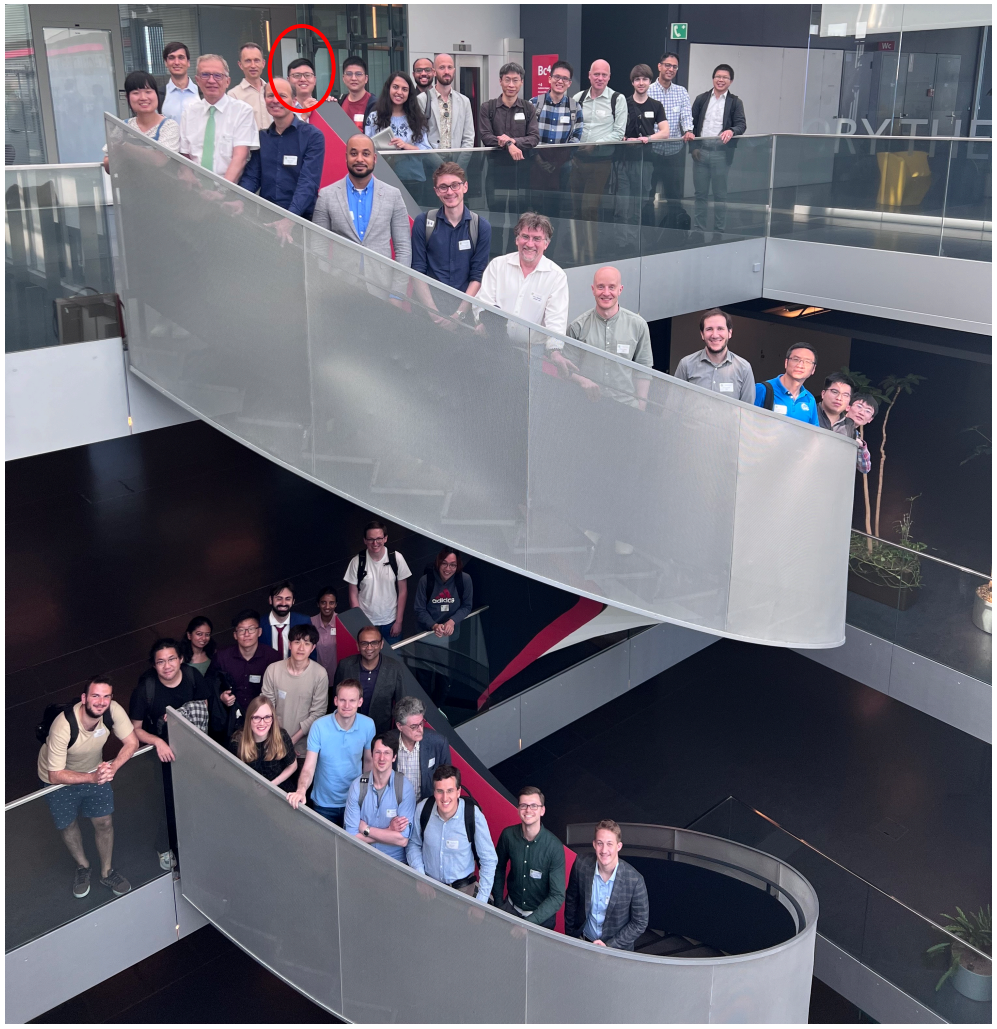
Session Chairs: Giovanni De Micheli, Cunxi Yu

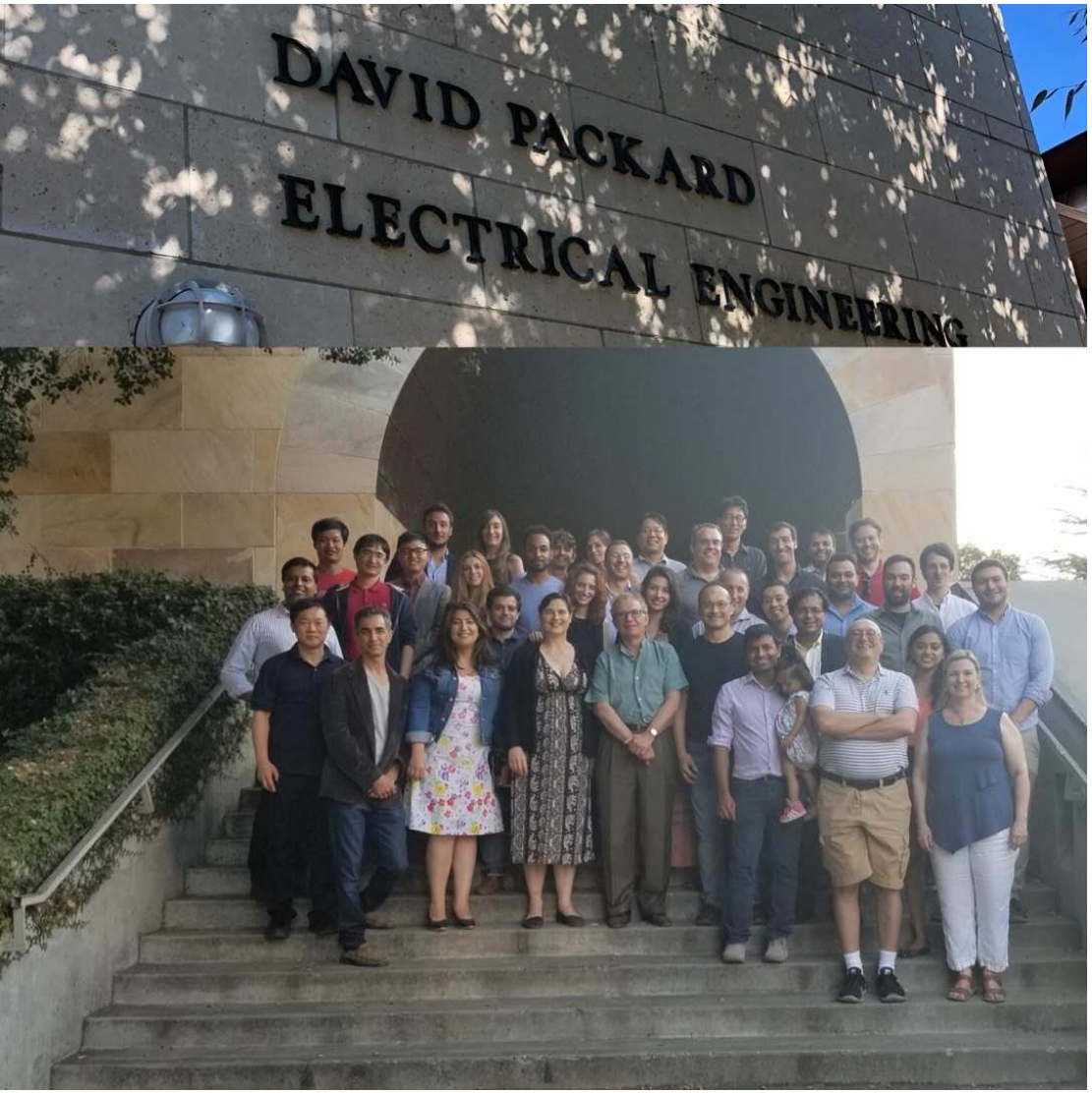
[DAC]

Book

Back to EPFL!


international workshop on logic & synthesis
IWLS
2023
32nd International Workshop on Logic & Synthesis
June 5 – 6, 2023
EPFL, Lausanne, Switzerland




DAVID PACKARD
ELECTRICAL ENGINEERING

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