Multiple-Independent-Gate Field-Effect Transistors for High Computational Density and Low Power Consumption

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Abstract

Transistors are the fundamental elements in *Integrated Circuits* (IC). The development of transistors significantly improves the circuit performance. Numerous technology innovations have been adopted to maintain the continuous scaling down of transistors. With all these innovations and efforts, the transistor size is approaching the natural limitations of materials in the near future. The circuits are expected to compute in a more efficient way. From this perspective, new device concepts are desirable to exploit additional functionality. On the other hand, with the continuously increased device density on the chips, reducing the power consumption has become a key concern in IC design.

To overcome the limitations of *Complementary Metal-Oxide-Semiconductor* (CMOS) technology in computing efficiency and power reduction, this thesis introduces the multiple-independent-gate *Field-Effect Transistors* (FETs) with silicon nanowires and FinFET structures. The device not only has the capability of polarity control, but also provides dual-threshold-voltage and steep-subthreshold-slope operations for power reduction in circuit design.

By independently modulating the Schottky junctions between metallic source/drain and semiconductor channel, the dual-threshold-voltage characteristics with controllable polarity are achieved in a single device. This property is demonstrated in both experiments and simulations. Thanks to the compact implementation of logic functions, circuit-level benchmarking shows promising performance with a configurable dual-threshold-voltage physical design, which is suitable for low-power applications.

This thesis also experimentally demonstrates the steep-subthreshold-slope operation in the multiple-independent-gate FETs. Based on a positive feedback induced by weak impact ionization, the measured characteristics of the device achieve a steep subthreshold slope of 6 mV/dec over 5 decades of current. High I_{on}/I_{off} ratio and low leakage current are also simultaneously obtained with a good reliability. Based on a physical analysis of the device operation, feasible improvements are suggested to further enhance the performance.

A physics-based surface potential and drain current model is also derived for the polarity-controllable *Silicon Nanowire FETs* (SiNWFETs). By solving the carrier transport at Schottky junctions and in the channel, the core model captures the operation with independent gate control. It can serve as the core framework for developing a complete compact model by integrating advanced physical effects.

Abstract

To summarize, multiple-independent-gate SiNWFETs and FinFETs are extensively studied in terms of fabrication, modeling, and simulation. The proposed device concept expands the family of polarity-controllable FETs. In addition to the enhanced logic functionality, the polarity-controllable SiNWFETs and FinFETs with the dual-threshold-voltage and steep-subthreshold-slope operation can be promising candidates for future IC design towards low-power applications.

Keywords: Gate-all-around, nanowire, FinFET, Schottky barrier, polarity control, multi-threshold-voltage, steep subthreshold slope, fabrication, simulation, compact modeling, logic design, tunneling, impact ionization, feedback, leakage, low power

Résumé

Les transistors sont les éléments fondamentaux des circuits intégrés (IC). Le développement des transistors améliore significativement la performance du circuit. De nombreuses innovations technologiques ont été adoptées pour maintenir la réduction continue des dimensions des transistors. Grâce à ces innovations, la taille des transistors approchera les limites naturelles des matériaux dans un proche avenir. Par ailleurs, les circuits doivent calculer d'une manière plus efficace. Dans cette perspective, de nouveaux concepts de dispositifs sont souhaitables pour disposer de fonctionnalités supplémentaires. D'autre part, avec l'augmentation de la densité des puces, la réduction de la consommation d'énergie est devenue une préoccupation majeure dans la conception IC.

Pour surmonter les limites de la technologie CMOS en termes d'efficacité de calcul et de réduction de la puissance, cette thèse présente des transistors à effet de champ (FET) à multiples grilles indépendantes utilisant des nanofils de silicium et des structures FinFET. Le dispositif a non seulement la capacité de contrôler sa polarité, mais offre également des propriétés de double tension de seuil ou de forte pente sous le seuil afin de permettre réduction de la puissance des circuits.

En modulant indépendamment les barrières Schottky entre les contacts métalliques de source ou de drain et le canal semi-conducteur, des propriétés de double tension de seuil et de polarité contrôlable sont atteintes en un seul et même transistor. Cette propriété est démontrée expérimentalement et par simulation. Grâce à la réalisation compacte de fonctions logiques, notre analyse au niveau du circuit montre des performances prometteuses pour la conception de circuits à double tension de seuil configurable et son intérêt pour des applications de faible puissance.

Cette thèse démontre également expérimentalement le fonctionnement à pente sous le seuil raide dans des FETs à grilles multiples indépendantes. Basées sur une rétroaction positive induite par une ionisation par impact faible, les caractéristiques mesurées des transistors atteignent une pente sous le seuil raide de 6 mV/dec sur plus de 5 décades de courant. Un fort rapport I_{on}/I_{off} et un faible courant de fuite sont également simultanément obtenus avec une bonne fiabilité. Basées sur une analyse physique du fonctionnement du dispositif, de possibles améliorations sont suggérées pour améliorer encore la performance.

Un modèle compact physique du potentiel de surface et du courant de drain est également

dérivé pour les transistors à nanofils de silicium (SiNWFETs) à polarité contrôlable. En dérivant le transport de porteurs de charge au niveau des jonctions de Schottky et dans le canal, le modèle capture le fonctionnement des grilles de commande indépendantes. Ce modèle peut servir de base pour l'élaboration d'un modèle compact plus complet intégrant des effets physiques avancés.

Pour résumer, les SiNWFETs et FinFETs à grilles indépendantes multiples sont largement étudiés en termes de fabrication, modélisation et simulation. Le concept de dispositif proposé élargit la famille de FET à polarité contrôlable. En plus de disposer de fonctions logiques améliorées, les SiNWFETs et FinFET à polarité contrôlable possèdent une double tension de seuil et un fonctionnement en pente sous le seuil raide et peuvent ainsi être des candidats prometteurs pour la conception des circuits intégrés du futur pour des applications de faible puissance.

Mots-clés : grilles enrobantes, nanofil, FinFET, barrière de Schottky, contrôle de la polarité, tensions de seuil multiples, pente sous seuil raide, fabrication, simulation, modélisation compacte, conception logique, effet tunnel, ionisation par impact, rétroaction, fuites, faible puissance

Contents

List of Figures

List of Tables

1 Introduction

The first electronic general-purpose computer ENIAC was born in 1946 [1]. Since then, people have been keen on pursuing smaller but more powerful computers. After the invention of semiconductor devices and integrated circuits, there has been a fast development of computers for more than half a century [2–5]. Fig. 1.1 illustrates the development of computers from ENIAC to Personal Computer, and the recent Compute Stick. Thanks to the greatly enhanced computing capability of integrated circuits with a deeply scaled feature size, the whole system of computation, control, and memory perfectly fits in a small stick [6].

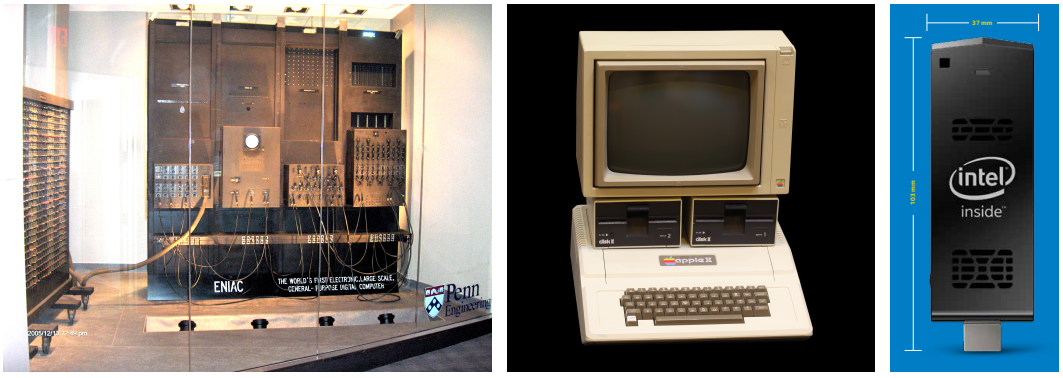


Figure 1.1: Development of computers, (a) ENIAC (part), (year 1946), (b) Apple-II, (year 1977), (c) Intel Compute Stick, (year 2015).

With such a speedy development, not only computers, but also consumer products containing semiconductor devices and integrated circuits have arrived at almost every corner of human society. They are changing every part of people's life.

This revolution greatly relies on the scaling down of transistors, which are the fundamental elements of integrated circuits [7]. The benefits from the scaling down of transistors was described by the famous "Moore's law" proposed by Gordon E. Moore in 1965 [8]. Generally, the scaling down of transistor size dramatically increases the device density on chips, and

decreases the relative cost, at an exponential pace.

Driven by the benefits from downscaling, there is the need to maintain this trend, which is referred to as "More Moore". On the other hand, with the progress in both process technology and design, the capability of non-digital technologies is significantly enhanced. This brings the migration of non-digital components, such as analog circuits and sensors, into the package. Thus, the highly integrated systems can efficiently interact with people and environment. The so-called "More-than-Moore" trend is characterized by functional diversification of semiconductor-based devices. As shown in Fig. 1.2, the dual trend of "More Moore" and "More-than-Moore" summarizes the combined need for digital and non-digital functionalities in an integrated system [9].

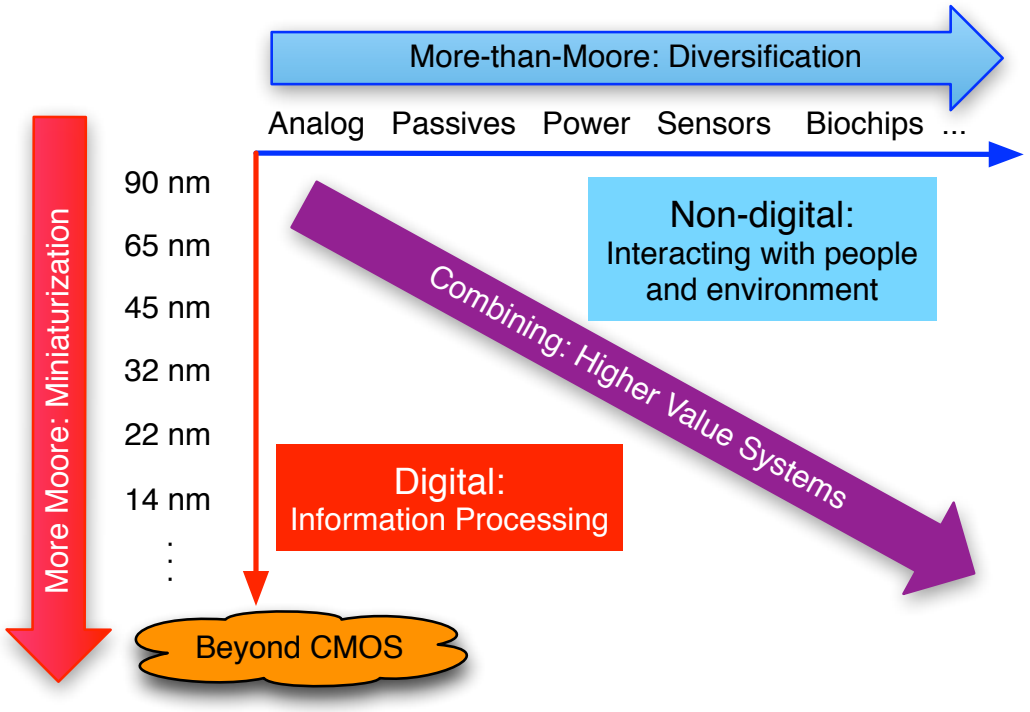


Figure 1.2: The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the *International Technology Roadmap for Semiconductors* (ITRS): miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore") [9]

The technologies to maintain the trend of "More Moore" are introduced in Sec. 1.1. Then, Sec. 1.2 introduces the current limitations of CMOS technology on computing efficiency and power reduction. Sec. 1.3 discusses the global objectives of this thesis to overcome these limitations with the proposed device concept. Sec. 1.4 summarizes the contributions of the thesis. Finally, Sec. 1.5 gives the organization of this thesis at the end of this chapter.

1.1 Technologies Towards "More Moore"

This section introduces the innovations in CMOS technology for continuous miniaturization, and beyond-CMOS technologies expected to keep the trend of "More Moore" when CMOS devices approach the material limit.

1.1.1 Innovations in CMOS Technology

Numerous key technology innovations have been adopted in CMOS technology to keep the device performance while scaling down:

1. **Strained Silicon:**

   In CMOS technology, faster velocity of carriers (electrons and holes) can provide a higher current in *Metal-Oxide-Semiconductor Field-Effect Transistors* (MOSFETs), which consequently improves the performance of circuits. At low electric field, the drift velocity is proportional to the electric field strength, and the proportionality constant is defined as mobility of the carriers [10]. Therefore, increasing the mobility can boost the performance of CMOS circuits.

   Study shows that by applying appropriate tensile or compressive stress to the channel, the energy band structure can be slightly tuned, resulting in the enhancement of the

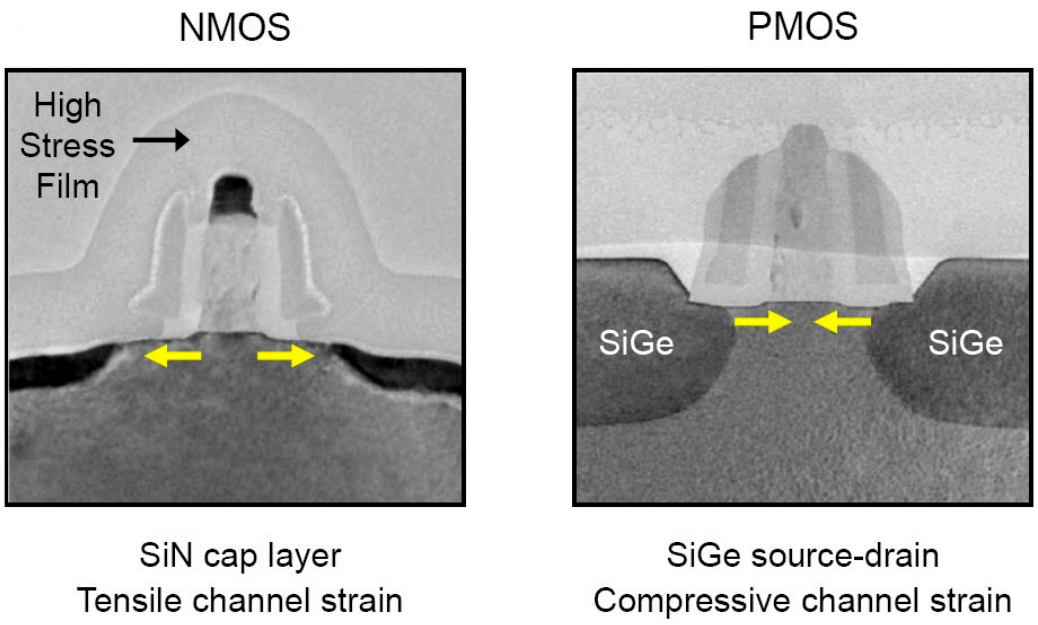


Figure 1.3: Strained silicon technology for enhancing the carrier mobility. Tensile strain in the NMOS channel is created by adding a high-stress layer that wrapped around the transistor, while compressive strain in PMOS channel is created by replacing the conventional source/drain region with strained SiGe [11]

mobility of carriers [12]. Fig. 1.3 shows the technology to achieve strained silicon channel in both *N-type Metal-Oxide-Semiconductor* (NMOS) and *P-type Metal-Oxide-Semiconductor* (PMOS) [11]. The technology of strained silicon has been introduced since the technology node of 90 nm, which increases the saturated currents by 10%~20% and mobility by >50% [13].

2. **High-κ Gate Oxide:**

   SiO_2 has served as gate insulator since the advent of MOS devices. As the scaling down of MOSFETs, the SiO_2 layer became thiner and thiner to maintain the electrostatic control over the channel. Unfortunately, the leakage current through the thin layer of SiO_2 also increased with decreased SiO_2 thickness [14].

   In order to continue the scaling down without sacrificing the leakage power, oxide materials with higher dielectric constant (κ) have been introduced since the technology node of 45 nm [15]. The high-κ materials such as HfO_2 provide sufficient electrostatic control (i.e., sufficiently small equivalent SiO_2 thickness) while having a much thicker physical thickness, which efficiently prevents the gate leakage.

3. **Metal Gate:**

   Polycrystalline silicon was used as the gate material for the easy integration with CMOS technology. In the meantime, the polysilicon gate also suffers from a high gate resistance and a depletion effect [16]. The depleted region in polysilicon behaves as an additional gate oxide, thus increasing the oxide thickness and reducing the electrostatic control [17].

   Since the technology node of 45 nm, metal gates have replaced polysilicon gates to reduce the gate resistance and eliminate the depletion effect [15]. Moreover, the metal gates further enhance the benefits from the high-κ dielectric by reducing the mobility degradation caused by the phonon scattering [18]. Fig. 1.4 shows the conceptual sketch and *Transmission Electron Microscopy* (TEM) image of high-κ dielectric and metal gate stack [15].

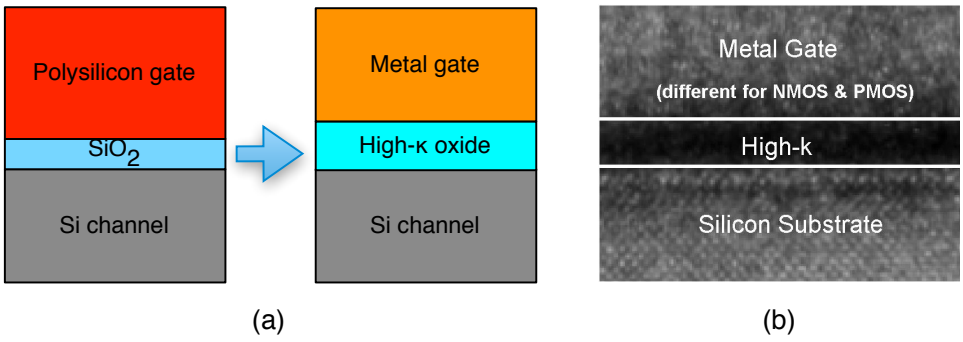


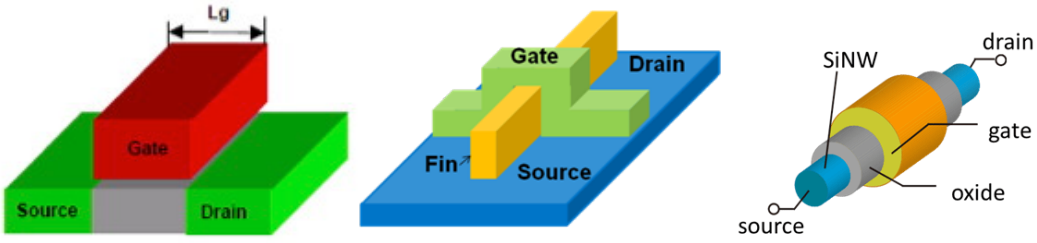
Figure 1.4: (a) High-κ material and metal gate replace SiO_2 and polysilicon gate, (b) *Transmission Electron Microscopy* (TEM) image of hafnium-based high-κ dielectric and metal gate stack [15].

4. **FinFET Structure:**

   When coming to the technology node of 22 nm, the planar bulk structure of MOSFETs cannot provide sufficient electrostatic control over such a short channel (Fig. 1.5(a)). *Short Channel Effects* (SCE) and *Drain-Induced-Barrier-Lowering* (DIBL) can severely degrade the device performance with such a short channel in a planar bulk structure [19, 20].

   In order to maintain the continuous downscaling, different device structures are investigated, including *Partially-Depleted* (PD) *Silicon-On-Insulator* (SOI), *Fully-Depleted* (FD) SOI, *Ultra Thin Body and Buried Oxide FD SOI* (UTBB-FD SOI), FinFET (Fig. 1.5(b)), and gate-all-around nanowires (Fig. 1.5(c)), etc. [21–33]. Yan *et al.* and Colinge studied a "natural length" λ in different device structures to characterize their scalability [34, 35]. Smaller λ indicates a better electrostatic control with a short channel. The study shows that $\lambda = \sqrt{(\varepsilon_{si}/\varepsilon_{ox}/N)\, t_{ox} t_{si}}$, where $N = 1, 2, 4$ for single-gate SOI, double-gate SOI (FinFET), and quadruple-gate (gate-all-around) structures, respectively. Therefore, FinFET has a smaller λ compared to single-gate structure with the same gate oxide (ε_{ox}, t_{ox}) and silicon film (ε_{si}, t_{si}). FinFET is consequently introduced in products at the 22 nm node [36]. The FinFET structure significantly improves the electrostatic control, and enables the continuous scaling down to the present 14 nm technology node [37].

A further improvement on the MOSFET structure will be silicon nanowires that exploiting a *Gate-All-Around* (GAA) structure, which is illustrated in Fig. 1.5(c) [31–33]. As discussed in [35], gate-all-around structure features a even smaller λ as compared to FinFET. Therefore, the GAA SiNWFETs can provide the ultimate electrostatic control with the MOS structure [38, 39].



(a) Planar MOSFET (b) FinFET (c) Silicon Nanowire FET

Figure 1.5: Evolution of MOSFET structures from planar MOSFET to FinFET and silicon nanowire FET.

Besides the evolution on MOSFET structures, channel materials with high carrier mobility (e.g., germanium, III-V materials) or intrinsic *One-Dimensional* (1-D) / *Two-Dimensional* (2-D) structure (e.g., carbon nanotube, graphene, MoS_2) have also been explored to extend the CMOS scaling down [40–44]. Still based on the field effects, they are referred to as "CMOS extension".

1.1.2 Beyond-CMOS Technologies

With all these innovations and efforts in CMOS technology, the transistor size is approaching the natural limitations of materials in the near future [45, 46]. Moreover, the switching energy of silicon FET is also fairly close to a fundamental limit of switching energy of a binary charge-based switch controlled by energy barrier modulation [47]. Therefore, emerging logic devices beyond CMOS technology are expected to continuously address the need of "More Moore". They explore non-charge state variables (e.g., spintronics devices) or novel mechanisms for charge-based devices (e.g., Tunnel FET based on tunneling transport, single electron transistor based on Coulomb blockade) [48–52]. Fig. 1.6 summarizes a classification of emerging logic devices based on the state variables and the switching mechanisms [53].

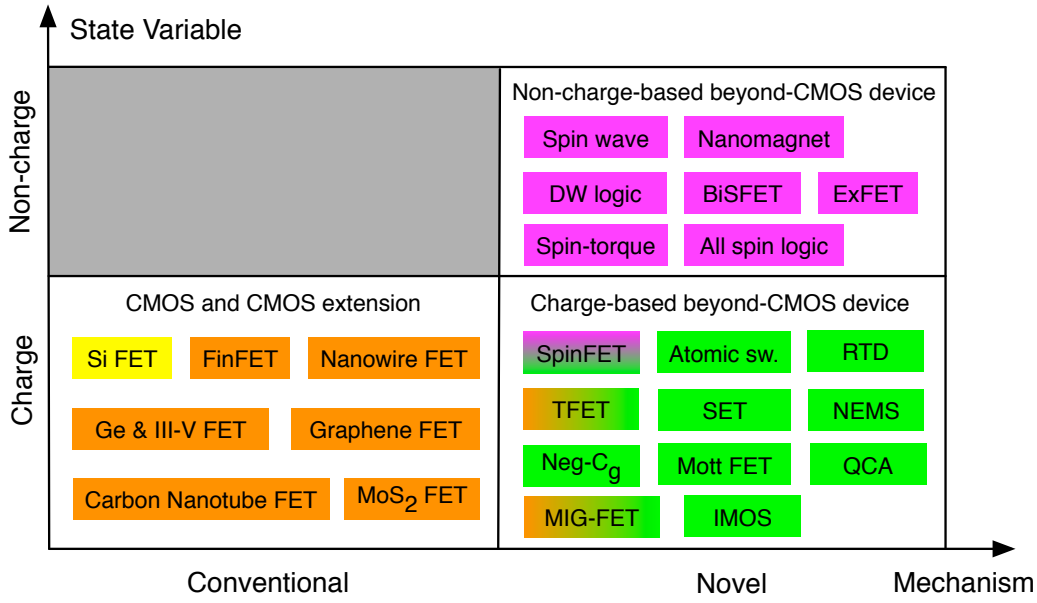


Figure 1.6: A classification of emerging logic devices based on the state variables and the switching mechanisms [53]. The Different colors represent different mechanisms or state variables, and the mixed color reflects the multiplicity of the mechanisms or state variables.

In addition, the circuits are also expected to compute in a more efficient way to keep the trend of "More Moore" when the transistor size approaches the limitations. Therefore, new device concepts are desirable to exploit additional logic functionality. Moreover, with the dramatically increased device density on the chips, reducing the power consumption has become a key concern for circuit applications.

From this perspective, this thesis aims at exploiting the multiple-independent-gate field-effect transistors. The device concept is investigated with silicon nanowire and fin-shaped channels. The devices provide enhanced logic functionality by introducing the electrostatically controlled polarity. The computing efficiency is consequently improved with the proposed devices thanks to the efficient implementation of unate and binate functions. In addition

to the enhanced logic functionality, this thesis further exploits this device concept towards low-power applications. A unique dual-threshold-voltage design with the devices is proposed to achieve a fine trade off between performance and leakage power consumption. Moreover, a steep-subthreshold-slope operation is also demonstrated in the devices, which breaks the limit of subthreshold slope in conventional CMOS technology.

1.2 Current Limitations of CMOS Technology

This section discusses the current limitations of CMOS technology on computing efficiency, as well as the power reduction with multi-threshold-voltage design and supply voltage lowering.

1.2.1 Computing Efficiency

In a majority of real applications, NAND/NOR and exclusive-OR (XOR) intensive functions are the most frequent functions within the circuits [54]. CMOS technology is very efficient in implementing NAND/NOR-based functions. As shown in Fig. 1.7(a), a NAND gate consists of only 4 transistors.

In contrast, to implement the XOR function, CMOS technology has to employ more devices in a complex form as compared to implementing NAND function. Fig. 1.7(b) shows a XOR gate built with 8 transistors excluding the inverters for the input signals.

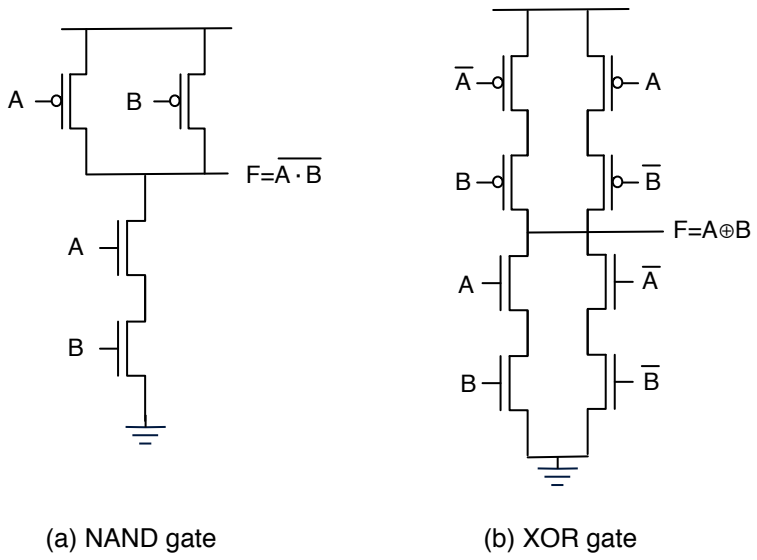


Figure 1.7: Implementation of logic functions with CMOS technology, (a) NAND gate with 4 transistors, (b) XOR gate with 8 transistors excluding the inverters for the input signals.

XOR-based functions are widely used in various circuits, such as arithmetic circuits, parity checker, comparator, etc.. Thus, a less efficient XOR gate can directly affect the performance of these circuits in terms of speed, power consumption and area [55]. Even though many designs

of XOR function have been proposed, the implementation of XOR intensive functions still limits the computing efficiency of CMOS technology [55, 56].

1.2.2 Multi-Threshold-Voltage Design

With the dramatically-increased device density on the chips, the power consumption has to be considered as a prime constraint in the design of integrated circuits, especially for portable equipments that have a limited battery capacity.

The main source of power consumption in integrated circuits can be divided into dynamic power consumption and static power consumption. Dynamic power is consumed whenever the device is utilized. In contrast, static power is consumed as long as the power supply is maintained [57]. Static power consumption is mainly caused by the leakage current through the device in its *off* state, and is called leakage power consumption. Therefore, transistors with low leakage currents can reduce the leakage power consumption in circuit design.

According to the operation of MOSFETs in a certain technology, the subthreshold drain leakage of MOSFETs (I_{off}) exponentially decreases with higher *Threshold Voltage* (V_T). Hence, the utilization of high-V_T devices can reduce the leakage power. Nevertheless, the devices with higher V_T provide lower *on*-state current (I_{on}). Fig. 1.8 shows the characteristics of FinFETs with different threshold voltages [58]. It can be observed that the high-V_T devices provide lower I_{off} by 3 decades but only 50% I_{on} as compared to low-V_T devices.

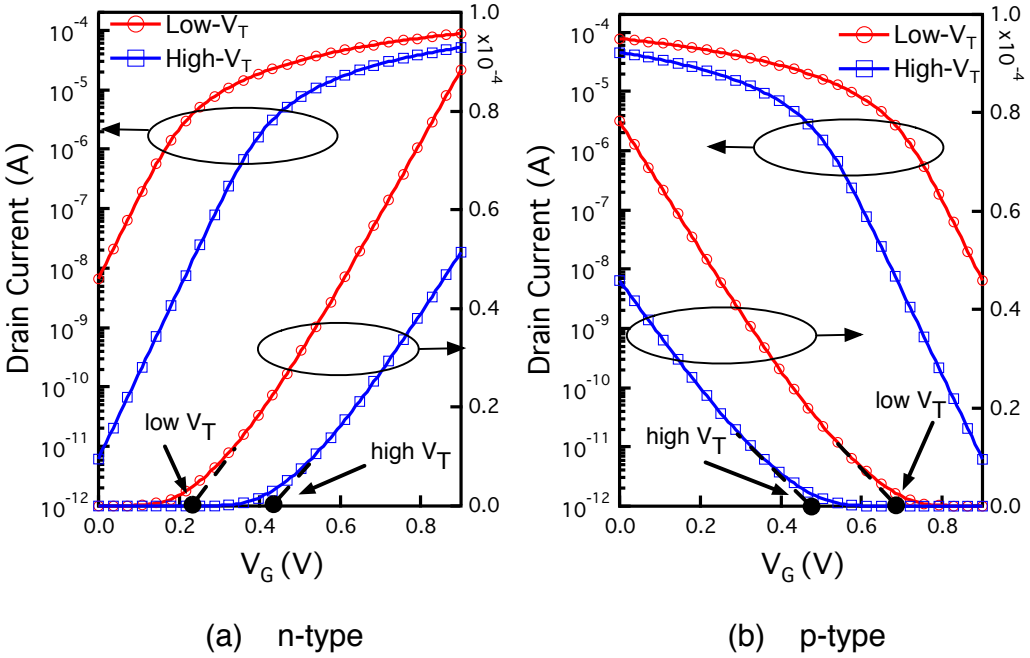


Figure 1.8: Characteristics of low-V_T and high-V_T FinFETs extracted from PTM-MG 20 nm model [58]. (a) *n*FET, (b) *p*FET.

High-V_T devices can efficiently reduce the leakage power consumption with lower I_{off}. However, the lower I_{on} of high-V_T devices may harm the circuit performance at the same time. This can be easily understood by considering the operation of a fundamental CMOS logic gate, i.e., an inverter. As shown in Fig. 1.9, the change of the output value can be simply modeled as charging/discharging the load capacitance C_L through a transistor with the current I_{on}. Thus, the delay of this operation τ can be approximately estimated as:

$$\tau = \frac{C_L V_{DD}}{I_{\text{on}}} \tag{1.1}$$

Eq. (1.1) clearly shows the effect of I_{on} on the circuit performance. Lower I_{on} of high-V_T devices can significantly degrade the circuit speed.

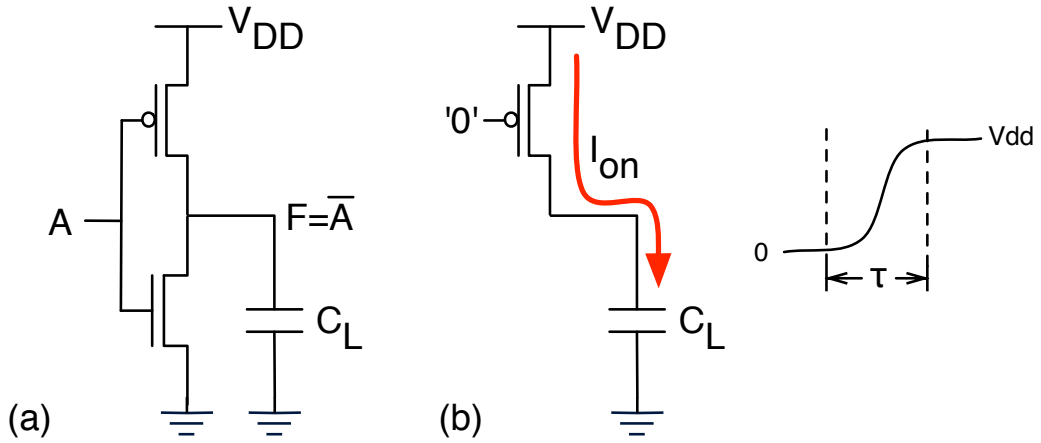


Figure 1.9: A simple way to estimate the delay of an inverter. (a) An inverter with a load capacitance C_L, (b) When input is '0', the NMOS is *off*, and the load capacitance is charged by PMOS with the current I_{on}. The output rises from 0 to V_{DD} in a delay of τ.

In order to make a trade off between the performance and leakage power consumption, the multi-threshold-voltage (multi-V_T) design is widely used in CMOS technology [59]. This method mixes devices with different threshold voltages in the design. In general, low-V_T devices with higher I_{on} are used in the critical paths to meet timing constraints, while high-V_T devices with lower leakage current are used in slack paths to reduce the leakage power consumption.

Fig. 1.10 shows an example of the multi-V_T design. By assuming all the input signals (A0~A6) arrive at the same time, the path G2-G4-G5-G6 has the tightest timing constraint, while the paths G1-G6 and G2-G3-G6 are slack paths. Therefore, the gates G2, G4, G5 and G6 can be built with low-V_T devices to improve the speed of the circuit. G1 and G3 can be built with high-V_T devices to reduce the leakage power without degrading the circuit performance.

However, the above analysis and design of Fig. 1.10 are based on an important condition: the circuit still meets the timing constraint when using G1 and G3 built with high-V_T devices. In

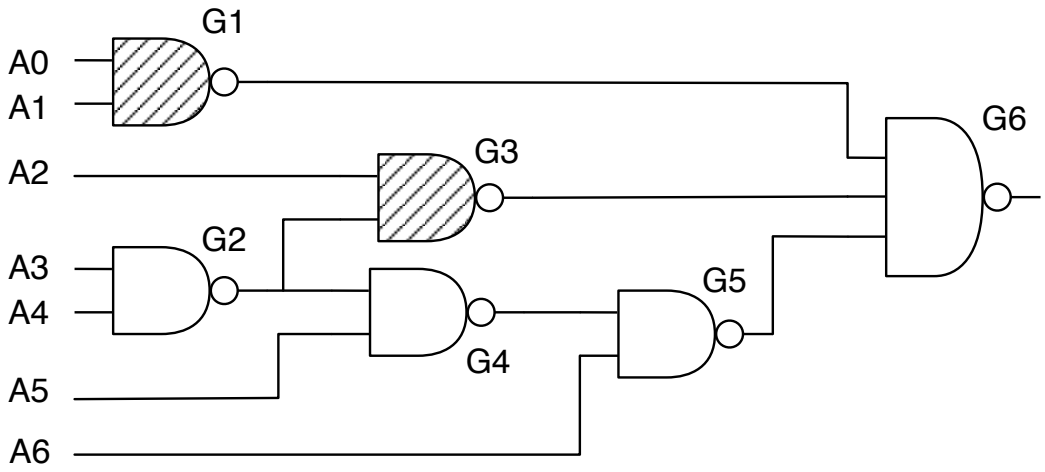


Figure 1.10: An example of multi-V_T design. G1 and G3 in slack paths are built with high-V_T devices, while the other gates are in the critical path, thus using low-V_T devices.

other words, the high-V_T devices should provide significant leakage reduction with acceptable performance degradation. Otherwise, G1 and G3 have to be built with low-V_T devices, and the leakage power is not reduced.

As shown in Fig. 1.8, lower I_{on} in high-V_T devices can significantly degrade the speed of the components. Consequently limited by the discussed condition, the conventional multi-V_T technology can only provide a *coarse* trade off between the circuit performance and the leakage power consumption.

On the other hand, in order to fabricate devices with different threshold voltages, additional process steps are required in conventional multi-V_T design with CMOS technology. This increases the fabrication cost and also reduces the regularity of design.

1.2.3 Supply Voltage Lowering

The total power (dynamic power and static power) consumed by a logic circuit can be approximately estimated as [60]:

$$P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} = I_{\text{leak}} V_{DD} + A \cdot C_L V_{DD}^2 f \tag{1.2}$$

where I_{leak} is the leakage current, V_{DD} is the supply voltage, C_L is the load capacitance, and f is the operating frequency. The activity factor A models the average switching activity in the circuits.

Eq. (1.2) shows that, lowering the supply voltage V_{DD} is an efficient way to reduce both the dynamic and static power consumption.

However, as shown in Fig. 1.11, reducing V_{DD} while keeping the original *Subthreshold Slope* (SS) (Line (1)) leads to a lower I_{on} (Line (2)) and/or a higher I_{off} (Line (3)), i.e., a worse I_{on}/I_{off} ratio. As discussed in Sec. 1.2.2, the degraded I_{on}/I_{off} ratio will lower the circuit speed or increase the static power consumption. In order to maintain good switching properties at lower supply voltage, the transistor requires a steeper SS (Line (4)).

The subthreshold slope (or subthreshold swing) is commonly defined as the *inverse* of the slope of the I_D-V_G characteristics in the logarithmic scale at the subthreshold region. It is thus written as:

$$SS = \frac{\partial V_G}{\partial \log_{10} I_D} \tag{1.3}$$

Therefore, a steeper subthreshold slope means a smaller SS.

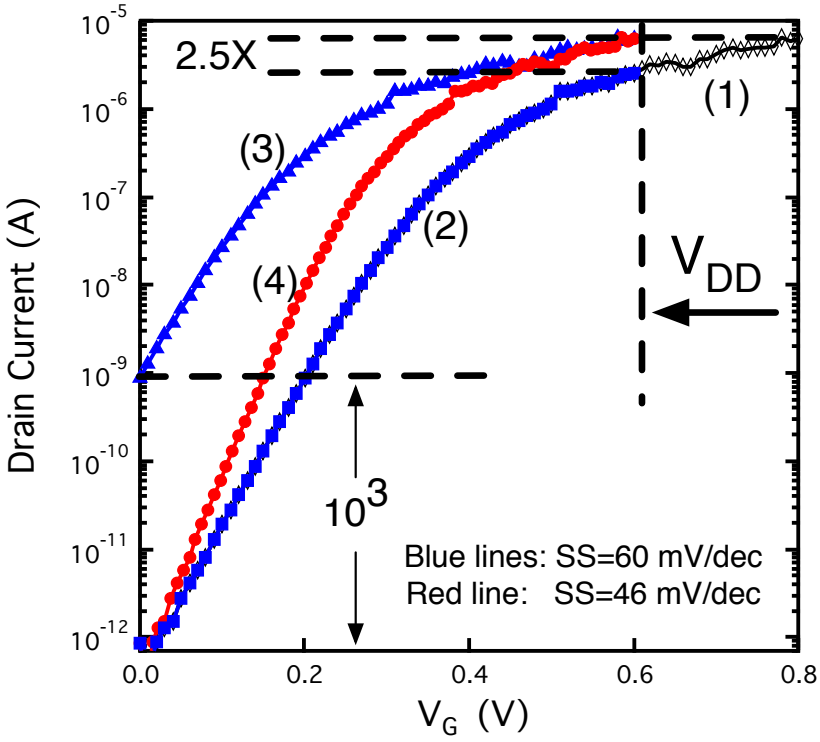


Figure 1.11: Supply voltage lowering requires devices with a steeper subthreshold slope to maintain good switching properties. (1) Original device characteristics with $V_{DD} = 0.8V$, (2) Characteristics by directly reducing V_{DD} to 0.6 V, (3) Shifted characteristics with the same I_{on} and SS as in original device, (4) Characteristics of device with a steeper SS which maintains the I_{on}/I_{off} ratio as in the original device.

Note that, there is a lower bound of the SS in conventional MOSFETs. According to the working principle, the subthreshold current can be considered as majority carriers at source overcome the barrier in the channel, and finally reach the drain. As shown in Fig. 1.12, the barrier is lowered with the increased gate voltage. Thus, the density of carriers with the energy

above the barrier exponentially increases, leading to the exponentially increased subthreshold current [61]. This relationship can be written as:

$$I_{\text{subthreshold}} \propto \exp\left(\frac{q\phi_s}{kT}\right) \tag{1.4}$$

where q is the elementary charge, k is the Boltzmann constant, and T is the temperature, ϕ_s is the surface potential in the channel, which determines the barrier for carrier injection. If the gate has an ideal electrostatic control over the channel, the applied gate voltage completely translates into the drop of the barrier, i.e., $\partial V_G/\partial\phi_s = 1$.

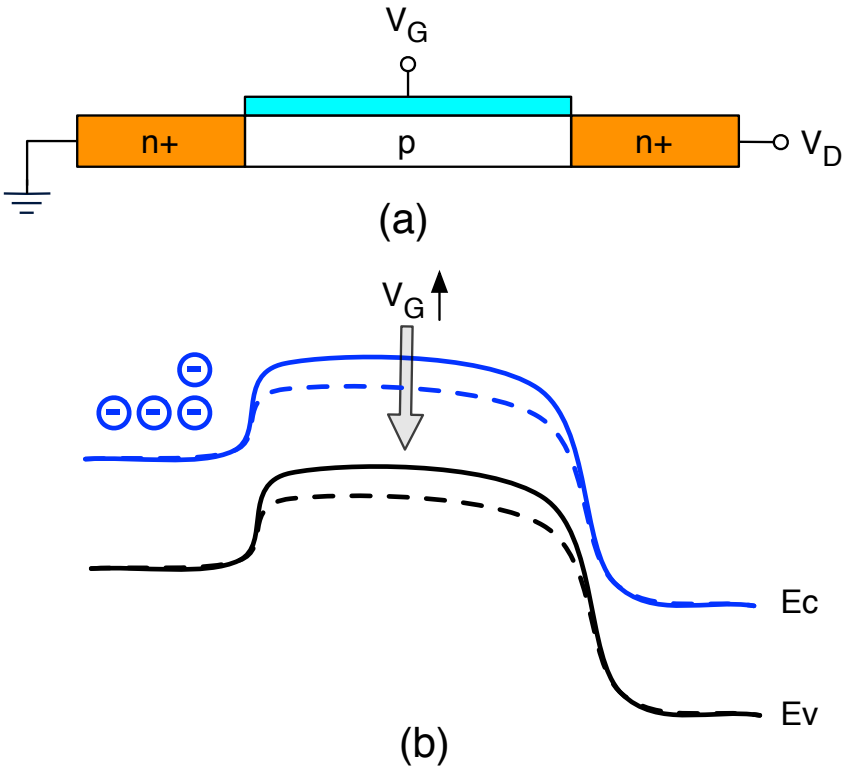


Figure 1.12: (a) Structure of a n-type MOSFET. (b) Band diagram showing the potential barrier lowered by increasing V_G.

Therefore, by substituting (1.4) into (1.3), the lower bound of SS is derived as:

$$SS_{\text{min}} = \frac{kT}{q} \cdot \ln 10 \tag{1.5}$$

Eq. (1.5) gives the limit of subthreshold slope in conventional MOSFETs. At room temperature, this limit is nearly 60 mV/dec.

During the past development of MOSFET technology, this limit provided enough room for reducing the supply voltage while keeping the acceptable performance. Numerous innovations

focused on maintaining a good electrostatic control with the gradually shrunk channel to keep the SS close to this limit [13, 15, 36].

However, the pace of reducing the V_{DD} has to slow down recently. To target ultra-low-power applications with a V_{DD} far below 1.0 V, new device technologies which are not suffering from this limit are highly desired.

1.3 Global Objectives

This thesis aims at exploiting a new device concept that can overcome these limitations of CMOS technology by introducing multiple independent gate terminals. The device is expected to improve the computing efficiency with enhanced logic functionality and enable a fine-tunned multi-threshold-voltage design without sacrificing the regularity of design. In addition, it is also expected to break the limit of subthreshold slope in CMOS technology.

From this perspective, the concept of multiple-independent-gate FETs is proposed. This device concept is investigated with both silicon nanowire and fin-shaped channels. By efficiently utilizing the unique structure to modulate the Schottky barriers, the device can demonstrate three key properties:

(1) Polarity Controllability. The polarity of the device is controlled by an additional bias, which decides the conduction of different types of carriers. With the polarity controllability, the device can efficiently implement XOR-based functions in addition to NAND/NOR-based functions.

(2) Multi-Threshold-Voltage Characteristics. By independently modulating the Schottky barriers at contacts and the barrier in the channel, low-V_T and high-V_T configurations are obtained with the same I_{on} in a single device. The proposed technology can provide a *fine* trade off between performance and leakage power with improved layout regularity. It also brings additional opportunities in design of efficient logic gates.

(3) Steep-Subthreshold-Slope Operation. By introducing a feedback with dynamic modulation of Schottky barriers, the device can achieve a steep SS below 10 mV/dec over the subthreshold region with high $I_{\text{on}}/I_{\text{off}}$ ratio.

This device concept is validated through the characterization of fabricated devices and simulations. Further evaluation at circuit level is carried out, showing the potential of multiple-independent-gate SiNWFETs and FinFETs towards low-power applications.

1.4 Thesis Contributions

This thesis exploits a new device concept: multiple-independent-gate field-effect transistors. The devices are built up with silicon nanowire and fin-shaped channels. The polarity-

controllable device provides new opportunities for circuit design thanks to its enhanced functionality. In the meantime, the proposed technology can improve the low-power design method with the dual-threshold-voltage characteristics and the steep-subthreshold-slope operation.

The proposed device concept is extensively studied on fabrication, dual-V_T characteristics and design, steep-SS operation, and compact modeling. The contributions in each category are introduced as follows:

Device Structure and Fabrication: This device concept is originally proposed in this thesis by efficiently utilizing the electrostatic control of Schottky barriers with a multiple-independent-gate structure. A process flow is developed to fabricate the devices with a top-down approach. Multiple-independent-gate SiNWFETs and FinFETs are experimentally demonstrated in the academic cleanroom of EPFL.

Dual-Threshold-Voltage Characteristics and Design: The reconfigurability of threshold voltage in a single device is achieved by independently modulating the Schottky barriers. This property is validated through the characterization of a *Three-Independent-Gate* (TIG) SiNWFET. The results clearly demonstrate the modulation of threshold voltage and leakage current between low-V_T and high-V_T configurations. Moreover, the device has the same I_{on} in low-V_T and high-V_T operations. This feature can provide a fine trade off between performance and leakage power consumption in circuit design. This device concept also brings new opportunities in efficiently implementing unate and binate logic functions. In the physical design, an uncommitted logic gate pattern is introduced to improve the layout regularity. Dual-V_T design is thus achieved by applying different wiring schemes on the same pattern.

Steep-Subthreshold-Slope Operation: The steep-SS operation is achieved by realizing the weak impact ionization induced feedback. In particular, the electrostatic control of the Schottky barriers in the proposed device concept provides not only the polarity controllability, but also a dynamic modulation of the feedback, which can enhance the steep-SS operation. This property is validated by characterizing the fabricated *Dual-Independent-Gate* (DIG) silicon FinFETs. The measurements show a steep SS of 6 mV/dec over 5 decades of current with high $I_{\text{on}}/I_{\text{off}}$ ratio and good reliability. In addition, feasible improvements are proposed to further improve the device performance.

Compact Modeling: In order to build the bridge between device technology and circuit design, a physics-based potential and drain current model of DIG SiNWFETs is developed. The presented core model captures the basic operation of the device with a good accuracy as compared to *Technology-Computer-Aided-Design* (TCAD) simulation. Advanced physical effects can be integrated into this core framework to accurately model the behavior of the device.

The presented device concept employs the electrostatic control of Schottky barriers at metal-semiconductor contacts. Therefore, it is not limited in silicon nanowire or fin-shaped channel,

but can be extended to SOI or other non-planar structures and other channel materials, such as germanium, etc..

1.5 Thesis Organization

This thesis is organized in five chapters following the introduction. Chapter 2 presents the device structure and fabrication of multiple-independent-gate FETs. Chapter 3 introduces the dual-threshold-voltage characteristics and the design with TIG SiNWFETs. Chapter 4 demonstrates the steep-subthreshold-slope operation with DIG FinFETs. In Chapter 5, a compact model is developed for DIG SiNWFETs. Chapter 6 concludes this thesis and discusses the future work. In detail,

Chapter 2 first introduces the functionality-enhanced technologies presented in literature. Among different device structures, SiNWFETs and FinFETs with multiple independent gates are chosen by considering their advantages in fabrication and design. Then, the fabrication of multiple-independent-gate SiNWFETs and FinFETs is step-by-step presented following a top-down process flow.

Chapter 3 presents the device characteristics with dual threshold voltages and the relevant circuit and physical design. Following the review of conventional multi-V_T technologies, the exploitation on the proposed dual-V_T operation is carried out at both device-level and circuit-level.

Device-Level: First, the working principle of the dual-V_T operation is introduced. Then, the reconfigurability of both the polarity and V_T is experimentally validated by characterizing a TIG SiNWFET with vertically-stacked nanowires. Through TCAD simulation, the effect of structural and physical parameters on the dual-V_T characteristics is discussed. A table-based device model is extracted from TCAD simulation, which is applied in the following circuit-level study.

Circuit-Level: A circuit and physical design approach with TIG SiNWFETs is studied to exploit their applications in dual-V_T circuits. By applying low-V_T and high-V_T configurations, logic gates are compactly implemented towards either high performance or low leakage applications. In physical design, an uncommitted logic gate pattern is introduced to improve the layout regularity. Combinational and sequential elements are mapped onto the uncommitted pattern with different wiring schemes. Benchmarking of logic gates and circuits shows promising performance in dual-V_T design with TIG SiNWFETs as compared to low-standby-power FinFET technology.

Chapter 4 first introduces the steep-SS devices presented in literature. Then, it discusses the steep-SS operation in the proposed device. With a feedback induced by weak impact ionization, the device achieves a steep subthreshold slope in addition to the polarity controllability.

The steep-SS characteristics are studied in terms of experiments and theoretical analysis. In the experimental work, the steep-SS operation is demonstrated through the characterization of DIG FinFETs under different bias and temperature conditions. In the physical analysis, the steep-SS characteristics assisted by the dynamic modulation of Schottky barriers are discussed. Feasible improvements are also suggested to further improve the device performance.

Chapter 5 focuses on the compact modeling of DIG SiNWFETs, as the DIG SiNWFET is the basic structure in the multiple-independent-gate SiNWFET / FinFET concept. A physics-based surface potential and drain current model is derived. Then, the proposed model is validated by comparing the characteristics predicted by the model with TCAD simulation.

Chapter 6 concludes the presented results, and summarizes the achievements of this thesis. Finally, a perspective on future work related to and envisaged from this work is discussed.

2 Device Structure and Fabrication

This chapter first introduces the general principle behind the functionality-enhanced transistors and the previous work presented in literature. Then, the structures of multiple-independent-gate SiNWFET and FinFET employed in this thesis are illustrated in Sec. 2.2. The fabrication of the proposed devices with a top-down process flow is presented step by step in Sec. 2.3. Finally, this chapter is summarized in Sec. 2.4.

2.1 Functionality-Enhanced Transistors

In this section, we first introduce the operation of Schottky-barrier FETs. Then, the functionality-enhanced transistors presented in literature and that rely on a dynamic control of the Schottky barrier contacts are introduced.

2.1.1 Schottky-Barrier FETs

Conventional MOSFETs use heavily doped semiconductor as *Source and Drain* (S/D) to provide electrons or holes for device operation. The chemical doping at S/D determines the type of the device. For example, the implantation of boron forms *p*-type doped S/D. Thus, the fabricated PMOS are based on the conduction of holes. In contrast, NMOS can be obtained with the implantation of arsenic at S/D to supply electrons.

Instead of using heavily doped semiconductor, metal can also be used as S/D material [62, 63]. The contact between metal S/D and semiconductor channel forms a potential barrier at the interface, i.e., Schottky barrier [10]. The conduction of the device can thus be controlled by electrostatically trimming the Schottky barriers.

Fig. 2.1(a) illustrates the structure of a *Schottky-Barrier FET* (SB-FET) with a single gate. Since metal can provide both electrons and holes, the SB-FET can achieve the conductions of both carriers. Fig. 2.1(b) illustrates the band diagram for electrically neutral. In Fig. 2.1(c), the energy band in semiconductor is bent downwards by applying positive gate and drain

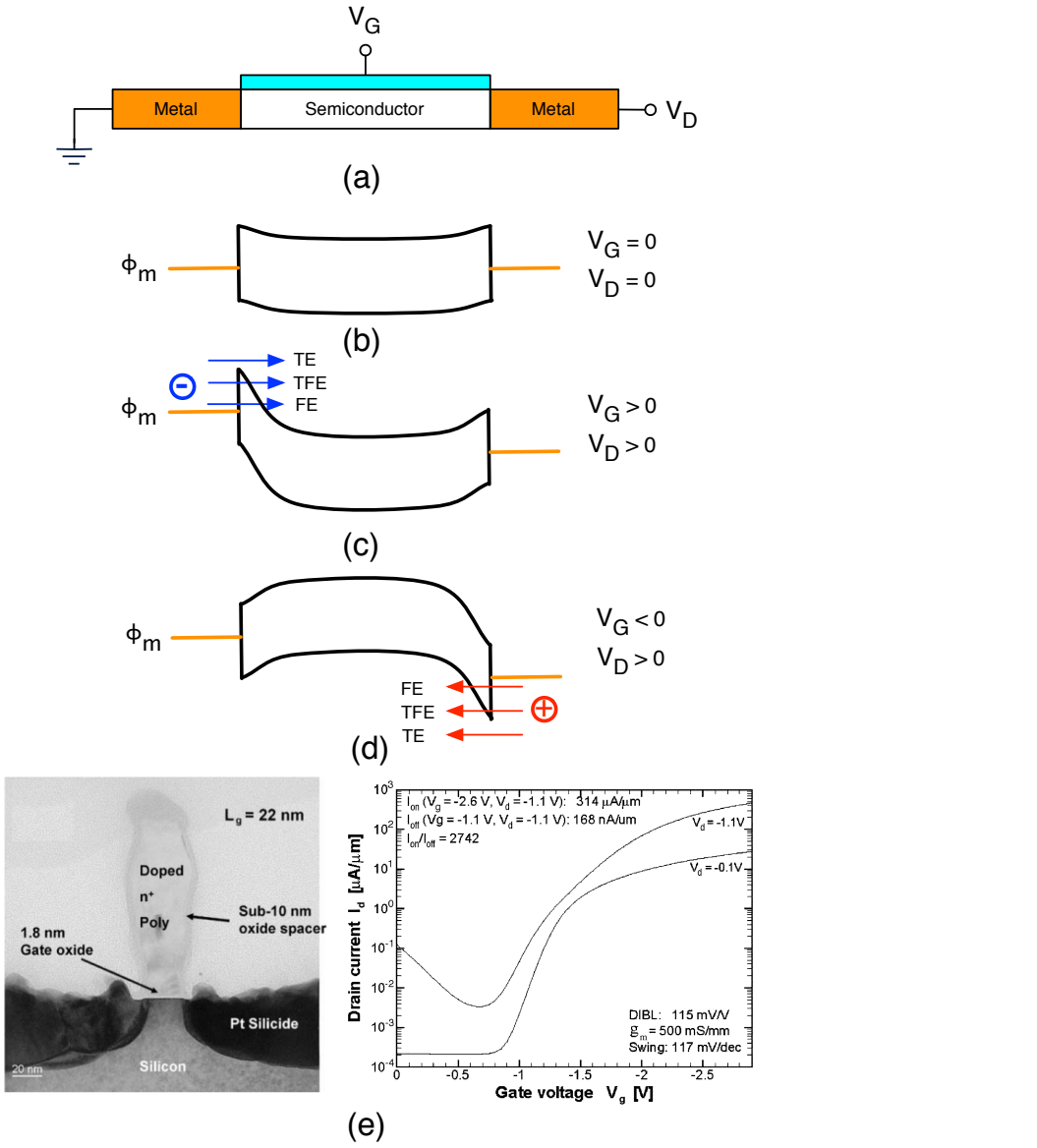


Figure 2.1: Conduction of both electrons and holes in a SB-FET. (a) Schematic of a single-gate SB-FET. (b) Band diagram for electrically neutral. (c) Conduction of electrons in SB-FET with $V_G > 0$. (d) Conduction of holes in SB-FET with $V_G < 0$. (e) Cross-section of a 22-nm p-type SB-FET and the measured characteristics [64].

voltages. Thus, electrons can come into the semiconductor channel from metal by means of *Thermionic Emission* (TE), *Thermionic-Field Emission* (TFE) and *Field Emission* (FE) [10,65,66]. In contrast, the upward band bending obtained by applying a negative gate voltage allows the conduction of holes at the Schottky barrier (Fig. 2.1(d)). Therefore, the device exhibits ambipolar characteristics as shown in Fig. 2.1(e) [64]. However, the ambipolar characteristics may degrade the SS and reduce the I_{on}/I_{off} ratio of the device, thus degrading the circuit performance and increasing the power consumption.

In order to overcome the drawbacks of the ambipolar characteristics and improve the device performance, many techniques are adopted in the development of SB-FETs [67–71]. For example, Fig. 2.2 shows the Schottky-barrier height engineering with dopant segregation technique [67]. The Schottky-barrier height for electrons and holes are tuned by implanting dopant with different dose (Fig. 2.2(a)). The device thus achieves a good I_{on}/I_{off} ratio, which is comparable with conventional MOSFETs (Fig. 2.2(b)). Nevertheless, the obtained SB-FETs have to abandon the conduction of either electrons or holes in a single device. Therefore, the functionality of the SB-FETs with a fixed polarity are still the same as conventional MOSFETs.

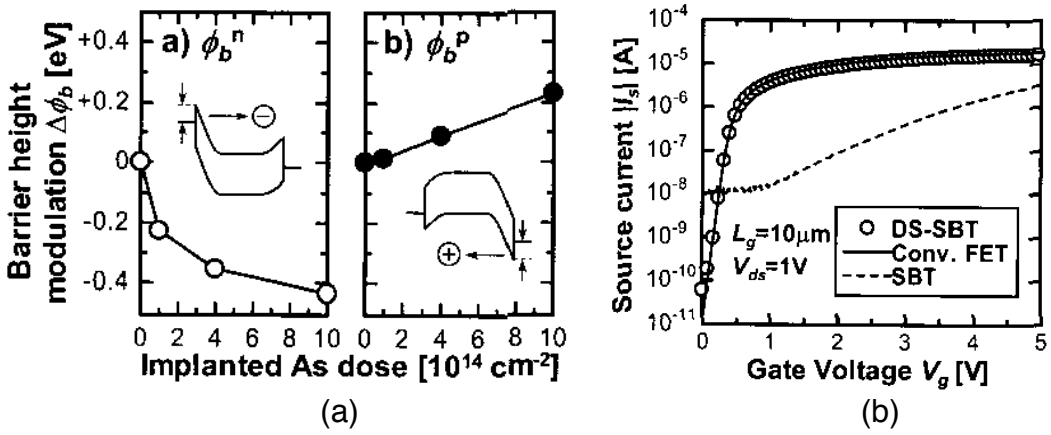


Figure 2.2: (a) Schottky-barrier height engineering with dopant segregation technique, (b) Improved *n*-type performance in SB-FET with dopant segregation, which is comparable to conventional MOSFETs.

2.1.2 Functionality-Enhanced Transistors

As compared to SB-FETs, functionality-enhanced transistors efficiently utilize the inherent ambipolar conduction at Schottky junctions. Relying on the electrostatic trim of Schottky barriers, the devices select the desired type of carriers with one gate. Moreover, the functionality-enhanced transistors employ an additional gate to modulate the conduction of the carriers. Thanks to the cooperation of both gates, the functionality-enhanced transistors can achieve independent control of the polarity and the conduction of the devices, and exhibit both *n*-type and *p*-type characteristics in a single device.

Starting from this principle, functionality-enhanced transistors have been demonstrated with different structures and channel materials. [72–81]. Fig. 2.3 shows some of them.

Heinzig *et al.* fabricate a functionality-enhanced transistor with silicon nanowire as the channel (Fig. 2.3(a)) [73]. Two top gates separately modulate the Schottky barriers at source and drain. During the operation, one gate blocks the unwanted type of carriers, thus determining the polarity of the device. The other gate modulates the tunneling of selected carriers through the corresponding Schottky barrier, thus controlling the channel conduction.

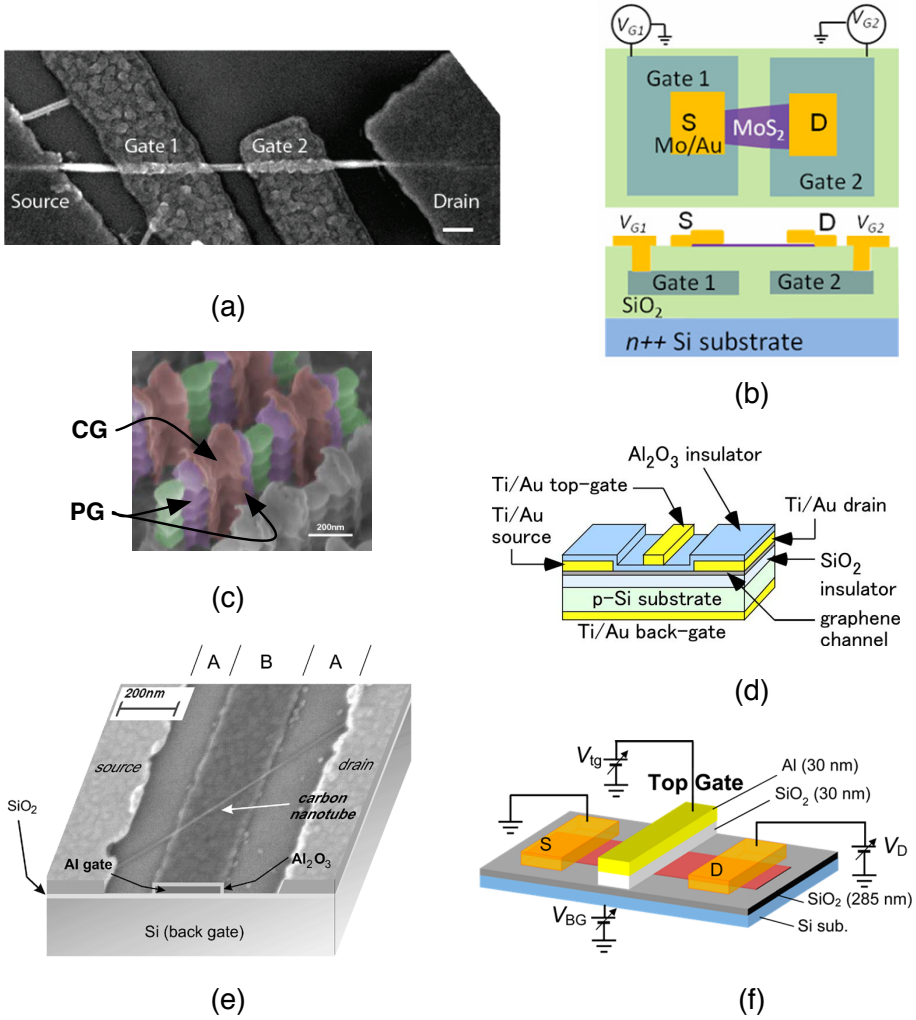


Figure 2.3: Polarity-controllable transistors built with different device structures and materials: (a) single silicon nanowire with two top gates [73], (b) MoS_2 channel with two buried gates [74], (c) vertically-stacked silicon nanowires with double gate-all-around gates [72], (d) graphene with a top gate and a back gate [78], (e) carbon nanotube with a top gate and a back gate [79], (f) α-$MoTe_2$ with a top gate and a back gate [80].

Sutar *et al.* use MoS_2 as the channel material as shown in Fig. 2.3(b) [74] . The device also has two independent gates and consequently similar operation as in Fig. 2.3(a), but the gates are buried in the oxide.

De Marchi *et al.* present a functionality-enhanced device based on vertically-stacked silicon nanowires (Fig. 2.3(c)) [72]. The channel is controlled by three gate-all-around structures . Two gate structures close to source and drain are connected to modulate the Schottky barriers. Therefore, this gate selects the desired carrier type, and is called *Polarity Gate* (PG). The *Control Gate* (CG) modulates a potential barrier in the middle of the channel, which consequently controls the channel conduction.

In Fig. 2.3(d), (e) and (f), the devices feature a top gate controlling the channel conduction, and a back gate modulating the Schottky barriers. The operation of these three devices are similar to the device in Fig. 2.3(c). However, these devices are built with different channel materials. Lin *et al.* use carbon nanotube as the channel materials, while 2-D materials graphene and α-$MoTe_2$ are applied in the work of Harada *et al.* and Nakaharai *et al.* [78–82].

The similarities and the differences between these devices are further discussed as follows:

- **Similarities:**
  1. They all employ metallic S/D contacts with semiconductor channel. Therefore, the operation of the devices is based on the carrier transport at the Schottky barriers.
  2. The devices all use two separate gates to independently control the polarity of the device and the channel conduction.
- **Differences:**
  1. Material:

     Different semiconductor materials are applied to these devices as the channel. Fig. 2.3(a) and (c) both use silicon nanowires. In (a), the channel is made by a single nanowire, while (c) consists of vertically-stacked nanowires; (e) is based on carbon nanotube; (b), (d) and (f) exploit 2-D materials, including MoS_2, graphene, and α-$MoTe_2$.
  2. Number of gated regions:

     Each channel of the devices can be divided into several gated regions from source to drain. Although these devices all have two gates for independent control, the number of gated regions in each device can be different.

     For example, Fig. 2.3(a) and (b) have two gated regions. Each gate controls a Schottky barrier. While (c), (d), (e), (f) all have three gated regions. The two gated regions close to S/D are controlled by a common gate, which modulates both Schottky barriers. The other gate at the middle of the channel controls the conduction of the carriers in the channel.
  3. Placement of Gates:

     These devices place the gates in different ways. In Fig. 2.3(a), two top gates are placed on the nanowires, while (b) buries the two gates underneath the MoS_2 channel. In (c), the two gates are both made with gate-all-around structures. (d), (e) and (f) all build the devices with a top gate and a back gate connected from the substrate.

From the perspective of fabrication, the functionality-enhanced transistors exploit a dopant-free process by replacing heavily doped S/D in CMOS technology with metal. The use of metallic S/D helps to fabricate ultra-shallow S/D junctions with a low resistance [83]. In

addition, the dopant-free process may eliminate the ion implantation and reduce the variation due to random dopant fluctuation in nano-scale devices [84, 85].

More importantly, the polarity controllability can be utilized to implement new logic architectures in a compact form [86–89]. In particular, the polarity-controllable FETs can efficiently implement both NAND-based and XOR-based functions with the enhanced logic functionalities [54, 86, 90]. Therefore, the application of polarity-controllable FETs can promote the design of more efficient logic circuits, which will be discussed in details in Chapter 3.

2.2 Structure of Multiple-Independent-Gate FETs

Functionality-enhanced transistors introduced before are fabricated with different channel materials and gate structures. In this thesis, we consider that:

1. Compared to new materials such as carbon nanotube or MoS_2, silicon is preferred as the channel material in this study because of the mature technology for device fabrication and large-scale integration. The mature technology can enhance the yield of high-quality devices and circuits during the complex fabrication steps, including etching, oxidation, and Schottky-barrier formation, etc..

2. Compared to the bulk structure, the use of the silicon nanowire or fin-shaped channel is best suited for excellent electrostatic control, which is considered as a primary requirement for deeply scaled devices, especially when the channel length shrinks to below 20 nm [36, 38, 39].

3. When employing the device structure with a top gate and a back gate, it is difficult to independently control each device on the substrate. In contrast, the structure with independent top gates provides independent control of each device from the top, thus enabling the circuit-level fabrication with the proposed devices.

4. Moreover, the multiple-gate structure can enhance the degree of freedom and range of functionalities in one transistor by independently controlling each Schottky barrier and the conduction of the channel.

Finally, this thesis proposes the multiple-independent-gate field-effect transistors through the investigation of different materials and structures. Silicon nanowire and fin-shaped channel are applied to this device concept based on the above considerations.

The conceptual sketches of two representatives of the multiple-independent-gate SiNWFET and FinFET are shown in Fig. 2.4. In Fig. 2.4(a), vertically-stacked silicon nanowires are confined within the source and drain pillars. The channels are surrounded by three independent gates, named *Polarity Gate at Source* (PG_S), *Control Gate* (CG) and *Polarity Gate at Drain* (PG_D). Nickel silicide is used as S/D material to form Schottky junctions with the silicon channel.

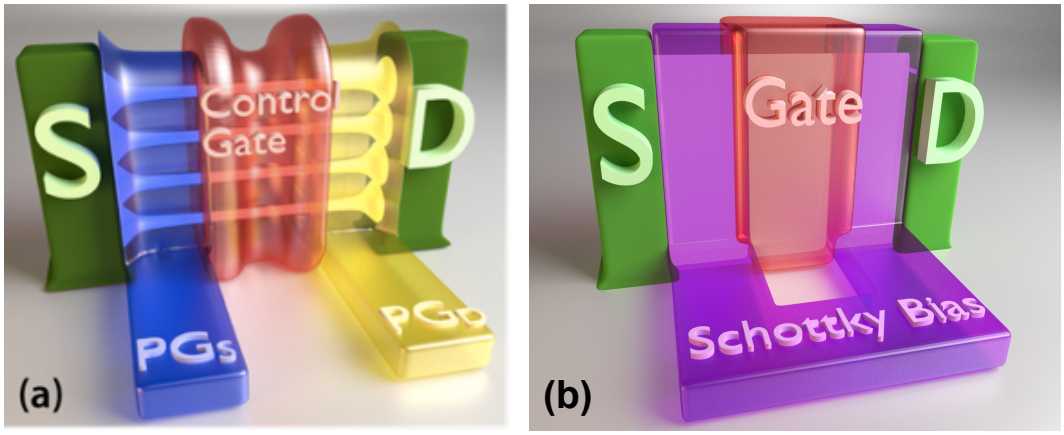


Figure 2.4: Structure of (a) three-independent-gate SiNWFET and (b) dual-independent-gate silicon FinFET.

Therefore, PG_S and PG_D in the structures modulate the Schottky barriers at the source and drain contacts, while CG controls the current flow through the channel.

Fig. 2.4(b) shows a dual-independent-gate silicon FinFET. As compared to the device in Fig. 2.4(a), PG_S and PG_D in this device are connected together to bias the Schottky barriers. Therefore, the connected polarity-gates are renamed as *Schottky Barrier Bias* (SBB), and the control gate is simply called *Gate* (G). Note that, the dual-independent-gate structure is a simplified multiple-independent-gate structure, which can be directly obtained by connecting PG_S and PG_D in the layout design.

The three-independent-gate SiNWFET in Fig. 2.4(a) will be used to discuss the dual-threshold-voltage characteristics and design in Chapter 3, and the dual-independent-gate FinFET in Fig. 2.4(b) will be used to demonstrate the steep-subthreshold-slope operation in Chapter 4.

2.3 Device Fabrication

In order to experimentally demonstrate the multiple-independent-gate SiNWFETs and FinFETs, a process flow is developed and completely implemented at the facilities in the Center of MicroNanoTechnlogy (CMi) of EPFL. In this section, we show the process flow and runcard of the fabrication of three-independent-gate SiNWFETs and FinFET. Devices with dual independent gates can be fabricated with the same process by connecting the two polarity gates in the layout design.

First, a lightly *p*-type boron doped ($\sim 10^{15}/cm^3$) SOI 100 mm wafer with a 340 nm thick silicon device layer is used as the substrate. The thickness of the *Buried Oxide* (BOX) is $2\mu m$. The crystal orientation of the SOI layer is (100), and the resistivity of the SOI layer is between $8.5\Omega \cdot cm$ to $11.5\Omega \cdot cm$.

The desired critical feature size of the devices is around 50 nm, which is the diameter of nanowires and thickness of fins. In order to write such small patterns, the Vistec EBPG5000 electron-beam lithography system is used, which is capable of writing <10 nm features and placing structures on a substrate with an accuracy of less than 20 nm [91].

The fabrication of the devices is implemented with a CMOS-compatible top-down approach, which is suitable for circuit fabrication and large-scale integration. The process consists of six main steps, i.e., the fabrication of (1) alignment markers, (2) channel, (3) polarity gates, (4) control gate, (5) nitride spacers, and finally (6) nickel silicide. The detailed process flow is introduced below.

(1) **Alignment markers:** In order to perform the good alignment between the different masks used in the following steps, alignment markers are first fabricated on the wafer. The makers are defined as $20\mu m \times 20\mu m$ squares using e-beam lithography. Then, the 340 nm SOI layer is completely etched through with plasma dry etching, followed by a BHF etching of the $2\mu m$ buried oxide. After etching through the buried oxide, the silicon substrate is continuously etched by $\sim 1.2\mu m$ using plasma etching. Finally, the markers with a depth of around $\sim 3.5\mu m$ are obtained to provide enough contrast for the following alignment operation. Fig. 2.5 sketches the cross-section of the SOI wafer and the finally obtained alignment maker. Table 2.1 lists the process runcard for fabricating the alignment markers.

Table 2.1: Process for fabricating alignment markers

Step	Description	Equipment	Program/Parameters	Target
1.1	Sub. dehydratation	Z7 / hot plate	180°C	5 min
1.2	ZEP coating	Z7 / spin coater	ZEP 100%, 2000rpm	550 nm
1.3	ZEP baking	Z7 / hot plate	180°C	5 min
1.4	Exposure	Z7 / Vistec EBPG5000	**Mark**, 220 μC/cm^2	/
1.5	Development	Z7 / wetbench	n-amyl-acetate	2 min
1.6	Substrate rinsing	Z7 / wetbench	90:10 MiBK:IPA	1 min
1.7	SOI layer etching	Z2 / AMS 200	Si_opto, 1 min	0.34 μm
1.8	BOX layer etching	Z2 / Plade oxide	BHF 2nd bath, 35 min	2 μm
1.9	Substrate etching	Z2 / AMS 200	Si_opto, 1 min	1.2 μm
1.10	ZEP removal	Z2 / Oxford	O_2	20 min
1.11	Piranha cleaning	Z2 / Piranha	/	/

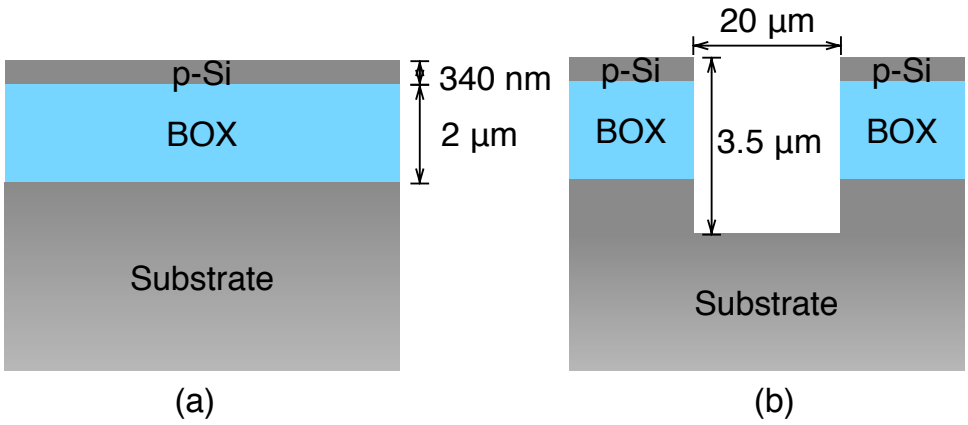


Figure 2.5: (a) Cross-section of the SOI wafer with 340 nm silicon device layer and 2μm buried oxide, (b) Dimensions of the fabricated alignment markers.

(2) **Channel fabrication (silicon nanowires and fins):**

The processes of fabricating silicon nanowires and fins are introduced separately.

(2.1) **Silicon nanowires:** First, the nanowires and the S/D regions are defined using e-beam lithography (Fig. 2.6(a)). The length and the diameter of the defined nanowires are 350 nm and 50 nm, respectively. Then, vertically-stacked nanowires are formed in a top-down fashion, using a single *Deep Reactive Ion Etching* (DRIE) process step (i.e., Bosch process) [72, 92]. This DRIE process is illustrated in Fig. 2.6(b)-(f) [93]. A silicon dry etching with SF_6 plasma is interleaved with a C_4F_8 plasma induced passivation. These two steps are cycled a number of times, thus creating a number of vertically-stacked nanowires under the protection of photo resist. By co-optimizing the etching rate and the number of etching cycles, four nanowires are finally obtained in the 340 nm silicon layer as shown in Fig. 2.7(a).

Table 2.2: Process for fabricating vertically-stacked silicon nanowires

Step	Description	Equipment	Program/Parameters	Target
2.1	Sub. dehydratation	Z7 / hot plate	180°C	5 min
2.2	HSQ coating	Z7 / spin coater	HSQ 2%, 3500rpm	50 nm
2.3	Exposure	Z7 / Vistec EBPG5000	NW, 900-1300 $\mu C/cm^2$	/
2.4	Development	Z7 / wetbench	MF_CD_26, then rinse	2 min
2.5	Substrate Rinsing	Z7 / wetbench	DI water rinse until R>	15Mohms
2.6	NW formation	Z2 / AMS 200	MM_SOI_ACCU	4 cycles
2.7	HSQ removal	Z2 / Plade oxide	BHF, Bath 1	20 sec

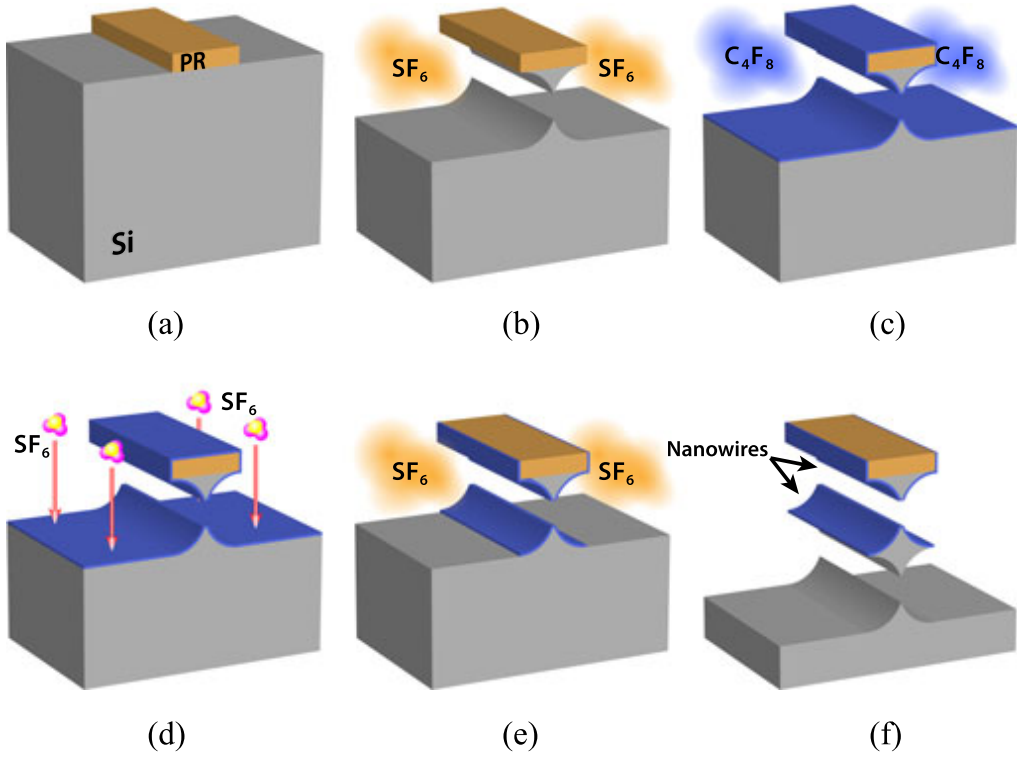


Figure 2.6: DRIE (Bosch) process applied to the fabrication of vertically-stacked silicon nanowires. (a) The diameter and the length of the nanowires are defined with photoresist mask on silicon; (b) physical/chemical SF_6 etching is applied, creating an undercut below the mask pattern; (c) C_4F_8 plasma forms conformal thin passivation on the structure; (d) SF_6 is applied again, (e) vertically accessible surface passivation is readily removed by the partly anisotropic SF_6 etching; (f) finally, a new undercut is produced by chemical etching by the SF_6, leading to a new nanowire. [93]

The typical vertical spacing between the nanowires is 40 nm. Table 2.2 lists the process runcard for fabricating the vertically-stacked silicon nanowires.

(2.2) **Silicon fin:** After defining the length and the width of the fin as well as the S/D region, a vertical dry etching of silicon is applied to the SOI layer. Table 2.3 lists the detailed process for fabricating the silicon fins. Fig. 2.7(b) shows a fabricated fin-shaped channel with a length of 800 nm and a width of 50 nm.

(3) **Polarity gates:** The necessary piranha cleaning and RCA cleaning steps are first performed [94, 95]. Then, a 15 nm SiO_2 gate dielectric is formed with high-temperature oxidation process, and 50 nm polycrystalline silicon layer is deposited.

To fabricate SiNWFETs, two *G*ate-*A*ll-*A*round (GAA) structures with a length of 120 nm are patterned on the 380 nm long silicon nanowires.

To fabricate FinFETs with a fin-shaped channel of 800 nm long, two structures covering

Table 2.3: Process for fabricating silicon fins

Step	Description	Equipment	Program/Parameters	Target
2.1	Sub. dehydratation	Z7 / hot plate	180°C	5 min
2.2	ZEP coating	Z7 / spin coater	ZEP 100%, 2000rpm	550 nm
2.3	ZEP baking	Z7 / hot plate	180°C	5 min
2.4	Exposure	Z7 / Vistec EBPG5000	**Fin**, 185-255 μC/cm^2	/
2.5	Development	Z7 / wetbench	n-amyl-acetate	2 min
2.6	Substrate rinsing	Z7 / wetbench	90:10 MiBK:IPA	1 min
2.7	Fin formation	Z2 / AMS 200	Si_opto_slow, 40 sec	0.34 μm
2.8	ZEP removal	Z2 / Oxford	O_2	20 min

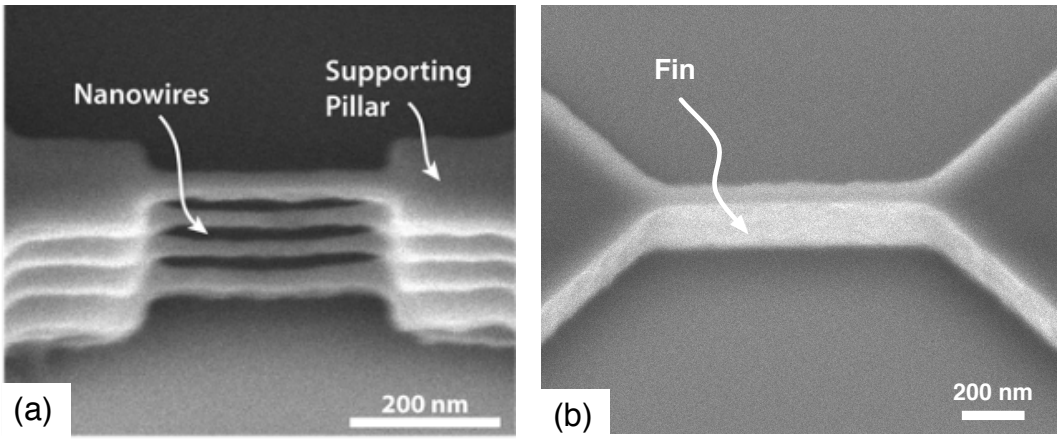


Figure 2.7: (a) Fabricated four vertically-stacked silicon nanowires confined within supporting pillars, (b) fabricated silicon fin-shaped channel.

the top and the sidewalls of the fin are patterned with a length of 200 nm.

The unwanted polysilicon is removed by the Bosch process similar to the one used in the fabrication of nanowires. As shown in Fig. 2.8, the Bosch process can completely remove the polysilicon between the two gate structures, therefore guaranteeing a good isolation and consequently a low leakage current between PG_S and PG_D.

Table 2.4 lists the process for fabricating the polarity gates.

(4) **Control gate:** A second 15 nm gate oxidation and 50 nm polycrystalline silicon deposition are performed following necessary cleaning steps. Considering the silicon consumed during oxidation, the resulting diameter of nanowires and the width of the fin are around 30~40 nm. Then, CG is patterned in a self-aligned way.

Fig. 2.9 shows the cross-section of the vertically-stacked nanowires, the PG and the CG,

Table 2.4: Process for fabricating polarity gates

Step	Description	Equipment	Program/Parameters	Target
3.1	Piranha cleaning	Z2 / Piranha	/	/
3.2	RCA2 only	Z3 / RCA wetbench	/	/
3.3	Gate oxidation	Z3 / Centrotherm	gox	15 nm
3.4	LPCVD Polysilicon	Z3 / Centrotherm	poly	50 nm
3.5	Sub. dehydratation	Z7 / hot plate	180°C	5 min
3.6	ZEP coating	Z7 / spin coater	ZEP 100%, 2000rpm	550 nm
3.7	ZEP baking	Z7 / hot plate	180°C	5 min
3.8	Exposure	Z7 / Vistec EBPG5000	PG, 200- 220 μC/cm^2	/
3.9	Development	Z7 / wetbench	n-amyl-acetate	2 min
3.10	Substrate rinsing	Z7 / wetbench	90:10 MiBK:IPA	1 min
3.11	Native oxide etching	Z2 / AMS 200	SiO2_PR_1:1	3 sec
3.12	Polysilicon etching	Z2 / AMS 200	MM_NW_REL	25 sec
3.13	ZEP removal	Z2 / Oxford	O_2	20 min

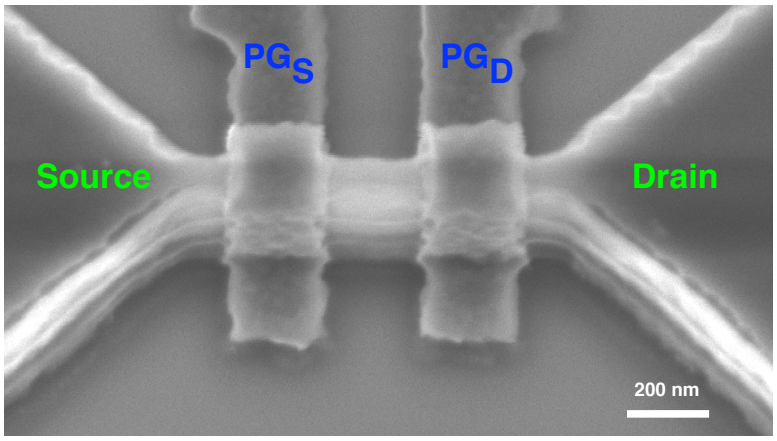


Figure 2.8: Fabricated polarity gates in the multiple-independent-gate FinFET.

while Fig. 2.10 shows the fabricated gates on a fin-shaped channel. From both images, we can identify the overlaps between PG and CG, which are produced in the self-aligned CG patterning. These overlaps ensure that the silicon channel is completely covered by the gates in both SiNWFETs and FinFETs. The obtained structure not only provides good electrostatic control over the entire channel, but also protects the channel from the following silicidation.

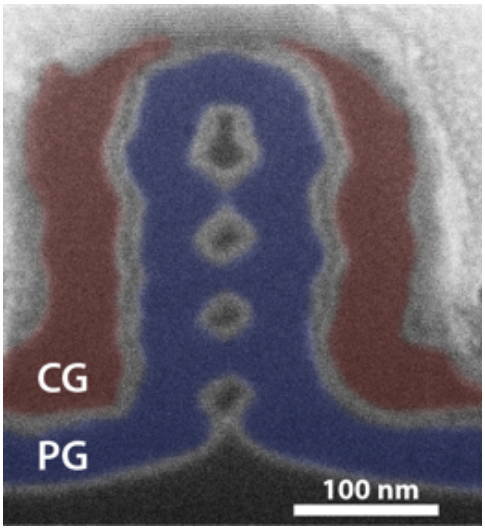


Figure 2.9: Cross-sectional view of the vertically-stacked nanowires, PG and CG.

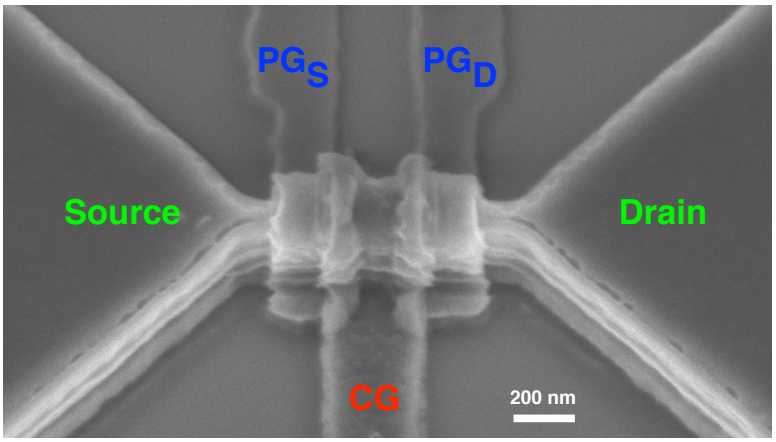


Figure 2.10: Tilted top view of the fabricated polarity gates and CG on a fin-shaped channel.

Table 2.5 lists the runcard for fabricating the control gate. Note that, in the current fabrication setup, the thick gate oxide is used to maximize the fabrication yield within our academic clean room facility by guaranteeing the correct connectivity and reduce the risk of gate leakage. Nevertheless, no physical constraints limit gate oxide scaling in this device with state-of-the-art high-κ dielectric stacks directly implementable in the fabrication process.

(5) **Spacer:** After the formation of PG and CG, 5 nm SiO_2 and 20 nm low-stress silicon nitride are formed on top of the whole structure. Then, an anisotropic etching of silicon nitride is performed to obtain spacers at the edges of the steps. The principle of the formation of spacers is illustrated in Fig. 2.11, and the fabricated spacers in a multiple-independent-gate FinFET are shown in Fig. 2.12. The spacers are used as the isolation

Table 2.5: Process for fabricating control gate

Step	Description	Equipment	Program/Parameters	Target
4.1	Piranha cleaning	Z2 / Piranha	/	/
4.2	RCA2 only	Z3 / RCA wetbench	/	/
4.3	Gate oxidation	Z3 / Centrotherm	gox	15 nm
4.4	LPCVD Polysilicon	Z3 / Centrotherm	poly	50 nm
4.5	Sub. dehydratation	Z7 / hot plate	180°C	5 min
4.6	ZEP coating	Z7 / spin coater	ZEP 100%, 2000rpm	550 nm
4.7	ZEP baking	Z7 / hot plate	180°C	5 min
4.8	Exposure	Z7 / Vistec EBPG5000	CG, 200- 220 μC/cm^2	/
4.9	Development	Z7 / wetbench	n-amyl-acetate	2 min
4.10	Substrate rinsing	Z7 / wetbench	90:10 MiBK:IPA	1 min
4.11	Native oxide etching	Z2 / AMS 200	SiO2_PR_1:1	3 sec
4.12	Polysilicon etching	Z2 / AMS 200	MM_NW_REL	25 sec
4.13	ZEP removal	Z2 / Oxford	O_2	20 min

between source/drain and the gates during the following silicidation in order to avoid short circuits between different structures.

Table 2.6 lists the process runcard for fabricating the spacers.

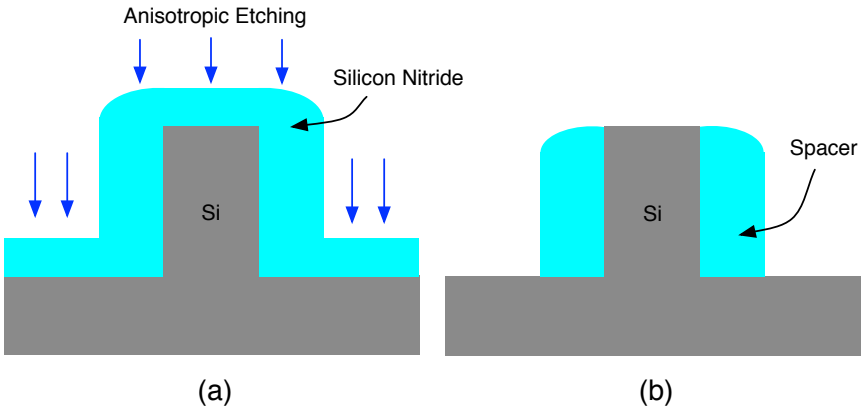


Figure 2.11: Principle of the formation of spacers. (a) Anisotropic etching of deposited silicon nitride over a silicon step, (b) Spacers obtained at the edges after the anisotropic etching.

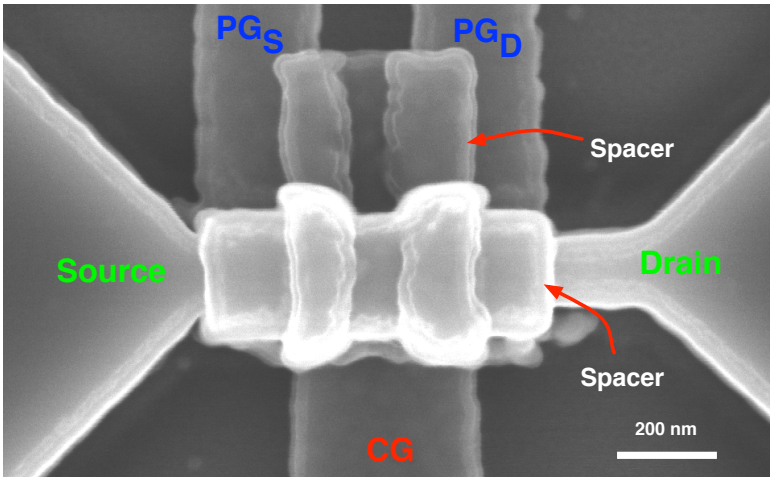


Figure 2.12: Fabrication of spacers in the multiple-independent-gate FinFET. The spacers form necessary isolation between S/D and PG, as well as between PG and CG.

Table 2.6: Process for fabricating spacers

Step	Description	Equipment	Program/Parameters	Target
5.1	Piranha cleaning	Z2 / Piranha	/	/
5.2	RCA2 only	Z3 / RCA wet bench	/	/
5.3	Dry oxide	Z3 / Centrotherm	dox	5 nm
5.4	Low stress nitride	Z3 / Centrotherm	lsnt	20 nm
5.5	Spacer etching	Z2 / AMS200	SiO2_PR_1:1	8 sec

(6) **Silicide:** The wafer is first cleaned with oxygen plasma and BHF solution to obtain a high-quality surface for silicidation. Directly following the cleaning process, a 20 nm nickel layer is deposited with sputtering. Compared to the evaporation method, sputtering supports an in-situ cleaning and also increases the layer uniformity and adhesion to the substrate [96]. Then, the nickel layer is subsequently annealed to form nickel silicide. The annealing is performed in forming gas with a step-like process: 20 minutes at $200°C$, then 20 minutes at $300°C$, then 20 minutes at $400°C$. Finally, the unreacted nickel is removed in a hot piranha solution (4:1 mixture of 96% H_2SO_4 and 30% H_2O_2). The detailed process of the silicidation step is listed in Table 2.7.

The silicidation step creates Schottky junctions at source and drain with the silicon channel. At the same time, the nickel silicide is also formed on the polycrystalline silicon gates to reduce the resistance of the gate contacts. By controlling the annealing temperature and duration, Ni_1Si_1 is selected among different phase of nickel silicide [72, 97]. The Ni_1Si_1 phase is preferred because of its near mid-gap workfunction with

Table 2.7: Process of silicidation

Step	Description	Equipment	Program/Parameters	Target
6.1	Plasma O2 clean	Z2 / Oxford	O_2	5 min
6.2	Native oxide removal	Z2 / Plade oxide	BHF, 2nd bath	20 sec
6.3	Nickel sputtering	Z11 / DP650	RT_Ni_E_Unif, 1 min	20 nm
6.4	Annealing	Z3 / Centrotherm	N_2 + 5%H_2 @(200°C + 300°C + 400°C)	20 min+ 20 min+ 20 min
6.5	Piranha nickel etch	Z14 / Acid wetbench	160 ml H_2SO_4 + 40 ml H_2O_2	5 min

respect to silicon (~4.8 eV) and low resistivity, further providing low interface defects at the junctions [93, 98, 99].

Fig. 2.13 shows the *Scanning Electron Microscopy* (SEM) image of the final structures of the fabricated multiple-independent-gate SiNWFET and FinFET.

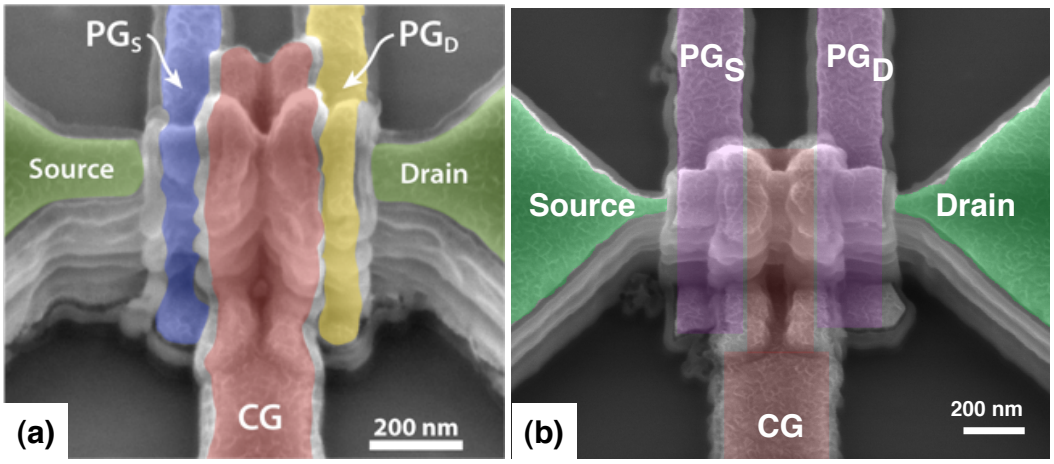


Figure 2.13: SEM images of the fabricated (a) multiple-independent-gate SiNWFET and (b) multiple-independent-gate silicon FinFET.

Note that, the device may be more aggressively scaled without any fundamental limitations coming from the device physics. Specifically, the gate-all-around and fin-shaped channel geometries are best suited for strong suppression of short channel effects. In addition, the absence of abrupt doping profiles in the channel relaxes constraints on doping levels down to the technology nodes at 22 nm and beyond [100].

2.4 Chapter Summary

Functionality-enhanced transistors have been demonstrated with different channel materials and different gate structures. The enhanced functionality is achieved by a polarity control through independently modulating the carrier transport at Schottky barriers and in the channel of the devices. Based on this principle, multiple-independent-gate silicon nanowire FETs and FinFETs are proposed. The structures of the proposed devices are suitable for device fabrication and large-scale integration. A process flow for fabricating the devices in a top-down approach is introduced step by step. In addition to polarity control, the multiple-independent-gate structure can further enhance the functionality of the devices, which will be discussed in following chapters.

3 Dual-Threshold-Voltage Characteristics and Design

This chapter exploits the capability of multiple-independent-gate FETs in the general field of multi-V_T design. It shows the dual-V_T characteristics of the devices, as well as circuit design opportunities and physical design method. Sec. 3.1 briefly reviews the multi-V_T technologies in CMOS. Sec. 3.2 discusses the dual-V_T operation of the multiple-independent-gate FETs. The device characterization is presented in Sec. 3.3 followed by discussion on the dual-V_T operation in Sec. 3.4. Then, the circuit design opportunities and physical design method are shown in Secs. 3.5 and 3.6. Finally, the chapter is summarized in Sec. 3.7.

3.1 Multi-Threshold-Voltage Technologies

As discussed in Sec. 1.1.2, for a given technology node, devices with low V_T normally show larger I_{on} but also much larger I_{off} when compared to high-V_T devices. For example, the drive current of low-V_T devices is ~ 1.4× larger than in high-V_T devices, but I_{off} is also ~ 100× higher with Intel's 32 nm technology [101].

Therefore, in multi-V_T design, low-V_T devices with larger I_{on} are used in the critical paths to reduce delay and meet timing constraints. In non-critical paths, leakage power consumption becomes the main constraint. Then, high-V_T devices with lower I_{off} are preferred. The mix of different threshold voltages is a common technique to reduce the overall leakage power consumption, without degrading the performance of circuits [59].

3.1.1 Threshold Voltage in MOSFETs

In CMOS technology, in order to obtain devices with different threshold voltages, the knowledge on the relationship between V_T and structural parameters of MOSFETs is first needed. Eq. (3.1) gives the V_T in a n-type MOSFET with a sufficiently long channel (i.e., $L \gg \lambda$) [10]:

$$V_{T,\text{long}} = V_{FB} + 2\phi_F + \frac{\sqrt{2\epsilon_{si} q N_A (2\phi_F - V_{BS})}}{C_{ox}} \tag{3.1}$$

where ϵ_{si} is the dielectric constant of silicon, N_A is the doping concentration of the channel, V_{BS} is the bias between the body and the source, and $C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$ is the oxide capacitance in unit area with ϵ_{ox} and t_{ox} the dielectric constant and the thickness of gate oxide, respectively. In addition, the flat-band voltage V_{FB} and the Fermi potential ϕ_F can be written as:

$$V_{FB} = \phi_{\text{ms}} - \frac{Q_f}{C_{\text{ox}}} \tag{3.2}$$

$$\phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{3.3}$$

where ϕ_{ms} is the workfunction difference between the gate material and the semiconductor, Q_f is the fixed charge in the oxide, and n_i is the intrinsic carrier density.

With the continuous scaling down, the long-channel V_T in (3.1) is not accurate any more. Due to the SCE and DIBL, the V_T gradually decreases with shorter channel. The finally obtained V_T in short channel devices can be expressed as [102]:

$$V_T = V_{T,\text{long}} - 2.0 \cdot EI \cdot \phi_d - 2.5 \cdot EI \cdot V_{DS} \tag{3.4}$$

where ϕ_d is the built-in voltage at the source-channel junction, V_{DS} is the drain-to-source bias, and the *Electrostatic Integrity* (EI) is given by:

$$EI \equiv \left(1 + \frac{x_j^2}{L^2}\right) \frac{t_{\text{ox}}}{L} \frac{t_{\text{dep}}}{L} \tag{3.5}$$

with x_j the junction extension depth, t_{dep} the depletion depth in the channel, and L the channel length. In (3.4), the second and the third terms at the right-hand side stand for the V_T reduction due to SCE and DIBL, respectively.

3.1.2 Process Engineering

It is observed from (3.1) that devices with different threshold voltages can be obtained in different ways. A straightforward method is the use of different gate materials to tune the gate workfunction, thereby modifying the threshold voltage of the device [103, 104]. For example, Fig. 3.1(a) shows the dual metal gate CMOS with Ta/Mo diffusion technology for multi-V_T applications. Ta diffuses into the underlying Mo layer and piles up at the metal/dielectric interface. By annealing at proper condition, it reduces the gate workfunction [103]. Therefore, the Ta/Mo gate decreases the V_T of NMOS and oppositely increases the V_T of PMOS as shown in Fig. 3.1(b).

Another efficient way to tune V_T is provided by (3.4), which explains the "V_T roll-off" with shorter channel. For instance, Intel's 32 nm technology uses 4 nm longer gate length to obtain $\sim 0.1V$ higher V_T. Together with low-damage implants and junction grading, the subthreshold leakage of high-V_T devices is reduced by 2 orders of magnitude as compared to

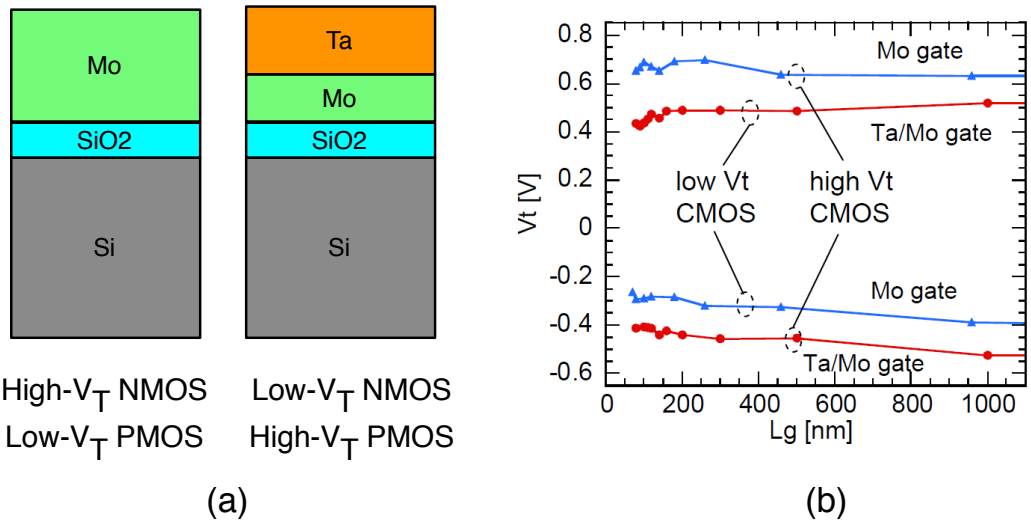


Figure 3.1: (a) Dual metal gate CMOS with Ta/Mo diffusion technology for multi-V_T applications, (b) V_T values in each type of devices [103].

low-V_T devices [101].

Similar as tuning the gate oxide thickness and channel doping concentration to modify V_T, these methods require extra process steps, which eventually lengthen the design time, increases fabrication complexity, and may reduce yield [60].

3.1.3 Body Biasing

Through the examination of (3.1), it is found that the threshold voltage of a device can also be modulated by separately biasing its source and body terminals, i.e., changing V_{BS}. A *Forward Body Bias* (FBB) reduces V_T, while a *Reverse Body Bias* (RBB) increases V_T. By utilizing this body effect of MOSFETs, *Adaptive Body Biasing* (ABB) is thereby proposed to achieve multi-V_T design [105, 106].

In bulk CMOS technology, the applicable maximum body bias limits the magnitude of V_T shift due to the isolation restriction. The maximum FBB is limited by current flows across the P-N junction formed between the *p*-well and *n*-well. A thyristor-like device is formed in the substrate by the two bipolar transistors as shown in Fig. 3.2 [107]. Thus, the FBB has to be limited to avoid the latch-up. On the other hand, the maximum RBB is limited by the leakage current and possible breakdown across the reverse biased drain-body junction.

Moreover, separately tuning threshold voltage of each transistor is hard to achieve with this approach due to the area overhead of additional circuits and routing resources. Therefore, the body bias is usually applied to an island to tune transistors in group [108]. In addition, the body bias may be distributed a significant distance as an analog signal. This becomes increasingly problematic with scaling because of the crosstalk between wires [107].

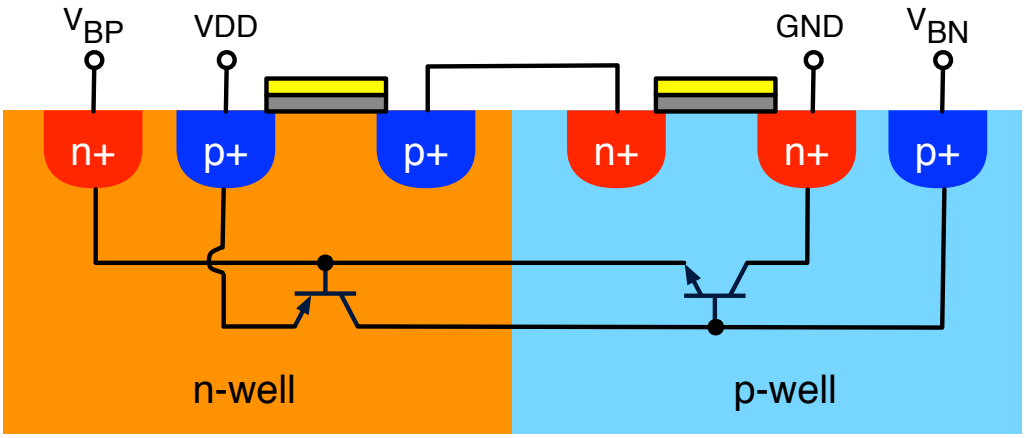
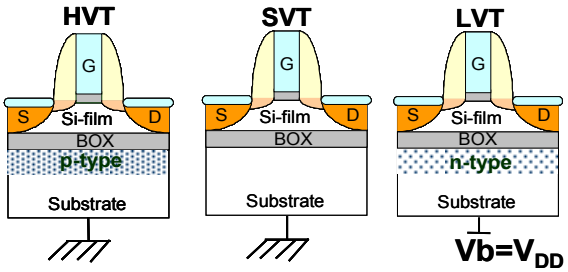


Figure 3.2: Leakage path in bulk CMOS with forward body biasing.

Compared to bulk MOSFETs, UTBB-FD SOI technology provides more flexibility to utilize the body effect [109]. Thanks to the isolation provided by thin buried oxide, a wide range of body bias can be applied to the substrate (Fig. 3.3). Thus, a large V_T range can be obtained by tuning the back bias. Nevertheless, it is still not convenient for routing.

In UTBB-FD SOI technology, with the trench isolation in the substrate, the threshold voltage of the device can be also tuned by properly doping a *Back Plane* (BP) layer below the buried oxide (Fig. 3.3) [27, 109]. The doped BP has the similar effect as applying a bias to the substrate. However, this method still requires extra process steps.

Table 3.1 summarizes the limitations of these conventional multi-V_T technologies. Extra process steps, group tuning or special substrate is required to implement the multi-V_T design. These technologies cannot perfectly avoid all the limitations.



(a)

	BP type	Vb
SVT family	No BP	from -Vdd to Vdd
HVT family	NMOS BP P/ PMOS BP N	from -Vdd to Vdd
LVT family	NMOS BP N/ PMOS BP P	from -Vdd to Vdd

(b)

Figure 3.3: (a) NMOS FD SOI multi-V_T devices obtained by applying doped BP and body bias. (b) the multi-V_T family with different BP doping and a wide range of body bias. [109]

To overcome these limitations, this chapter introduces the dual-V_T characteristics of multiple-independent-gate FETs, which are demonstrated with a three-independent-gate SiNWFET technology. It can realize dual-V_T circuits with a unified process for all the devices. The threshold voltage of pre-defined devices is tuned by applying different biases on extra gate terminals. This voltage biasing is decided individually by applying different connection schemes.

Table 3.1: Limitations of conventional multi-V_T technologies

Limitations	Process engineering	Adaptive body biasing	BP doping
Extra process	Yes	No	Yes
Group tuning	No	Yes	No
FDSOI only	No	No	Yes

3.2 Device Operation

This sections shows the operation states of a *Three-Independent-Gate* (TIG) SiNWFET and the configurations with a single input or two inputs.

3.2.1 Operation States

The structure of TIG SiNWFET has been introduced in Chapter 2. For convenience, the conceptual sketch of the device is reproduced in Fig. 3.4.

Figure 3.4: Schematic of three-independent-gate SiNWFET.

In this device, PG_S and PG_D independently modulate the thickness of the corresponding Schottky barrier. The desired type of carriers is selected to tunnel into the channel through the thin Schottky barrier, and the other type of carriers is blocked by the thick Schottky barriers. The device thereby achieves the electrostatically-controlled polarity. Located between PG_S and PG_D, CG induces a potential barrier in the inner region of the channel to control the selected carriers flow through the channel.

By independently biasing the three gates to either GND ('0') or V_{DD} ('1'), 8 operation modes of this device are divided into 4 groups. We can identify two ON states, two standard OFF states, two low-leakage OFF states, and two uncertain states which will not be used [90, 110]. Fig. 3.5 illustrates the six most important operation modes and their corresponding band diagrams when V_{DS}=V_{DD} (i.e., S='0' and D='1').

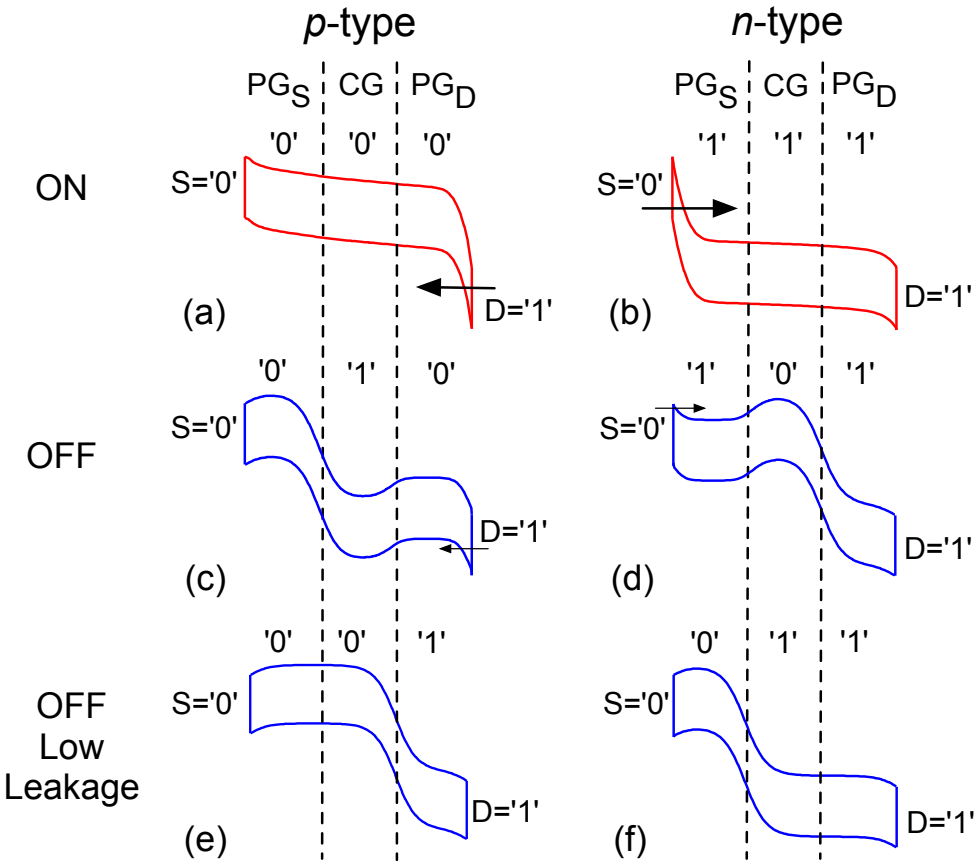


Figure 3.5: ON, OFF and low-leakage OFF states and their corresponding band diagrams.

1. ***ON states:*** As shown in Fig. 3.5(a)(b), when PG_S=PG_D=CG, one of the Schottky barriers is thin enough to allow hole tunneling from drain (*p*-type) or electron tunneling from source (*n*-type), and there is no barrier in the channel. Thus, majority carriers flow through the device easily.

2. ***OFF states:*** Current is shut off due to the barrier induced by opposite biasing of control gate and polarity gates as shown in Fig. 3.5(c)(d). Nevertheless, small number of carriers are still tunneling through the thin barrier into the channel. This mode is similar to the double-gate SiNWFET [72].

3. ***Low-leakage OFF states:*** When PG_S=S and PG_D=D in Fig. 3.5(e)(f), thick barriers prevent carriers from tunneling at both source and drain and ensure minimum leakage in the device. This mode corresponds to the two-gate SiNWFET [73].

4. ***Uncertain states:*** When PG_S='1' and PG_D='0', barriers are thin enough for tunneling. However, this condition may also create an unexpected barrier in the inner region that will block the current flow, and cause signal degradation. Hence, the uncertain states should be prohibited by always fixing PG_D='1' (PG_S='0') for *n*FET (*p*FET), or using PG_D=PG_S.

3.2.2 Single-Input Configuration

A symbol of TIG SiNWFET is shown in Fig. 3.6(a), with all five terminals. According to the transition between *on* and *off* states, four configurations of TIG SiNWFET are also depicted in Fig. 3.6, including *Low-*V_T (LVT) *n*FET/*p*FET and *High-*V_T (HVT) *n*FET/*p*FET. The uncertain states are naturally avoided in these configurations.

1. ***Low-*V_T *pFET*** (Fig. 3.6(b)): PG_S and PG_D are biased to GND. The voltage sweep on CG makes a transition between *p*-type ON (Fig. 3.5(a)) and standard OFF states (Fig. 3.5(c)).

2. ***Low-*V_T *nFET*** (Fig. 3.6(c)): PG_S and PG_D are biased to V_{DD}. The voltage sweep on CG makes a transition between *n*-type ON (Fig. 3.5(b)) and standard OFF states (Fig. 3.5(d)).

3. ***High-*V_T *pFET*** (Fig. 3.6(d)): GND is applied to CG and PG_S, and a voltage sweep is applied on PG_D. In this configuration, the device switches between *p*-type ON (Fig. 3.5(a)) and low-leakage OFF states (Fig. 3.5(e)).

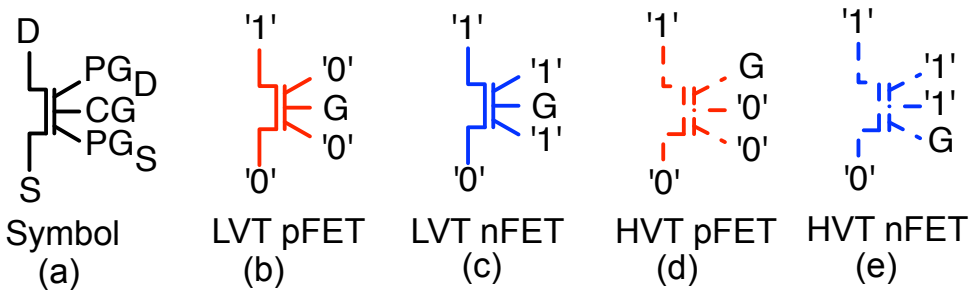


Figure 3.6: Bias configurations of TIG SiNWFET with a single input.

4. ***High-V_T nFET*** (Fig. 3.6(e)): V_{DD} is applied to CG and PG_D, and a voltage sweep is applied on PG_S. In this configuration, the device switches between *n*-type ON (Fig. 3.5(b)) and low-leakage OFF states (Fig. 3.5(f)).

3.2.3 Two-Inputs Configuration

The configuration of TIG SiNWFET can be further extended for two inputs by combining the bias configurations for a single input in Fig. 3.6.

1. ***2 series nFETs*** (Fig. 3.7(a)): By combining the LVT and HVT *n*FET configurations, two inputs on CG and PG_S implement the function of 2 series *n*FETs.
2. ***2 series pFETs*** (Fig. 3.7(b)): Similarly, the configuration of 2 series *p*FETs is obtained by combining the LVT and HVT *p*FET configurations.
3. ***DG configuration*** (Fig. 3.7(c)): The TIG SiNWFET can also work as a *Double-Gate* (DG) SiNWFET demonstrated in [72]. In this configuration, the device is *on* when G1=G2. Thus, this configuration is efficient for implementation of XOR-based functions [111].

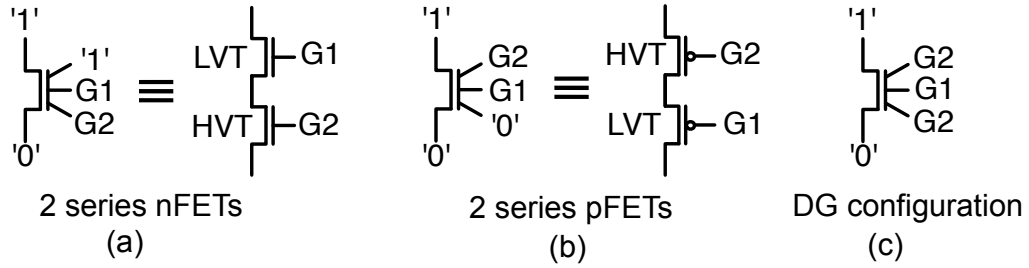


Figure 3.7: Bias configurations of TIG SiNWFET for two inputs.

Even though a specified gate is used for polarization in TIG SiNWFETs, these two-inputs configurations efficiently utilize the extra gates without source/drain region between two inputs, thereby mitigating the area overhead compared to conventional CMOS devices. In addition, the internal node capacitance between two inputs does not exist in TIG SiNWFETs. This helps to reduce the delay of circuits.

3.3 Device Characterization

To validate the working principle, we measure the transfer characteristics of the fabricated device in Chapter 2 as shown in Fig. 3.8. Both *n*-type and *p*-type behaviors with different threshold voltages (low-V_T and high-V_T) are observed in the same device.

In all demonstrated characteristics in Fig. 3.8, the applied voltages at source and drain are set to 0 V and 2 V, respectively.

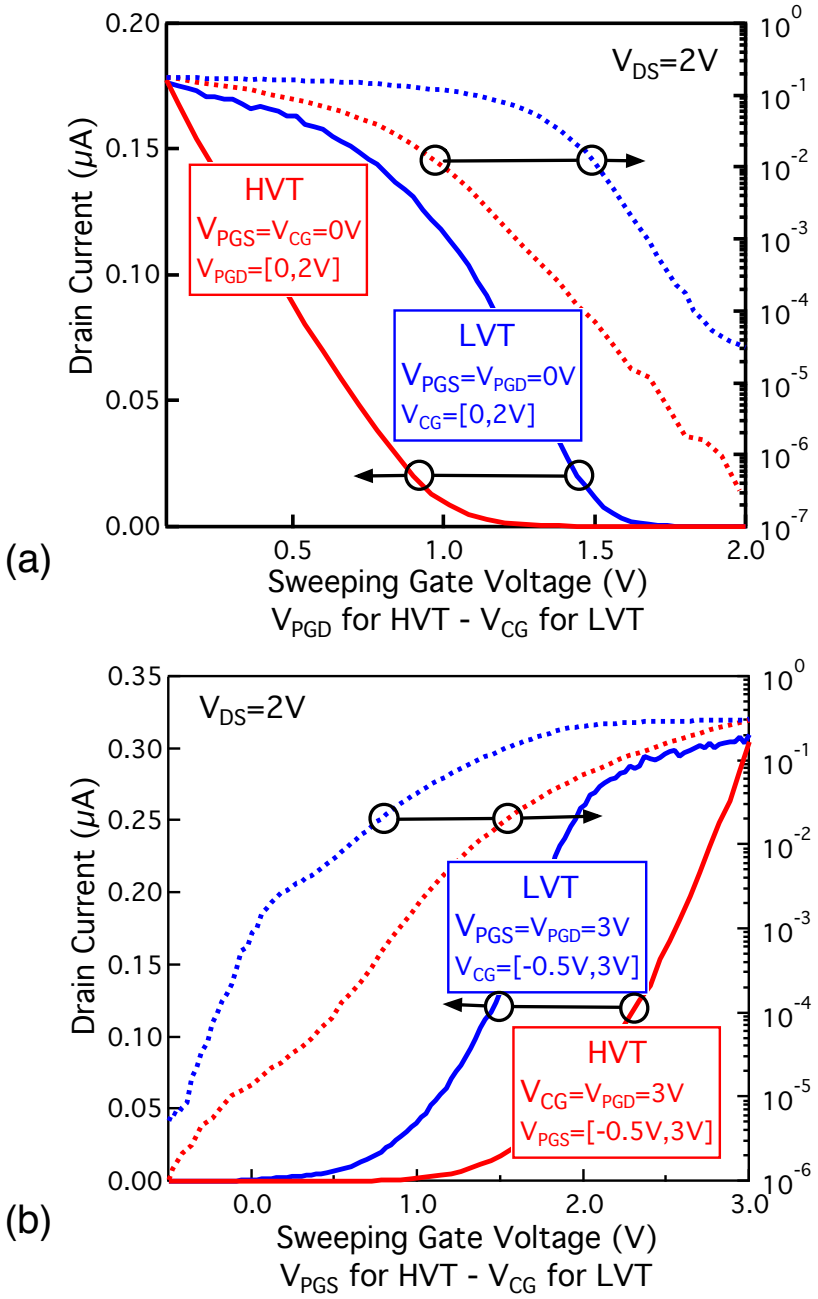


Figure 3.8: Measured characteristics of a three-independent-gate SiNWFET. (a) *p*-type transfer characteristic, (b) *n*-type transfer characteristic in the same device.

Low-V_T *p*FET configuration (LVT curves in Fig. 3.8(a)) is observed when V_{PGS} and V_{PGD} are set to 0 V. Thus, electrons are blocked at source, and band bending at drain leads to a reduction of the width of the Schottky barrier, i.e., thin Schottky barrier, which enables holes to tunnel from drain into the channel. The CG modulates the barrier in the channel, thereby turning the

device *on* or *off* as in conventional MOSFETs [112–114]. While in the *on*-state, the Schottky barrier is thin enough and has a limited impact on the device operation. When V_{CG} is set to 0 V, the barrier for holes along the CG is suppressed. Holes flow through the device easily. While setting V_{CG} to 2 V, the potential barrier induced by the CG cuts the current flow and turns the device *off*.

In contrast, high-V_T *p*FET configuration (HVT curves in Fig. 3.8(a)) is obtained when V_{PGS} and V_{CG} are set to 0 V to block the electrons tunneling from source. PG_D modulates the Schottky junction at drain and thereby controls the hole tunneling. By setting V_{PGD} to 0 V, holes can tunnel through the thin barrier and flow through the channel. Because this condition is exactly the same as in low-V_T *p*FET configuration (Fig. 3.5(a)), the *on*-state currents of both high-V_T and low-V_T modes are exactly the same value, regardless of the supply voltage. Although a lower V_T, i.e., earlier turn-*on*, is helpful for improving the circuit speed, the high-V_T mode with the same *on*-state current will not significantly degrade the circuit performance. This property of the proposed SiNWFET is not achievable in conventional multi-V_T techniques, and represents one of the key advantages of our approach. For the *off* state, V_{PGD} is set to 2 V. The opposite band bending at the Schottky contacts prevents both electron and hole injection into the channel, and also ensures the whole channel to be unpopulated [73]. This *off*-state current suppression is thereby more effective than in the low-V_T configuration, where holes are induced in the PG_D-controlled region. Therefore, the *off*-state current is reduced by two orders of magnitude as compared to low-V_T configuration, and reaches a leakage floor of 10.5 pA/μm (315 fA) normalized to the nanowire diameter.

Similarly, low-V_T *n*FET configuration (LVT curves in Fig. 3.8(b)) is reached when V_{PGS} and V_{PGD} are set to 3 V. The Schottky barrier at drain blocks holes. At the same time, the Schottky barrier at source is thin enough for electrons tunneling due to a band bending induced by PG_S. CG controls the current flow as in the low-V_T *p*FET configuration. High-V_T *n*FET configuration (HVT curves in Fig. 3.8(b)) is reached for V_{PGD} and V_{CG} fixed to 3 V, that blocks holes tunneling from drain. PG_S controls the Schottky junction at source and consequently turns the device *on* or *off*. With the same principle as *p*FET configurations, the *on*-state currents of low-V_T and high-V_T *n*FET configurations are the same since they share the same *on* state (Fig. 3.5(b)), and the leakage current is also suppressed in high-V_T configurations.

To summarize the performance of the fabricated device, the *on*-state currents of *p*FET and *n*FET configurations are 177 nA (5.9 μA/μm) and 310 nA (10.3 μA/μm), respectively, which are comparable to recent works on polarity-controllable devices [72, 115]. Extracted at 1 nA drain current [116], the threshold difference in *p*FET configurations and in *n*FET configurations are 0.48 V and 0.86 V respectively. The *off*-state currents of high-V_T *p*FET and *n*FET configurations reach 315 fA (10.5 pA/μm) and 1 pA (33.3 pA/μm) compared to 30 pA (1 nA/μm) and 4.6 pA (153.3 pA/μm) in low-V_T configurations. Thus, the total $I_{\text{on}}/I_{\text{off}}$ ratio for the high-V_T *p*FET and *n*FET configurations are 6×10^5 and 3×10^5, respectively. Currently limited by the thick oxide used in fabrication process, low-V_T configurations demonstrate subthreshold slopes of 155 mV/dec (*p*FET) and 217 mV/dec (*n*FET). However, the performance of the device can

be further improved by optimizing the fabrication steps to enhance the electrostatic control, such as reducing the gate oxide thickness.

Regarding scaling issues, high-κ gate dielectric materials and metal gates, together with channel strain techniques can be directly applied to the presented structure. We do not foresee fundamental limitations to size downscaling in terms of DIBL effect and power consumption compared to conventional MOSFET. Moreover, the proposed device concept may be applied to other materials (e.g., carbon nanotube, graphene, and MoS_2 [74, 78, 79]), giving the opportunities for continuous scaling down.

3.4 Discussion on Dual-V_T characteristics

After showing *n*-type and *p*-type operations in both high-V_T and low-V_T configurations, this section discusses the reason of the dual-V_T characteristics, and the effects of structural and physical parameters.

3.4.1 Origin of Dual Threshold Voltages

Let us take the *n*FET configurations for example. Band bending induced by a positive voltage on PG_S reduces the thickness of the source Schottky barrier and enhances the tunneling of electrons through the source barrier. This leads to a reduction of the effective barrier height [112]. In low-V_T configuration, sufficiently positive voltage configured on PG_S can help to suppress the effective Schottky barriers at the source. V_{CG} is swept to tune the conduction of the device. Therefore, the current transport is dominated by thermionic emission of electrons over a potential barrier induced by CG [117], i.e.,

$$I_D = AA^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \tag{3.6}$$

where A is the junction area, A^* is the effective Richardson constant, T is the temperature, q is the elementary charge, k is the Boltzmann constant, and ϕ_B is the effective barrier height. This barrier height is determined by the electrostatic potential in the CG-controlled region. If we assume that there is no induced charge in the channel under subthreshold operation, the applied voltage on CG directly translates into a reduction of ϕ_B. Therefore,

$$\Delta\phi_B = -\Delta V_{CG} \tag{3.7}$$

In contrast, in high-V_T configuration, a sufficiently positive voltage is applied to CG and PG_D to make sure there is no barrier inside the silicon channel. The current is therefore determined by an effective Schottky barrier height at source. A positive voltage on PG_S reduces the thickness of the Schottky barrier at source, and the consequent enhancement of tunneling by V_{PGS} leads

to a reduction of ϕ_B. Thus,

$$\Delta\phi_B = -\eta \cdot \Delta V_{PGS} \tag{3.8}$$

where the coefficient η represents the dependence of the effective barrier height on V_{PGS}. Since the tunneling probability is smaller than 1, η is also smaller than 1 [112–114].

Due to the lower efficiency of tuning the effective barrier height by PG_S than CG, a higher V_{PGS} than V_{CG} is needed to turn on the device. That results in a higher threshold voltage in this configuration.

Through the above analysis, we can also explain the saturation trend of the drain current with a large positive V_{CG} in low-V_T *n*FET configuration [V_{CG} from 2.0 V to 3.0 V in Fig. 3.8(b)]. First, when the applied voltage on CG goes above the threshold voltage, electrons are induced in the channel, and the electrostatic potential in the channel gradually saturates [118, 119]. More importantly, when the bent conduction band edge is lower than the Fermi level in the source, the current starts to be dominated by the source injection, and cannot be further modulated by CG. Therefore, the current saturates at a large positive V_{CG}.

The above analysis is also applicable for *p*FET configurations. Tuning the effective barrier height for holes by PG_D is less efficient than tuning it by CG. Thus, higher voltage on PG_D is required to turn on the device in high-V_T *p*FET configuration. Similar to the *n*FET configuration, the current also saturates in low-V_T *p*FET configuration [V_{CG} from 0 V to 0.7 V in Fig. 3.8(a)].

3.4.2 Effects of Structural and Physical Parameters

According to the previous analysis, the V_T difference is determined by the efficiency of tuning effective barrier height, i.e., η in Eq. 3.8. Devices with different parameters related to this efficiency are studied to show the effects of the parameters on the dual-V_T characteristics.

TCAD simulation provides a efficient method to perform this kind of study. By solving physics equations with finite element method, TCAD simulation can predict device performance with self-defined structural and physical parameters. In this thesis, all the TCAD simulation are performed with *Sentaurus Device*, a commercial tool developed by Synopsys [120].

First, a single TIG SiNWFET is simulated. The simulation employs drift-diffusion transport in the silicon channel, while thermionic emission and quantum mechanical tunneling with *Wentzel-Kramers-Brillouin* (WKB) approximation are used at the Schottky junctions [121]. The simulated SiNWFET has the same structure than the fabricated one except that an optimized 2 nm gate oxide and a finely-adjusted Schottky barrier height (0.35 eV for electrons and 0.75 eV for holes) are used. Fig. 3.9 shows the structure of the device and simulation results. By optimizing the gate oxide, the performance of the device reaches levels of regular advanced MOSFETs. Finely-adjusted Schottky barrier height also gives symmetric *n*-type and *p*-type characteristics, which is important to achieve energy-efficient circuits with balanced

delay [115]. The simulated device reproduces all the key properties demonstrated in the measured characteristics, including the shared *on*-state current but different threshold voltages in dual-V_T configurations, as well as the saturation trend of the *on*-state current in low-V_T configurations.

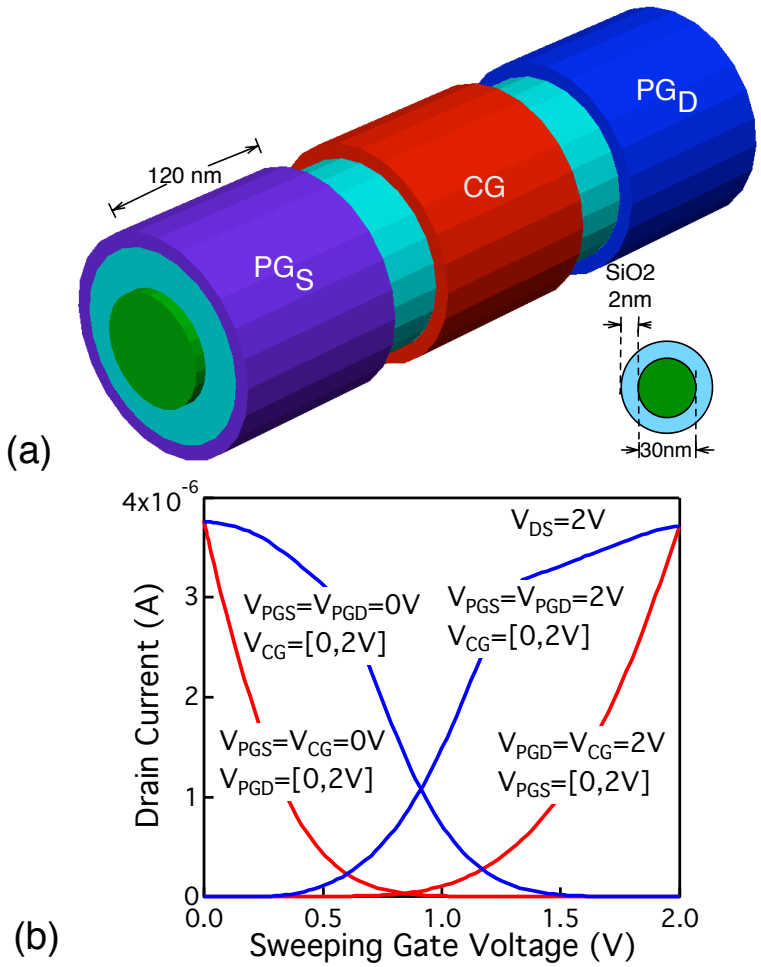


Figure 3.9: (a) Structure of the simulated TIG SiNWFET, (b) Simulation results of the device, showing the dual-V_T characteristic and polarity control.

Then, we simulated a series of devices with different parameters related to the efficiency of tuning effective barrier height, including the oxide thickness (Tox), the radius of nanowire (Rnw), the tunneling effective mass (m_h*) and the Schottky barrier height (SBH_h). The V_T difference of *p*FET configurations of different devices is plotted in Fig. 3.10. The reduction of Tox and Rnw enhances the electrostatic control of the gate, thus resulting in a thinner Schottky barrier at a given gate voltage in high-V_T configurations. Tunneling current is thereby improved and reduces the effective barrier height further [112], implying a larger η and a decreased V_T difference. A smaller effective mass also results in a larger tunneling probability and the V_T difference is consequently reduced. The V_T difference is also proportional to the

Schottky barrier height. Other than the previous three parameters, a reduction of Schottky barrier height for holes leads to an increase of Schottky barrier height for electrons. Thus, tuning of Schottky barrier height can achieve a trade-off between V_T differences in *n*-type configurations and in *p*-type configurations.

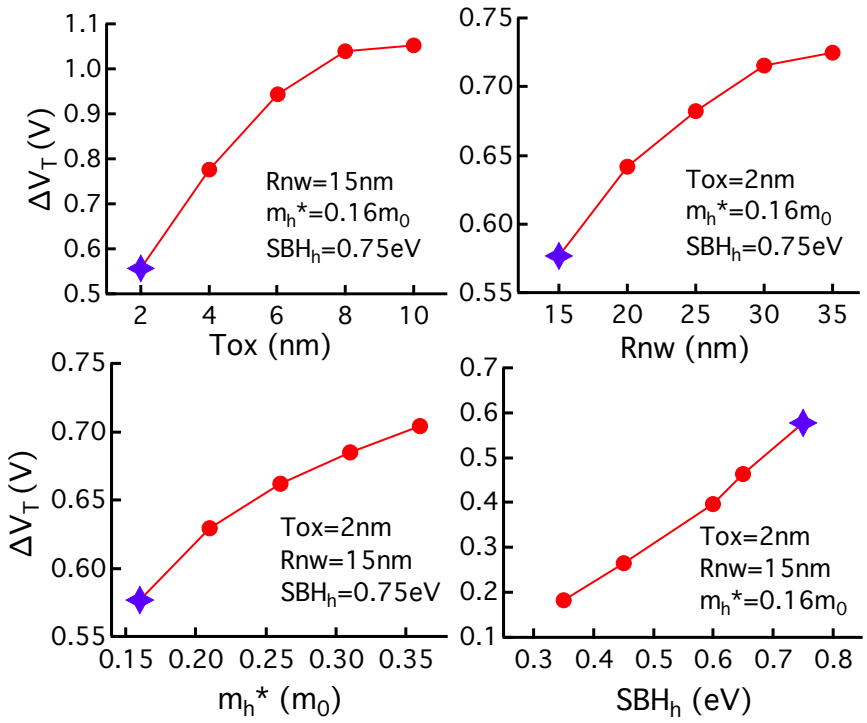


Figure 3.10: The V_T difference of *p*FET configurations in simulated devices. m_0 is the free electron mass. Stars represent the simulated device in Fig. 3.9.

3.5 Circuit and Physical Design

Recently, design with functionality-enhanced devices has been widely investigated, showing design opportunities compared to CMOS technology [89,111,122–131]. Zukoski *et al.* proposed universal logic modules to exploit the full potential of the embedded XOR function in the devices [127]. De Marchi *et al.* studied the regular fabric design for *Field-Programmable Gate Array* (FPGA) and structured *Application-Specific Integrated Circuit* (ASIC) applications [131]. O'Connor *et al.* introduced the fine-grain reconfigurable circuit design with the devices [124]. Trommer *et al.* showed the efficient logic gate design enabled by the full symmetry between *p*-type and *n*-type functionality in the devices [89], and Gaillardon *et al.* performed a comprehensive study on logic and memory design as well as system-level impact [123].

Moreover, the dual-V_T characteristics of TIG SiNWFETs bring additional interest as circuits can achieve either *High Performance* (HP) or *Low Leakage* (LL) by changing the connection scheme on the devices.

In this section, a circuit and physical design approach for dual-V_T circuits is proposed in order to fully exploit the flexibility of TIG SiNWFETs. By using both low-V_T and high-V_T configurations, logic gates towards either high performance or low leakage applications are efficiently implemented. An uncommitted logic gate pattern is introduced and basic logic functions are mapped onto it using different connection schemes.

3.5.1 Dual-Threshold-Voltage Design

Delay and leakage of logic gates can be tuned by applying LVT and HVT configurations of TIG SiNWFET. For example, Fig. 3.11(a) illustrates two inverters for HP and LL applications. According to the device operation, the HP inverter is obtained by assigning the input signal to the control gates of the two devices, while LL inverter is obtained by connecting the input to corresponding polarity gates. Fig. 3.11(b) gives the transient results of the two inverters using mixed-mode TCAD simulation. This evaluation takes into account the parasitics, such as the impact of gate capacitances. Thanks to a low-V_T, the HP inverter demonstrates a 0.8 ns propagation delay as compared to 1.4 ns of LL inverter. In contrast, the LL inverter consumes a leakage power of 8.5×10^{-14} W as compared to 2.8×10^{-13} W of HP inverter.

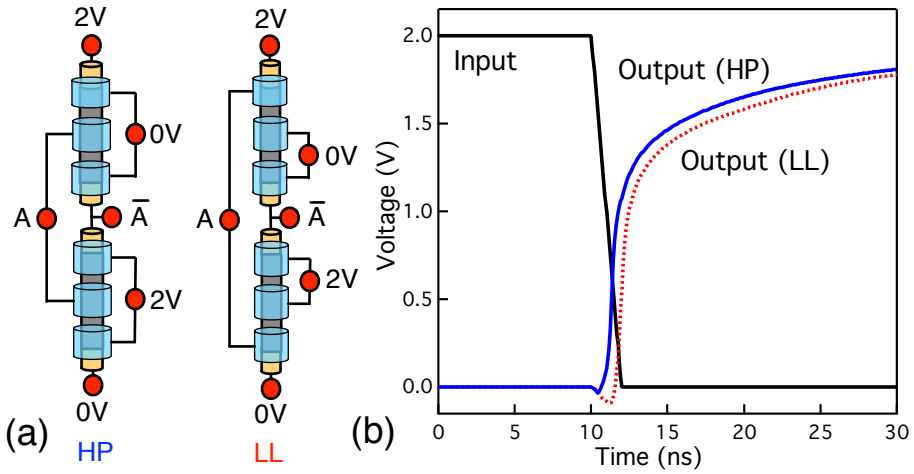


Figure 3.11: (a) The different wiring schemes of the inverters with two identical devices presented in Fig. 3.9. (b) Transient simulation of two inverters for HP and LL applications. The load capacitance is assumed to be the same as input gate capacitance.

Fig. 3.12 further illustrates two different mapping schemes of NAND gate for HP and LL applications. In Fig. 3.12(a), the HP gate is obtained by connecting inputs to the CG of *p*FETs. Thus, the performance for pulling the logic gate up is improved by applying the LVT configuration of the devices. In contrast, the LL gate (Fig. 3.12(b)) is obtained by controlling the *p*FETs from the PG_D. Leakage power is thereby reduced by forcing the devices into HVT operation. In both HP and LL gates, PG_S and CG of *n*FETs are connected to input signals to realize the logic function.

In a circuit, the signals A and B usually have different constraints. Since the CG of *n*FET shows low-V_T capability, while the PG_S of *n*FET shows high-V_T capability (as shown in Fig. 3.7(a)), we can map the signals in critical paths onto the CG and the signals belonging to non-critical paths onto PG_S. This method is also applicable for the pull-up path. Thus, the delay and leakage of the NAND gates can be even better tuned with more mapping schemes. Fine-grained dual-V_T design is thereby achievable with TIG SiNWFETs.

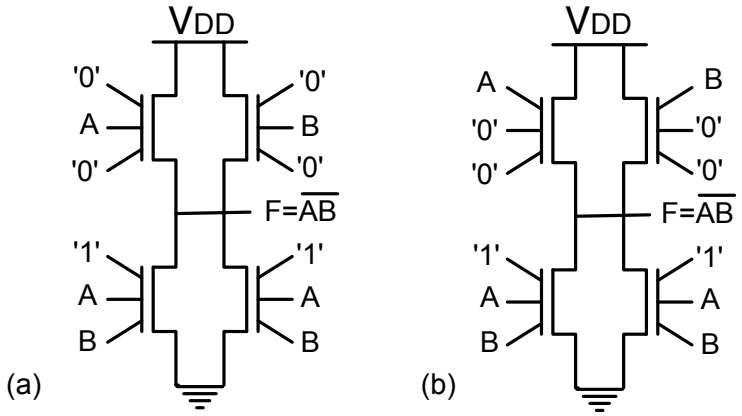


Figure 3.12: Mapping of NAND gate towards (a) HP and (b) LL application.

3.5.2 Additional Logic Implementation

By applying the single-input and two-inputs configurations in a single device, we can efficiently implement both combinational and sequential functions in logic circuits with TIG SiNWFETs.

1. **Combinational Elements:**

   Fig. 3.13(a) presents an example of an AOI gate. Its functionality is obtained by applying

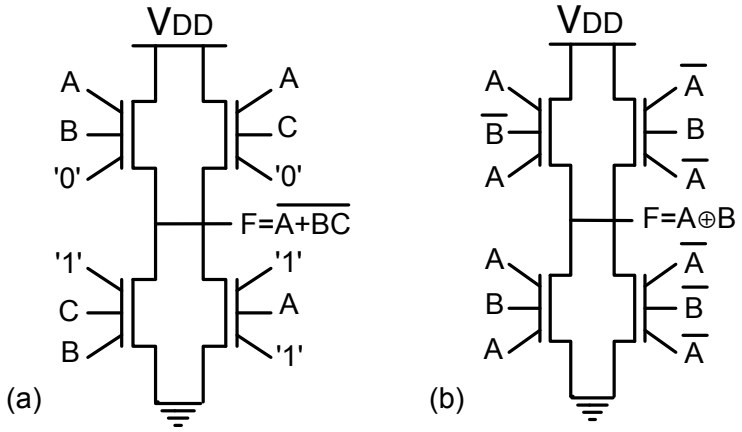


Figure 3.13: (a) AOI and (b) XOR gates implemented with TIG SiNWFETs in a compact form.

the configurations of 2 series *p*FETs/*n*FETs and LVT *n*FET. Thus, only 4 transistors are needed for this AOI gate, instead of 6 conventional MOSFETs. In Fig. 3.13(b), an XOR gate is mapped onto the same pattern as the AOI gate. In this XOR circuit, the DG configuration of TIG SiNWFET is applied, which is efficient to implement binate logic functions. The transistor count is significantly reduced as compared to 8 transistors in conventional static CMOS technology.

Moreover, along with the characteristic of electrostatic polarization, more logic functions can be implemented in a compact form [89, 126], showing the potential applications of TIG SiNWFET.

In conventional CMOS circuits, PMOS can only efficiently transmit '1' and NMOS can only efficiently transmit '0'. Due to the restriction of the full swing of output signal, the *Pull-Up Network* (PUN) with PMOS can only be connected to V_{DD} and *Pull-Down Network* (PDN) with NMOS can only be connected to GND. This is the conventional implementation of the static CMOS circuits (Fig. 3.14(a)). When transmitting a variable, CMOS transmission gate is necessary, which consists of complementary transistors. With transmission gates, PMOS and NMOS are both *on* to avoid output signal degradation (Fig. 3.14(b)).

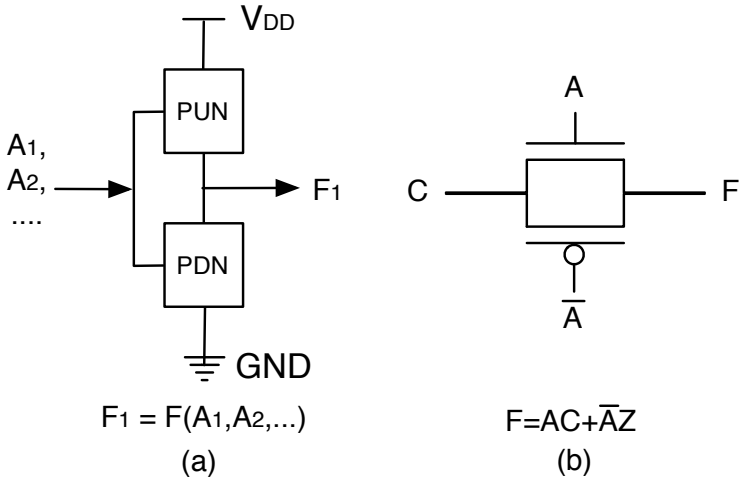


Figure 3.14: (a) Static CMOS logic function, (b) Conventional CMOS transmission gate. Z is the high-resistivity state.

In contrast, a polarity-controllable device is able to switch its polarity. This property enables the design of other transmission gates corresponding to different logic functions. Fig. 3.15(a) shows an XOR-based transmission gate, which is very efficient for binate logic function implementations [111]. This property can be extended to the transmission of variables using a single device. Indeed, by selecting the device polarity according to the transmitted variable, it is possible to use a unique device. Since *C* determines the device polarity in Fig. 3.15(b), single-input and two-input configurations of TIG SiNWFET (see Fig. 3.6 and Fig. 3.7) can be applied to obtain two novel transmission

gates, respectively. By using this property, we can then extend the standard PUN/PDN to transmit a variable. Therefore, the fixed V_{DD} and GND in original design are extended to any complementary signals (Fig. 3.15(c)). More complex functions are thereby derived from original functions without any additional transistors, with a compact form intrinsically not implementable with conventional static CMOS logic or CMOS transmission gates.

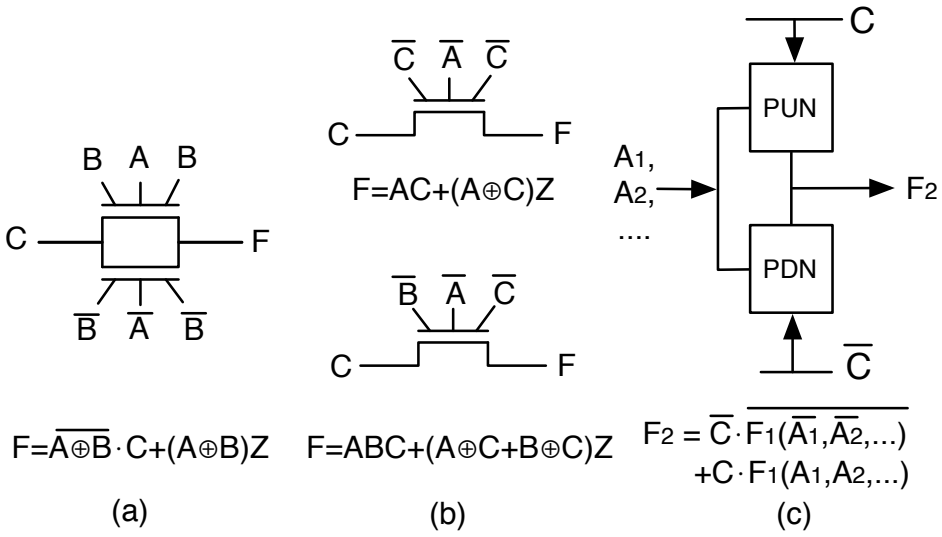


Figure 3.15: (a) XOR-based transmission gate, (b) Transmission gate with single polarity-controllable device. Z is the high-resistivity state. (c) Compact implementation of logic functions with polarity-controllable devices.

To illustrate this compact implementation in detail, an example of 1-bit full adder is illustrated in Fig. 3.16, which is realized in a very compact form.

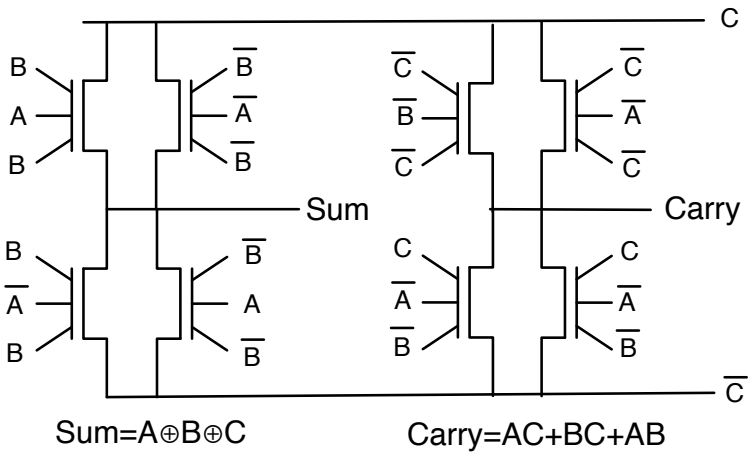


Figure 3.16: Compact implementation of 1-bit full adder with TIG SiNWFETs.

The relationship between the original function and derived new function is shown in Fig. 3.15(c). It is found that the sum and carry of 1-bit full adder can be directly derived from 2-input XNOR and NAND functions. In the sum function, the two devices in either PUN or PDN have complementary polarities, and hence transmit the third input C or $\overline{C}$ without signal degradation. This also refers to the XOR transmission gate (Fig. 3.15(a)). In the carry function, the polarities of all devices are determined by the complementary signals C and $\overline{C}$. Each device can be considered as a transmission gate shown in Fig. 3.15(b). When C='1', it is the NAND gate as shown in Fig. 3.12(a). When C='0', it becomes a NOR gate. This is exactly the expected carry function.

In order to verify the proposed implementation, the carry function is simulated with TCAD tool in mixed-mode [120]. Fig. 3.17 shows the transient simulation results, validating the functionality in different input conditions.

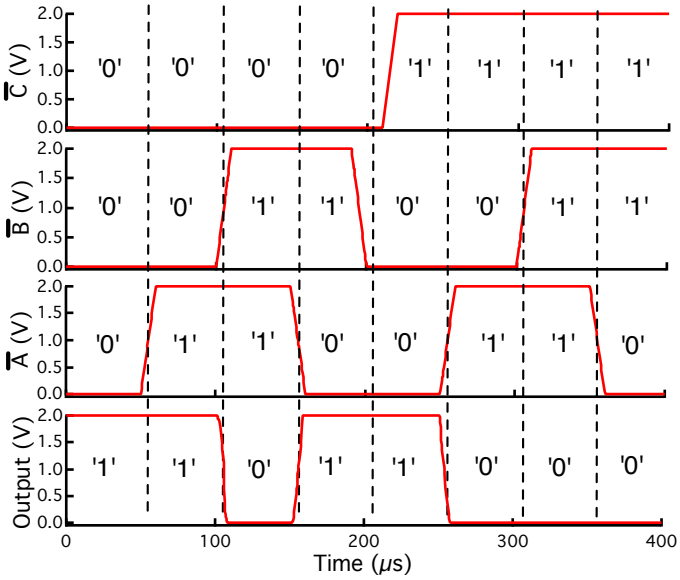


Figure 3.17: Mixed-mode TCAD simulation of the carry function with the device in Fig. 3.9.

2. **Sequential Elements:**

   True-Single-Phase-Clock D-Flip-Flop (TSPC DFF) is an efficient implementation of storage element in synchronous circuits [132, 133]. Based on the configurations of TIG SiNWFET for 1-input and 2-input conditions, a TSPC DFF is implemented with 8 transistors, as compared to 11 transistors in conventional CMOS circuit (Fig. 3.18(a)). The equivalent logic structure is given in Fig. 3.18(b). This rising-edge triggered DFF is composed of 4 stages: a CLK-low enabled inverter at the first stage, a dynamic inverter at the second stage, and a CLK-high enabled inverter at the third stage, followed by a static inverter.

   Fig. 3.19 shows another example, which demonstrates the application of the transmission gate built with TIG SiNWFET. The asynchronous set/reset functions is implemented

within the framework of TSPC DFF in Fig. 3.18 by adding only two transistors. In this design, the transistors N1, N2 and N3 utilize the transmission gate with a single TIG SiNWFET shown in Fig. 3.15(b). This design saves the area of 7 transistors as compared to the CMOS TSPC DFF counterpart, and also significantly improves the timing performance [134, 135].

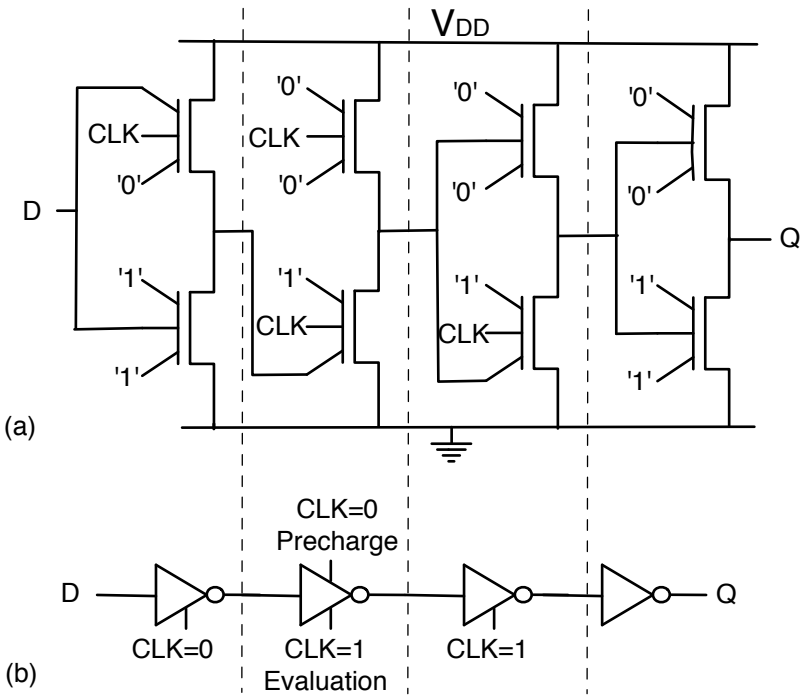


Figure 3.18: TSPC DFF (a) implemented with TIG SiNWFETs in a compact form, and (b) the equivalent gate-level circuit.

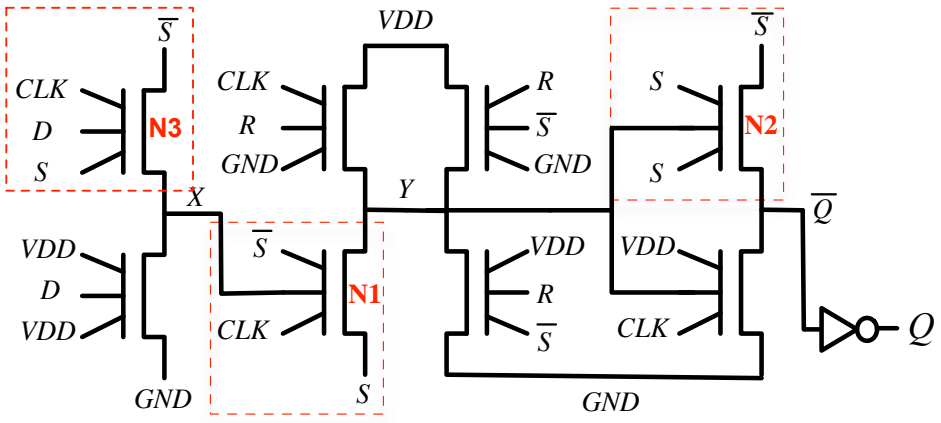


Figure 3.19: Implementation of TSPC DFF with asynchronous set/reset functions with TIG SiNWFETs. N1, N2 and N3 implement the transmission gate with a single TIG SiNWFET.

3.5.3 Uncommitted Logic Gate Pattern

Regularity is one of the key features to increase the yield of integrated circuits at advanced technology nodes [136]. If logic functions can be mapped onto an uncommitted pattern, the layout regularity will be consequently improved.

Therefore, an uncommitted logic gate pattern built with four TIG SiNWFETs is proposed in Fig. 3.20. There are two pull-up paths and two pull-down paths. Each path consists of only one transistor. Even though this pattern is very simple, a large range of functions can be mapped onto it with different configurations of TIG SiNWFETs. For example, the unate and binate logic functions and D-flip-flops presented in Sec. 3.5.1 and 3.5.2 can all be mapped onto this uncommitted gate pattern.

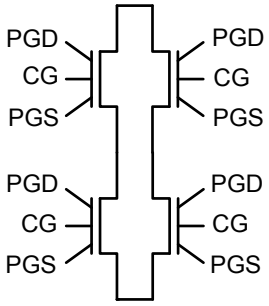


Figure 3.20: Uncommitted logic gate pattern.

Although a single TIG SiNWFET is larger than a conventional MOSFET, the area gap of circuits between the two technologies is reduced thanks to the lower transistor count and the lack of ion-implanted wells in the fabrication. Moreover, in the proposed gate pattern, each pull-up /pull-down path has only one series transistor. There is no internal node capacitance which needs to be charged or discharged. The speed of circuits is consequently improved.

3.5.4 Connection Schemes for Uncommitted Gate Pattern

According to the presented mapping schemes, wiring on the uncommitted gate pattern can implement different functions with fine-grained tuning of delay and leakage of circuits. In order to maintain the layout regularity, the TIG SiNWFETs and contacts are pre-fabricated according to the uncommitted pattern proposed previously. It is worth pointing out that all the devices are identical as their properties are tuned electrically, therefore uniformizing the technology.

As observed previously, most of the TIG SiNWFET access gates have a fixed polarity. Hence, power and ground signals are spread all over the proposed logic gate pattern. In order to minimize the routing effort for power lines, the power distribution network is consequently optimized. A grid network is built with a mesh of power and ground lines. Based on this novel power distribution grid, logic gates implementing different functions towards HP and LL

applications are obtained by wiring metal lines on the pre-fabricated gate pattern. For example, different connection schemes of NAND gate are demonstrated in Fig. 3.21, corresponding to the HP and the LL configurations shown in Fig. 3.12, respectively.

Because a single TIG SiNWFET has 5 terminals in a compact area, routing on these devices is challenging. An additional metal layer may be needed for a convenient routing as compared to CMOS technology. To mitigate routing efforts, a regular layout technique called sea-of-tiles could be applied, which has shown the potential on routing and area utilization with dual-independent-gate SiNWFETs [137].

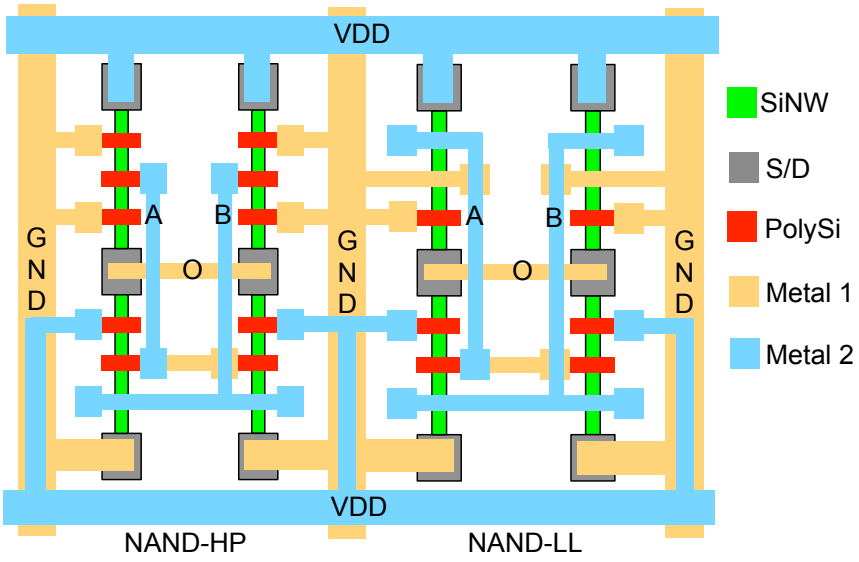


Figure 3.21: Connection schemes of NAND gate towards HP and LL applications.

3.6 Architectural Benchmarking

In this section, the effect of performance tuning and leakage power reduction by applying the physical design approach for dual-V_T configurable circuits is discussed for logic gates and benchmark circuits.

3.6.1 Methodology

To perform the benchmarking for large-scale circuits, a logic cell library is characterized using *Cadence Encounter Library Characterizer* (ELC) with a table-based device model extracted from TCAD simulation. The library consists of combinational logic cells INV, NAND, NOR, XOR, XNOR, AOI, OAI in both HP and LL configurations. More than these basic cells, the library also consists of the sum and carry functions implemented as in Fig. 3.16. To simulate sequential circuits, a TSPC DFF with asynchronous set/reset is also characterized. All the cells in the library are built from the uncommitted gate pattern described in Section IV. The

area estimation of these cells is done according to the 22-nm design rules [36]. The impact of proposed connection scheme is considered in cell area estimation. A wire-load model is applied to take into account the capacitance and resistance of the interconnections. The supply voltage of vertically-stacked TIG SiNWFET library is 1.2 V.

Since we are demonstrating a design approach to implement dual-V_T circuits for standby power reduction, a counterpart library with supply voltage of 0.9 V is built with *Predictive Technology Model* (PTM) 20-nm *Low-Standby-Power* (LSTP) FinFET model [58]. The LSTP FinFET library consists of all basic combinational cells and a TSPC DFF as in the TIG SiNWFET library [135]. Considering that the sum and carry functions cannot be implemented with FinFET in such a compact form as with TIG SiNWFET, these functions are not included in the FinFET library. The area of a FinFET is also estimated according to the 22-nm design rules.

With both TIG SiNWFET and LSTP FinFET libraries, combinational and sequential benchmark circuits are synthesized by *Synopsys Design Compiler*. Circuit-level performances results are extracted from the post-synthesis reports.

3.6.2 Table-Based Device Model

In order to estimate device performance at advanced technology node, a single TIG SiNWFET is simulated by using *Synopsys Sentaurus* [120]. Schematic of the device is shown in Fig. 3.22. Diameter of the lightly *p*-type doped silicon nanowire is 15 nm. Three 24-nm metal gates with mid-gap workfunction are placed on 5.1 nm HfO_2 high-κ dielectric layer (Equivalent Oxide Thickness=0.8 nm). Schottky barrier height for electrons is set to 0.35 eV in the simulation to get nearly symmetric *n*-type and *p*-type characteristics. This barrier height is achievable in actual process by using barrier height modulation technique [138, 139]. The symmetric *n*-type and *p*-type characteristics have also been observed in polarity-controllable SiNWFETs by applying radially compressive strain [115]. In the simulation, V_{DD}=1.2 V is applied. The requirement of larger V_{DD} than conventional MOSFETs is due to the presence of Schottky barriers and the longer channel length.

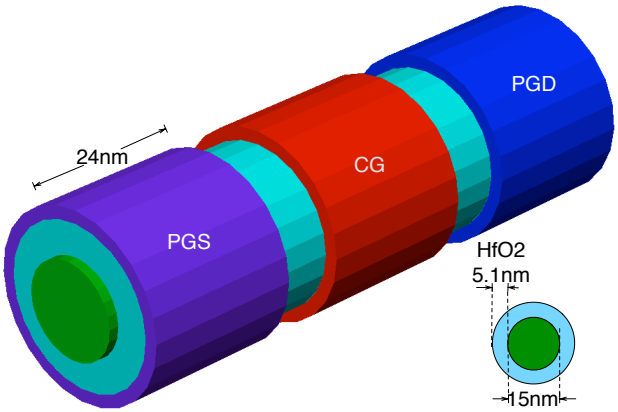


Figure 3.22: Schematic of simulated 22-nm TIG SiNWFET.

This TIG SiNWFET is simulated with the four configurations in Fig. 3.6. Dual-V_T characteristic of TIG SiNWFET is depicted in Fig. 3.23 in both linear and logarithmic scales. Solid lines indicate the low-V_T configurations, and dash lines indicate the high-V_T configurations. The threshold difference between the low-V_T and the high-V_T configurations is about 0.3 V.

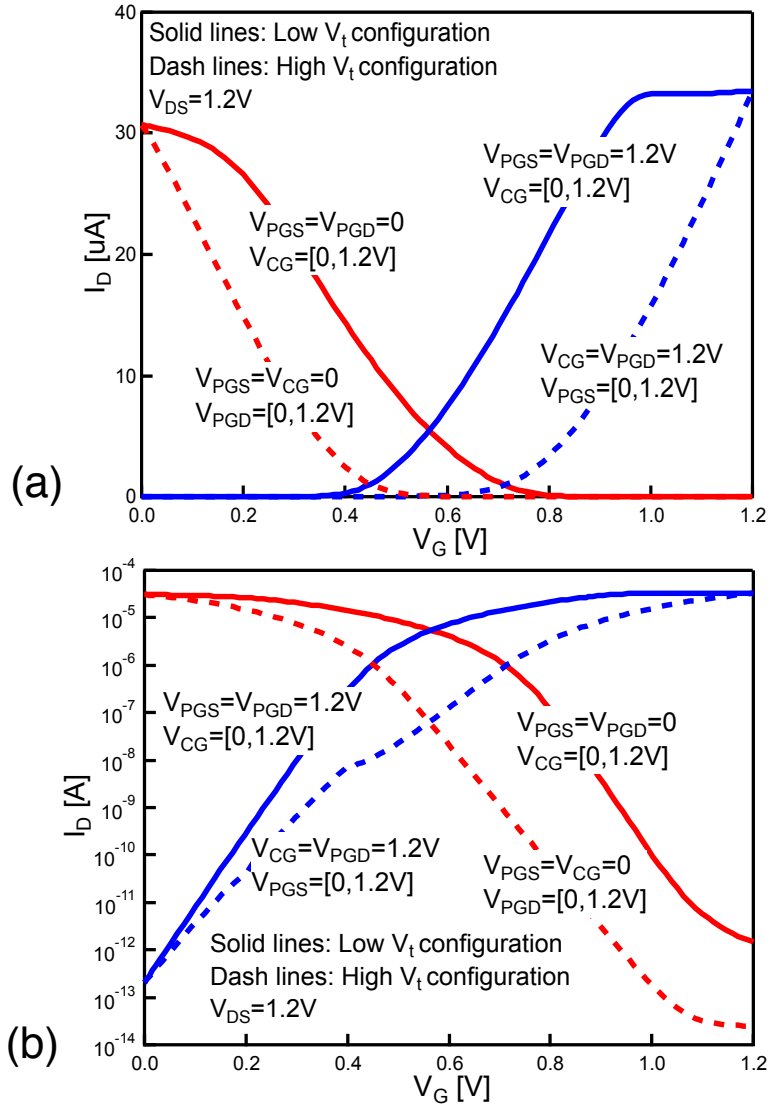


Figure 3.23: Transfer characteristic of simulated 22-nm TIG SiNWFET illustrating the dual-V_T property - (a) linear scale, (b) logarithmic scale.

In conventional dual-V_T technology, the high-V_T devices achieve lower leakage current but also reduce I_{on} compared to low-V_T devices. However, with TIG SiNWFET, I_{on} of both low-V_T and high-V_T configurations keep the same value since they share the same *on* states shown in Fig. 3.5(a)(b). Thus, despite the degraded subthreshold slope (29% increase in

simulation), the use of high-V_T devices reduces the leakage power consumption (by 86% in simulation) without significantly degrading the speed of circuits. This is a natural advantage of the dual-V_T technology based on TIG SiNWFETs. Since velocity saturation has been taken into account in the simulation, the characteristics above threshold voltage in LVT configurations are approximately linear in Fig. 3.23(a) [140]. With even higher/lower V_{CG} in LVT *n*FET/*p*FET configurations, the drain current saturates due to the limitation of source injection from the Schottky barrier.

The performance of simulated TIG SiNWFET with different configurations is listed in Table 3.2. The subthreshold slopes were extracted at the lowest point following the methodology in [10]. As discussed in Sec. 3.4, the control of the barrier height in the channel from CG is more efficient than the Schottky barrier thickness modulation from polarity gates. Therefore, LVT configurations demonstrate better subthreshold slope than HVT configurations. The simulation result also shows that the leakage current of *p*FET can be significantly reduced by effectively modulating the Schottky barrier thickness with HVT configuration. In contrast, HVT and LVT *n*FET configurations demonstrate the same leakage current. The reason for this is that, the leakage current is now dominated by thermionic emission over a potential barrier induced by CG (LVT) or PG_S (HVT). Differently from tunneling current, thermionic current mainly depends on the barrier height, not the barrier thickness.

Table 3.2: Performance of simulated 22-nm TIG SiNWFET

Configuration	I_{on}/I_{off}	I_{off} [pA]	SS [mV/dec]
LVT nFET	10^8	0.21	64
LVT pFET	10^7	1.5	64
HVT nFET	10^8	0.21	86
HVT pFET	10^9	0.025	79

With the help of TCAD simulation, a simple model for the proposed TIG SiNWFET is written in Verilog-A to enable circuit-level simulations. The equivalent circuit of a single TIG SiNWFET

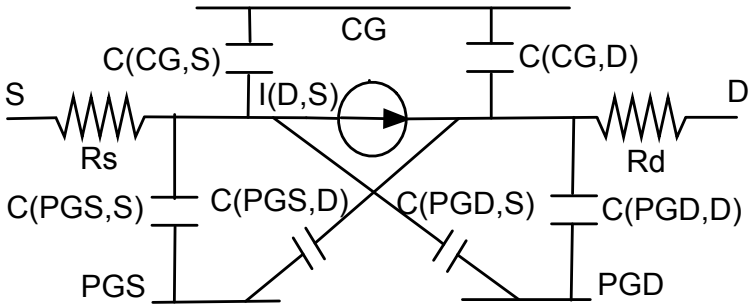


Figure 3.24: Equivalent circuit model of TIG SiNWFET.

is shown in Fig. 3.24. The current source is described by a table model extracted from TCAD simulation. Access resistances are estimated according to the device geometry. Each capacitance is extracted from TCAD simulation as an average value under all possible bias conditions. The coupling capacitances between the gates are much smaller than the total capacitance of the device, and therefore neglected in the model. According to the capability of vertically-stacked silicon nanowire technology, we assume that there are four nanowires per stack. The stack is modeled by parallel arrangement of single TIG SiNWFET model.

3.6.3 Gate-Level Characterization

Table 3.3 lists the maximum delay under a load of four INV×1 gates, leakage power and area of some logic gates. These gates are built with different configurations using the different V_T modes of TIG SiNWFETs. The traditional CMOS counterparts are realized with LSTP FinFETs. The average comparison results are depicted in Fig. 3.25.

The LL TIG SiNWFET gates demonstrate a leakage power reduction of 65% compared to LSTP FinFET gates, at a cost of a 4% increase in delay. The low-leakage property stems from the

Table 3.3: Performance of logic gates with TIG SiNWFET and LSTP FinFET

Logic Gates		HP TIGNW	LL TIGNW	LSTP FinFET
INV	Delay [ps]	22.2	25.3	20.5
	Leakage [pW]	4.02	0.56	6.43
	Area [μm^2]	0.166	0.166	0.109
NAND	Delay [ps]	25.7	29.3	25.5
	Leakage [pW]	7.17	1.11	6.88
	Area [μm^2]	0.332	0.332	0.218
XOR	Delay [ps]	33.5	36.7	40.0
	Leakage [pW]	15.23	6.15	41.36
	Area [μm^2]	0.664	0.664	0.654
AOI	Delay [ps]	26.4	28.8	30.4
	Leakage [pW]	7.19	4.60	7.06
	Area [μm^2]	0.332	0.332	0.327
DFF	Delay [ps]	41.5	43.5	47.4
	Leakage [pW]	239.7	176.7	257.4
	Area [μm^2]	0.996	0.996	1.036

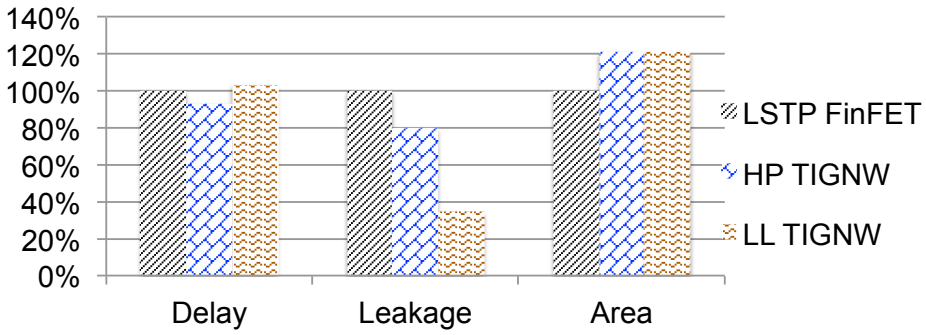


Figure 3.25: Comparison results of logic gates with TIG SiNWFET and LSTP FinFET.

good control of the thick Schottky barriers in the device that prevents carriers from tunneling into the channel during *off* state.

The HP TIG SiNWFET gates demonstrate a slight 6% reduction in delay as compared to LSTP FinFET gates. Among HP gates, AOI and XOR gates and DFF show 15% gain in performance and comparable area than FinFET, while INV and NAND gates show larger delay and area. While INV and NAND gates have the same implementation as in CMOS and suffer from the use of larger transistors, AOI and XOR gates and DFF are implemented on the proposed uncommitted logic gate pattern in a very different way. Indeed, the gates have only one transistor in each pull-up and pull-down path that is consequently of benefit to the different metrics.

Noise margins were also characterized for the inverters. The HP inverter demonstrates noise margins of 0.52 V for '1' and 0.35 V for '0'. In contrast, noise margins of LL inverter are 0.60 V for '1' and 0.51 V for '0'. These results show 13% improvement compared to FinFET (0.38 V for '1' and 0.36 V for '0') when normalized to the supply voltages.

3.6.4 Circuit-Level Results

The performance and leakage power consumption with TIG SiNWFETs and LSTP FinFETs are evaluated for both combinational and sequential circuits.

1. **Combinational Circuits Results:**

   Critical path delay, leakage power, and area of ISCAS'85 benchmark circuits are reported for HP, LL, dual-V_T TIG SiNWFET and LSTP FinFET libraries in Table 3.4 [141]. Fig. 3.26 shows the average comparison results.

   HP library demonstrates comparable performance with 32% leakage power reduction compared to FinFET library. While LL library shows a leakage power reduction of 78%, but with a 32% increase in delay. In contrast, by applying HP gates in critical path and LL gates in non-critical path, dual-V_T circuits with TIG SiNWFET keep comparable

performances but reduce the leakage power consumption by 53% compared to LSTP FinFET circuits. An additional area cost of 28% is due to the larger size of TIG devices.

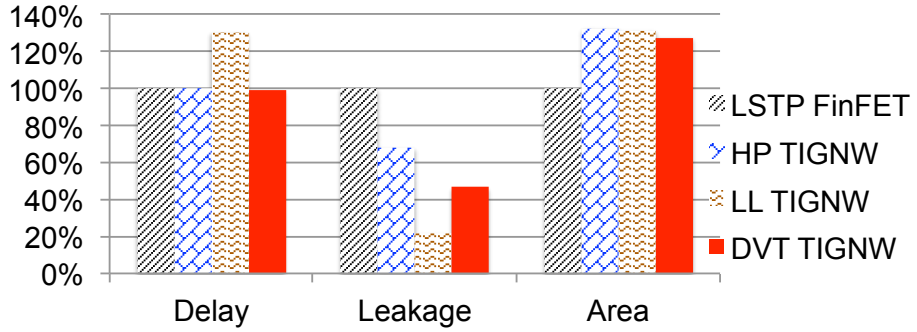


Figure 3.26: Average comparison results of ISCAS'85 benchmark circuits with Dual-V_T TIG SiNWFET and LSTP FinFET.

2. **Sequential Circuits Results:**

   To compare the performance of sequential circuits built with TIG SiNWFETs and LSTP FinFET, the *Verilog-To-Routing* (VTR) sequential benchmark circuits are synthesized [142]. Results are shown in Table 3.5 and Fig. 3.27.

   Benchmark circuits with dual-V_T TIG SiNWFET gates show the same performance as with HP TIG SiNWFET gates, and also the same leakage power consumption as with LL TIG SiNWFET gates. Thus, comparable performance with 51% leakage power reduction are achieved with dual-V_T TIG SiNWFET compared to LSTP FinFETs despite an additional area cost of 16%.

   Note that, the results are obtained with logic synthesis tool which is efficient for unate logic function. In contrast, TIG SiNWFET is efficient at implementing both unate and binate logic functions. Hence, it is expected to obtain even better performance of TIG SiNWFET based circuits thanks to novel logic synthesis tools exploiting a large class of functions [54, 143, 144].

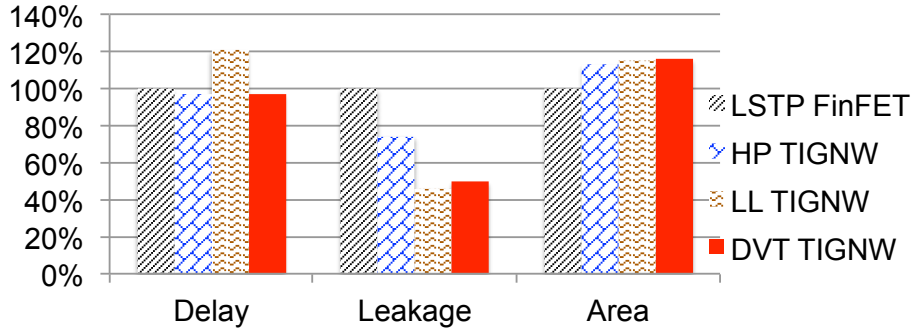


Figure 3.27: Average comparison results of VTR benchmark circuits with Dual-V_T TIG SiNWFET and LSTP FinFET.

3.7 Chapter Summary

This chapter demonstrates the dual-threshold-voltage characteristics of three-independent-gate silicon nanowire FET. The uniqueness of the proposed device lays in the high degree of configurability. By biasing separately the three independent gates, this device is configured as *n*-type or *p*-type transistor in either high-V_T or low-V_T mode. The threshold voltage tuning of this device is achieved by independently modulating the carrier transport at source/drain interface and in the channel. By enabling the tunneling at Schottky barriers and controlling the potential barrier in the channel, low-V_T configuration with earlier turn-*on*, is helpful for improving the circuit speed. In contrast, by efficiently controlling the Schottky barriers at both source and drain, high-V_T configuration achieves a suppression of leakage current without sacrificing the *on*-state current, showing advantages over the conventional multi-V_T techniques.

This chapter also presents an efficient approach to implement dual-threshold-voltage configurable circuits with TIG SiNWFETs. Logic gates using these devices can be realized to either fit high performance or low leakage applications, simply by wiring an uncommitted gate structure. Moreover, a range of logic functions are realized in a very compact form by utilizing the polarity and threshold controllability of TIG SiNWFETs. By applying this strategy, dual-V_T design is achievable without additional process steps for the SiNWFETs. This property increases the configurability of the circuits while reducing the process complexity compared to dual-V_T technologies for conventional CMOS. Benchmarking results show that, before place and route, comparable performance can be achieved with a 51% reduction of leakage power consumption for circuits based on TIG SiNWFET compared to low-standby-power FinFET technology, at a limited 16% increase in area. The results can be further improved by using novel logic synthesis tools targeting the intrinsic primitives supported by our devices.

Table 3.4: Delay, leakage, and area of ISCAS'85 benchmark circuits with dual-V_T TIG SiNWFET and LSTP FinFET

Circuits	HP TIG SiNWFET			LL TIG SiNWFET			Dual-V_T TIG SiNWFET			LSTP FinFET		
	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]
c432	0.30	1.87	100.89	0.38	0.60	102.55	0.31	1.28	95.75	0.31	2.54	81.89
c499	0.28	3.66	188.41	0.37	1.33	208.45	0.25	2.51	190.80	0.25	7.56	154.09
c880	0.24	4.04	219.42	0.29	1.19	202.67	0.24	2.34	192.76	0.24	5.36	166.63
c1355	0.29	3.34	166.87	0.38	1.12	190.53	0.26	2.47	184.02	0.25	7.29	148.40
c1908	0.33	3.75	207.20	0.45	1.11	182.49	0.36	2.67	187.13	0.36	6.36	153.14
c2670	0.22	4.94	269.68	0.29	1.68	264.43	0.22	3.48	289.45	0.23	8.05	221.74
c3540	0.42	9.32	515.74	0.55	3.25	519.76	0.43	6.65	502.85	0.45	10.95	354.35
c5315	0.31	12.02	662.60	0.41	4.49	703.15	0.30	8.57	668.80	0.31	17.07	490.89
c6288	1.08	32.92	1814.34	1.40	9.64	1672.77	1.10	22.55	1546.86	1.15	32.77	1070.82
c7552	0.27	15.94	852.10	0.37	4.60	783.79	0.28	11.04	790.70	0.27	25.56	647.23

Table 3.5: Delay, leakage, and area of VTR benchmark circuits with dual-V_T TIG SiNWFET and LSTP FinFET

Circuits	HP TIG SiNWFET			LL TIG SiNWFET			Dual-V_T TIG SiNWFET			LSTP FinFET		
	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]	Delay [ns]	Leakage [nW]	Area [μm^2]
diffeq1	1.90	145.77	5869.4	2.43	74.51	6011.9	1.90	107.03	6034.2	1.94	244.72	5228.6
diffeq2	2.30	113.59	5264.4	2.75	54.07	5349.8	2.30	70.77	5345.7	2.44	204.16	4654.3
or1200	2.25	315.36	8576.6	2.81	190.33	8786.1	2.25	208.78	9139.5	2.25	416.62	7343.0
bgm	1.62	2924.70	96260.5	2.06	1664.3	100521.8	1.63	1837.6	98219.7	1.63	3569.90	78945.1
blob_merge	1.37	346.35	12717.3	1.65	193.06	12667.4	1.38	195.64	13165.2	1.38	516.00	11179.0
sha	0.76	263.58	3801.2	0.98	180.99	3841.7	0.76	185.36	3807.0	0.88	301.95	3400.2
boundtop	0.49	530.80	6842.8	0.62	372.03	6721.8	0.50	379.93	6830.9	0.50	590.06	5824.8
raygentop	1.12	503.56	12118.1	1.36	320.07	12625.4	1.13	350.19	12561.1	1.13	723.81	11193.9
stereovision1	0.68	3793.20	56869.9	0.83	2544.1	58099.5	0.69	2621.3	57874.0	0.69	4796.80	54338.3
stereovision2	1.31	5666.80	98028.1	1.72	3713.5	97402.9	1.32	3793.9	100068.9	1.38	7177.90	87749.9

4 Steep-Subthreshold-Slope Operation

In this chapter, we explore the capability of multiple-independent-gate transistors to break the limit of the *Subthreshold Slope* (SS) in CMOS technology. Steep-SS operation is demonstrated in a *Dual-Independent-Gate* (DIG) FinFET. After reviewing different kinds of devices which achieve steep SS, the working principle of the steep-SS DIG FinFET is introduced. Then, the device is comprehensively characterized. The device shows an average SS of 6 mV/dec over 5 decades of current swing at room temperature. Ultra-low leakage floor is also achieved with high I_{on}/I_{off} ratio of 10^7. The steep-SS behavior is further discussed and feasible improvements to enhance the device performance are consequently suggested.

4.1 Steep-Subthreshold-Slope Devices

The limit of the SS in conventional CMOS technology (~60 mV/dec at room temperature) has been introduced in Chapter 1. This fundamental limitation becomes the bottleneck for continuously lowering the operation voltages. In order to break this limit, new device concepts employing different mechanisms other than conventional CMOS have been proposed and demonstrated. This section introduces several steep-SS devices, which have been extensively studied in literature.

1. ***Tunnel FET:***

   Tunnel FET (TFET) employs a n^+-i-p^+ structure as shown in Fig. 4.1(a) [49]. The steep SS in this device is achieved by injecting carriers into the channel by means of *Band-To-Band Tunneling* (BTBT). First identified by Zener in 1934, the BTBT mechanism describes that the carriers transfer from one energy band into another in heavily-doped p^+-n^+ junctions [145, 146].

   The operation of TFET is based on the control of the band bending in the channel by applying a gate bias. The band bending can switch the BTBT *on* or *off*, and therefore turn the device *on* or *off*. As shown in the band diagram in Fig. 4.1(a), at *off* state, the valence band edge of the channel is below the conduction band edge of the source. The

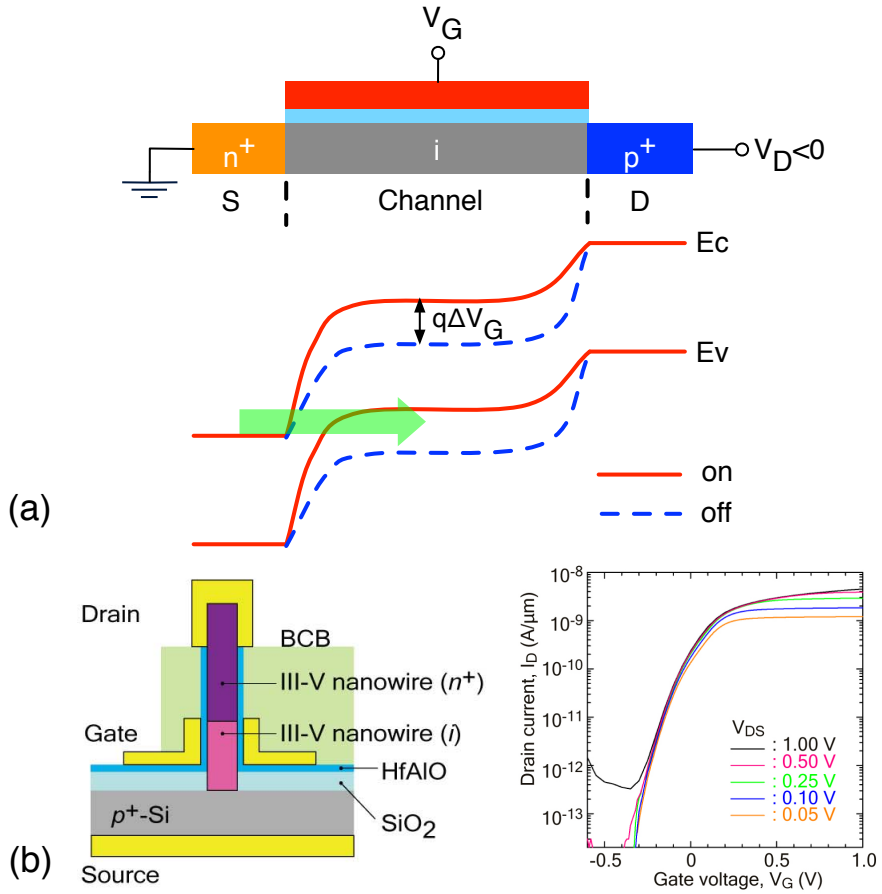


Figure 4.1: (a) Structure and band diagrams of a *p*-type TFET at *on* and *off* states, illustrating the working principle of the TFET. (b) *n*-type TFET based on vertical III-V nanowire/Si heterojunction and the characteristics with minimal SS below 30 mV/dec [147].

BTBT is thereby suppressed. In contrast, with a sufficiently large negative gate bias at *on* state, the valence band edge of the channel is lifted up above the conduction band edge of the source, thus enabling BTBT.

TFETs have been demonstrated in experiments and simulations using different materials, including silicon, III-V semiconductors, and carbon nanotube, etc. [49, 114, 147–150]. Tomiokal *et al.* shows a TFET based on vertical III-V nanowire/Si heterojunction, and minimal SS below 30 mV/dec is observed in fabricated devices (Fig. 4.1(b)) [147]. Nevertheless, in addition to the demand of an abrupt junction, the SS in TFET varies as a function of gate voltage as compared to a constant SS in the subthreshold region of MOSFETs [49]. This sensitivity of SS to gate voltage leads to a worse average SS over the entire subthreshold region of TFET. As demonstrated in Fig. 4.1(b), the average SS is only 80 mV/dec over 4 decades of current. Regarding the reliability, the quality of the semiconductor/insulator interface in TFETs is also more critical than in MOSFETs, which is mainly due to the change in tunneling field induced by interface traps [151, 152].

2. ***Impact-Ionization MOS:***

   With an electric field larger than a certain value, carriers in semiconductor can gain enough energy to excite electron-hole pairs by a mechanism called impact ionization [10]. By utilizing the carrier multiplication effect during impact ionization, *Impact-Ionization MOS* (IMOS) achieves sub-5 mV/dec SS [52, 153–155].

   Fig. 4.2(a) illustrates the structure and the operation principle of IMOS. It features a n^+-i-p^+ structure with a gate partly covering the intrinsic region. When increasing the gate voltage, the electric field above the threshold is obtained in the uncovered intrinsic region. Therefore, impact ionization is triggered and finally avalanche multiplication occurs. This multiplication leads to an abrupt increase of drain current. A steep SS is consequently observed in IMOS.

   Toh *et al.* demonstrate a IMOS with SiGe impact-ionization region (Fig. 4.2(b)) [155]. Despite of the steep SS, IMOS requires high V_{DS} (>5 V with SiGe channel in Fig. 4.2(b))

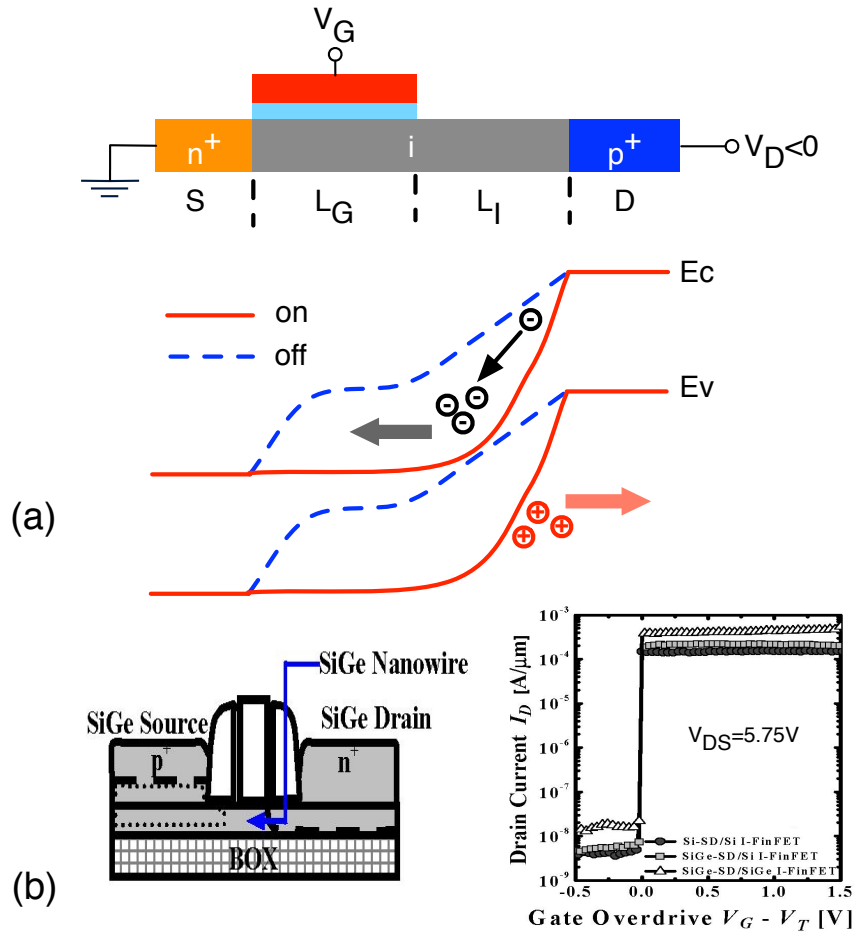


Figure 4.2: (a) Structure and band diagrams of a *n*-type IMOS at *on* and *off* states, illustrating the working principle of IMOS. (b) An IMOS with SiGe impact-ionization region, and the steep-SS characteristics obtained with $V_{DS} = 5.75V$ [155].

to trigger the avalanche multiplication, which limits its application in low-power circuits. In addition, the generated high-energy hot carriers in IMOS also cause important reliability issues, such as large threshold voltage shifts and SS degradation [154, 156].

3. ***Feedback FET:***

The feedback FET is also based on an asymmetric structure similar to TFET and IMOS as shown in Fig. 4.3(a) [157]. It achieves a steep SS based on a positive feedback between the flow of carriers and their injection barriers. As illustrated in the band diagram in Fig. 4.3(a), the barriers for carrier injection are formed by the trapped charges in sidewall spacers. When turning on the device, electrons flowing in the device decreases the injection barrier for holes, and more holes into the channel further lower the injection barrier for electrons, thus forming a positive feedback.

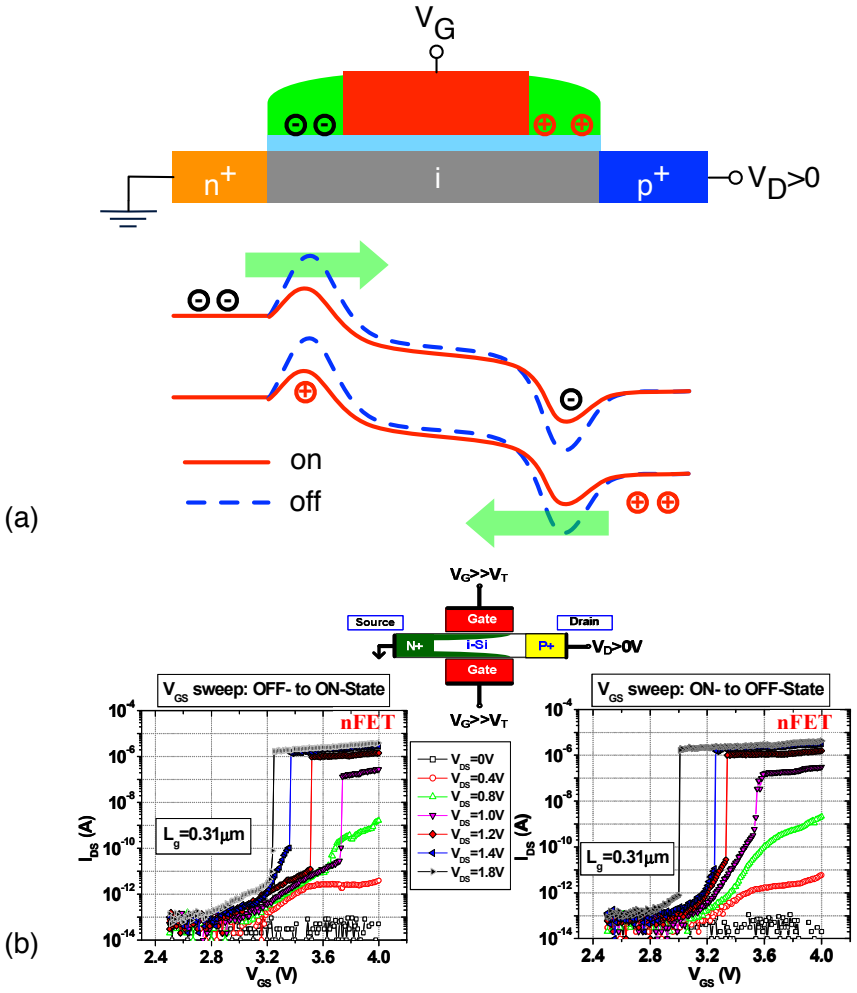


Figure 4.3: (a) Structure and band diagrams of a feedback FET at *on* and *off* states, illustrating the working principle. (b) the steep-SS characteristics in a feedback FET during turn-*on* and turn-*off*, showing the large hysteresis [157].

Padilla *et al.* demonstrate the steep SS in the feedback FETs, in which trapped charges in sidewall spacers are applied to form the barriers for carrier injection (Fig. 4.3(b)) [157]. Recently, Wan *et al.* reports another type of feedback FET by forming injection barriers with an additional back-gate bias [158].

As shown in Fig. 4.3(b), feedback FETs demonstrate characteristics with steep SS but also large hysteresis due to different mobile charge densities in *on* and *off* states [157]. The large hysteresis also significantly degrades the effective SS. In addition, the formation of barriers with trapped charges requires a programming operation with high voltages to inject charges into the sidewall spacers.

4. ***Nanoelectromechanical FET:***

   Nanoelectromechanical FET (NEMFET) realizes a steep-SS switch with nanoelectromechanical components [159–161]. Kam *et al.* propose a NEMFET with a suspended gate as shown in Fig. 4.4(a) [159]. The device is *off* due to the fully-depleted channel when gate is in contact with the dielectric. When increasing V_G to a threshold voltage, the gate abruptly pull away from the channel due to the spring restoring force. As a result, the current abruptly increases, showing a steep SS. Recently, Kim *et al.* experi-

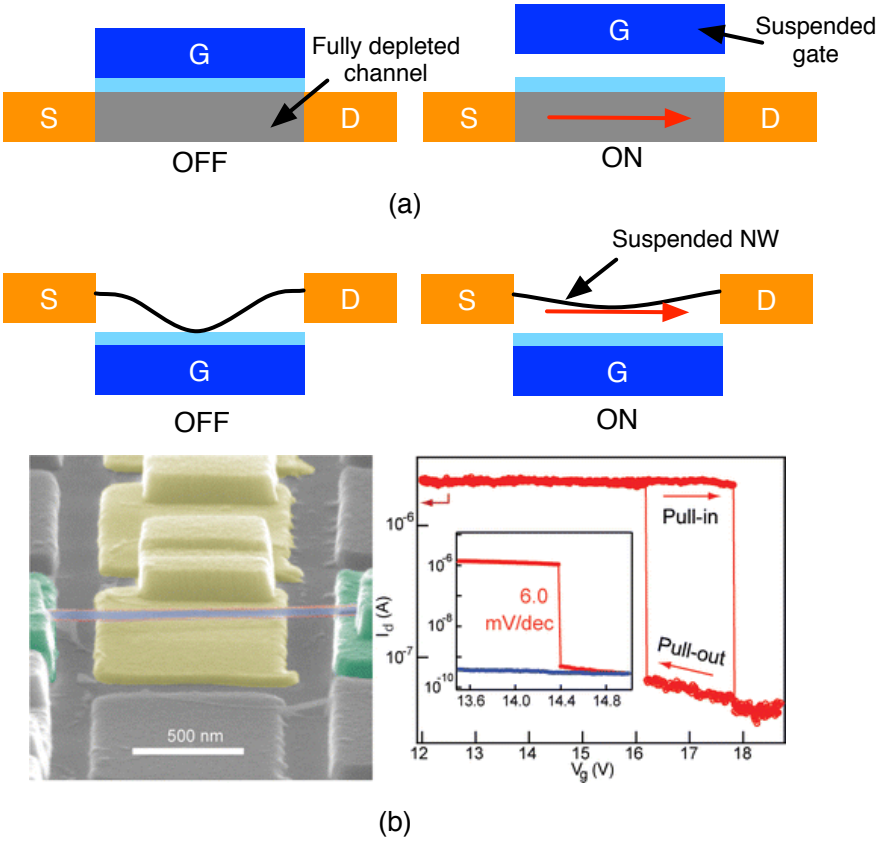


Figure 4.4: (a) NEMFET with a suspended gate [159], (b) NEMFET with a suspended nanowire channel [160].

mentally demonstrate a NEMFET by employing a suspended nanowire as conducting channel [160]. The structure and characteristics are shown in Fig. 4.4(b).

However, similar to feedback FET, NEMFET also suffers from hysteresis and reliability issues due to the movable components. Vacuum packaging is also needed in the proper functioning and long term reliability to suppress stiction and control damping [162, 163]. Furthermore, NEMFET does not begin to conduct current until sometime after the gate turn-*on* voltage is applied, which also increases the delay of the switch operation [164].

5. ***Negative-Capacitance FET:***

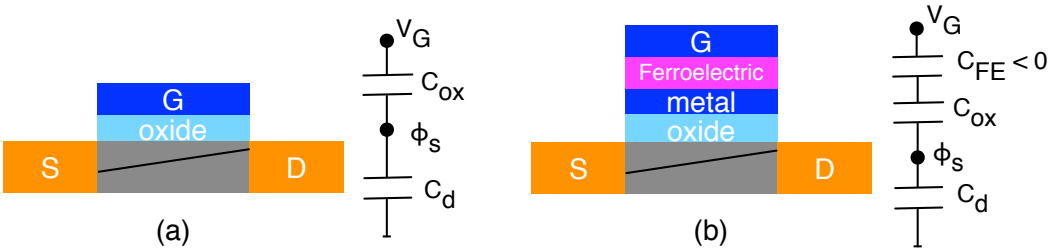


Figure 4.5: Structures and equivalent capacitive partition schematic of (a) conventional MOSFET and (b) negative-capacitance FET with ferroelectric gate material.

As introduced in Chapter 1, the SS in conventional MOSFETs can be written as

$$SS = \frac{\partial V_G}{\partial \phi_s} \cdot \frac{kT}{q} \ln 10 \tag{4.1}$$

By considering the MOSFET as a capacitive partition (Fig. 4.5(a)), it is derived that

$$\frac{\partial V_G}{\partial \phi_s} = 1 + \frac{C_\mathrm{d}}{C_\mathrm{ox}} \tag{4.2}$$

where C_ox is the oxide capacitance, and the C_d is the depletion capacitance in the channel.

In conventional CMOS technology, the effort of applying FinFET or ultra-thin-body channel with high-κ dielectric aims at $C_\mathrm{d}/C_\mathrm{ox}$ as small as possible to obtain better SS. However, $\partial V_G/\partial \phi_s \geq 1$ still lets the SS above the thermal limit.

In contrast, *Negative-Capacitance FET* (NC-FET) inserts ferroelectric materials that show negative capacitance into the gate insulator stack (Fig. 4.5(b)). The negative-capacitance property gives the opportunity to obtain $\partial V_G/\partial \phi_s < 1$ [165]. Therefore, the NC-FET can also demonstrate a steep SS below the thermal limit [166].

NC-FET is a topic of great interest in steep-SS device technology. However, it is still expecting more theoretical work on the mechanism and experimental work on the performance enhancement, such as improving average SS and non-hysteretic operation [166–170].

In the following part of this chapter, a steep-SS operation in a DIG FinFET is presented. The steep SS is achieved by introducing weak impact ionization induced feedback with dynamic modulation of Schottky barriers. The measured characteristics show a very steep average SS over the subthreshold region with high I_{on}/I_{off} ratio, as well as negligible hysteresis and good reliability.

4.2 Working Principle of Steep-Subthreshold-Slope DIG FinFET

Chapter 3 introduced the dual-V_T characteristics of multiple-independent-gate FETs with silicon nanowire channel. In this chapter, we further demonstrate the steep-SS operation in multiple-independent-gate FETs by using a FinFET structure. Despite of different channel structures, the working principle is also applicable to multiple-independent-gate SiNWFETs.

For the steep-SS operation, we consider the DIG silicon FinFET as shown in Fig. 4.6, in which PG_S and PG_D are connected together to bias the Schottky barriers. To better indicate their role during operation, the connected polarity gates are renamed as *Schottky Barrier Bias* (SBB), and the control gate is simply called *Gate* (G) in this chapter.

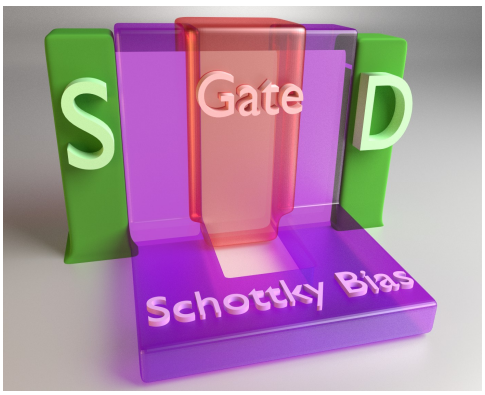


Figure 4.6: Structure of a dual-independent-gate silicon FinFET.

First, it is worth mentioning that the device keeps the capability of polarity control by using SBB to modulate the Schottky barriers and select the carrier type. Thus, it can also provide high computational density thanks to the enhanced functionality.

Then, the principle of the steep-SS operation in the device is shown in Fig. 4.7. For *n*-type behavior, i.e., when $V_{SBB} > 0$, the Schottky barrier at source is thin enough, thus electrons are selected to tunnel through the Schottky barrier into the channel. When V_G is at the threshold voltage, a transition occurs in the device. Electrons flowing in the channel may gain enough energy to trigger the weak impact ionization, which generates electron/hole pairs (Step 1). The generated electrons drift to the drain, and the holes accumulate in the potential well induced by the gate (Step 2). This lowers the potential barrier in the channel, and provides more electrons for impact ionization. Then, more accumulated holes continue to lower the barrier and thus form a positive feedback [171–178].

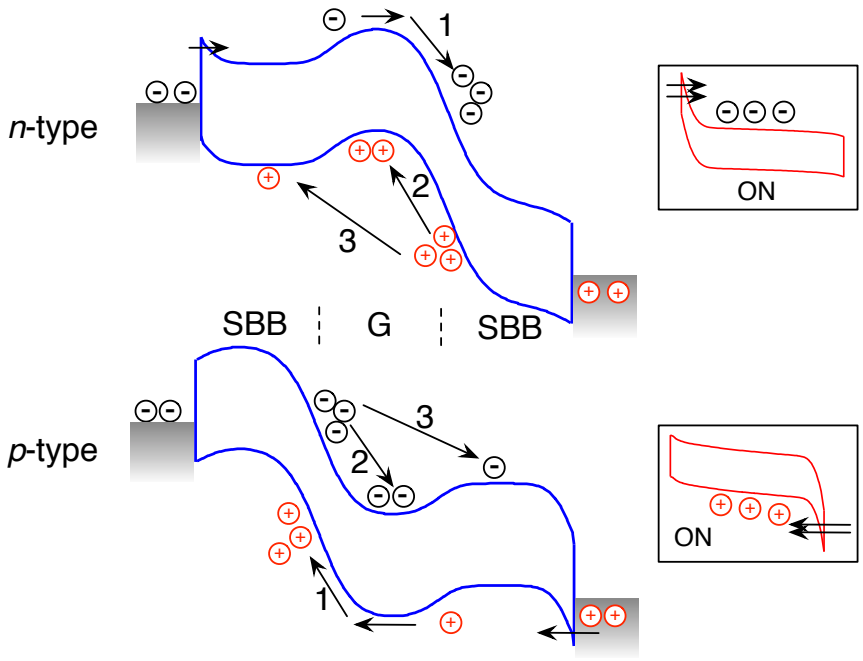


Figure 4.7: Band diagram of *n*-type ($V_{SBB} > 0$) and *p*-type ($V_{SBB} < 0$) operation in DIG FinFET. Main switching mechanisms: 1: impact ionization, 2: generated carriers accumulating in the potential well induced by the gate, 3: carriers swept towards the SBB region. When completely *on*, impact ionization and potential well vanish.

FinFET structure provides superior gate control of impact ionization, thus enhancing carrier multiplication [155]. Moreover, another important contribution is from the dynamic modulation of the Schottky barrier. Parts of the generated holes are swept towards the source, increasing the hole density in the SBB region at source (Step 3). Quasi-Fermi potential in the region controlled by SBB at source also increases during the switch operation. This is due to the reduced resistivity at the junction between the gate-controlled region and the region controlled by SBB at drain. The increased hole density and quasi-Fermi potential help to lower the energy band under the SBB at source. Therefore, Schottky barrier at source becomes thinner and more electrons tunnel through it. In the meantime, the potential well under the gate is kept, allowing Step 2 to occur longer until the final *on* state. This mechanism improves the I_{on}/I_{off} ratio, and is considered as a key to achieve steep transition over the entire subthreshold region. The operation of *p*-type is similar but with $V_{SBB} < 0$.

To better illustrate the operation principle, Fig. 4.8 shows the TCAD simulation of a DIG FinFET with gate length of 100 nm, 2 nm SiO_2 and fin width of 40 nm. Polarity of the device changes by adapting the polarity of V_{SBB}. Steep-SS transition is observed in both *n*-type (~5 mV/dec) and *p*-type (~35 mV/dec) (Fig. 4.8(a)). A sudden change of the surface potential just before and after the *on* state is observed under both Gate and SBB in Fig. 4.8(b). The hole

density in the device shows the accumulation of holes after the *on* state as predicted in the mechanism (Fig. 4.8(c)).

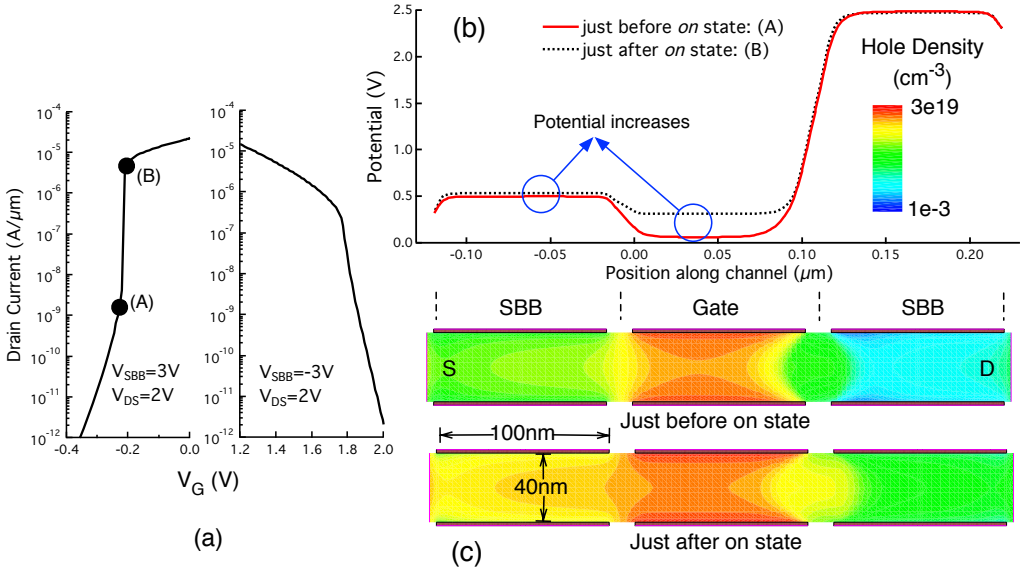


Figure 4.8: (a) TCAD-predicted device characteristics. The device polarity changes by adapting the polarity of V_{SBB}. (b) Surface potential distribution just before and after *on* state (n-type). (c) Hole density showing the accumulation of holes under Gate and SBB.

4.3 Device Characterization

The DIG FinFET is fabricated following the process flow presented in Chapter 2. The device is then extensively characterized under different temperature conditions.

4.3.1 Room-Temperature Characterization

Fig. 4.9 shows the measured characteristics of the DIG FinFET. Minimum SS of 3.4 mV/dec is achieved with $V_{DS} = 5V$. When decreasing V_{DS}, the lateral electric field is reduced. Thus, the impact ionization rate decreases, and the SS gradually degrades to 61 mV/dec at $V_{DS} = 1V$. It is also observed that SS below 10 mV/dec and 60 mV/dec are obtained with $V_{DS} = 4V$ and $V_{DS} = 2V$, respectively. The applied V_{DS} are much smaller compared to IMOS [155], confirming the weak impact ionization in the DIG FinFET rather than avalanche breakdown in IMOS. Moreover, compared to counterparts with significant hysteresis [157, 179], double sweep shown in the inset of Fig. 4.9 confirms the negligible hysteresis in the characteristics of the DIG FinFET. The gate induced drain leakage is also well suppressed at $V_G = -1V$.

Fig. 4.10 illustrates the SS as a function of drain current. The average SS of 6 mV/dec is observed for 5 decades of current at $V_{DS} = 5V$. When decreasing V_{DS}, not only the minimal SS, but also the average SS degrades. It is clearly shown in this figure that the steep SS exits at

much lower current level with smaller V_{DS}. The reason is that smaller surface potential under the gate is required to maintain the lateral electric field for impact ionization with reduced V_{DS}. The smaller surface potential thus leads to lower drain current with steep SS.

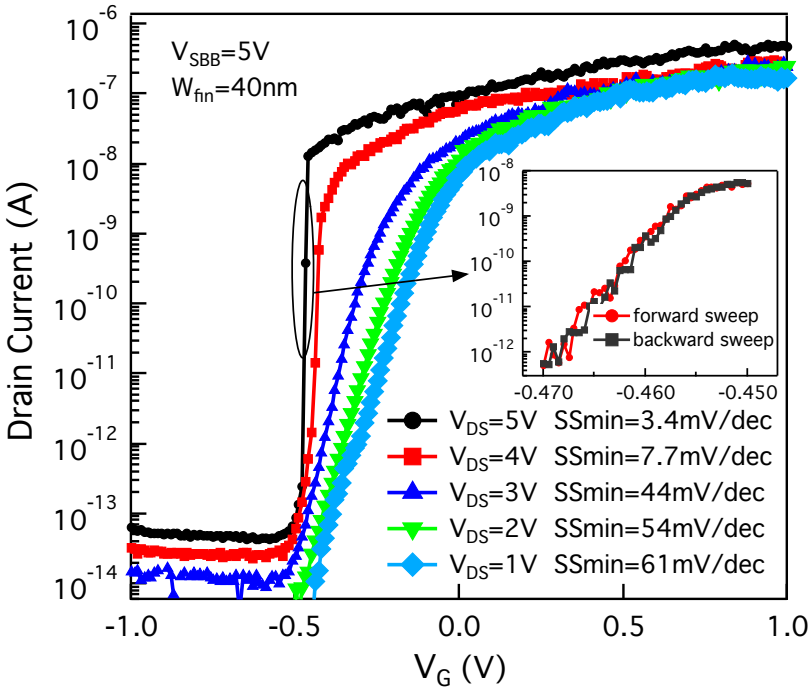


Figure 4.9: Measured characteristics of the DIG FinFET at different V_{DS} with $V_{SBB} = 5V$. Inset: double sweep showing negligible hysteresis and the minimal SS of 3.4 mV/dec.

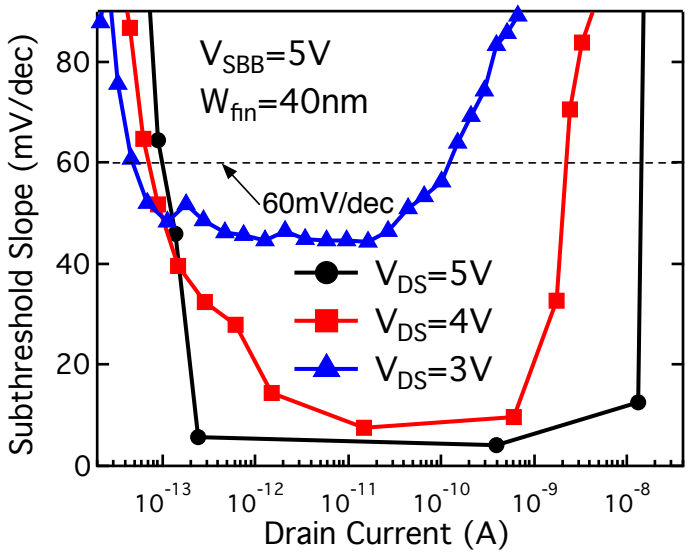


Figure 4.10: SS as a function of drain current with different V_{DS}, showing average SS of 6 mV/dec for 5 decades of current with $V_{DS} = 5V$. Dash line indicates the 60 mV/dec limit.

V_{SBB} controls the tunneling of carriers from the Schottky barriers, and therefore modulates the SS and I_{on}/I_{off} ratio. As shown in Fig. 4.11, with the same V_{DS}, higher V_{SBB} improves both SS and I_{on}/I_{off} ratio thanks to a better control of Schottky barriers.

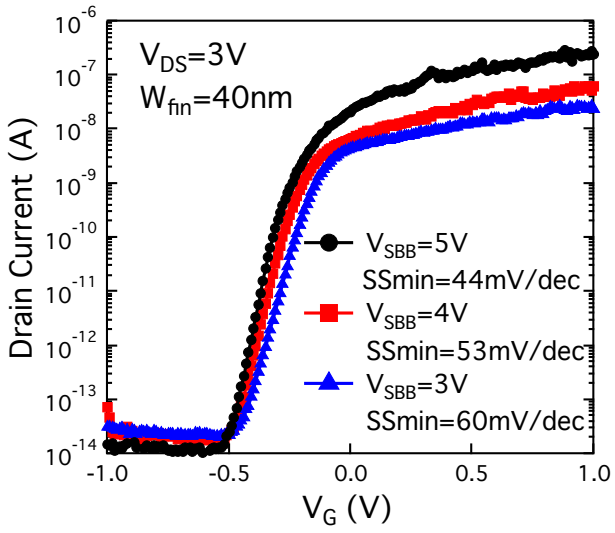


Figure 4.11: $I_D - V_G$ characteristics at different V_{SBB}. The SS and I_{on}/I_{off} ratio are both improved with higher V_{SBB}.

DIG FinFETs have the capability of polarity control by changing the polarity of V_{SBB}. Fig. 4.12 shows the measured n-type and p-type characteristics in the same device with $V_{DS} = 4V$. Both n-type and p-type characteristics show I_{on}/I_{off} ratio above 10^7. The steep SS is observed

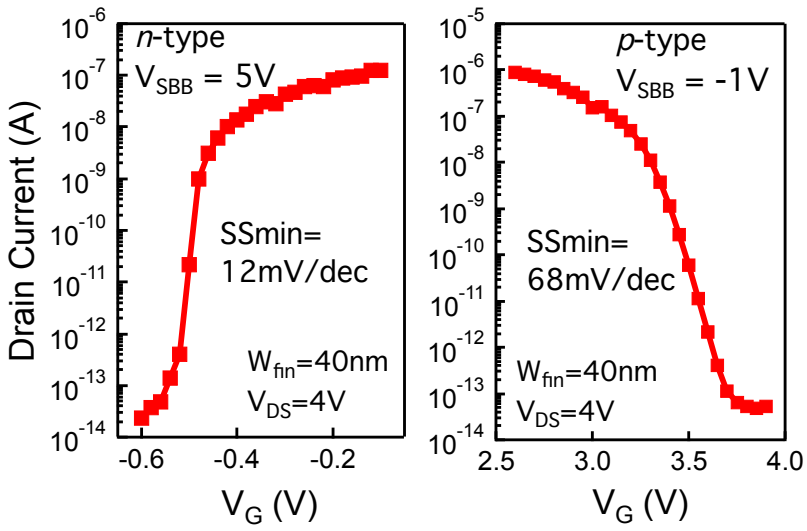


Figure 4.12: Measured n-type and p-type characteristics in the same DIG FinFET. The polarity of V_{SBB} determines the device polarity. Steep SS is achieved in n-type operation.

in n-type operation, where the minimal SS is 12 mV/dec. In contrast, the minimal SS of p-type operation is above 60 mV/dec due to a lower impact ionization rate of holes. The effect of the ionization rate of holes on the p-type operation will be further discussed through a temperature-dependent characterization since the ionization rate varies with different temperatures.

Fig. 4.13 illustrates the statistical distribution of SS in all measured DIG FinFETs under different operation voltages. At operation voltage of 5 V, 63% of the measured devices demonstrate SS below 10 mV/dec. The SS in 100% of the devices is below 50 mV/dec. When reducing the operation voltage to 4 V, there are still 80% showing SS below 50 mV/dec. The statistical study not only confirms the very steep SS in DIG FinFETs, but also shows the good yield of the steep-SS transistor fabricated with the presented process flow even with the academic cleanroom facilities.

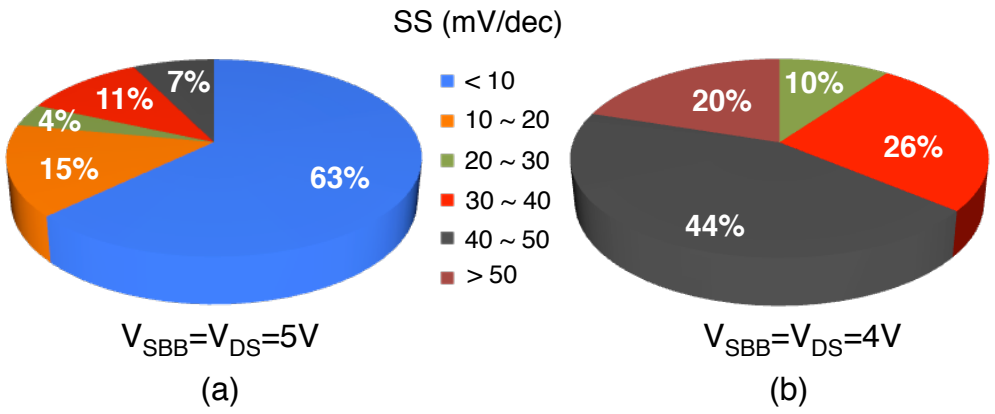


Figure 4.13: Statistical distribution of SS of the DIG FinFETs under different operation voltages. (a) 63% of the measured devices are working with SS < 10 mV/dec at $V_{SBB} = V_{DS} = 5V$. (b) 80% of the devices show SS below 50 mV/dec at $V_{SBB} = V_{DS} = 4V$.

Interestingly, an ambipolar steep-SS characteristic is observed in Fig. 4.14. The steep SS at $V_G \sim -0.5V$ in the n-branch is due to the feedback induced by weak impact ionization. Another steep SS in the p-branch is obtained when applying a strong negative gate bias. It is considered as an IMOS-like operation due to avalanche breakdown. The threshold voltage and SS in p-branch consequently show larger sensitivity to V_{DS} compared to the n-branch because of different mechanisms.

4.3.2 Temperature-Dependent Characterization

In order to study the temperature dependency of the steep SS and the effect of ionization rate of holes in p-type operation, DIG FinFET is characterized under different temperatures ranging from 100 K to 380 K.

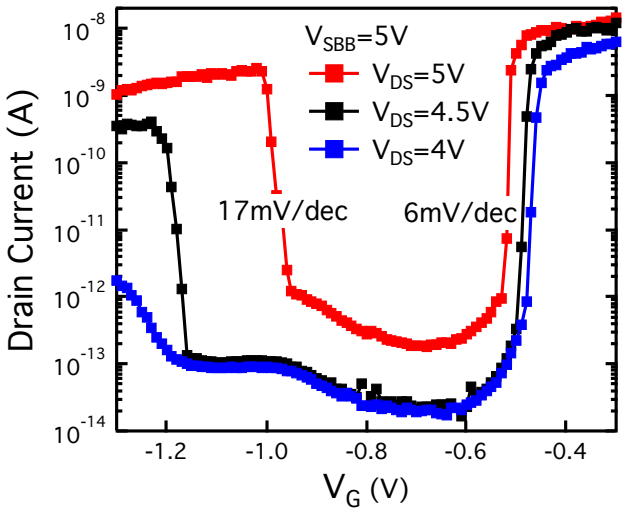


Figure 4.14: Ambipolar characteristics with steep SS in both n-type and p-type branches.

The n-type characteristics at different temperatures are shown in Fig. 4.15(a). The steep SS is observed from 100 K to 380 K without significant degradation. With decreased temperature, I_{on} and I_{off} decrease but the threshold voltage increases. The minimal SS values obtained for different V_{DS} and temperature conditions are reported in Fig. 4.15(b). The results show that the SS can be significantly improved by increasing V_{DS}. When $V_{DS} \geq 3V$, the device shows a SS well below thermal limit from 300 K to 380 K. In contrast to the normal-SS operation ($V_{DS} = 2V$), the lines with $V_{DS} \geq 3V$ in Fig. 4.15(b) shows smaller slope, which indicates a reduced sensitivity to temperature.

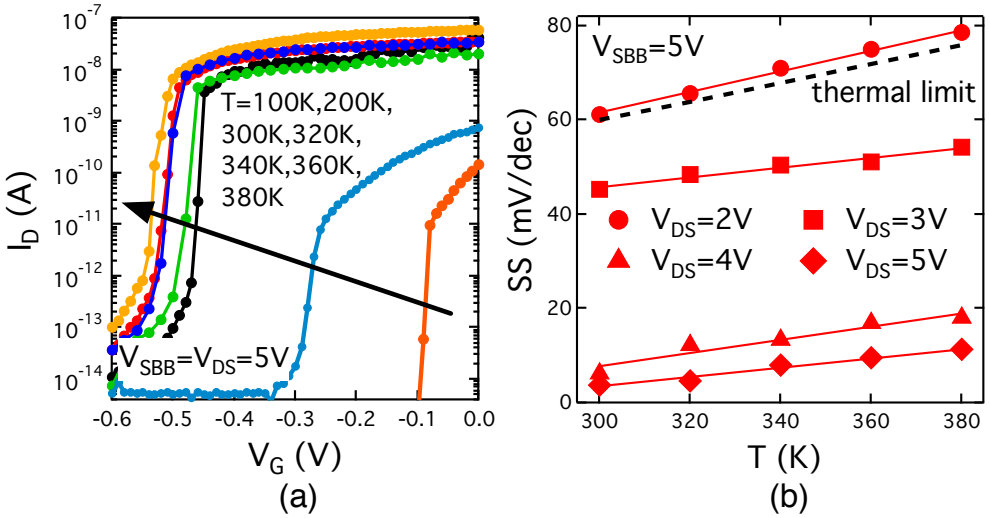


Figure 4.15: (a) n-type characteristics with steep SS at different temperatures, (b) Minimal SS extracted at different temperatures and V_{DS}.

Compared to the steep SS in *n*-type characteristics, the *p*-type behavior of the device at room temperature is similar to normal MOSFETs. The weaker impact ionization in *p*-type characteristics than in *n*-type operation is considered as due to the lower impact ionization rate of holes than electrons, which is caused by a much larger phonon scattering rate of holes than electrons [10, 180].

Since the ionization rate decreases with higher temperature, the high-temperature *p*-type characteristics are also similar to normal MOSFETs. In contrast, the main concern in the *p*-type operation is at low temperatures that enhance the ionization rate. Therefore, it is interesting to try to also observe the impact ionization induced SS improvement in *p*-type configuration by lowering the temperature.

As shown in Fig. 4.16(a), there is nearly no improvement of SS by increasing V_{DS} from 2 V to 4 V with $V_{SBB} = -1V$ at 200 K. However, by further lowering the temperature to 100 K in Fig. 4.16(b) or increasing V_{SBB} to $-2V$ in Fig. 4.16(c), the V_{DS}-dependent SS becomes evident, according to the enhancement of the impact ionization with lower temperature and/or higher electric field.

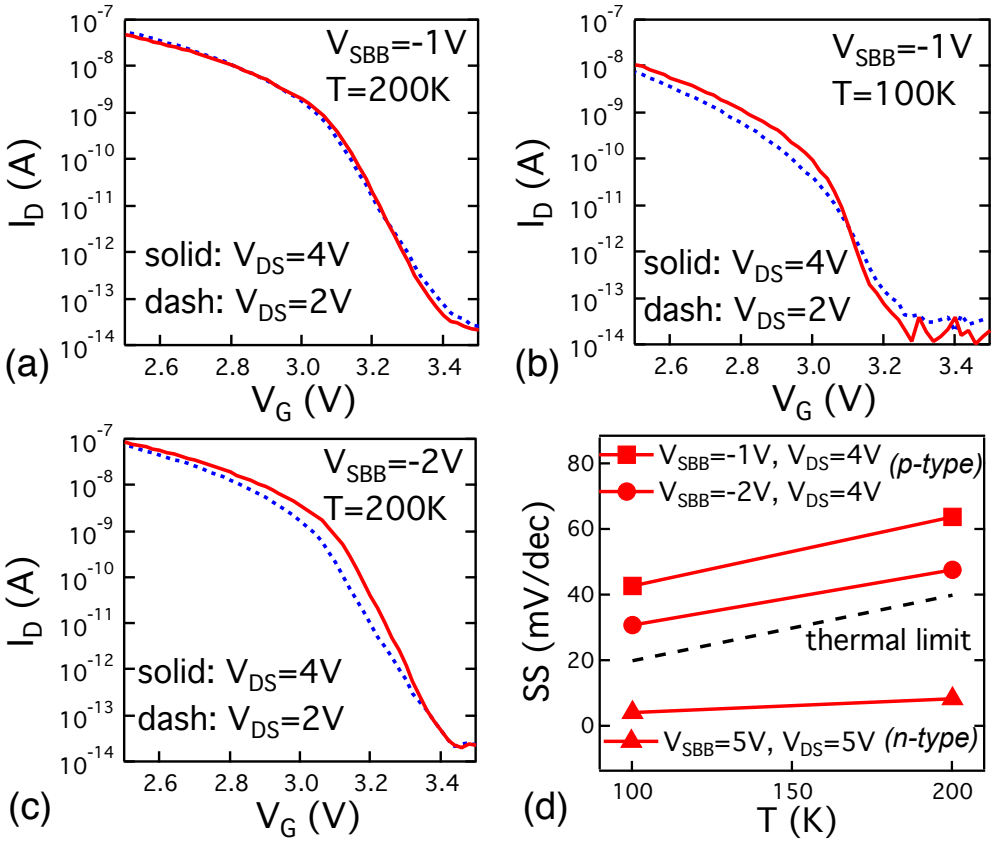


Figure 4.16: (a)-(c) *p*-type characteristics with different V_{SBB} and V_{DS} at 100 K and 200 K. (d) SS of *n*-type and *p*-type configurations at low temperatures.

Fig. 4.16(d) summarizes the SS under low temperatures and different V_{SBB} conditions for both n-type and p-type operations. The steep SS in n-type behavior at low temperatures keeps the reduced sensitivity to temperature similar to the high-temperature range. For p-type operation, although still above the thermal limit, the SS becomes less sensitive to temperature when $V_{SBB} = -2V$, similarly to the n-type behavior.

4.3.3 Influence of Fin Width

The dependency of the steep SS and the threshold voltage V_T on the width of the fin (W_{fin}) is also studied. DIG FinFETs with the W_{fin} of 40 nm, 50 nm, and 60 nm are fabricated on the same wafer. The characteristics of these devices with different W_{fin} are shown in Fig. 4.17(a). The SS does not significantly depend on W_{fin} in the range of 40-60 nm, while V_T increases in devices with a thinner fin, similar to conventional SOI and double-gate MOSFET with fully depleted channel [119, 181]. The device with W_{fin} = 40nm shows better electrostatic control of the Schottky barriers, thus enhancing the I_{on}/I_{off} ratio. The statistics based on all the measured devices (~50) at lower voltages support the observed dependency as shown in Fig. 4.17(b).

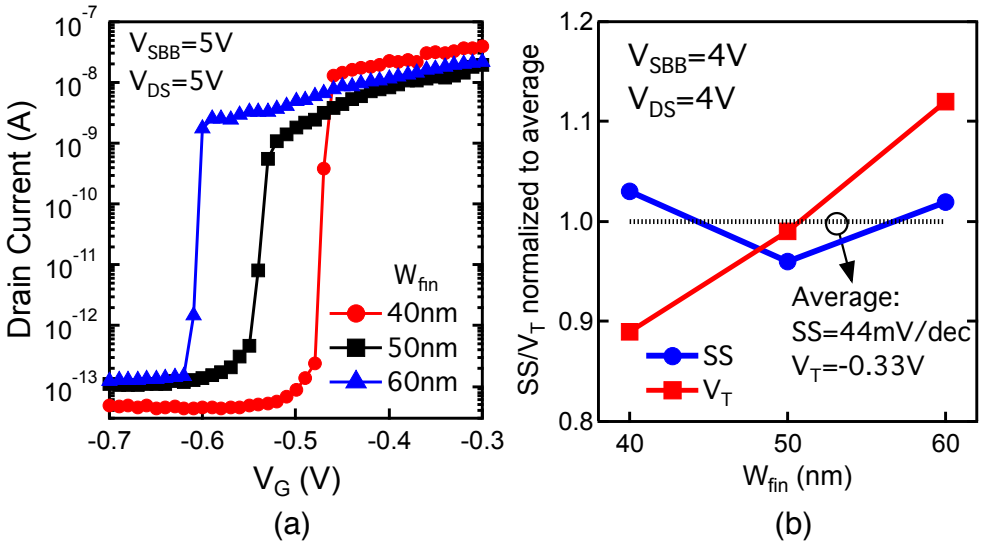


Figure 4.17: (a) Measured characteristics in devices with different W_{fin} at $V_{SBB} = V_{DS} = 5V$. (b) Statistics of SS and V_T based on all measured devices (~50) at lower voltage ($V_{SBB} = V_{DS} = 4V$), confirming the dependence of V_T on W_{fin}. The values are normalized to the average value.

4.3.4 Influence of Potential Well under Gate

As discussed in the working principle, the potential well under the gate built with the SBB region is a key to achieve SS far below the thermal limit. Carriers accumulate in the potential well, thus forming the positive feedback. In order to show the effect of the potential well and the SBB region, a FinFET with a single SBB region is built (Fig. 4.18(a)). The operation of this

device is shown in Fig. 4.18(b). In this device, a single SBB region controlling the Schottky barrier at drain to block holes tunneling. Gate controls the Schottky barrier at source and electrons tunneling, thus turning the device *on* or *off*. The channel length and the impact ionization region are the same as in the proposed device. However, there is no potential well for accumulating holes under the gate due to the absence of the SBB at source, leading to a very weak positive feedback. This device is fabricated with the DIG FinFETs on the same wafer to minimize unexpected process variations (Fig. 4.18(c)).

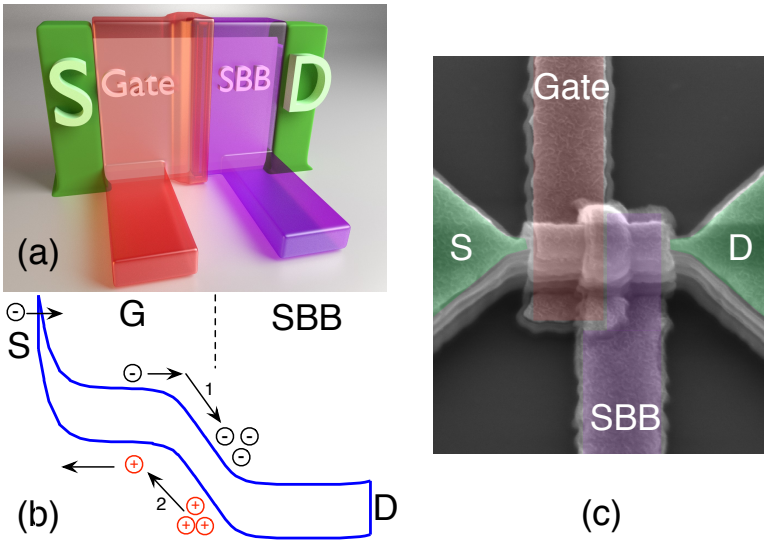


Figure 4.18: (a) Sketch of the FinFET with a single SBB region. (b) Band diagram shows no potential well under the gate, leading to a weak positive feedback. (c) SEM image.

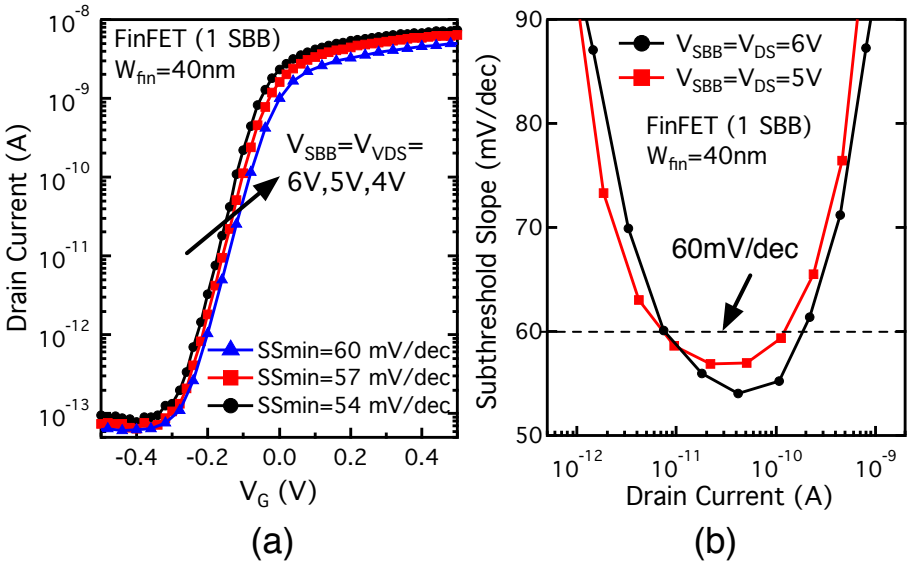


Figure 4.19: (a) Characteristics of the single-SBB FinFET with biases on SBB and drain up to 6 V. (b) SS as a function of drain current.

Fig. 4.19 shows the characteristics of the single-SBB FinFET. As a result of the weak positive feedback, the minimal SS is slightly below 60 mV/dec with even higher biases on both SBB and drain. The steep-SS operation is kept for less than 2 decades of current. This result verifies the importance of the potential well and the SBB at source.

4.3.5 Reliability Assessment

According to the working principle of the steep SS in DIG FinFET, the weak impact ionization only occurs at low V_G, where the lateral electric field is large enough to accelerate carriers to the threshold energy for impact ionization. When increasing V_G, the lateral electric field decreases due to a sudden potential drop caused by the feedback, and the impact ionization finally vanishes when the device completely turns *on*. This is also observed in the output characteristics in Fig. 4.20. The impact ionization induces a non-saturated current at low V_G and high V_{DS}, which is similar to the well-known "kink" effect in SOI MOSFETs [182]. As indicated by the dots in Fig. 4.20, the required V_{DS} to trigger this effect is below 2 V with $V_G = -0.2V$, then significantly increases with higher V_G. When $V_G \geq 0.5V$, this effect can no longer be observed.

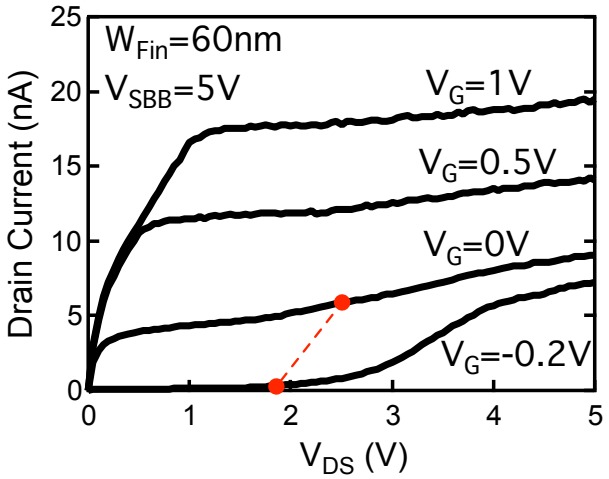


Figure 4.20: Output characteristics of the DIG FinFET. Impact ionization occurs at low V_G, but vanishes when the device is completely *on* (high V_G).

Compared to IMOS, which is based on strong impact ionization (i.e., avalanche breakdown) and suffers from reliability problems, the weak impact ionization in DIG FinFETs requires lower V_{DS} and only occurs during the transition. Thus, good reliability can be achieved in the DIG FinFETs.

Hot carrier injection and bias temperature instability are two main concerns in device reliability [183, 184]. Carriers with high energy (hot carriers) may be injected into the gate dielectric and get trapped or cause interface states to be generated. The resulted defects will lead to threshold voltage shifts and transconductance degradation of the device. On the other hand,

when devices are stressed with a constant gate voltage, positive charge can build up either at the interface or in the gate dielectric, and also leads to performance degradation.

Fig. 4.21 shows the reliability assessment of the DIG FinFET with steep-SS operation (SS <10 mV/dec). In Fig. 4.21(a), the stress condition of large V_{DS} up to 4 V is applied to test the hot carrier injection. While in Fig. 4.21(b), The negative bias temperature instability is tested under the stress condition of $V_G = -0.8V$. With different stress periods, no significant degradation is observed in terms of threshold voltage, I_{on}/I_{off} ratio or SS, which proves the good reliability of the DIG FinFET.

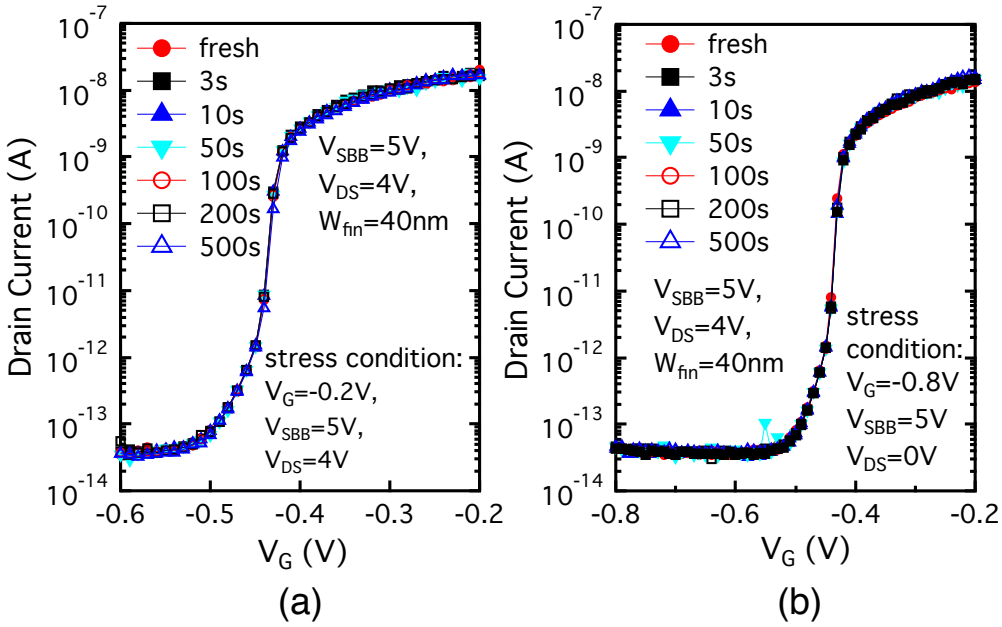


Figure 4.21: Reliability assessment of the DIG FinFET during the steep-SS transition: (a) hot carrier injection and (b) negative bias temperature instability with different stress periods.

4.3.6 Low-Voltage Operation

Moreover, considering the low doping concentration ($\sim 10^{15}/cm^3$) and the thin thickness, the fin-shaped channel is fully depleted. Therefore, the device exhibits an excellent electrostatic control at low operation voltages (both V_{SBB} and V_{DS}) down to 0.5 V. Subthreshold slope close to the thermal limit and a good control of DIBL effect are observed in Fig. 4.22.

4.4 Discussion

This section analyzes the steep-SS behavior and the formulas. Then, based on the discussion, feasible improvements are suggested to improve the device performance.

This study builds on the results obtained for SOI-based steep-SS transistor, which is also

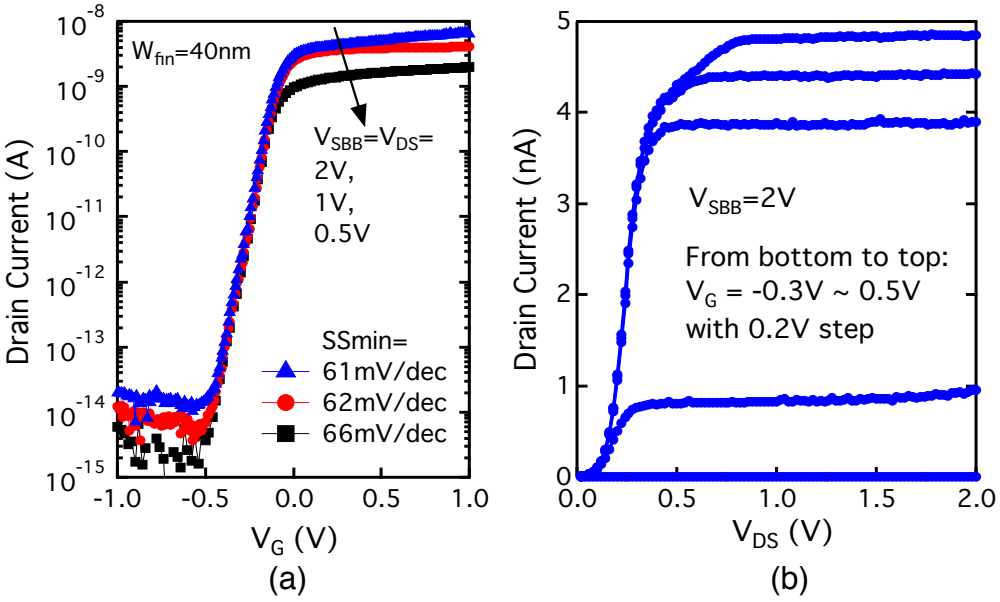


Figure 4.22: Characteristics of DIG FinFET under low operation voltages. (a) Near-ideal SS and high I_{on}/I_{off} ratio show the excellent electrostatic control, (b) Output characteristics show a good control of the DIBL effect.

based on the impact ionization induced feedback [172]. Similarly to the SOI-based device, the expression of SS in DIG FinFET is derived as:

$$SS = \frac{kT}{q}\ln 10 \cdot n \tag{4.3}$$

In this equation,

$$n = \frac{1+r}{1+r\dfrac{\mathrm{d}V_{\mathrm{BS}}}{\mathrm{d}V_{\mathrm{GS}}}}$$

and

$$r = \frac{2\varepsilon_{\mathrm{si}}\, t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}\, t_{\mathrm{si}}}$$

where $\varepsilon_{\mathrm{si/ox}}$ and $t_{\mathrm{si/ox}}$ stand for the dielectric constant of silicon/gate dielectric and the thickness of the fin/gate dielectric, respectively.

In the DIG FinFET, V_{B} is the potential at the middle point between the two sidewalls of the fin in the gate-controlled region as shown in Fig. 4.23(a). V_{BS} is the difference between V_{B} and the voltage at source. In contrast, V_{B} in the SOI-based device stands for the potential at the bottom of the silicon channel [172]. Although the positions of V_{B} indicated in DIG FinFET and SOI-based device are different, they both represent the locations where the accumulated

charges are stored, thus having similar effects on the steep-SS operation.

The DIG FinFET structure consequently excludes the influence on the SS from a back bias applied through the SOI wafer. It has been validated on the device by varying the back bias from -4 V to +4 V. As a result, a consistent subthreshold behavior, i.e., the same steep SS (~18 mV/dec) and V_T, is observed under different back biases as demonstrated in Fig. 4.23(b). The difference of I_{on} with different back biases is due to the insufficient control of the Schottky barriers at the bottom of the fin. The back bias can provide enhanced control of the Schottky barriers as an additional SBB from the bottom of the channel. Therefore, I_{on} is enhanced with larger back bias. This result also implies that a better control of the Schottky barriers at the bottom of the channel, such as producing fully silicided pillars at source and drain, can help to improve the drive current of the device.

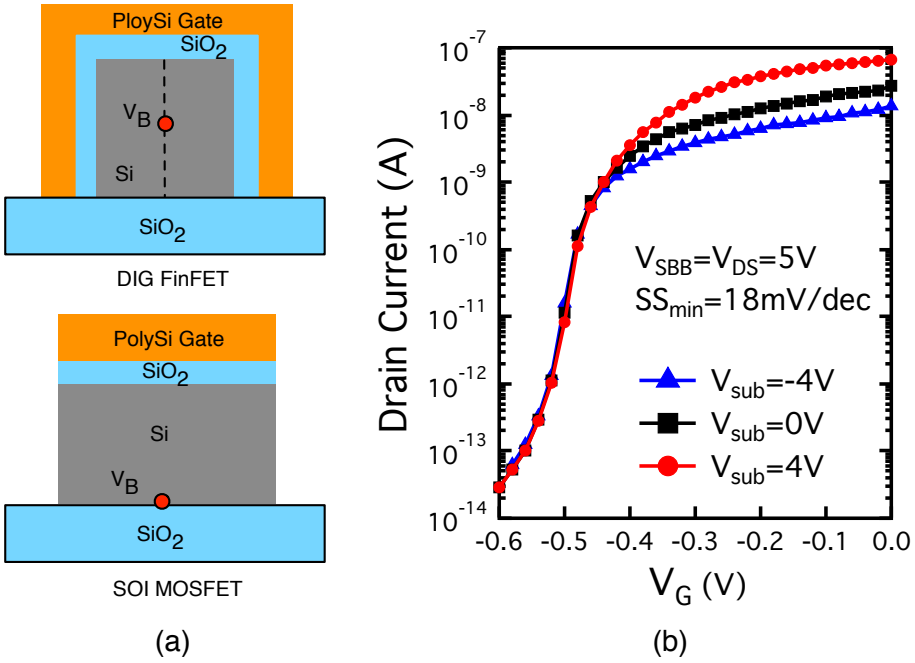


Figure 4.23: (a) V_B indicates different positions in DIG FinFET and SOI MOSFET. (b) The back bias (V_{sub}) applied to the SOI wafer shows no influence on the steep SS or V_T in DIG FinFET.

Eq. (4.3) also shows that when $dV_{BS}/dV_{GS} < 1$, a small r will lead to a SS approaching the thermal limit. This explains why scaling conventional MOSFET efforts tend to thin the gate oxide. However, when the carriers generated by impact ionization charge the body, it is possible to have $dV_{BS}/dV_{GS} > 1$. In this case, a large r (i.e., thick gate oxide) can magnify the feedback and further reduce the SS. Therefore, in this kind of steep-SS devices, the scaling down of t_{ox} can be relaxed.

In the presented n-type characteristics of the DIG FinFET, the SS below thermal limit indicates that $dV_{BS}/dV_{GS} > 1$. In contrast, the SS of the p-type characteristics is beyond the thermal limit with $dV_{BS}/dV_{GS} < 1$. Nevertheless, the improvement of SS with increased V_{SBB} and V_{DS}

(Fig. 4.16) implies that a SS below thermal limit may be also achieved in *p*-type operation by further optimizing dV_{BS}/dV_{GS}.

To better understand this operation, Fig. 4.24 shows dV_{BS}/dV_{GS} extracted from the *n*-type characteristics according to Eq. (4.3). When $V_{DS} \geq 2.5V$, dV_{BS}/dV_{GS} starts to be larger than one. When $V_{DS} \geq 3.5V$, it is observed that dV_{BS}/dV_{GS} significantly decreases with higher temperature. In addition, dV_{BS}/dV_{GS} also increases with larger V_{DS}.

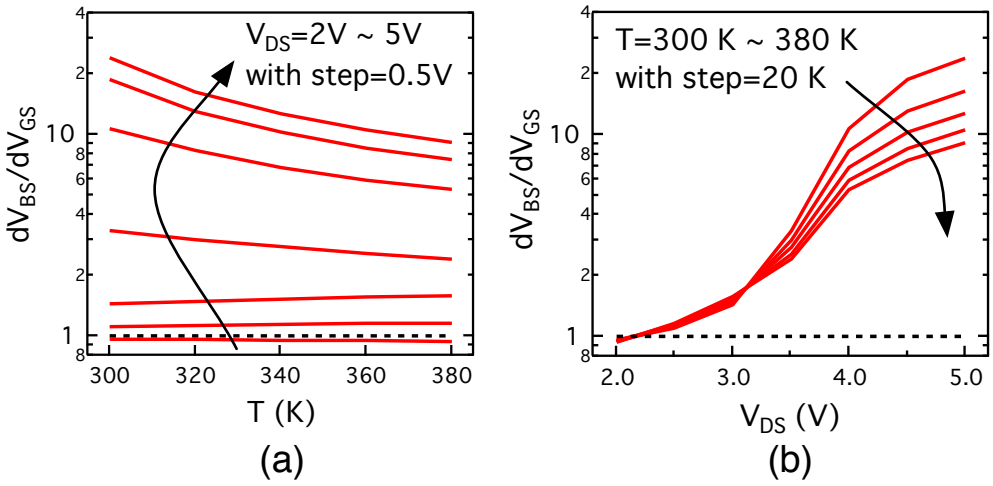


Figure 4.24: Extracted dV_{BS}/dV_{GS} from the *n*-type characteristics shown in Fig. 4.15 at different temperatures (T) and V_{DS}.

An expression is then derived to describe the temperature-dependent behavior of dV_{BS}/dV_{GS}. By extending the analysis on SOI-based device to DIG FinFET [172, 185], the expression for *n*-type operation is obtained as:

$$\begin{aligned} \frac{dV_{BS}}{dV_{GS}} &\simeq \frac{m}{n} \cdot \frac{1}{1+I_{gt}/I_{gi}} \\ &\propto \frac{m}{n} \exp\left[\frac{q}{kT}\left(\frac{V_{GS}}{n} - \frac{V_B - V_{B,SBBs}}{m}\right)\right] \cdot \exp\left(-\frac{\beta_i l}{V_{DS}}\right) \end{aligned} \tag{4.4}$$

where I_{gt} is the *off*-state leakage current and I_{gi} is the impact-ionization current [172]. β_i is a constant and l is a structural parameter. m is the ideality factor of the junction between the gated region and the region controlled by the SBB at source (SBBs). Eq. (4.4) well captures the dependency of dV_{BS}/dV_{GS} on temperature and drain bias in Fig. 4.24.

Note that, there is a significant difference in Eq. (4.4) compared to the SOI-based devices: the centric potential at the SBBs region ($V_{B,SBBs}$) replaces the V_S in [172]. Compared to the fixed V_S, $V_{B,SBBs}$ continuously increases during the transition thanks to the increase of quasi-Fermi potential and the effects of the holes generated by the impact ionization. Thus, the improved dV_{BS}/dV_{GS} during the transition can support a better SS over the subthreshold region. As already demonstrated by the characterization, the DIG FinFET has much better SS compared

to the similar device but without the SBB region at source. This shows the importance of the Gate-SBBs junction in the feedback operation. A better control on the SBB region, such as tuning the oxide thickness and the fin width at the SBB region, can thus further optimize the device performance.

Eq. (4.4) also suggests that lower leakage current I_{gt} helps to improve the SS. With a very small I_{gt}, $\mathrm{d}V_{\mathrm{BS}}/\mathrm{d}V_{\mathrm{GS}} > 1$ may be triggered by a very small impact-ionization current I_{gi}, and hence, by a low V_{DS}. Therefore, a gate-all-around nanowire structure with low density of defects may be applicable for future improvements.

Through the above study on the steep-SS operation in DIG FinFETs, the following feasible improvements on the device performance are suggested.

First, the device performance can be improved by applying an optimized process with scaled dimensions and technology boosters, such as strain technology for enhancing the carrier mobility and tuning ionization rates [115, 186–188]. As a Schottky-barrier device, the drive current is limited by the Schottky-barrier height. Thus, a reduced Schottky-barrier height for electrons improves the drive current of *n*-type configuration. Furthermore, a channel material with smaller bandgap can be used to form lower Schottky barriers for both electrons and holes, thus improving the drive currents for both *n*-type and *p*-type configurations [189].

Towards low-power applications, the steep-SS devices are desired to operate with a sufficiently low V_{DS}. The strategy to reduce V_{DS} for DIG FinFETs is consequently discussed as follows.

First, as demonstrated in [173], a similar steep-SS operation is achieved in a 25 nm SOI device with $V_{DS} = 1.2V$. With the additional aid of the DIG structure, the dynamic modulation of Schottky barriers can further improve the average SS. Therefore, the DIG FinFET with deeply scaled dimensions and optimized source/drain resistance may require a $V_{DS} \leq 1.2V$, which is close to the threshold energy to trigger impact ionization in silicon as the bandgap of silicon is ~1.12 eV at 300 K.

On the other hand, as discussed above, the steep SS indeed depends on the ratio between the impact-ionization generation and the recombination. Although with fewer generation, the impact ionization can still occur with a sub-bandgap drain bias [190, 191]. Thus, a steep SS below thermal limit is still conceivable with a sub-bandgap drain bias if the feedback is optimized with the improvements for leakage reduction, such as applying a low-defect nanowire structure.

In addition, the threshold energy to trigger impact ionization decreases with the decreasing bandgap of the material [10]. Thus, the required V_{DS} can also be reduced by replacing silicon with other materials with smaller bandgap or higher impact ionization rate, such as germanium or carbon nanotube [192]. This is consistent with the suggestion for improving the drive current. For instance, the bandgap of germanium is ~0.66 eV at 300 K, giving enhanced ionization rates for both electrons and holes [10]. In this respect, the inherent suppression

of *off*-currents in the DIG-FET approach allows to keep I_{gt} sufficiently low as a further requirement for obtaining steep slopes in Eq. (4.4) [73]. Thus, the steep SS can be expected in germanium-based devices with a V_{DS} below 1 V for both *n*-type and *p*-type conductions.

Table 4.1 summarizes the strategy and suggested solutions for reducing V_{DS} in multiple-independent-gate FETs without sacrificing the steep SS.

Table 4.1: Suggestions for reducing V_{DS} in steep-SS multiple-independent-gate FETs

V_{DS} Objective	Strategy	Solution
$\sim E_g/q$ (~ Bandgap)	Enhance effective V_{DS} for impact ionization	Scaled dimensions and optimized S/D resistance
$< E_g/q$ (< Bandgap)	Reduce leakage to utilize sub-bandgap impact ionization	Low-defect nanowire structure
$\ll 1V$	Reduce threshold energy of impact ionization	Small bandgap material, e.g., germanium

4.5 Chapter Summary

This chapter experimentally demonstrate the steep SS in a polarity-controllable FinFET with dual independent gates, exploiting the electrostatic biasing of the S/D Schottky barriers. Minimal SS of 3.4 mV/dec and average SS of 6 mV/dec over 5 decades of current are achieved with ultra-low leakage floor and high $I_{\text{on}}/I_{\text{off}}$ ratio at room temperature. The steep SS in DIG FinFET also shows reduced sensitivity to temperature as compared to conventional MOSFETs through characterization of *n*-type and *p*-type operation from 100 K to 380 K.

Based on the characterization, this chapter further analyzed the epitomized SS in the formula and suggested feasible improvements to optimize the device performance and reduce the operation voltage without sacrificing the steep SS.

5 Compact Modeling

As shown in the previous chapters, multiple-independent-gate FETs provide new opportunities for circuit design thanks to their enhanced functionality, and have been extensively studied as far as fabrication, circuit design and architecture are concerned [72, 90, 93, 97, 100, 110, 122, 123, 185]. Nevertheless, a physics-based compact model for multiple-independent-gate SiNWFETs is not yet available, which is the critical interface between device technology and circuit design. This is the topic of this chapter.

There are many works on compact modeling of doped source/drain SiNWFETs and Schottky-barrier SiNWFETs [193–197]. Compared to these devices, polarity-controllable SiNWFETs introduce additional gated regions between source and drain. Therefore, it is necessary to model the different regions in order to predict the device characteristics. To address this discontinuity of the gate voltages along the channel, a simple assumption of constant capacitances between different gated regions is proposed to model a dual-independent-gate carbon nanotube FET [198, 199]. However, the ballistic solution for carbon nanotube FET used in [198, 199] is difficult to be applied to SiNWFETs due to lower carrier mobility in silicon [43, 200].

In this chapter, we fill the gap in modeling polarity-controllable SiNWFETs by presenting a long-channel model for DIG SiNWFETs based on the solution of conventional SiNWFET equations. Starting from Poisson's equation, the potential distribution and the drain current are obtained by solving the current continuity between Schottky-barrier contacts and the drift-diffusion of both carriers in the channel. The model captures the device operation in different bias configurations, and shows good agreements with TCAD simulation. Advanced physical effects can be easily embedded into the model to develop a complete compact model for polarity-controllable SiNWFETs.

This chapter is organized as follows: Sec. 5.1 shows the device structure investigated in this chapter. Then, the surface potential model and drain current model are derived in Sec. 5.2 and Sec. 5.3, respectively. The results are shown and discussed in Sec. 5.4. Finally, the chapter is summarized in Sec. 5.5.

5.1 Structure of DIG Silicon Nanowire FET

The model presented in this chapter focuses on the DIG SiNWFET. It has a simplified structure of TIG SiNWFETs presented in Chapter 3 by connecting the two polarity gates together. Fig. 5.1 shows the device structure studied in the model and for TCAD verification. The two external gates (PG_S and PG_D) are connected to modulate the Schottky barriers. Since this gate determines the type of carriers through the Schottky barriers, it is named *Polarity Gate* (PG). The gate in the middle of the channel induces a potential barrier to control the current, and is named *Control Gate* (CG).

The DIG SiNWFETs have been experimentally demonstrated in [72]. In the development of the model, we assume an intrinsic nanowire channel within the device. The thickness of gate dielectric t_{ox} and the radius of the nanowire R are assumed to be uniform from source to drain. The metallic contacts at source and drain have a workfuncition of Φ_m.

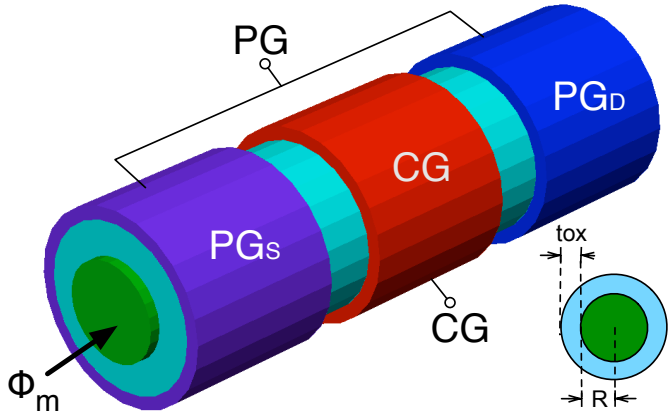


Figure 5.1: Structure of a dual-independent-gate SiNWFET.

The band diagrams in different configurations are shown in Fig. 5.2. PG modulates the thickness of Schottky barriers, while CG controls a potential barrier in the channel. In *n*-type

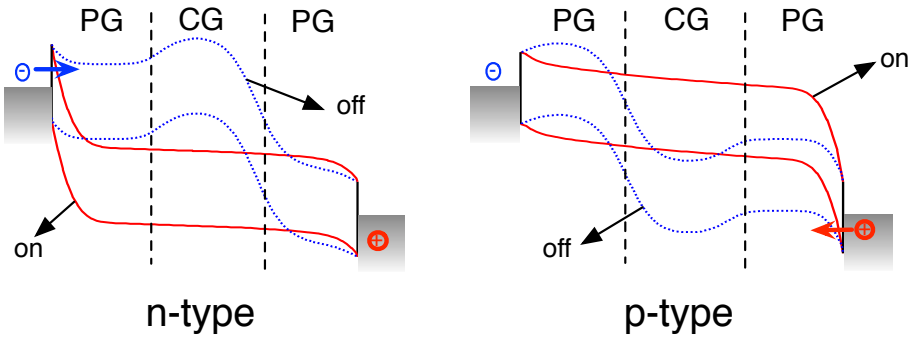


Figure 5.2: Band diagrams at *on* and *off* states in *n*-type and *p*-type configurations of a dual-independent-gate SiNWFET.

configuration (i.e., $V_{\mathrm{PG}} > 0$), electrons may tunnel through the thin Schottky barrier at source into the channel. At *on* state, CG is polarized to allow electrons flowing through the channel easily without barriers in the channel. In contrast, at *off* state, the potential barrier induced by CG prevents the current from flowing. The *p*-type operation (i.e., $V_{\mathrm{PG}} \leq 0$) is similar, but relies on holes tunneling through the barrier at drain.

5.2 Surface Potential Model

Polarity-controllable devices exploit the conduction due to both electrons and holes. Therefore, it is necessary to consider the transport of both carriers in the model. Thus, we start from 1-D Poisson's equation with both carriers in an intrinsic silicon nanowire channel:

$$\frac{d^2\phi}{dr^2} + \frac{1}{r}\frac{d\phi}{dr} = \frac{q(n-p)}{\varepsilon_{\mathrm{si}}} = \frac{qn_{\mathrm{i}}}{\varepsilon_{\mathrm{si}}}\left(e^{\frac{q(\phi-V_{\mathrm{n}})}{kT}} - e^{\frac{q(V_{\mathrm{p}}-\phi)}{kT}}\right) \tag{5.1}$$

where ϕ is the electrostatic potential in the channel, r indicates the distance from the center of the nanowire, n and p are the density of electrons and holes, respectively. The intrinsic carrier density is represented by n_i, and $\varepsilon_{\mathrm{si}}$ is the dielectric constant of silicon, V_{n} and V_{p} are the quasi-Fermi potentials of electrons and holes, respectively.

However, it is difficult to directly obtain an accurate and explicit solution to (5.1). Therefore, we first consider the case where there are only electrons as the majority carrier in the channel. Then, $n \gg p$ gives that $\phi \gg (V_p + V_n)/2$. Under this condition, Eq. (5.1) is simplified as:

$$\frac{d^2\phi}{dr^2} + \frac{1}{r}\frac{d\phi}{dr} = \frac{qn}{\varepsilon_{\mathrm{si}}} = \frac{qn_{\mathrm{i}}}{\varepsilon_{\mathrm{si}}}e^{\frac{q(\phi-V_{\mathrm{n}})}{kT}} \tag{5.2}$$

An exact solution to (5.2) has been reported [201–203]:

$$\phi = V_{\mathrm{n}} + \frac{kT}{q}\ln\left(\frac{-8B_{\mathrm{n}}}{\delta(1+B_{\mathrm{n}}r^2)^2}\right) \tag{5.3}$$

where $\delta = q^2 n_{\mathrm{i}}/kT\varepsilon_{\mathrm{si}}$, and B_n is a parameter that will be solved from the boundary condition.

Then, by assuming the effective gate voltage $V_{\mathrm{geff}} = V_G - V_{\mathrm{FB}} \approx \phi$, the bias condition for only considering electrons is derived as $V_{\mathrm{geff}} \gg (V_p + V_n)/2$.

Similarly, the solution when only considering holes is also derived. By combining these two results, a piecewise solution to (5.1) is obtained as:

$$\phi = \begin{cases} \phi_{\mathrm{n}} = V_{\mathrm{n}} + \frac{kT}{q}\ln\left(\frac{-8B_{\mathrm{n}}}{\delta(1+B_{\mathrm{n}}r^2)^2}\right) & \text{if } V_{\mathrm{geff}} \gg \frac{V_{\mathrm{p}}+V_{\mathrm{n}}}{2} \\ \phi_{\mathrm{p}} = V_{\mathrm{p}} - \frac{kT}{q}\ln\left(\frac{-8B_{\mathrm{p}}}{\delta(1+B_{\mathrm{p}}r^2)^2}\right) & \text{if } V_{\mathrm{geff}} \ll \frac{V_{\mathrm{p}}+V_{\mathrm{n}}}{2} \end{cases} \tag{5.4}$$

Finally, we derive a smoothing function to connect ϕ_{n} and ϕ_{n}. Thus, a single-piece approximation of ϕ is written as:

$$\phi = \sigma_1 \cdot \phi_{\mathrm{n}} + \sigma_2 \cdot \phi_{\mathrm{p}} \tag{5.5}$$

where $\sigma_1 = (1+\tanh\alpha)/2$, $\sigma_2 = (1-\tanh\alpha)/2$, and $\alpha = q(2V_{\mathrm{geff}} - V_{\mathrm{n}} - V_{\mathrm{p}})/2kT$.

Eq. (5.5) gives an accurate and smooth transition between the electron-dominated and hole-dominated operations as shown later in the Sec. 5.4.

In order to obtain the potential, B_{n} and B_{p} in (5.4) are solved from the boundary condition at the interface between nanowire and gate dielectric, which is given by Gauss's law:

$$C_{\mathrm{ox}}(V_{\mathrm{geff}} - \phi_{s,0}) = \varepsilon_{\mathrm{si}} \frac{d\phi}{dr}\Big|_{r=R} = Q_{\mathrm{n}} - Q_{\mathrm{p}} \tag{5.6}$$

where the gate oxide capacitance $C_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/[R \cdot \ln(1 + t_{\mathrm{ox}}/R)]$ with $\varepsilon_{\mathrm{ox}}$ the dielectric constant of gate oxide. The surface potential $\phi_{s,0}$ is located at the interface between the gate oxide and the silicon nanowire, and Q_{n} (Q_{p}) are the density of electrons (holes) within a unit area.

By substituting (5.5) into (5.6) with $\sigma_1 + \sigma_2 = 1$, we approximately derive the equations for majority carriers as [193]:

$$\frac{q(V_{\mathrm{geff}} - V_{\mathrm{n}} - \Delta V)}{kT} = \frac{q}{kT}\frac{Q_{\mathrm{n}}}{C_{\mathrm{ox}}} + \ln\frac{Q_{\mathrm{n}}}{Q_0} + \ln\frac{Q_{\mathrm{n}} + Q_0}{Q_0} \tag{5.7}$$

$$\frac{q(V_{\mathrm{p}} - V_{\mathrm{geff}} - \Delta V)}{kT} = \frac{q}{kT}\frac{Q_{\mathrm{p}}}{C_{\mathrm{ox}}} + \ln\frac{Q_{\mathrm{p}}}{Q_0} + \ln\frac{Q_{\mathrm{p}} + Q_0}{Q_0} \tag{5.8}$$

where $Q_0 = 4(kT/q)(\varepsilon_{\mathrm{si}}/R)$, and $\Delta V = (kT/q)\ln(8/\delta R^2)$.

Now, with given gate voltage and quasi-Fermi potentials, the carrier density Q_{n} and Q_{p} can be solved from (5.7) and (5.8). Then, the surface potential $\phi_{s,0}$ are obtained by substituting the following equation into (5.5):

$$B_{\mathrm{n(p)}} = -\frac{Q_{\mathrm{n(p)}}}{Q_{\mathrm{n(p)}} + Q_0}\frac{1}{R^2} \tag{5.9}$$

Eqs. (5.7) and (5.8) are accurate for calculating the potential and the density of majority carriers, which are important for solving the current. Therefore, they are used as a good approximation for following calculations. In addition, we derive a refined expression to calculate the density of minority carriers, which may be required in an accurate capacitance model. In the case of electrons as minority carriers, we assume $\phi = \phi_{\mathrm{p}}$, thus:

$$Q_{\mathrm{n,min}} \approx \frac{qn_{\mathrm{i}}}{R}\int_0^R r\mathrm{e}^{\frac{q(\phi_{\mathrm{p}} - V_{\mathrm{n}})}{kT}}\,\mathrm{d}r \tag{5.10}$$

This integral is finished by substituting ϕ_{p} in (5.4) into it. Thus, an analytical solution for minority carriers is obtained as:

$$Q_{\mathrm{n,min}} = \frac{q n_{\mathrm{i}} \delta}{48 B_{\mathrm{p}}^2 R} \mathrm{e}^{\frac{q(V_{\mathrm{p}} - V_{\mathrm{n}})}{kT}} \left[1 - (1 + B_{\mathrm{p}} R^2)^3\right] \tag{5.11}$$

Eq. (5.11) shows the relationship between the minority carrier of electrons $Q_{\mathrm{n,min}}$ and the majority carrier of holes (B_p and V_p).

A unified solution valid for all bias conditions is thus given by combining the results for both majority carriers and minority carriers:

$$Q_{\mathrm{n}} = \sigma_1 \cdot Q_{\mathrm{n,maj}} + \sigma_2 \cdot Q_{\mathrm{n,min}} \tag{5.12}$$

where $Q_{\mathrm{n,maj}}$ is the result of (5.7).

The unified expression of hole density Q_{p} can be similarly derived as:

$$Q_{\mathrm{p}} = \sigma_1 \cdot Q_{\mathrm{p,min}} + \sigma_2 \cdot Q_{\mathrm{p,maj}} \tag{5.13}$$

The above analysis solves the long-channel surface potential $\phi_{s,0}$ without considering the boundary conditions at S/D. However, for Schottky-barrier devices, the potential distribution near the contacts is also required to calculate the carrier tunneling through the Schottky barriers. Therefore, we apply a quasi-2-D solution of the surface potential [196, 204].

The boundary condition at source is given by $\phi_s(0) = V_{\mathrm{bi}} + V_{\mathrm{S}}$. Thus, the surface potential near the contact at source is:

$$\begin{aligned} &\phi_s = \phi_{s,0} + \Delta\phi_{s,S}(y) \\ &\Delta\phi_{s,S}(y) = (V_{\mathrm{bi}} + V_{\mathrm{S}} - \phi_{s,0}) \frac{\sinh((L-y)/\lambda)}{\sinh(L/\lambda)} \end{aligned} \tag{5.14}$$

Similarly, the surface potential near the contact at drain is obtained under the boundary condition of $\phi_s(L) = V_{\mathrm{bi}} + V_{\mathrm{D}}$:

$$\begin{aligned} &\phi_s = \phi_{s,0} + \Delta\phi_{s,D}(y) \\ &\Delta\phi_{s,D}(y) = (V_{\mathrm{bi}} + V_{\mathrm{D}} - \phi_{s,0}) \frac{\sinh(y/\lambda)}{\sinh(L/\lambda)} \end{aligned} \tag{5.15}$$

where L is the length of each gate, and $V_{\mathrm{bi}} = \chi + E_g/2q - \Phi_m$ is the built-in potential with χ the electron affinity of silicon and E_g the bandgap of silicon.

In (5.14) and (5.15), the natural length λ can be assumed as a constant here only related to the geometry of the device in the subthreshold region, i.e., $\lambda = \sqrt{\varepsilon_{\mathrm{si}} R / 2 C_{\mathrm{ox}}}$ [204–206]. However, the simple assumption of λ does not perfectly capture the effect of the induced carriers. It can

be addressed by introducing a unified λ [196], but for simplicity, an empirical expression for λ is used instead in this model to approximately account for the effects of induced carriers beyond the subthreshold regime. This bias-dependent correction on λ is expressed as:

$$\lambda = \sqrt{\varepsilon_{\mathrm{si}} R / 2 C_{\mathrm{ox}}} \cdot m_1 \cdot m_2 \tag{5.16}$$

in which the effect of the bias on CG and PG is modeled by:

$$m_1 = \sqrt{a_0 + \frac{1}{V_{\mathrm{DD}}} \frac{kT}{q} \ln\left(1 + \exp\left(\frac{q(a_1 V_{\mathrm{CG}} - a_2 V_{\mathrm{PG}} + a_3)}{kT}\right)\right)} \tag{5.17}$$

And m_2 represents the effect of the drain-source voltage as:

$$m_2 = 1 + b_0 \left(1 - u^{\upsilon}\right) \tag{5.18}$$

with

$$u = 1 - \ln\left(1 + \exp\left(1 - \frac{V_{DS}}{b_1 V_{\mathrm{CG}} - b_2 V_{\mathrm{PG}} + b_3}\right)\right) \tag{5.19}$$

and a_{0-3}, b_{0-3} and υ are fitting parameters.

As demonstrated later in Sec. 5.4, the proposed potential model shows good agreement with the numerical solution, which further contributes to the accurate prediction of the current in different bias configurations.

5.3 Drain Current Model

According to the derived potential model, the potential along the channel can be obtained when the quasi-Fermi potentials V_{p} and V_{n} are known. To obtain V_{p} and V_{n} at each region, the current continuity condition needs to be solved.

Here, we only discuss the $V_{\mathrm{DS}} \geq 0$ case. The results when $V_{\mathrm{DS}} < 0$ is the same as the device is symmetric. Considering that the quasi-Fermi potentials mostly drop at the contacts and the interfaces between gated regions, it is assumed that V_{p} and V_{n} keep constant within each region. They are labeled as $V_{\mathrm{n(p),PG_S}}$, $V_{\mathrm{n(p),CG}}$, and $V_{\mathrm{n(p),PG_D}}$. The surface potentials at each region are also labeled as $\phi_{\mathrm{PG_S}}$, ϕ_{CG}, and $\phi_{\mathrm{PG_D}}$, respectively.

First, we consider the Schottky contacts. Electrons may tunnel through the Schottky barrier from source and holes may tunnel from drain based on certain bias conditions as shown in Fig. 5.3. To avoid the complexity of calculating the tunneling probability, the effective Schottky barrier heights $\Phi_{\mathrm{SBeff,n}}$ and $\Phi_{\mathrm{SBeff,p}}$ are applied based on the assumption of the tunneling distance d_t [199, 207]. The tunneling probability is assumed to be unity if the barrier is thinner than d_t and zero otherwise. By solving (5.14) at $y = d_t$ and (5.15) at $y = L - d_t$, the effective

Schottky barriers are given by:

$$\Phi_{\text{SBeff,n}} = \Phi_{\text{SB,n}} - (\phi_{\text{PG}_\text{S}} - V_{\text{bi}} - V_{\text{S}})(1 - e^{-d_t/\lambda}) \tag{5.20}$$

$$\Phi_{\text{SBeff,p}} = \Phi_{\text{SB,p}} - (V_{\text{bi}} + V_{\text{D}} - \phi_{\text{PG}_\text{D}})(1 - e^{-d_t/\lambda}) \tag{5.21}$$

where $\Phi_{\text{SB,n}} = \Phi_m - \chi$ and $\Phi_{\text{SB,p}} = \chi + E_g/q - \Phi_m$ are the Schottky barrier heights for electrons and holes, respectively. The voltages V_S and V_D are the biases applied to source and drain, respectively.

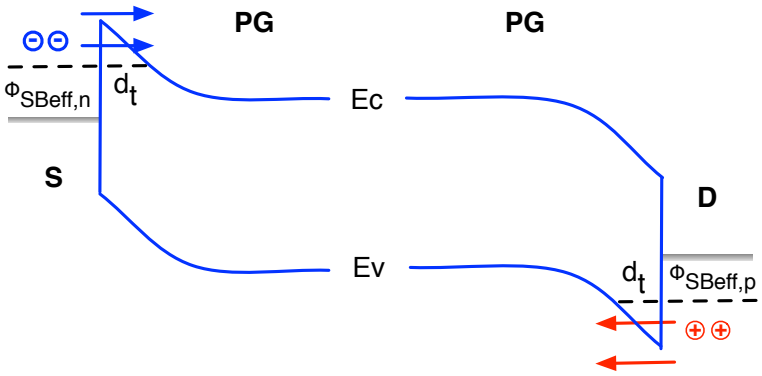


Figure 5.3: Schottky barriers at source and drain under different bias conditions, showing the effective Schottky barrier heights for electrons and holes.

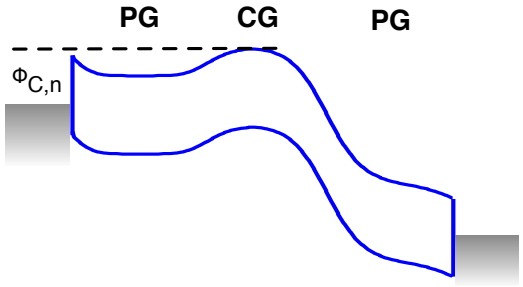


Figure 5.4: Potential barrier induced by CG in the middle of the channel.

In addition to the Schottky barriers, CG may also induce a potential barrier in the middle of the channel as shown in Fig. 5.4 for electrons. This barrier Φ_C can be expressed as:

$$\Phi_{\text{C,n}} = (V_{\text{bi}} + V_{\text{S}} + \phi_{\text{SB,n}}) - \phi_{\text{CG}} \tag{5.22}$$

$$\Phi_{\text{C,p}} = \phi_{\text{CG}} - (V_{\text{bi}} + V_{\text{D}} - \phi_{\text{SB,p}}) \tag{5.23}$$

Finally, the barrier height for carriers to overcome is the largest one between Φ_{SBeff} and Φ_{C}:

$$\Phi_{\text{eff,n}} = \max\left(\Phi_{\text{SBeff,n}}, \Phi_{C,n}\right) \tag{5.24}$$

$$\Phi_{\text{eff,p}} = \max\left(\Phi_{\text{SBeff,p}}, \Phi_{C,p}\right) \tag{5.25}$$

Therefore, the current through this barrier is given by the expression of thermionic emission:

$$I_{\mathrm{T,n(p)}} = \pi R^2 A^*_{\mathrm{n(p)}} T^2 \exp\left(-\frac{q\Phi_{\mathrm{eff,n(p)}}}{kT}\right) \tag{5.26}$$

in which $A^*_{\mathrm{n(p)}}$ is the effective Richardson's constant for electrons (holes).

After coming through the Schottky barriers, the carrier transport in the channel is described by the drift-diffusion model. Therefore, the inner part of the device operates like a conventional single-gate SiNWFET, which uses CG as the gate and PG-controlled regions as doped source and drain.

Based on this assumption, the drift-diffusion current of electrons in the channel can be expressed as [208]:

$$I_{\mathrm{DD,n}} = \mu_{\mathrm{n}} \frac{2\pi R}{L_{\mathrm{eff}}} \int_{PG_S}^{PG_D} Q_n \mathrm{d}V_n \tag{5.27}$$

We can also derive from (5.7) that:

$$\mathrm{d}V_n = -\left(\frac{1}{C_{ox}} + \frac{kT}{q}\frac{1}{Q_n} + \frac{kT}{q}\frac{1}{Q_n + Q_0}\right)\mathrm{d}Q \tag{5.28}$$

By substituting (5.28) into (5.27), the drift-diffusion current of electrons is finally obtained in a similar formula to charge-based model for conventional MOSFETs [195, 209–211]:

$$I_{\mathrm{DD,n}} = \mu_{\mathrm{n}} \frac{2\pi R}{L_{\mathrm{eff}}} \left[G(Q_{\mathrm{n,S}}) - G(Q_{\mathrm{n,D}})\right] \tag{5.29}$$
$$G(Q) = 2\frac{kT}{q}Q + \frac{Q^2}{2C_{\mathrm{ox}}} - \frac{kT}{q}Q_0 \ln\frac{Q_0 + Q}{Q_0}$$

in which $Q_{\mathrm{n,S(D)}}$ is obtained by solving (5.7) with $V_G = V_{\mathrm{CG}}$ and $V_{\mathrm{n}} = V_{\mathrm{n,PG_S}}$ at source or $V_{\mathrm{n}} = V_{\mathrm{n,PG_D}}$ at drain.

Similarly, the drift-diffusion current of holes is obtained as:

$$I_{\mathrm{DD,p}} = \mu_{\mathrm{p}} \frac{2\pi R}{L_{\mathrm{eff}}} \left[G(Q_{\mathrm{p,D}}) - G(Q_{\mathrm{p,S}})\right] \tag{5.30}$$

with $Q_{\mathrm{p,S(D)}}$ obtained by solving (5.8) with $V_G = V_{\mathrm{CG}}$ and $V_{\mathrm{p}} = V_{\mathrm{p,PG_S}}$ at source or $V_{\mathrm{p}} = V_{\mathrm{p,PG_D}}$ at drain.

If the recombination of carriers in the channel is neglected, the current continuity in the device gives that:

$$I_{\mathrm{T,n(p)}} = I_{\mathrm{DD,n(p)}} \tag{5.31}$$

In conventional MOSFETs, the quasi-Fermi potential mostly drops at the drain side because

the body-drain junction is a reverse-biased *p-n* junction. It is similar in the DIG SiNWFET that employs electrostatic doping. Thus, we get:

$$V_{\mathrm{n,CG}} = V_{\mathrm{n,PG_S}} \tag{5.32}$$

$$V_{\mathrm{p,CG}} = V_{\mathrm{p,PG_D}} \tag{5.33}$$

When reaching the other side of the channel, the carriers need to come over the other Schottky barrier under a forward bias. The corresponding current of electrons is thus modeled as [10]:

$$I_{\mathrm{T,n}} = \pi R^2 A_n^* T^2 \exp\left(-\frac{q\Phi_{\mathrm{SB,n}}}{kT}\right)\left(\mathrm{e}^{\frac{q(V_{\mathrm{D}}-V_{\mathrm{n,PG_D}})}{kT}} - 1\right) \tag{5.34}$$

And the current of holes is written as:

$$I_{\mathrm{T,p}} = \pi R^2 A_p^* T^2 \exp\left(-\frac{q\Phi_{\mathrm{SB,p}}}{kT}\right)\left(\mathrm{e}^{\frac{q(V_{\mathrm{p,PG_S}}-V_{\mathrm{S}})}{kT}} - 1\right) \tag{5.35}$$

Combining (5.34), (5.35) and (5.26) yields to:

$$V_{\mathrm{n,PG_D}} = V_{\mathrm{D}} - \frac{kT}{q}\ln\left[1+\exp\left(\frac{q(\Phi_{\mathrm{SB,n}}-\Phi_{\mathrm{eff,n}})}{kT}\right)\right] \tag{5.36}$$

$$V_{\mathrm{p,PG_S}} = V_{\mathrm{S}} + \frac{kT}{q}\ln\left[1+\exp\left(\frac{q(\Phi_{\mathrm{SB,p}}-\Phi_{\mathrm{eff,p}})}{kT}\right)\right] \tag{5.37}$$

By iteratively solving (5.31), (5.32) with (5.36) for electrons, and (5.31), (5.33) with (5.37) for holes, the distribution of surface potentials along the channel and the currents of both carriers are obtained.

According to the above analysis, the device can be described by three components in series as shown in Fig. 5.5. In the middle of the channel, CG modulates the barrier as in conventional MOSFETs, and PG-controlled regions are considered as doped source and drain. At the contacts, the Schottky barriers together with PG can be considered as back-to-back Schottky diodes with an additional modulation by PG. As a unique structure in polarity-controllable device, PG not only modulates the Schottky barriers, but can also reverse the direction of the diodes, thus changing the polarity of the device.

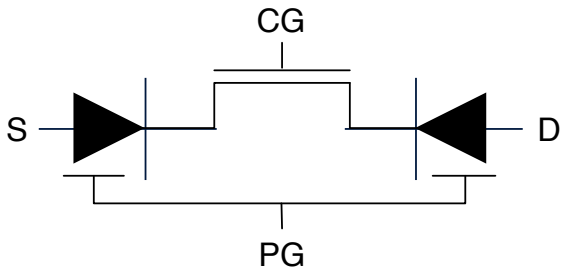


Figure 5.5: Equivalent circuit symbol of the dual-independent-gate SiNWFET.

The different components, i.e., the Schottky barriers and the nanowire channel, are separately modeled by using similar formulas for Schottky diodes and MOSFETs. Therefore, advanced physical effects associated with Schottky barriers and the channel can be easily integrated into the proposed core framework, such as short-channel effects, mobility degradation, velocity saturation, Schottky barrier lowering, etc. [206, 212–217]. A complete and accurate model for DIG SiNWFETs can thus be developed based on the presented core model.

5.4 Results and Discussion

Based on the potential model presented in Sec. 5.2, we obtain the potential in the nanowire with given gate voltage and quasi-Fermi potentials. The model is verified with respect to a numerical solution of Poisson's equation (5.1) using a finite element method. In the demonstrated device, an undoped silicon nanowire with a diameter of 30 nm is used as the channel. The thickness of SiO_2 is 2 nm.

The potential distribution along the radial direction is shown in Fig. 5.6(a). The quasi-Fermi potentials V_n and V_p are set to 0.2 V and 1.0 V, respectively. The potential increases from the center of the nanowire to the surface with $V_{\text{geff}} \geq 0.75V$, which corresponds to a n-type operation. While with $V_{\text{geff}} = 0$, the potential decreases from the center to the surface as a p-type behavior dominated by holes.

The potentials at the surface and the center of the nanowire with different gate voltages are

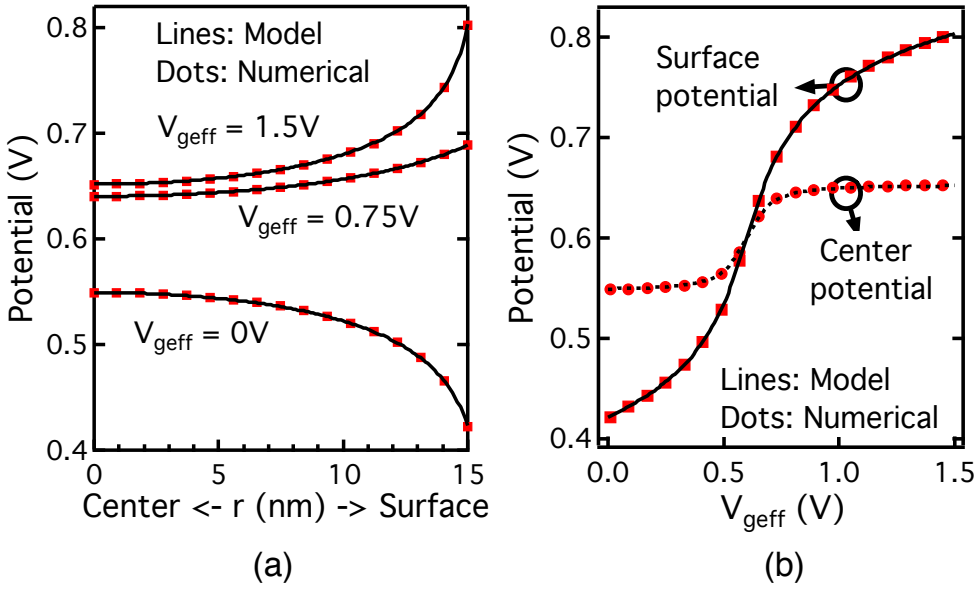


Figure 5.6: (a) Potential distribution along the radial direction in the silicon nanowire. (b) Surface potential and center potential. Quasi-Fermi potentials V_{n} and V_{p} are set to 0.2 V and 1.0 V, respectively.

shown in Fig. 5.6(b). Consistent with the results in Fig. 5.6(a), the surface potential is higher than the center potential with larger V_{geff}, but lower with small V_{geff}. When $V_{\text{geff}} = (V_p + V_n)/2 = 0.6V$, the surface potential is equal to the center potential. As observed from these results, the proposed potential model agrees well with the numerical solution and provides a smooth transition between different gate voltages.

Fig. 5.7 shows the calculated carrier densities with different approximations. Compared to the numerical results, the equations (5.7) and (5.8) are accurate for calculating majority carriers, and can be used to further calculate the current which is mostly composed of majority carriers. Furthermore, the unified solution of (5.12) and (5.13) presents a good match with the numerical results, and thus may be applied in a capacitance model as future work.

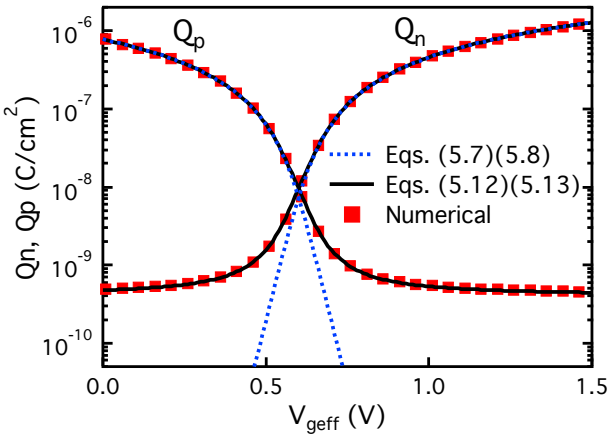


Figure 5.7: Carrier density calculated with the equations for majority carriers (5.7) (5.8) and the unified solution (5.12) (5.13).

In order to further verify the drain current model, a DIG SiNWFET using the geometries in Fig. 5.1 is simulated using Synopsys Sentaurus [120]. In the *Three-Dimensional* (3-D) simulation, the coupled Poisson's equation and drift-diffusion model are self-consistently solved. The length of each gate is set to be 200 nm. The diameter of the nanowire is 30-50 nm. The thickness of SiO_2 is 2 nm. Metal gates with mid-gap workfunction and Schottky barrier contacts with the workfunction of 4.45 eV are applied. WKB approximation is used to calculate the tunneling at Schottky contacts and a constant mobility model is applied in the channel [121].

By solving the continuity equation in the device, the potential distribution and drain current are obtained. The surface potential distribution along the channel for *n*-type configuration is shown in Fig. 5.8 by fixing V_{PG} and V_{DS} at 1.5 V. When increasing V_{CG} to turn *on* the device, not only ϕ_{CG}, but also ϕ_{PG_S} increase due to the change of quasi-Fermi potentials at PG_S-controlled region. Thus, the Schottky barrier at source becomes thinner. More electrons can thus tunnel through the lower barrier, which leads to the increase of current.

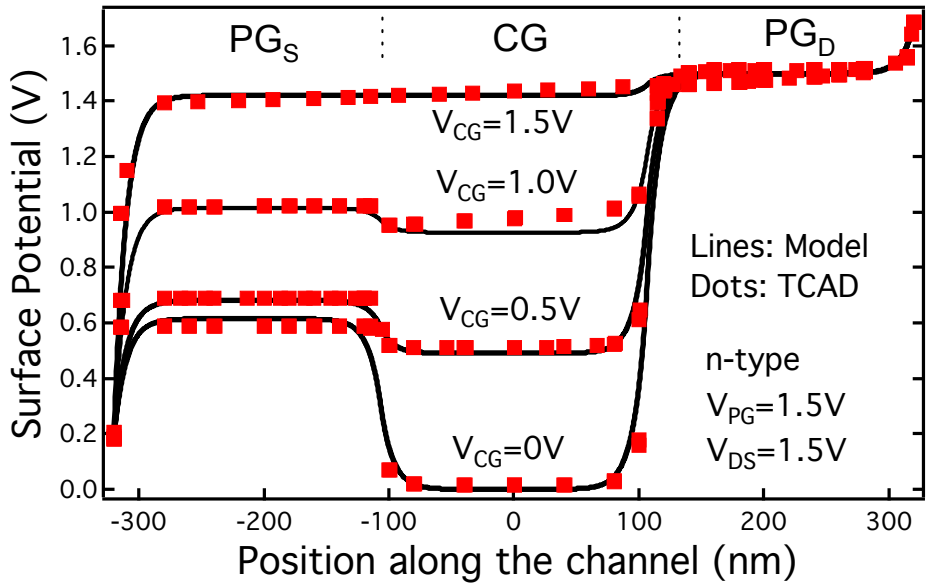


Figure 5.8: Surface potential distribution along the channel with different gate voltages and $V_{PG} = V_{DS} = 1.5V$ (n-type).

The transfer characteristics of DIG SiNWFET with different diameters are compared with TCAD simulation in Fig. 5.9. With a fixed V_{PG}, the device behaves in the deep subthreshold region as a conventional MOSFET. As observed in Fig. 5.9(a), the SS is approaching the ideal

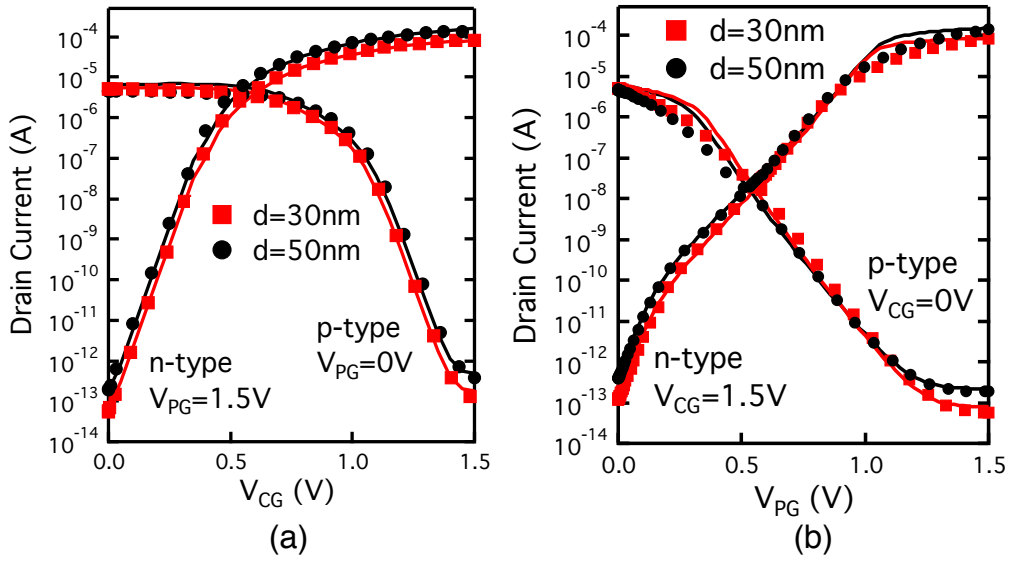


Figure 5.9: The predicted drain current with different nanowire diameters under (a) a fixed V_{PG} and (b) a fixed V_{CG} for both n-type and p-type configurations. $V_{DS} = 1.5V$ (lines: model, dots: TCAD simulation).

value, since the effective barrier height is determined by Φ_C. Beyond this region, the current starts to be dominated by the effective Schottky barrier $\Phi_{SBeff,n}$ or $\Phi_{SBeff,p}$, limiting the SS. On the other hand, the I_{on} of n-type operation is larger than in p-type operation due to the lower Schottky barrier height for electrons, which is determined by the workfunction of the Schottky contacts. Similar to fully-depleted SOI, DIG SiNWFET with larger nanowire diameter shows lower threshold V_{CG}. Note that, the electron current also contributes to the leakage in p-type configuration, resulting in a degraded gate control over the leakage current near $V_{CG} = 1.5V$.

In contrast, when varying V_{PG} while applying a fixed bias on CG, the drain current is determined by the Schottky barriers within the whole subthreshold region. In this case, the SS is worse than varying V_{CG} as shown in Fig. 5.9(b). However, in the deep subthreshold region of n-type characteristics, $\phi_{PG_S} < V_{bi} + V_S$ in the simulated device. Thus, the effective barrier height is determined by ϕ_{PG_S}. This effect is included in the model by replacing ϕ_{CG} by $\min[\phi_{CG}, \phi_{PG_S}]$ in (5.22). The resulted different regimes of SS in n-type configuration can also be observed in Fig. 5.9(b). Moreover, the nanowire diameter shows negligible effects on the characteristics when the carrier transport is dominated by tunneling through the Schottky barriers. Slight difference between the prediction and TCAD simulation is also observed when the device completely turns *on* because of the simple expression of λ used in the model.

If PG and CG are connected together, the device works as a single-gate Schottky-barrier MOSFET. The resulted ambipolar characteristics are shown in Fig. 5.10. While Schottky-barrier devices are appealing because they do not require chemical doping, they also suffer from low I_{on}/I_{off} ratio with poor subthreshold slope due to the ambipolar behavior. In contrast, polarity-controllable devices utilize the ambipolar conduction of both carriers, and further exploit electrostatic control of the Schottky barriers with an additional gate to achieve high I_{on}/I_{off} ratio as well as near-ideal subthreshold slope [72].

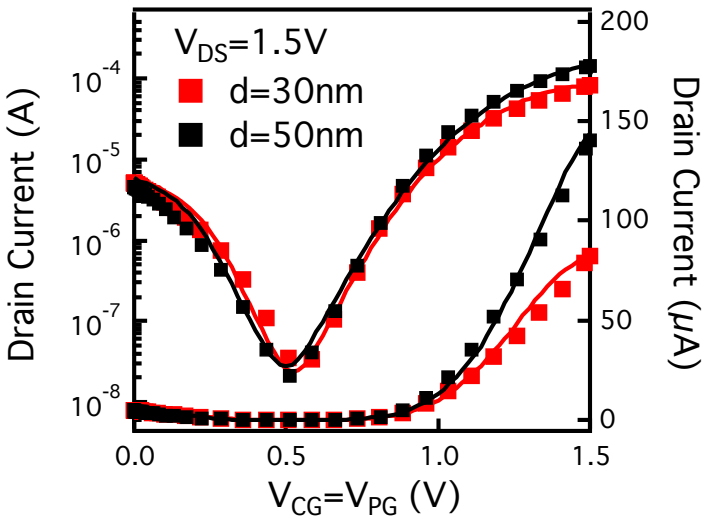


Figure 5.10: Ambipolar characteristics by applying the same V_{CG} and V_{PG} in DIG SiNWFET (lines: model, dots: TCAD simulation).

Fig. 5.11 shows the output characteristics with a fixed $V_{PG} = 1.5V$ in n-type configuration. The current saturation is observed with large V_{DS}. On the other hand, we also observe the resistance due to the existence of the Schottky barriers with V_{DS} near 0 V. Despite that, the characteristics with $V_{CG} = 1V$ and $V_{CG} = 1.5V$ shows similar resistance. This implies that the biased PG helps to reduce the resistance by improving the tunneling through the Schottky barrier.

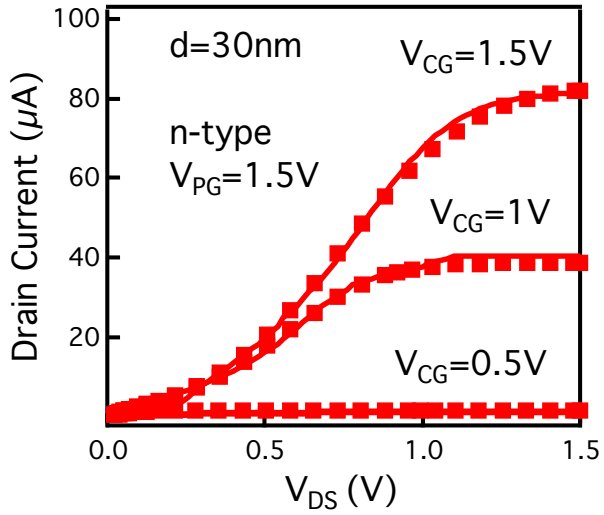


Figure 5.11: Output characteristics with a fixed V_{PG} (lines: model, dots: TCAD simulation).

Finally, we discuss a little about the capacitance model for DIG SiNWFET. With the derived carrier density equation, the total charge in each region Q_{CG}, Q_{PG_S} and Q_{PG_D} can be calculated by integrating the carrier density along the channel. Then, the partition of these charges to source and drain terminals can be investigated by TCAD simulation. The simulation result shows that Q_{PG_S} mostly contributes to the capacitance between PG_S and source, and Q_{PG_D} mostly contributes to the capacitance between PG_D and drain. Q_{CG} needs a similar partition to source and drain as in the capacitance model of conventional MOSFETs [218]. The capacitance model for DIG SiNWFET can thus be developed based on these assumptions.

5.5 Chapter Summary

This chapter presents a surface potential and current model for dual-independent-gate SiNWFETs. By solving both carrier tunneling at Schottky contacts and the drift-diffusion in the channel, the potential distribution and drain current are obtained. The proposed model captures the operation of the device under different bias configurations, and shows good agreements with TCAD simulation. A complete and more accurate model can be built based on the presented core framework, and used for the exploration of the functionality-enhanced device with controllable polarity.

6 Conclusions and Future Work

Functionality-enhanced devices are desirable to improve the computing efficiency when the size of CMOS transistors approaches the material limit. In addition, low power consumption is a critical challenge due to the dramatically increased device density on the chip. From this perspective, this thesis exploits a new device concept: multiple-independent-gate field-effect transistors. The functionality-enhanced devices provide high computational density thanks to the polarity controllability. In the meantime, the proposed technology can also reduce the power consumption with the dual-threshold-voltage characteristics and the steep-subthreshold-slope operation.

The proposed device concept is applied to different channel geometries, including SiNWFET and FinFET. These devices are extensively studied on fabrication, dual-V_T characteristics and design, steep-SS operation, and compact modeling. In the following section, a summary of contributions in each chapter is highlighted. Then, possible future works are discussed.

6.1 Summary of Contributions

Chapter 1 discusses the current limitations of CMOS technology, and gives the global objective of this thesis.

Chapter 2 introduces functionality-enhanced devices with controllable polarity based on different channel materials and structures. Then, multiple-independent-gate FETs are proposed. The device structure exploits both silicon nanowire channel and fin-shaped channel. With multiple independent gates, the proposed devices achieve independent modulation of the carrier transport at Schottky barriers and the channel conduction. The fabrication of the devices in a top-down approach is also demonstrated step by step, which is suitable for large-scale integration.

Chapter 3 exploits multiple-independent-gate FETs for multi-V_T design. Dual-V_T characteristics are demonstrated with TIG SiNWFET. The uniqueness of the proposed device lays in the high degree of configurability. This device is configured as *n*-type or *p*-type transistor in

either high-V_T or low-V_T mode by biasing separately the three independent gates. Low-V_T configuration with earlier turn-*on* is helpful for improving the circuit speed, while high-V_T configuration achieves a suppression of leakage current without sacrificing the *on*-state current, showing advantages over the conventional multi-V_T techniques. Chapter 3 also presents an efficient approach to implement dual-V_T configurable circuits with TIG SiNWFETs. Logic gates using these devices can be realized to either fit high performance or low leakage applications, simply by wiring an uncommitted gate structure. Dual-V_T design is thus achievable without additional process steps by applying this strategy. This property not only increases the configurability of the circuits, but also reduces the process complexity compared to dual-V_T technologies for conventional CMOS.

Chapter 4 extends the multiple-independent-gate FETs to achieve a steep-SS operation. The steep SS is demonstrated by exploiting the electrostatic biasing of the Schottky barriers in DIG FinFETs. The measured characteristics show minimal SS of 3.4 mV/dec and average SS of 6 mV/dec over 5 decades of current with ultra-low leakage floor and high I_{on}/I_{off} ratio at room temperature. Temperature-dependent characterization indicates that the steep SS has reduced sensitivity to temperature as compared to conventional MOSFETs. The devices also show negligible hysteresis and good reliability. Chapter 4 further analyzed the epitomized SS in the formula and suggested feasible improvements to optimize the device performance and reduce the operation voltage.

Chapter 5 presents compact modeling of multiple-independent-gate FETs. A surface potential and current model is developed for DIG SiNWFETs. The potential distribution and drain current are calculated based on both carrier tunneling at Schottky contacts and the drift-diffusion in the channel. The proposed model captures the operation of the device under different bias configurations, and shows good agreements with TCAD simulation. A complete and more accurate model can be built based on the presented core framework, and be used for the exploration of the functionality-enhanced device with controllable polarity.

6.2 Future Work

This section highlights the future research directions in development of technology and *Electronic Design Automation* (EDA) with the multiple-independent-gate FETs.

There are many challenges in the fabrication of multiple-independent-gate FETs. Limited by our academic cleanroom facility, the devices experimentally demonstrated in the thesis have relatively long gate length (100~200 nm) and thick oxide (10~15 nm) compared to state-of-the-art MOSFETs. Therefore, process optimization is expected to improve the performance of multiple-independent-gate FETs at advanced technology nodes.

Besides the process optimization, the high Schottky barrier height in the devices also limits the *on*-state current of devices, and the circuit speed is consequently limited. Moreover, the steep-SS operation is also suppressed at low operation voltage due to the large threshold

energy for impact ionization in silicon. To overcome these issues, a solution consists of using semiconductors with narrower band gap, like germanium. Nevertheless, lower barrier height can also result in larger leakage current and degraded I_{on}/I_{off} ratio. Therefore, the fabrication process of germanium-based multiple-independent-gate FETs and the possible performance improvement require more investigation in both experiments and theory in the future.

On the other hand, symmetric *n*-type and *p*-type characteristics of the device are desired to yield energy efficient circuits with a single type of transistor [89]. Recently, the strain technology has been investigated to achieve this symmetry by tuning the tunneling through the barrier [115, 186]. The effect of strain deserves further study as a very attractive technique for performance optimization of the multiple-independent-gate FETs.

In the physical design with multiple-independent-gate FETs, an optimal mapping scheme yields to the fine-grained tuning at transistor level for each circuit as presented in Chapter 3. With the mapping result, direct routing on the prefabricated devices is desired. However, a single TIG SiNWFET has 5 terminals in a compact area. Thus, routing on these devices is challenging. To mitigate routing efforts, a regular layout technique called sea-of-tiles could be applied to multiple-independent-gate FETs, which has shown the potential on routing and area utilization with DIG SiNWFETs [137].

Finally, state-of-the-art logic synthesis tools are efficient for unate logic functions. In contrast, multiple-independent-gate FETs are efficient at implementing both unate and binate logic functions. Hence, new logic synthesis tools exploiting a large class of functions are desired to design highly efficient circuits with multiple-independent-gate FETs [54, 143, 144].

In conclusion, multiple-independent-gate field-effect transistors enable attractive opportunities in design of integrated circuits with high computational density and low power consumption. The work presented in this thesis also brings interesting opportunities from device technology to EDA. It will be exciting to see how this new technology performs with future advancement in research and engineering on related topics.

A List of Abbreviations

Abbreviation	Definition
1-D	One-Dimensional
2-D	Two-Dimensional
3-D	Three-Dimensional
ABB	Adaptive Body Biasing
ASIC	Application-Specific Integrated Circuit
BOX	Buried Oxide
BP	Back Plane
BTBT	Band-To-Band Tunneling
CG	Control Gate
CMOS	Complementary Metal-Oxide-Semiconductor
DFF	D-Flip-Flop
DG	Double-Gate
DIBL	Drain-Induced-Barrier-Lowering
DIG	Dual-Independent-Gate
DRIE	Deep Reactive Ion Etching
EDA	Electronic Design Automation
EI	Electrostatic Integrity
FBB	Forward Body Bias
FD	Fully-Depleted
FE	Field Emission

Abbreviation	Definition
FET	Field-Effect Transistor
FPGA	Field-Programmable Gate Array
G	Gate
GAA	Gate-All-Around
HP	High Performance
HVT	High-V_T
IC	Integrated Circuits
IMOS	Impact-Ionization MOS
LL	Low Leakage
LSTP	Low-Standby-Power
LVT	Low-V_T
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NC-FET	Negative-Capacitance FET
NEMFET	Nanoelectromechanical FET
NMOS	N-type Metal-Oxide-Semiconductor
PD	Partially-Depleted
PDN	Pull-Down Network
PG	Polarity Gate
PG_S	Polarity Gate at Source
PG_D	Polarity Gate at Drain
PMOS	P-type Metal-Oxide-Semiconductor
PTM	Predictive Technology Model
PUN	Pull-Up Network
RBB	Reverse Body Bias
SBB	Schottky Barrier Bias
SB-FET	Schottky-Barrier Field-Effect Transistor
SCE	Short Channel Effects
S/D	Source and Drain

Abbreviation	Definition
SEM	Scanning Electron Microscopy
SiNWFET	Silicon Nanowire Field-Effect Transistor
SOI	Silicon-On-Insulator
SS	Subthreshold Slope
TCAD	Technology-Computer-Aided-Design
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TFE	Thermionic-Field Emission
TFET	Tunnel FET
TIG	Three-Independent-Gate
TSPC	True-Single-Phase-Clock
UTBB	Ultra Thin Body and Buried Oxide
V_T	Threshold Voltage
VTR	Verilog-To-Routing
WKB	Wentzel-Kramers-Brilloui

Bibliography

[1] A. W. Burks, "Electronic computing circuits of the ENIAC," *Proceedings of the IRE*, vol. 35, no. 8, pp. 756–767, 1947.

[2] J. Bardeen and W. H. Brattain, "The transistor, a semi-conductor triode," *Physical Review*, vol. 74, no. 2, p. 230, 1948.

[3] W. Shockley, "The theory of p-n junctions in semiconductors and p-n junction transistors," *Bell System Technical Journal*, vol. 28, no. 3, pp. 435–489, 1949.

[4] K. Dawon, "Electric field controlled semiconductor device," Aug. 27 1963. US Patent 3,102,230.

[5] J. Kilby, "Invention of the integrated circuit," *Electron Devices, IEEE Transactions on*, vol. 23, pp. 648–654, Jul 1976.

[6] "Introducing the Intel Compute Stick." http://www.intel.com/content/www/us/en/compute-stick/intel-compute-stick.html. [Online; accessed 04-Oct-2015].

[7] R. Dennard, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *Solid-State Circuits, IEEE Journal of*, vol. 9, pp. 256–268, Oct 1974.

[8] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, pp. 114–117, April 1965.

[9] ""More-than-Moore" white paper." http://www.itrs.net/papers.html. [Online; accessed 25-August-2015].

[10] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John Wiley & Sons, 2006.

[11] M. Bohr, "The invention of uniaxial strained silicon transistors at Intel," *Intel Corporation*, 2007.

[12] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *Journal of Applied Physics*, vol. 80, no. 4, pp. 2234–2252, 1996.

[13] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber, and M. Bohr, "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 μm^2 SRAM cell," in *Electron Devices Meeting, 2002. IEDM '02. International*, pp. 61–64, Dec 2002.

[14] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors," in *VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on*, pp. 174–175, June 2000.

[15] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mcintyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pp. 247–250, Dec 2007.

[16] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of high-κ gate dielectric materials on metal and silicon gate workfunctions," *Electron Device Letters, IEEE*, vol. 23, pp. 342–344, June 2002.

[17] Y. Taur, C. Wann, and D. Frank, "25 nm CMOS design considerations," in *Electron Devices Meeting, 1998. IEDM '98. Technical Digest., International*, pp. 789–792, Dec 1998.

[18] R. Kotlyar, M. Giles, P. Matagne, B. Obradovic, L. Shifren, M. Stettler, and E. Wang, "Inversion mobility and gate leakage in high-k/metal gate MOSFETs," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, pp. 391–394, Dec 2004.

[19] H. Iwai, "Roadmap for 22nm and beyond," *Microelectronic Engineering*, vol. 86, no. 7, pp. 1520–1528, 2009.

[20] F.-L. Yang, J.-R. Hwang, and Y. Li, "Electrical characteristic fluctuations in sub-45nm CMOS devices," in *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE*, pp. 691–694, Sept 2006.

[21] K. Mistry, T. Ghani, M. Armstrong, S. Tyagi, P. Packan, S. Thompson, S. Yu, and M. Bohr, "Scalability revisited: 100 nm PD-SOI transistors and implications for 50 nm devices,"

in *VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on*, pp. 204–205, June 2000.

[22] M. Pelella and J. Fossum, "On the performance advantage of PD/SOI CMOS with floating bodies," *Electron Devices, IEEE Transactions on*, vol. 49, pp. 96–104, Jan 2002.

[23] V. Trivedi and J. Fossum, "Nanoscale FD/SOI CMOS: thick or thin BOX?," *Electron Device Letters, IEEE*, vol. 26, pp. 26–28, Jan 2005.

[24] D. Hisamoto, "FD/DG-SOI MOSFET-a viable approach to overcoming the device scaling limit," in *Electron Devices Meeting, 2001. IEDM '01. Technical Digest. International*, pp. 19.3.1–19.3.4, Dec 2001.

[25] M. Fujiwara, T. Morooka, N. Yasutake, K. Ohuchi, N. Aoki, H. Tanimoto, M. Kondo, K. Miyano, S. Inaba, K. Ishimaru, and H. Ishiuchi, "Impact of BOX scaling on 30 nm gate length FD SOI MOSFET," in *SOI Conference, 2005. Proceedings. 2005 IEEE International*, pp. 180–182, Oct 2005.

[26] J.-P. Noel, O. Thomas, M. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, F. Andrieu, M. Vinet, O. Rozeau, F. Boeuf, O. Faynot, and A. Amara, "Multi-V_t UTBB FDSOI device architectures for low-power CMOS circuit," *Electron Devices, IEEE Transactions on*, vol. 58, pp. 2473–2482, Aug 2011.

[27] L. Grenouillet, M. Vinet, J. Gimbert, B. Giraud, J. Noel, Q. Liu, P. Khare, M. Jaud, Y. Le Tiec, R. Wacquez, T. Levin, P. Rivallin, S. Holmes, S. Liu, K. Chen, O. Rozeau, P. Scheiblin, E. Mclellan, M. Malley, J. Guilford, A. Upham, R. Johnson, M. Hargrove, T. Hook, S. Schmitz, S. Mehta, J. Kuss, N. Loubet, S. Teehan, M. Terrizzi, S. Ponoth, K. Cheng, T. Nagumo, A. Khakifirooz, F. Monsieur, P. Kulkarni, R. Conte, J. Demarest, O. Faynot, W. Kleemeier, S. Luning, and B. Doris, "UTBB FDSOI transistors with dual STI for a multi-Vt strategy at 20nm node and below," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, pp. 3.6.1–3.6.4, Dec 2012.

[28] L. Grenouillet, Q. Liu, R. Wacquez, P. Morin, N. Loubet, D. Cooper, A. Pofelski, W. Weng, F. Bauman, M. Gribelyuk, Y. Wang, B. De Salvo, J. Gimbert, K. Cheng, Y. Le Tiec, D. Chanemougame, E. Augendre, S. Maitrejean, A. Khakifirooz, J. Kuss, R. Schulz, C. Janicki, B. Lherron, S. Guillaumet, O. Rozeau, F. Chafik, J. Bataillon, T. Wu, W. Kleemeier, M. Celik, O. Faynot, R. Sampson, B. Doris, and M. Vinet, "UTBB FDSOI scaling enablers for the 10nm node," in *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2013 IEEE*, pp. 1–2, Oct 2013.

[29] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *Electron Devices, IEEE Transactions on*, vol. 47, pp. 2320–2325, Dec 2000.

[30] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," in *Electron Devices Meeting, 2002. IEDM '02. International*, pp. 251–254, Dec 2002.

[31] H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, and M. Meyyappan, "Single crystal nanowire vertical surround-gate field-effect transistor," *Nano Letters*, vol. 4, no. 7, pp. 1247–1252, 2004.

[32] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano letters*, vol. 3, no. 2, pp. 149–152, 2003.

[33] S. Bangsaruntip, G. Cohen, A. Majumdar, Y. Zhang, S. Engelmann, N. Fuller, L. Gignac, S. Mittal, J. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. Frank, and J. Sleight, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, pp. 1–4, Dec 2009.

[34] R.-H. Yan, A. Ourmazd, and K. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *Electron Devices, IEEE Transactions on*, vol. 39, pp. 1704–1710, Jul 1992.

[35] J. Colinge, "Novel gate concepts for MOS devices," in *Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of the 34th European*, pp. 45–49, Sept 2004.

[36] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. Mcintyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *VLSI Technology (VLSIT), 2012 Symposium on*, pp. 131–132, June 2012.

[37] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, and K. Zhang, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 3.7.1–3.7.3, Dec 2014.

[38] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, C. Park, J.-B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, "High performance 5nm radius twin silicon nanowire MOSFET (TSNWFET) : fabrication on bulk Si wafer, characteristics, and reliability," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 717–720, Dec 2005.

[39] W. Lu, P. Xie, and C. M. Lieber, "Nanowire transistor performance limits and applications," *Electron Devices, IEEE Transactions on*, vol. 55, no. 11, pp. 2859–2876, 2008.

[40] C. O. Chui, H. Kim, D. Chi, B. Triplett, P. McIntyre, and K. Saraswat, "A sub-400°C germanium MOSFET technology with high-κ dielectric and metal gate," in *Electron Devices Meeting, 2002. IEDM '02. International*, pp. 437–440, Dec 2002.

[41] J. A. Del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.

[42] F. Schwierz, "Graphene transistors," *Nature nanotechnology*, vol. 5, no. 7, pp. 487–496, 2010.

[43] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *nature*, vol. 424, no. 6949, pp. 654–657, 2003.

[44] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature nanotechnology*, vol. 6, no. 3, pp. 147–150, 2011.

[45] D. Nikonov and I. Young, "Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits," *Exploratory Solid-State Computational Devices and Circuits, IEEE Journal on*, vol. 1, pp. 3–11, Dec 2015.

[46] I. L. Markov, "Limits on fundamental limits to computation," *Nature*, vol. 512, no. 7513, pp. 147–154, 2014.

[47] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling-a gedanken model," *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1934–1939, 2003.

[48] S. Wolf, D. Awschalom, R. Buhrman, J. Daughton, S. Von Molnar, M. Roukes, A. Y. Chtchelkanova, and D. Treger, "Spintronics: a spin-based electronics vision for the future," *Science*, vol. 294, no. 5546, pp. 1488–1495, 2001.

[49] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-κ gate dielectric," *Electron Devices, IEEE Transactions on*, vol. 54, no. 7, pp. 1725–1733, 2007.

[50] D. L. Klein, R. Roth, A. K. Lim, A. P. Alivisatos, and P. L. McEuen, "A single-electron transistor made from a cadmium selenide nanocrystal," *Nature*, vol. 389, no. 6652, pp. 699–701, 1997.

[51] M. Dragoman, A. Takacs, A. Muller, H. Hartnagel, R. Plana, K. Grenier, and D. Dubuc, "Nanoelectromechanical switches based on carbon nanotubes for microwave and millimeter waves," *Applied physics letters*, vol. 90, no. 11, p. 113102, 2007.

[52] K. Gopalakrishnan, P. Griffin, and J. Plummer, "I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q," in *Electron Devices Meeting, 2002. IEDM '02. International*, pp. 289–292, Dec 2002.

[53] A. Chen, "Emerging research device roadmap and perspectives," in *IC Design Technology (ICICDT), 2014 IEEE International Conference on*, pp. 1–4, May 2014.

[54] L. Amaru, P.-E. Gaillardon, and G. De Micheli, "MIXSyn: An efficient logic synthesis methodology for mixed XOR-AND/OR dominated circuits," in *Design Automation Conference (ASP-DAC), 2013 18th Asia and South Pacific*, pp. 133–138, Jan 2013.

[55] S.-C. Fang, J.-M. Wang, and W.-S. Feng, "A new direct design for three-input XOR function on the transistor level," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 43, pp. 343–348, Apr 1996.

[56] K.-H. Cheng and C.-S. Huang, "The novel efficient design of XOR/XNOR function for adder applications," in *Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on*, vol. 1, pp. 29–32 vol.1, 1999.

[57] B. Al-Hashimi, *System-on-Chip: Next Generation Electronics*. Institution of Engineering and Technology, 2006.

[58] "Predictive technology model (ptm)." http://ptm.asu.edu/. [Online; accessed 25-August-2015].

[59] M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi, *Low power methodology manual: for system-on-chip design*. Springer, 2007.

[60] P. R. Panda, B. Silpa, A. Shrivastava, and K. Gummidipudi, *Power-efficient system design*. Springer, 2010.

[61] K. Cheung, "On the 60 mV/dec @300 K limit for MOSFET subthreshold swing," in *VLSI Technology Systems and Applications (VLSI-TSA), 2010 International Symposium on*, pp. 72–73, April 2010.

[62] Y. Nishi, "Insulated gate field effect transistor and its manufacturing method," *Japan Patent*, vol. 587, no. 527, pp. 162–165, 1970.

[63] M. Lepselter and S. Sze, "SB-IGFET: An insulated-gate field-effect transistor using Schottky barrier contacts for source and drain," *Proceedings of the IEEE*, vol. 56, pp. 1400–1402, Aug 1968.

[64] M. Fritze, C. Chen, S. Calawa, D. Yost, B. Wheeler, P. Wyatt, C. Keast, J. Snyder, and J. Larson, "High-speed Schottky-barrier pMOSFET with fT=280 GHz," *Electron Device Letters, IEEE*, vol. 25, pp. 220–222, April 2004.

[65] D. Pearman, *Electrical Characterisation and Modelling of Schottky barrier metal source/drain MOSFETs*. PhD thesis, The University of Warwick, 2007.

[66] L. E. Calvet, *Electrical Transport in Schottky barrier MOSFETs*. PhD thesis, Yale University, 2001.

[67] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida, and J. Koga, "Solution for high-performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique," in *VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 168–169, June 2004.

[68] H.-C. Lin, M.-F. Wang, F.-J. Hou, H.-N. Lin, C.-Y. Lu, J.-T. Liu, and T.-Y. Huang, "High-performance p-channel Schottky-barrier SOI FinFET featuring self-aligned PtSi source/drain and electrical junctions," *Electron Device Letters, IEEE*, vol. 24, pp. 102–104, Feb 2003.

[69] B.-Y. Tsui and C.-P. Lin, "A novel 25-nm modified Schottky-barrier FinFET with high performance," *Electron Device Letters, IEEE*, vol. 25, pp. 430–432, June 2004.

[70] B. Liu, X. Gong, G. Han, P. Lim, Y. Tong, Q. Zhou, Y. Yang, N. Daval, C. Veytizou, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "High-performance germanium ω-gate MuGFET with Schottky-barrier nickel germanide source/drain and low-temperature disilane-passivated gate stack," *Electron Device Letters, IEEE*, vol. 33, pp. 1336–1338, Oct 2012.

[71] J. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 1048–1058, May 2006.

[72] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *IEEE International Electron Devices Meeting (IEDM) 2012*, pp. 8.4.1–8.4.4, Dec 2012.

[73] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," *Nano Letters*, vol. 12, no. 1, pp. 119–124, 2012.

[74] S. Sutar, P. Agnihotri, E. Comfort, T. Taniguchi, K. Watanabe, and J. U. Lee, "Reconfigurable pn junction diodes and the photovoltaic effect in exfoliated MoS_2 films," *Applied Physics Letters*, vol. 104, no. 12, p. 122104, 2014.

[75] F. Wessely, T. Krauss, and U. Schwalke, "CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors," *Solid-State Electronics*, vol. 70, pp. 33–38, 2012.

[76] S. Bhaskar and J. Singh, "Process variation immune dopingless dynamically reconfigurable FET," in *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on*, pp. 257–260, June 2015.

[77] S.-M. Koo, Q. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel, "Enhanced channel modulation in dual-gated silicon nanowire transistors," *Nano letters*, vol. 5, no. 12, pp. 2519–2523, 2005.

[78] N. Harada, K. Yagi, S. Sato, and N. Yokoyama, "A polarity-controllable graphene inverter," *Applied Physics Letters*, vol. 96, no. 1, p. 012102, 2010.

[79] Y.-M. Lin, J. Appenzeller, J. Knoch, and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," *Nanotechnology, IEEE Transactions on*, vol. 4, pp. 481–489, Sept 2005.

[80] S. Nakaharai, M. Yamamoto, K. Ueno, Y.-F. Lin, S. Li, and K. Tsukagoshi, "Electrostatically reversible polarity of ambipolar α-$MoTe_2$ transistors," *ACS nano*, vol. 9, no. 6, pp. 5976–5983, 2015.

[81] S. Nakaharai, T. Iijima, S. Ogawa, S. Suzuki, K. Tsukagoshi, S. Sato, and N. Yokoyama, "Electrostatically-reversible polarity of dual-gated graphene transistors with He ion irradiated channel: Toward reconfigurable CMOS applications," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, pp. 4.2.1–4.2.4, Dec 2012.

[82] S. Nakaharai, T. Iijima, S. Ogawa, S.-L. Li, K. Tsukagoshi, S. Sato, and N. Yokoyama, "Electrostatically reversible polarity of dual-gated graphene transistors," *Nanotechnology, IEEE Transactions on*, vol. 13, pp. 1039–1043, Nov 2014.

[83] R. Oxland, S. Chang, X. Li, S. Wang, G. Radhakrishnan, W. Priyantha, M. van Dal, C. Hsieh, G. Vellianitis, G. Doornbos, K. Bhuwalka, B. Duriez, I. Thayne, R. Droopad, M. Passlack, C. Diaz, and Y. Sun, "An ultralow-resistance ultrashallow metallic source/drain contact scheme for III-V NMOS," *Electron Device Letters, IEEE*, vol. 33, pp. 501–503, April 2012.

[84] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study," *Electron Devices, IEEE Transactions on*, vol. 45, pp. 2505–2513, Dec 1998.

[85] G. Leung and C. O. Chui, "Interactions between line edge roughness and random dopant fluctuation in nonplanar field-effect transistor variability," *Electron Devices, IEEE Transactions on*, vol. 60, pp. 3277–3284, Oct 2013.

[86] M. H. Ben Jamaa, D. Atienza, Y. Leblebici, and G. De Micheli, "Programmable logic circuits based on ambipolar CNFET," in *Proceedings of the 45th annual Design Automation Conference*, pp. 339–340, ACM, 2008.

[87] I. O'Connor, J. Liu, D. Navarro, I. Hassoune, S. Burignat, and F. Gaffiot, "Ultra-fine grain reconfigurability using CNTFETs," in *2007 14th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2007)*, pp. 194–197, IEEE, 2007.

[88] S. Bobba, P.-E. Gaillardon, J. Zhang, M. De Marchi, D. Sacchetto, Y. Leblebici, and G. De Micheli, "Process/design co-optimization of regular logic tiles for double-gate silicon nanowire transistors," in *Nanoscale Architectures (NANOARCH), 2012 IEEE/ACM International Symposium on*, pp. 55–60, IEEE, 2012.

[89] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, and W. Weber, "Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors," *Nanotechnology, IEEE Transactions on*, vol. 14, pp. 689–698, July 2015.

[90] J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 61, pp. 2851–2861, Oct 2014.

[91] "Vistec EBPG5000." https://cmi.epfl.ch/ebeam/VistecEBPG5000_introduction.php. [Online; accessed 25-August-2015].

[92] R. Ng, T. Wang, F. Liu, X. Zuo, J. He, and M. Chan, "Vertically stacked silicon nanowire transistors fabricated by inductive plasma etching and stress-limited oxidation," *Electron Device Letters, IEEE*, vol. 30, pp. 520–522, May 2009.

[93] M. De Marchi, D. Sacchetto, J. Zhang, S. Frache, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Top-down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity," *Nanotechnology, IEEE Transactions on*, vol. 13, pp. 1029–1038, Nov 2014.

[94] W. Kern, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," *RCA review*, vol. 31, pp. 187–206, 1970.

[95] W. Kern, "The evolution of silicon wafer cleaning technology," *Journal of the Electrochemical Society*, vol. 137, no. 6, pp. 1887–1892, 1990.

[96] M. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization, Second Edition*. Taylor & Francis, 2002.

[97] J. Zhang, M. De Marchi, P.-E. Gaillardon, and G. De Micheli, "A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 13.4.1–13.4.4, Dec 2014.

[98] Y.-J. Chang and J. Erskine, "Diffusion layers and the Schottky-barrier height in nickel silicide—silicon interfaces," *Physical Review B*, vol. 28, no. 10, p. 5766, 1983.

[99] Q. Zhao, U. Breuer, E. Rije, S. Lenk, and S. Mantl, "Tuning of NiSi/Si schottky barrier heights by sulfur segregation during Ni silicidation," *Applied physics letters*, vol. 86, no. 6, pp. 62108–62108, 2005.

[100] J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-controllable silicon nanowire transistors with dual threshold voltages," *Electron Devices, IEEE Transactions on*, vol. 61, pp. 3654–3660, Nov 2014.

[101] C.-H. Jan, M. Agostinelli, M. Buehler, Z.-P. Chen, S.-J. Choi, G. Curello, H. Deshpande, S. Gannavaram, W. Hafez, U. Jalan, M. Kang, P. Kolar, K. Komeyli, B. Landau, A. Lake, N. Lazo, S.-H. Lee, T. Leo, J. Lin, N. Lindert, S. Ma, L. McGill, C. Meining, A. Paliwal, J. Park, K. Phoa, I. Post, N. Pradhan, M. Prince, A. Rahman, J. Rizk, L. Rockford, G. Sacks, A. Schmitz, H. Tashiro, C. Tsai, P. Vandervoorn, J. Xu, L. Yang, J.-Y. Yeh, J. Yip, K. Zhang, Y. Zhang, and P. Bai, "A 32nm SoC platform technology with 2nd generation high-k/metal

gate transistors optimized for ultra low power, high performance, and high density product applications," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, pp. 1–4, Dec 2009.

[102] T. Skotnicki, J. Hutchby, T.-J. King, H.-S. Wong, and F. Boeuf, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *Circuits and Devices Magazine, IEEE*, vol. 21, pp. 16–26, Jan 2005.

[103] T. Matsukawa, K. Endo, Y. Liu, S. O'uchi, M. Masahara, Y. Ishikawa, H. Yamauchi, J. Tsukada, K. Ishii, K. Sakamoto, and E. Suzuki, "Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application," in *Solid-State Device Research Conference, 2008. ESSDERC 2008. 38th European*, pp. 282–285, Sept 2008.

[104] O. Weber, F. Andrieu, J. Mazurier, M. Casse, X. Garros, C. Leroux, F. Martin, P. Perreau, C. Fenouillet-Beranger, S. Barnola, R. Gassilloud, C. Arvet, O. Thomas, J.-P. Noel, O. Rozeau, M.-A. Jaud, T. Poiroux, D. Lafond, A. Toffoli, F. Allain, C. Tabone, L. Tosti, L. Brevard, P. Lehnen, U. Weber, P. Baumann, O. Boissiere, W. Schwarzenbach, K. Bourdelle, B.-Y. Nguyen, F. Boeuf, T. Skotnicki, and O. Faynot, "Work-function engineering in gate first technology for multi-VT dual-gate FDSOI CMOS on UTBOX," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, pp. 3.4.1–3.4.4, Dec 2010.

[105] J. Tschanz, J. Kao, S. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan, and V. De, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 1396–1402, Nov 2002.

[106] J. Le Coz, P. Flatresse, S. Engels, A. Valentian, M. Belleville, C. Raynaud, D. Croain, and P. Urard, "Comparison of 65nm LP bulk and LP PD-SOI with adaptive power gate body bias for an LDPC codec," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pp. 336–337, Feb 2011.

[107] A. Bonnoit, *Reducing power using body biasing in microprocessors with dynamic voltage/frequency scaling*. PhD thesis, Carnegie Mellon University, 2010.

[108] S. Garg and D. Marculescu, "System-level leakage variability mitigation for MPSoC platforms using body-bias islands," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 20, pp. 2289–2301, Dec 2012.

[109] C. Fenouillet-Beranger, O. Thomas, P. Perreau, J.-P. Noel, A. Bajolet, S. Haendler, L. Tosti, S. Barnola, R. Beneyton, C. Perrot, C. de Buttet, F. Abbate, F. Baron, B. Pernet, Y. Campidelli, L. Pinzelli, P. Gouraud, M. Casse, C. Borowiak, O. Weber, F. Andrieu, S. Denorme, F. Boeuf, O. Faynot, T. Skotnicki, K. Bourdelle, B. Nguyen, and F. Boedt, "Efficient multi-VT FDSOI technology with UTBOX for low power circuit design," in *VLSI Technology (VLSIT), 2010 Symposium on*, pp. 65–66, June 2010.

[110] J. Zhang, P.-E. Gaillardon, and G. De Micheli, "Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs," in *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, pp. 2111–2114, May 2013.

[111] M. Ben-Jamaa, K. Mohanram, and G. De Micheli, "An efficient gate library for ambipolar CNTFET logic," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, pp. 242–255, Feb 2011.

[112] J. Appenzeller, M. Radosavljević, J. Knoch, and P. Avouris, "Tunneling versus thermionic emission in one-dimensional semiconductors," *Physical review letters*, vol. 92, no. 4, p. 048301, 2004.

[113] M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, and S. De Franceschi, "Multifunctional devices and logic gates with undoped silicon nanowires," *Nano letters*, vol. 12, no. 6, pp. 3074–3079, 2012.

[114] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical Review Letters*, vol. 93, no. 19, p. 196805, 2004.

[115] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually active silicon nanowire transistors and circuits with equal electron and hole transport," *Nano letters*, vol. 13, no. 9, pp. 4176–4181, 2013.

[116] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate MOSFETs," in *Electron Devices Meeting, 2000. IEDM '00. Technical Digest. International*, pp. 719–722, Dec 2000.

[117] M. Lundstrom and D. Antoniadis, "Compact models and the physics of nanoscale FETs," *Electron Devices, IEEE Transactions on*, vol. 61, pp. 225–233, Feb 2014.

[118] W. Shangguan, X. Zhou, K. Chandrasekaran, Z. Zhu, S. Rustagi, S. Chiah, and G. H. See, "Surface-potential solution for generic undoped MOSFETs with two gates," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 169–172, Jan 2007.

[119] J. Zhang, L. Zhang, J. He, and M. Chan, "A noncharge-sheet channel potential and drain current model for dynamic-depletion silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Journal of applied physics*, vol. 107, no. 5, p. 054507, 2010.

[120] Synopsys, "Sentaurus device user guide," *Version C-2009.06*.

[121] M. Razavy, *Quantum theory of tunneling*. World Scientific, 2003.

[122] P.-E. Gaillardon, L. G. Amarù, S. Bobba, M. De Marchi, D. Sacchetto, and G. De Micheli, "Nanowire systems: technology and design," *Philosophical Transactions of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, vol. 372, no. 2012, p. 20130102, 2014.

[123] P.-E. Gaillardon, L. Amaru, J. Zhang, and G. De Micheli, "Advanced system on a chip design based on controllable-polarity FETs," in *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014*, pp. 1–6, March 2014.

[124] I. O'Connor, L. Junchen, F. Gaffiot, F. Pregaldiny, C. Lallement, C. Maneux, J. Goguet, S. Fregonese, T. Zimmer, L. Anghel, T.-T. Dang, and R. Leveugle, "CNTFET modeling and reconfigurable logic-circuit design," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, pp. 2365–2379, Nov 2007.

[125] J. Liu, I. O'Connor, D. Navarro, and F. Gaffiot, "Novel CNTFET-based reconfigurable logic gate design," in *Design Automation Conference, 2007. DAC '07. 44th ACM/IEEE*, pp. 276–277, June 2007.

[126] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, and W. Weber, "Elementary aspects for circuit implementation of reconfigurable nanowire transistors," *Electron Device Letters, IEEE*, vol. 35, pp. 141–143, Jan 2014.

[127] A. Zukoski, X. Yang, and K. Mohanram, "Universal logic modules based on double-gate carbon nanotube transistors," in *Design Automation Conference (DAC), 2011 48th ACM/EDAC/IEEE*, pp. 884–889, June 2011.

[128] L. Amaru, P.-E. Gaillardon, J. Zhang, and G. De Micheli, "Power-gated differential logic style based on double-gate controllable-polarity transistors," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 60, pp. 672–676, Oct 2013.

[129] J. Wang, G. Du, and X. Liu, "Invetigation of reconfigurable silicon nanowire Schottky barrier transistors-based logic gate circuits and SRAM cell," in *Silicon Nanoelectronics Workshop (SNW), 2015*, pp. 1–2, June 2015.

[130] M. De Marchi, S. Bobba, M. Ben Jamaa, and G. De Micheli, "Synthesis of regular computational fabrics with ambipolar CNTFET technology," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, pp. 70–73, Dec 2010.

[131] M. De Marchi, M. Haykel Ben Jamaa, and G. De Micheli, "Regular fabric design with ambipolar CNTFETs for FPGA and structured ASIC applications," in *Nanoscale Architectures (NANOARCH), 2010 IEEE/ACM International Symposium on*, pp. 65–70, June 2010.

[132] Y. Ji-Ren, I. Karlsson, and C. Svensson, "A true single-phase-clock dynamic CMOS circuit technique," *Solid-State Circuits, IEEE Journal of*, vol. 22, pp. 899–901, Oct 1987.

[133] M. Krishna, A. Do, K. S. Yeo, C. C. Boon, and W. M. Lim, "Design and analysis of ultra low power true single phase clock CMOS 2/3 prescaler," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 57, pp. 72–82, Jan 2010.

[134] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings," *Solid-State Circuits, IEEE Journal of*, vol. 32, pp. 62–69, Jan 1997.

[135] X. Tang, J. Zhang, P.-E. Gaillardon, and G. De Micheli, "TSPC Flip-Flop circuit design with three-independent-gate silicon nanowire FETs," in *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, pp. 1660–1663, June 2014.

[136] T. Jhaveri, V. Rovner, L. Pileggi, A. J. Strojwas, D. Motiani, V. Kheterpal, K. Y. Tong, T. Hersan, and D. Pandini, "Maximization of layout printability/manufacturability by extreme layout regularity," *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 6, no. 3, pp. 031011–031011, 2007.

[137] S. Bobba, M. De Marchi, Y. Leblebici, and G. De Micheli, "Physical synthesis onto a Sea-of-Tiles with double-gate silicon nanowire transistors," in *Proceedings of the 49th Annual Design Automation Conference*, pp. 42–47, ACM, 2012.

[138] Z. Zhang, Z. Qiu, R. Liu, M. Ostling, and S.-L. Zhang, "Schottky-barrier height tuning by means of ion implantation into preformed silicide films followed by drive-in anneal," *Electron Device Letters, IEEE*, vol. 28, no. 7, pp. 565–568, 2007.

[139] W.-Y. Loh, P. Hung, B. Coss, P. Kalra, I. Ok, G. Smith, C.-Y. Kang, S.-H. Lee, J. Oh, B. Sassman, P. Majhi, P. Kirsch, H. Tseng, and R. Jammy, "Selective phase modulation of NiSi using N-ion implantation for high performance dopant-segregated source/drain n-channel MOSFETs," in *VLSI Technology, 2009 Symposium on*, pp. 100–101, June 2009.

[140] T. Sakurai and A. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *Solid-State Circuits, IEEE Journal of*, vol. 25, pp. 584–594, Apr 1990.

[141] F. Brglez, D. Bryan, and K. Kozminski, "Combinational profiles of sequential benchmark circuits," in *Circuits and Systems, 1989., IEEE International Symposium on*, pp. 1929–1934 vol.3, May 1989.

[142] J. Rose, J. Luu, C. W. Yu, O. Densmore, J. Goeders, A. Somerville, K. B. Kent, P. Jamieson, and J. Anderson, "The VTR project: architecture and CAD for FPGAs from verilog to routing," in *Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, pp. 77–86, ACM, 2012.

[143] L. Amaru, P.-E. Gaillardon, and G. De Micheli, "Biconditional BDD: A novel canonical BDD for logic synthesis targeting XOR-rich circuits," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2013*, pp. 1014–1017, March 2013.

[144] L. Amaru, P.-E. Gaillardon, and G. De Micheli, "Majority-inverter graph: A novel data-structure and algorithms for efficient logic optimization," in *Design Automation Conference (DAC), 2014 51st ACM/EDAC/IEEE*, pp. 1–6, June 2014.

[145] C. Zener, "A theory of the electrical breakdown of solid dielectrics," *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, pp. 523–529, 1934.

[146] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.

[147] K. Tomioka, M. Yoshimura, E. Nakai, F. Ishizaka, and T. Fukui, "Integration of III-V nanowires on Si: From high-performance vertical FET to steep-slope switch," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, pp. 4.1.1–4.1.4, Dec 2013.

[148] Q. Huang, R. Huang, C. Wu, H. Zhu, C. Chen, J. Wang, L. Guo, R. Wang, Y. Le, and Y. Wang, "Comprehensive performance re-assessment of TFETs with a novel design by gate and source engineering from device/circuit perspective," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 13.3.1–13.3.4, Dec 2014.

[149] H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides," *Electron Devices, IEEE Transactions on*, vol. 58, pp. 2990–2995, Sept 2011.

[150] J. Knoch and J. Appenzeller, "A novel concept for field-effect transistors - the tunneling carbon nanotube FET," in *Device Research Conference Digest, 2005. DRC '05. 63rd*, vol. 1, pp. 153–156, June 2005.

[151] G. Jiao, Z. Chen, H. Yu, X. Huang, D. Huang, N. Singh, G. Lo, D. Kwong, and M.-F. Li, "New degradation mechanisms and reliability performance in tunneling field effect transistors," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, pp. 1–4, Dec 2009.

[152] Y. Qiu, R. Wang, Q. Huang, and R. Huang, "A comparative study on the impacts of interface traps on tunneling FET and MOSFET," *Electron Devices, IEEE Transactions on*, vol. 61, pp. 1284–1291, May 2014.

[153] K. Gopalakrishnan, P. Griffin, and J. Plummer, "Impact ionization MOS (I-MOS)-Part I: device and circuit simulations," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 69–76, Jan 2005.

[154] K. Gopalakrishnan, R. Woo, C. Jungemann, P. Griffin, and J. Plummer, "Impact ionization MOS (I-MOS)-Part II: experimental results," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 77–84, Jan 2005.

[155] E.-H. Toh, G. H. Wang, M. Zhu, C. Shen, L. Chan, G.-Q. Lo, C.-H. Tung, D. Sylvester, C.-H. Heng, G. Samudra, and Y.-C. Yeo, "Impact ionization nanowire transistor with multiple-gates, silicon-germanium impact ionization region, and sub-5 mV/decade subtheshold swing," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pp. 195–198, Dec 2007.

[156] C. Onal, R. Woo, H.-Y. Koh, P. B. Griffin, and J. D. Plummer, "A novel depletion-IMOS (DIMOS) device with improved reliability and reduced operating voltage," *Electron Device Letters, IEEE*, vol. 30, pp. 64–67, Jan 2009.

[157] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T.-J. K. Liu, "Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–4, Dec 2008.

[158] J. Wan, S. Cristoloveanu, C. Le Royer, and A. Zaslavsky, "A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection," *Solid-State Electronics*, vol. 76, pp. 109–111, 2012.

[159] H. Kam, D. Lee, R. Howe, and T.-J. King, "A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 463–466, Dec 2005.

[160] J.-H. Kim, Z. C. Chen, S. Kwon, and J. Xiang, "Three-terminal nanoelectromechanical field effect transistor with abrupt subthreshold slope," *Nano Letters*, vol. 14, no. 3, pp. 1687–1691, 2014.

[161] N. Abele, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. Ionescu, "Suspended-gate MOSFET: bringing new MEMS functionality into solid-state MOS transistor," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 479–481, Dec 2005.

[162] R. Maboudian and R. T. Howe, "Critical review: adhesion in surface micromechanical structures," *Journal of Vacuum Science & Technology B*, vol. 15, no. 1, pp. 1–20, 1997.

[163] A. Merdassi, P. Yang, and V. P. Chodavarapu, "A wafer level vacuum encapsulated capacitive accelerometer fabricated in an unmodified commercial MEMS process," *Sensors*, vol. 15, no. 4, pp. 7349–7359, 2015.

[164] H. Kam, T.-J. K. Liu, and E. Alon, "Design requirements for steeply switching logic devices," *Electron Devices, IEEE Transactions on*, vol. 59, pp. 326–334, Feb 2012.

[165] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano letters*, vol. 8, no. 2, pp. 405–410, 2008.

[166] A. Rusu, G. Salvatore, D. Jimenez, and A. Ionescu, "Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, pp. 16.3.1–16.3.4, Dec 2010.

[167] J. Wong and S. Salahuddin, "Can piezoelectricity lead to negative capacitance?," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 13.5.1–13.5.4, Dec 2014.

[168] H. Then, S. Dasgupta, M. Radosavljevic, L. Chow, B. Chu-Kung, G. Dewey, S. Gardner, X. Gao, J. Kavalieros, N. Mukherjee, M. Metz, M. Oliver, R. Pillarisetty, V. Rao, S. Sung, G. Yang, and R. Chau, "Experimental observation and physics of 'negative' capacitance and steeper than 40mV/decade subthreshold swing in $Al_{0.83}In_{0.17}N$/AlN/GaN MOS-HEMT on SiC substrate," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, pp. 28.3.1–28.3.4, Dec 2013.

[169] R. Jana, A. Ajoy, G. Snider, and D. Jena, "Sub-60 mV/decade steep transistors with compliant piezoelectric gate barriers," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 13.6.1–13.6.4, Dec 2014.

[170] A. Khan, C. Yeung, C. Hu, and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning and antiferroelectric operation," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, pp. 11.3.1–11.3.4, Dec 2011.

[171] J. Davis, A. Glaccum, K. Reeson, and P. L. Hemment, "Improved subthreshold characteristics of n-channel SOI transistors," *Electron Device Letters, IEEE*, vol. 7, pp. 570–572, Oct 1986.

[172] J. Fossum, R. Sundaresan, and M. Matloubian, "Anomalous subthreshold current-voltage characteristics of n-channel SOI MOSFET's," *Electron Device Letters, IEEE*, vol. 8, pp. 544–546, Nov 1987.

[173] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, J. Fossum, L. Altimime, and M. Jurczak, "Realizing super-steep subthreshold slope with conventional FDSOI CMOS at low-bias voltages," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, pp. 16.6.1–16.6.3, Dec 2010.

[174] J. Fossum and Z. Lu, "Anomalous floating-body effects in SOI MOSFETs: Low-voltage CMOS?," in *SOI Conference (SOI), 2011 IEEE International*, pp. 1–2, Oct 2011.

[175] C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J.-P. Colinge, "Low subthreshold slope in junctionless multigate transistors," *Applied Physics Letters*, vol. 96, no. 10, p. 102106, 2010.

[176] T. Mori and J. Ida, "Possibility of SOI based super steep subthreshold slope MOSFET for ultra low voltage application," in *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2013 IEEE*, pp. 1–2, Oct 2013.

[177] T. Mori and J. Ida, "Mechanism of super steep subthreshold slope characteristics with body-tied SOI MOSFET," in *Simulation of Semiconductor Processes and Devices (SISPAD), 2013 International Conference on*, pp. 101–104, Sept 2013.

[178] K. Nishiguchi and A. Fujiwara, "Nanowire metal-oxide-semiconductor field-effect transistors with small subthreshold swing driven by body-bias effect," *Applied Physics Express*, vol. 5, no. 8, p. 085002, 2012.

[179] C.-E. Chen, M. Matloubian, R. Sundaresan, B. Mao, C. Wei, and G. Pollack, "Single-transistor latch in SOI MOSFETs," *Electron Device Letters, IEEE*, vol. 9, pp. 636–638, Dec 1988.

[180] V. Robbins, T. Wang, K. Brennan, K. Hess, and G. Stillman, "Electron and hole impact ionization coefficients in (100) and in (111) Si," *Journal of applied physics*, vol. 58, no. 12, pp. 4614–4617, 1985.

[181] F. Liu, J. He, J. Zhang, Y. Chen, and M. Chan, "A non-charge-sheet analytic model for symmetric double-gate MOSFETs with smooth transition between partially and fully depleted operation modes," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 3494–3502, Dec 2008.

[182] J. Colinge, "Reduction of kink effect in thin-film SOI MOSFETs," *Electron Device Letters, IEEE*, vol. 9, pp. 97–99, Feb 1988.

[183] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *Electron Device Letters, IEEE*, vol. 4, pp. 111–113, Apr 1983.

[184] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability*, vol. 46, no. 2, pp. 270–286, 2006.

[185] J. Zhang, J. Trommer, W. M. Weber, P.-E. Gaillardon, and G. D. Micheli, "On temperature dependency of steep subthreshold slope in dual-independent-gate FinFET," *IEEE Journal of the Electron Devices Society*, p. accepted for publication, 2015.

[186] T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick, and W. Weber, "Stress dependent performance optimization of reconfigurable silicon nanowire transistors," *Electron Device Letters, IEEE*, vol. PP, no. 99, pp. 1–1, 2015.

[187] E.-H. Toh, G. H. Wang, G.-Q. Lo, L. Chan, G. Samudra, and Y.-C. Yeo, "Performance enhancement of n-channel impact-ionization metal-oxide-semiconductor transistor by strain engineering," *Applied physics letters*, vol. 90, no. 2, p. 3505, 2007.

[188] P. Su and J.-Y. Kuo, "On the enhanced impact ionization in uniaxial strained p-MOSFETs," *Electron Device Letters, IEEE*, vol. 28, pp. 649–651, July 2007.

[189] J. Trommer, A. Heinzig, A. Heinrich, P. Jordan, M. Grube, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Material prospects of reconfigurable transistor (RFETs)–from silicon to germanium nanowires," in *MRS Proceedings*, vol. 1659, pp. 225–230, Cambridge Univ Press, 2014.

[190] P. Su, K.-I. Goto, T. Sugii, and C. Hu, "A thermal activation view of low voltage impact ionization in MOSFETs," *Electron Device Letters, IEEE*, vol. 23, pp. 550–552, Sept 2002.

[191] J. Guo, M. A. Alam, and Y. Ouyang, "Subband gap impact ionization and excitation in carbon nanotube transistors," *Journal of applied physics*, vol. 101, no. 6, p. 064311, 2007.

[192] A. Liao, Y. Zhao, and E. Pop, "Avalanche-induced current enhancement in semiconducting carbon nanotubes," *Physical review letters*, vol. 101, no. 25, p. 256804, 2008.

[193] B. Iniguez, D. Jimenez, J. Roig, H. Hamid, L. Marsal, and J. Pallares, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 1868–1873, Aug 2005.

[194] L. Zhang, J. He, J. Zhang, F. Liu, Y. Fu, Y. Song, and X. Zhang, "An analytic model for nanowire MOSFETs with Ge/Si core/shell structure," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 2907–2917, Nov 2008.

[195] F. Liu, J. He, L. Zhang, J. Zhang, J. Hu, C. Ma, and M. Chan, "A charge-based model for long-channel cylindrical surrounding-gate MOSFETs from intrinsic channel to heavily doped body," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 2187–2194, Aug 2008.

[196] G. Zhu, X. Zhou, T. S. Lee, L. K. Ang, G. H. See, S. Lin, Y.-K. Chin, and K. L. Pey, "A compact model for undoped silicon-nanowire MOSFETs with Schottky-barrier source/drain," *Electron Devices, IEEE Transactions on*, vol. 56, pp. 1100–1109, May 2009.

[197] S. H. Lee, Y. S. Yu, S. W. Hwang, and D. Ahn, "A SPICE-compatible new silicon nanowire field-effect transistors (SNWFETs) model," *Nanotechnology, IEEE Transactions on*, vol. 8, pp. 643–649, Sept 2009.

[198] J. Goguet, S. Fregonese, C. Maneux, and T. Zimmer, "A charge approach for a compact model of dual gate CNTFET," in *Design and Technology of Integrated Systems in Nanoscale Era, 2008. DTIS 2008. 3rd International Conference on*, pp. 1–5, March 2008.

[199] C. Maneux, S. Fregonese, and T. Zimmer, "Innovative dual-gate CNTFET logic cell: Investigation of technological dispersion impact through compact modeling," *Nanotechnology, IEEE Transactions on*, vol. 13, pp. 1053–1062, Nov 2014.

[200] J. Wang and M. Lundstrom, "Ballistic transport in high electron mobility transistors," *Electron Devices, IEEE Transactions on*, vol. 50, pp. 1604–1609, July 2003.

[201] P. Chambre, "On the solution of the Poisson-Boltzmann equation with application to the theory of thermal explosions," *The Journal of Chemical Physics*, vol. 20, no. 11, pp. 1795–1797, 1952.

[202] Y. Chen and J. Luo, "A comparative study of double-gate and surroundinggate MOSFETs in strong inversion and accumulation using an analytical model," in *International Conference on Modeling and Simulation of Microsystems*, pp. 546–549, 2001.

[203] D. Jimenez, J. Saenz, B. Iniguez, J. Sune, L. Marsal, and J. Pallares, "Modeling of nanoscale gate-all-around MOSFETs," *Electron Device Letters, IEEE*, vol. 25, pp. 314–316, May 2004.

[204] Z.-H. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. Ko, and Y. Cheng, "Threshold voltage model for deep-submicrometer MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 40, pp. 86–95, Jan 1993.

[205] R. Vega, "On the modeling and design of Schottky field-effect transistors," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 866–874, April 2006.

[206] R. Vega, "Comparison study of tunneling models for Schottky field effect transistors and the effect of Schottky barrier lowering," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 1593–1600, July 2006.

[207] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *physica status solidi (a)*, vol. 205, no. 4, pp. 679–694, 2008.

[208] H. C. Pao and C.-T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," *Solid-State Electronics*, vol. 9, no. 10, pp. 927–937, 1966.

[209] C. C. Enz and E. A. Vittoz, *Charge-based MOS transistor modeling: the EKV model for low-power and RF IC design.* John Wiley & Sons, 2006.

[210] J.-M. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid-State Electronics*, vol. 49, no. 3, pp. 485–489, 2005.

[211] Z. Jian, H. Jin, Z. Xing-Ye, Z. Li-Ning, M. Yu-Tao, C. Qin, Z. Xu-Kai, Y. Zhang, W. Rui-Fei, H. Yu, *et al.*, "A unified charge-based model for SOI MOSFETs applicable from intrinsic to heavily doped channel," *Chinese Physics B*, vol. 21, no. 4, p. 047303, 2012.

[212] B. Yu, Y. Yuan, J. Song, and Y. Taur, "A two-dimensional analytical solution for short-channel effects in nanowire MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 56, pp. 2357–2362, Oct 2009.

[213] K. Lim and X. Zhou, "A physically-based semi-empirical effective mobility model for MOSFET compact i–v modeling," *Solid-State Electronics*, vol. 45, no. 1, pp. 193–197, 2001.

[214] G. Baccarani and S. Reggiani, "A compact double-gate MOSFET model comprising quantum-mechanical and nonstatic effects," *Electron Devices, IEEE Transactions on*, vol. 46, pp. 1656–1666, Aug 1999.

[215] G. Gildenblat, H. Wang, T.-L. Chen, X. Gu, and X. Cai, "SP: an advanced surface-potential-based compact MOSFET model," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 1394–1406, Sept 2004.

[216] G. Zhu, X. Zhou, Y.-K. Chin, K. L. Pey, J. Zhang, G. H. See, S. Lin, Y. Yan, and Z. Chen, "Subcircuit compact model for dopant-segregated Schottky gate-all-around Si-nanowire MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 57, pp. 772–781, April 2010.

[217] J. Deng and H.-S. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application - Part II: Full device model and circuit performance benchmarking," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 3195–3205, Dec 2007.

[218] D. Ward and R. Dutton, "A charge-oriented model for MOS transistor capacitances," *Solid-State Circuits, IEEE Journal of*, vol. 13, pp. 703–708, Oct 1978.

Publications Related to This Thesis

Journal Publications:

[1] **Jian Zhang,** J. Trommer, W. M. Weber, P.-E. Gaillardon, and G. De Micheli, "On temperature dependency of steep subthreshold slope in dual-independent-gate FinFET," ***IEEE Journal of the Electron Devices Society,*** vol. 3, no. 6, pp. 452-456, 2015.

[2] **Jian Zhang**, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-Controllable Silicon Nanowire Transistors with Dual Threshold Voltages," ***IEEE Transactions on Electron Devices***, vol. 61, no. 11, pp. 3654-3660, Nov. 2014.

[3] **Jian Zhang**, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs," ***IEEE Transactions on Circuits and Systems–I: Regular Papers***, vol. 61, no. 10, pp. 2851-2861, Oct. 2014.

[4] M. De Marchi, D. Sacchetto, **Jian Zhang**, S. Frache, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity," ***IEEE Transactions on Nanotechnology***, Vol. 13, no. 6, pp. 1029-1038, Nov. 2014.

[5] M. De Marchi, **Jian Zhang**, S. Frache, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-All-Around FETs," ***IEEE Electron Device Letters***, vol. 35, no. 8, pp. 880-882, Aug. 2014.

[6] L. Amaru, P.-E. Gaillardon, **Jian Zhang,** and G. De Micheli, "Power-Gated Differential Logic Style Based on Double-Gate Controllable Polarity Transistors," ***IEEE Transactions on Circuits and Systems–II: Express Briefs,*** Vol. 60, no. 10. pp. 672-676, Oct. 2013.

Conference Publications:

[1] **Jian Zhang**, P.-E. Gaillardon, and G. De Micheli, "A Surface Potential and Current Model for Polarity-Controllable Silicon Nanowire FETs," ***45th European Solid-State Device Conference (ESSDERC'15)***, pp. 48-51, Graz, Austria, Sep. 2015.

[2] **Jian Zhang,** M. De Marchi, P.-E. Gaillardon, and G. De Micheli, "A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current," ***International Electron Devices Meeting (IEDM'14)***, pp. 339-342, San Francisco, USA, Dec. 2014.

[3] **Jian Zhang,** P.-E. Gaillardon, and G. De Micheli, "Dual-Threshold-Voltage Configurable Circuits with Three-Independent-Gate Silicon Nanowire FETs," ***IEEE International Symposium on Circuits and Systems (ISCAS'13)***, pp. 2111-2114, Beijing, China, May 2013.

[4] P.-E. Gaillardon, **Jian Zhang**, M. De Marchi, G. De Micheli, "Towards Functionality-Enhanced Devices: Controlling the Modes of Operation in Three-Independent-Gate Transistors," ***10th IEEE Nanotechnology Materials and Devices Conference (NMDC)***, 13-16 September 2015, Anchorage, USA.

[5] H. Ghasemzadeh, P.-E. Gaillardon, **Jian Zhang**, M. S. Reorda, E. Sanchez and G. De Micheli, "On the Design of a Fault Tolerant Ripple-Carry Adder with Controllable-Polarity Transistors," ***IEEE Computer Society Annual Symposium on VLSI (ISVLSI'15)***, Montpellier, France, 2015.

[6] X. Tang, **Jian Zhang**, P.-E. Gaillardon, and G. De Micheli, "TSPC Flip-Flop Circuit Design with Three-Independent-Gate Silicon Nanowire FETs," ***IEEE International Symposium on Circuits and Systems (ISCAS'14)***, pp. 1660-1663, Melbourne, Australia, Jun. 2014.

[7] P.-E. Gaillardon, L. Amaru, **Jian Zhang**, and G. De Micheli, "Advanced System on a Chip Design Based on Controllable-Polarity FETs", ***Design, Automation & Test in Europe Conference and Exhibition (DATE'14),*** Dresden, Germany, Mar. 2014.

[8] M. De Marchi, D. Sacchetto, S. Frache, **Jian Zhang**, P.-E. Gaillardon, Y. Leblebici and G. De Micheli, "Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs," ***International Electron Devices Meeting (IEDM'12)***, pp. 183-186, San Francisco, USA, Dec. 2012.

[9] S. Bobba, P.-E. Gaillardon, **Jian Zhang**, M. De Marchi, D. Sacchetto, Y. Leblebici, and G. De Micheli, "Process/Design Co-optimization of Regular Logic Tiles for Double-Gate Silicon Nanowire Transistors," ***IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH'12)***, pp. 55-60, Amsterdam, Netherlands, Jul. 2012.

Book Chapter:

[1] P.-E. Gaillardon, **Jian Zhang,** L. Amaru, G. De Micheli, "Multiple-Independent-Gate Nanowire Transistors: From Technology to Advanced SoC Design," Nano-CMOS and Post-CMOS Electronics: Devices and Modeling (Eds.: S. P. Mohanty, A. Srivastava), IET, 2015, In press.

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Education

École Polytechnique Fédérale de Lausanne (EPFL), Switzerland *Oct. 2011 – Nov. 2015*

Ph. D. in Microsystems and Microelectronics

Direction: Fabrication, modeling and simulation of Si nanowire/FinFET devices and circuits.

Peking University, Beijing, China *Sep. 2008 – Jul. 2011*

Master of Science in Microelectronics and Solid State Electronics

Direction: Compact modeling of SOI/FinFET/nanowire devices.

Peking University, Beijing, China *Sep. 2004 – Jul. 2008*

Bachelor of Science in Microelectronics

Direction: Compact modeling of SOI/FinFET/nanowire devices.

Research Experience

Research Assistant, EPFL, Switzerland *Oct. 2011 – Dec. 2015*

- Nanosystems: architectures, design and applications
  - Fabrication and characterization of Si nanowire and FinFET devices at nm scale;
  - 4 years working experience in EPFL's advanced cleanroom;
  - Device physics, compact modeling and TCAD simulation of Si nanowire and FinFET;
  - Design of highly efficient logic gates/cells/circuits with novel device concepts;
  - SPICE simulation, characterization of standard logic cell library, logic synthesis.

Research Assistant, Peking University, China *Sep. 2006 – Jul. 2011*

- Next-generation FinFET/SOI MOSFET model development
  - Core physical model and advanced physical effects;
  - Non-quasi-static transient and high frequency small signal characteristics;
  - Parameter extraction, benchmark and implementation in SPICE;
  - Selected as candidates of industry standard SOI model by Compact Model Council.

Selected Publications

s1. **Jian Zhang,** J. Trommer, W. M. Weber, P.-E. Gaillardon, and G. De Micheli, "On temperature dependency of steep subthreshold slope in dual-independent-gate FinFET," ***IEEE Journal of the Electron Devices Society,*** vol. 3, no. 6, pp. 452-456, 2015.

s2. **Jian Zhang**, P.-E. Gaillardon, and G. De Micheli, " A surface potential and current model for polarity-controllable silicon nanowire FETs," ***45th European Solid-State Device Conference (ESSDERC'15),*** pp. 48-51, Graz, Austria, Sep. 2015.

s3. **Jian Zhang**, M. De Marchi, P.-E. Gaillardon, and G. De Micheli, "A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current," ***International Electron Devices Meeting (IEDM'14)***, pp. 339-342, San Francisco, USA, Dec. 2014.

s4. **Jian Zhang**, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-controllable silicon nanowire transistors with dual threshold voltages," ***IEEE Transactions on Electron Devices***, vol. 61, pp. 3654-3660, 2014.

s5. **Jian Zhang**, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs," ***IEEE Transactions on Circuits and Systems–I: Regular Papers***, vol. 61, pp. 2851-2861, 2014.

s6. **Jian Zhang,** P.-E. Gaillardon, and G. De Micheli, "Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs," ***IEEE International Symposium on Circuits and Systems (ISCAS'13),*** pp. 2111-2114, Beijing, China, May 2013.

s7. **Jian Zhang,** J. He, *et al.*, "A unified charge-based model for SOI MOSFETs applicable from intrinsic to heavily doped channel," ***Chinese Physics B,*** vol. 21, no. 4, 047303, 2012.

s8. **Jian Zhang,** L. Zhang, J. He, and M. Chan, "A noncharge-sheet channel potential and drain current model for dynamic-depletion silicon-on-insulator metal-oxide-semiconductor field-effect transistors," ***Journal of Applied Physics,*** vol. 107, 054507, 2010.

s9. **Jian Zhang**, J. He, and L. Zhang, "One-dimension continuous analytic potential solution to generic oxide-silicon-oxide system," ***Chinese Physics B***, vol. 19, no. 6, 067304, 2010.

s10. **Jian Zhang**, J. He, *et al.*, "A surface-potential-based non-charge-sheet core model for fully depleted SOI MOSFET," ***IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC'07)***, pp. 569-572, Tainan, Taiwan, Dec. 2007.

Patents

p1. Lining Zhang, Jin He, **Jian Zhang,** "A nanowire field effect transistor with independent gate control", filed by Peking University, CN101944539A, 2011.

p2. Jin He, Lining Zhang, **Jian Zhang,** Xing Zhang, "A nanowire field effect transistor", filed by Peking University, CN101740619A, 2010.

Professional Skills

Keywords: fabrication, characterization, device physics, compact modeling, simulation.

Software: Sentaurus, Cadence Virtuoso, ELC, HSPICE, BSIMPro+, Design Complier, Matlab.

Process Technologies: e-beam lithography, etching, film deposition, SEM, FIB, probe station, etc..

Languages: Verilog-A, Verilog/VHDL, C/C++.

Professional Activities

- Member of IEEE and IEEE Electron Devices Society;
- Reviewer of international journals and conferences, including *IEEE Electron Device Letters, IEEE Transactions on Nanotechnology, ECS Solid State Letters, JCSC, IEEE ICECS, etc..*

Social Activities

President, Association of Chinese-Scholarship-Funded Students & Scholars Lausanne, 2012-2014.

Awards & Honors

- 2012, Best Paper Award, IEEE/ACM International Symposium on Nanoscale Architectures;
- 2010, Outstanding Academic Award, Peking University;
- 2008, Outstanding Dissertation Award, Peking University;
- 2007, President Undergraduate Research Fellowship, Peking University.