Multi-Terminal Am-Bipolar Memristive Devices for Emerging Logic and Memory Architectures

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For a successful technology, reality must take precedence
over public relations, for nature cannot be fooled.
— Richard P. Feynman

To my wife, Martina and to my kids, Alessia and Nicolo...

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Abstract

The main source of the CMOS success lies in the exponential increase of device density that the silicon industry kept true for more than 40 years reducing the unit cost of integrated circuits. Recently, the pace of scaling has been slowing down due to approaching fundamental limits at the device level. While the paradigm of scaling is still alive, researchers are striving to follow Moore's law by focusing on new materials, new device structures and new state variables. The basic building block for circuits has always been the four-terminal planar transistor but new versions of the MOSFET structure such as the double-gate FET, the FinFET, the gate-all-around nanowire FET can be found in commercial products.

Due to the natural limitations of materials, future nano-scale circuits will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages an end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. A long list of fundamental state variables other than charge includes the spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states. Technologies using new state variables would have to be implemented within a completely new technological platform, and cannot be seen as CMOS-compatible alternatives.

This thesis work presents new ways to integrate added functionality to nanoscale devices, while keeping a top-down CMOS-compatible fabrication flow. In this respect, the devices herein proposed can be divided into two categories, depending on the level of integration required: either *Front-End-of-the-Line (FEoL)* or *Back-End-of-the-Line (BEoL)*. Moreover, the devices studied can enhance the functionality of CMOS, by introducing either *ambipolar conductance* and/or *memory effects* from devices for logic, memory or sensing applications.

First, a FEoL top-down process flow for ambipolar vertically-stacked Si nanowire devices has been developed and adapted for a list of nanoscaled devices, including: Si nanowire FET, vertically-stacked Si nanowire FETs with single or double gate, poly-Si nanowire (simple or vertically-stacked) transistors with *Nano-Stencil* lithography and a special focus has been put on the fabrication of ultra-dense vertically-stacked Si nanowires.Then, a BEoL top-down process flow for resistive RAM devices has been developed in the framework of CMOS post-processing.

Concerning *ambipolar conductance* or *"ambipolarity"*, the main applications target logic, and devices have been fabricated targeting *Ternary* logic elements, *Theshold-gate* logic with perspective towards Multi-Valued logic and *Polarity-control* devices targeting Sea-of-Gates architectures.

Abstract

Considering *memory effects* or *"memristance"* dedicated process flows have been developed for the fabrication of two-terminal memristive devices for *standalone memories*, *Field-Programmable-Gate-Arrays (FPGA)* and programmable *Through Silicon Via (TSV)*. At the same time, the memory effects found in ambipolar Si nanowire devices have been exploited for a new sensing mechanism, enabling the detection of heat, current and/or bio-molecules. The memory effects responsible for the sensing operation have been classified as part of general properties of multi-terminal memristive devices.
Keywords: nanotechnology, emerging technology, vertically-stacked nanowires, silicide, Schottky-barrier FETs, SBFET, multi-gate, logic design, ternary-logic, ambipolarity, polarity-control, memristance, multi-terminal memristive devices, resistive RAM, crossbar, bipolar resistive switching, CMOS post-processing.

Résumé

Depuis 40 ans, la principale source du succès du CMOS réside dans l'augmentation exponentielle de la densité de dispositif semiconducteur et, par conséquent, la réduction exponentielle du coût unitaire de circuits intégrés. Récemment, le rythme d'innovation a ralentie en raison de l'approche des limites fondamentales au niveau du dispositif. Alors que le paradigme de la mise à l'échelle est encore en vie, les chercheurs s'efforcent de suivre la loi de Moore en mettant l'accent sur de nouveaux matériaux, de nouveaux concept de dispositifs et de nouvelles variables d'état. Le bloc de construction de base pour circuits intégrés a toujours été le transistor planaire à quatre terminaux, mais de nouvelles versions de la structure de transistor tels que le MOSFET a double-grille, le FinFET, le *Gate-All Around (GAA)* FET a nanofil peut être trouvée dans des produits commerciaux.
En raison des limites naturelles des matériaux, les futur circuits a la nano-échelle devront exploiter davantage des moyens efficaces pour le calcul et le stockage de la mémoire. Un possible scénario envisage une fin des technologies basée sur la charge électrique, et une introduction sur de variables d'état alternatives. Une longue liste de variables fondamentales autres que la charge comprend le spin, la phase, l'orientation multipolaire, la position mécanique, la polarité orbital symétrie, le quanta du flux magnétique, la configuration moléculaire, et d'autres états quantiques. Le technologies utilisant de nouvelles variables d'état devront être mises en œuvre dans un tout nouvelle plate-forme technologique, et ne peut pas être considérée comme des alternatives compatibles CMOS.
Ce travail de thèse présente de nouvelles façons d'intégrer des fonctionnalités supplémentaires aux dispositifs nanométriques, tout en conservant un flux de fabrication CMOS-compatible et top-down. À cet égard, les dispositifs proposée ici peut être divisé en deux catégories, selon le niveau d'intégration nécessaire : soit le Front-End-of-the-Line (FEoL) ou le Back-End-of-the-Line (BEoL) niveau d'intégration. Une autre classification peut être faite en fonction de la nature des phénomènes qui porte une majeure fonctionnalité, et en tant que tels, les appareils peuvent être séparés soit comme conducteur ambipolaire soit comme dispositif avec memristance ou avec effets de mémoire. Tout d'abord, un flux de processus top-down FEoL pour les dispositif a nanofil de Si verticalement empilés avec conductance ambipolaire a été développé et adapté pour une liste des dispositifs nanométriques, y compris : FET a nanofil de Si, FET a nanofil de Si verticalement empilés à grille simple ou double, le FET a nanofil de poly-Si (simple ou empilées verticalement) fabriquée avec la lithographie *nano-stencil*. Une attention particulière a été mis sur la fabrication de tres dense nanofils de Si verticalement empilés. En suite, un flux de processus top-down BEoL a été développé pour les appareils résistifs RAM à la

fois pour BEoL et CMOS post-processing. Vu du côté de la demande, les appareils ambipolaires avec et sans mémoire ont été fabriqué et caractérisé, en ciblant plusieurs applications à la logique, la mémoire et la détection.
En ce qui concerne "ambipolarity", les principales applications sont dédié a la logique et, de cette cote, plusieurs dispositifs ont été fabriqué comme éléments pour logiques ternaires, pour la logique Theshold-Gate avec perspective vers Multi-Valued logic and dispositifs a contrôle de polarité.
Considérant "memristance" un ensemble de processus a été développé pour la fabrication de dispositifs memristive a deux terminaux pour les mémoires standalone, pour le Field-Programmable-Gate-Arrays (FPGA) et programmable Through Silicon Via (TSV). Dans le même temps, les effets de mémoire trouvé dans les dispositifs ambipolaire à nanofils de Si ont été exploités en tant que nouveau mécanisme de détection, permettant la détection de la chaleur, du courant électrique et de les bio-molécules. Les effets de mémoire responsables pour l'opération de détection ont été classés comme faisant partie des propriétés générales de dispositifs memristive a multi-terminals.
Mots clefs : nanotechnologie, tecnologies émergentes, nanofils a impilage vertical, silicide, FETs a barrier Schottky, SBFET, multi-grille, logique polyvalente, logique ternaire, ambipolarité, control de polarité, memristance, dispositif memristifs a multi-terminaux, RAM résistive , crossbar, commutation résistive bipolaire, post-fabrication CMOS.

Sommario

Per 40 anni, la fonte principale di successo della tecnologia CMOS si deve all'aumento esponenziale nella densità di integrazione dei dispositivi a semiconduttore e, conseguentemente, alla riduzione esponenziale del costo unitario per un dato circuito integrato. Recentemente, il ritmo d'innovazione è rallentato a causa dell'avvicinamento a limiti fondamentali legati alla fisica dei dispositivi a semiconduttori. Mentre il paradigma della riduzione delle dimensioni, altrimenti noto come *scaling* è ancora vivo, i ricercatori si sforzano di seguire la *Legge di Moore* concentrandosi su nuovi materiali, nuovi dispositivi e nuove variabili di stato. L'elemento di base per i circuiti integrati è stato per molto tempo il transistor planare a quattro terminali, ed ora nuove versioni della struttura del MOSFET, come per esempio il FET a doppio gate o il FinFET o ancora il *nanowire FET* a *Gate-All-Around (GAA)* sono gia presenti in prodotti commerciali.

A causa dei limiti fisici dei materiali, i futuri circuiti su scala nanometrica dovranno sfruttare nuove tecnologie per il calcolo e la memorizzazione dei dati. Un possibile scenario prevede la fine delle tecnologie basate sulla manipolazione della carica elettrica e una migrazione verso l'uso di variabili di stato alternative. Una lunga lista di variabili fondamentali diverse dalla carica comprende: lo stato di spin, la fase, l'orientazione di multi-polo, la posizione meccanica, la polarità, la simmetria orbitale, il quanto del flusso magnetico, la configurazione molecolare e altri stati quantici. Tuttavia, le tecnologie che utilizzano nuove variabili di stato dovranno essere implementate su una nuova piattaforma tecnologica, e non possono essere considerate come alternative compatibili con i processi di fabbricazione CMOS.

Questa tesi presenta nuovi metodi di integrazione che apportano funzionalità aggiuntive ai dispositivi elettronici in nanoscala, mantenendo un processo di fabbricazione compatibile con il CMOS e una fabbricazione top-down. A questo proposito, i dispositivi qui proposti possono essere divisi in due categorie in base al livello di integrazione richiesto: *Front-End-of-the-Line (FEOL)* o *Back-End-of-the- Line (BEoL)*. Inoltre, i dispositivi studiati possono aumentare la funzionalità del CMOS, grazie a due caratteristiche di base; la conduttanza ambipolare e/o gli effetti di memoria per applicazioni di computazione logica, memoria o sensoristiche.

Nella prima parte della tesi, un flusso di processi top-down FEoL per la fabbricazione di dispositivi a nanofili impilati verticalmente e stato sviluppato e discusso per un elenco di dispositivi su scala nanometrica, tra cui: *Si nanowire FET*, *Vertically-Stacked Si Nanowire FETs* a gate singolo o doppio, nanowire FET in Si policristallino (a singolo nanowire oppure vertically-stacked) realizzato con litografia nano-stencil e un'attenzione particolare è stata data alla produzione di vertically-stacked nanowires ad alta densità. Inoltre, un processo di

fabbricazione BEoL top-down è stato sviluppato per i dispositivi di memoria *resistive RAM* nel contesto di post-fabbricazione CMOS.
Considerando la conduttanza ambipolare, le principali applicazioni sono dedicate alla logica e in questo contest, diversi dispositivi sono stati fabbricati come elementi per la logica ternaria, per la logica *Threshold-Gate* con prospettive verso *Multi-Valued Logic* e logica con controllo della polarità per architetture *Sea-of-Gates*.
Considerando gli *effetti di memoria* o la *memristance*, un processo di fabbricazione è stato sviluppato per la produzione di dispositivi memristivi a due terminali, sia per applicazioni *Standalone* che per *Field-Programmable-gate (FPGA)*. Inoltre, un nuovo tipo di interconnessione programmabile e stato concepito, quale il *Programmable Through Silicon Via (TSV)*. Allo stesso tempo, gli effetti di memoria riscontrati in dispositivi FET ambipolari sono stati sfruttati come nuovo meccanismo di *sensing*, per rilevare il calore, corrente elettrica e bio-molecole. Gli effetti di memoria responsabili delle operazioni di rilevamento sono state classificate come parte delle proprietà generali dei dispositivi memristivi a multi-terminali.
Parole chiave: nanotecnologia, tecnologie emergenti, nanofili impilati verticalmente, siliciuro, FETs a barriera Schottky, SBFET, multi-gate, design di circuiti logici, logica ternaria, ambipolarità, controllo di polarità, mem-resistenza, dispositivi memristivi a multi-terminali, RAM resistiva, crossbar, commutazione resistiva bipolare, post-fabbricazione CMOS.

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List of Acronyms

1D1R	1-Diode 1-Resistor
1T1C	1-Transistor 1-Capacitor
1T1R	1-Transistor 1-Resistor
6T	6-Transistors
AB	Anti-Body
AFM	Atomic Force Microscopy
AG	Anti-Gen
ALD	Atomic Layer Deposition
BE	Bottom Electrode
BEoL	Back-End-of-the-Line
BOX	Buried OXide
BRS	Bipolar Resistive Switching
CMOL	hybrid CMOS/nanoelectronic circuit
CMOS	Complementary-Metal-Oxyde-Semiconductor
CNT	Carbon NanoTube
DIBL	Drain Induced Barrier Lowering
DIG	Double Independent Gate
DRAM	Dynamic RAM
FEoL	Front-End-of-the-Line
FET	Field Effect Transistor

FPGA	Field Programmable Gate Array
FRAM	Ferroelectric RAM
GAA	Gate-All-Around
GIDL	Gate Induced Drain Lowering
GMS	Generic Memory Structure
GPTS	3-GlycidoxyPropylTrimethoxySilane
HRS	High Resistance State
HSQ	Hydrogen SilsesQuioxane
IC	Integrated Circuit
ILD	Inter-Layer Dielectric
IR	Intermidiate Resistance state
LPCVD	Low-Pressure Chemical Vapour Deposition
LRS	Low Resistance State
LUT	Look-Up Table
MEMS	Micro-Electro-Mechanical System
ML	Multi-Level
MOS	Metal Oxide Semiconductor
MRAM	Magnetic RAM
MUX	MUltipleXer
MVL	Multi-Valued Logic
NEMS	Nano-Electro-Mechanical System
NVM	Non-Volatile Memory
PMMA	Poly-Methil-MethAcrylate
POI	Polysilicon-On-Insulator
PRAM	Phase change RAM
RAM	Random Access Memory
RCA	Radio Corporation of America cleaning

ROM	Read Only Memory
RRAM	Resistive RAM
SB	Schottky Barrier
SBFET	Schottky Barrier FET
SCE	Short Channel Effect
SCLC	Space Charge Limited Conductance
SiNW	Silicon NanoWire
SOI	Silicon-On-Insulator
SoC	System-On-Chip
SRAM	Static RAM
TE	Top Electrode
TSV	Through Silicon Via
ULSI	Ultra-Large-Scale Integration
VLSI	Very-Large-Scale Integration
WORM	Write-Once Read-Many

1 Introduction

Humans are primates of the family *Hominidae* and the genus *Homo* (*homo sapiens*). Throughout the *millenia* humans have become the dominating specie in nature thanks to its unique abilities of abstract reasoning, language, introspection, problem solving and culture through social learning. These mental capabilities have allowed humans to make far greater use of tools than any other species. Humans are uniquely adept at utilizing systems of symbolic communication such as language and art of self-expression, the exchange of idea and self expression. Culture evolution in humans has always been sustained by inventions (see Fig. 1.1.

More recently, i.e. in the last two centuries, technological innovations have enabled an exponential development in the level of information processing capabilities. Ealier information processing started with the invention of the alphabeths and its use as a memory code to store the oral transmitted information on solid substrates (stones, wood and then paper). Throughout the centuries, the use of the alphabet and its transcription in printed form enabled more reliable transmission of knowledge and, consequently the evolution of disciplines. Of particular interest is the development of mathematics and the early search for tools enabling faster and powerful calculus. It is in the 1617 that the Scottish mathematician John Napier invented logarithms and invented a set of 'rods' for performing matematical calculation. In 1642 another matematician, Blaise Pascal, invented a mechanical adding machine. In 1666

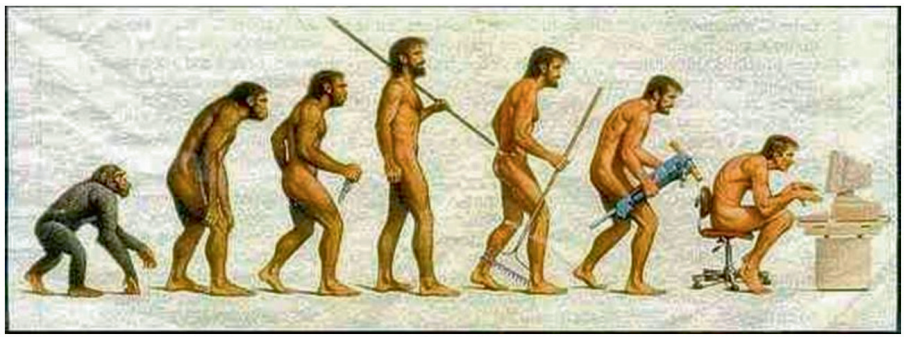
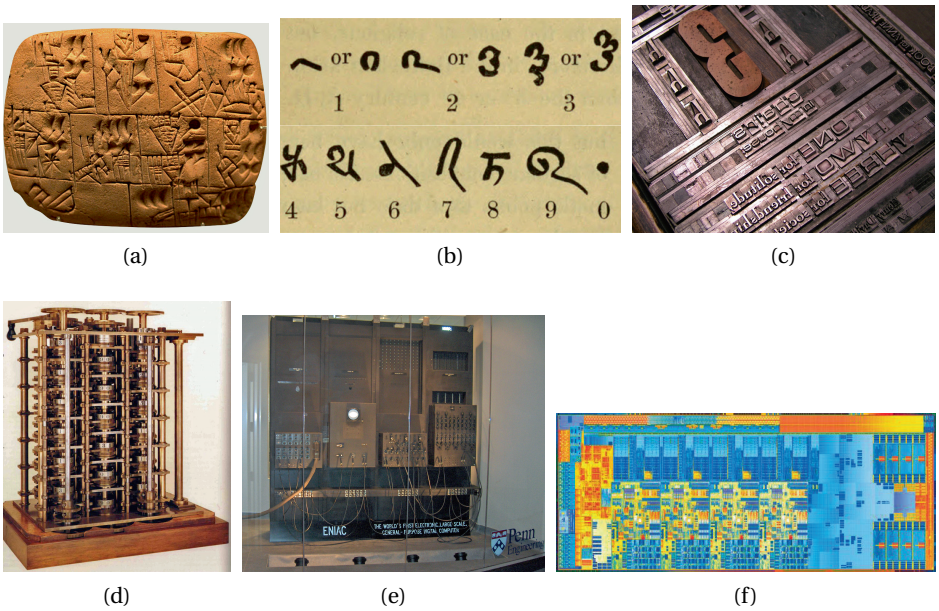


Figure 1.1: Human Evolution

the German mathematician Gottfried Leibniz writes on the value of binary numbers and later, in 1694 he constructs the first mechanical device able to perform all classical arithmetic functions (addition, subtraction, division and multiplication). Later, in 1823 Charles Babbage invents the first mechanical computer which could be programmed through punch-cards (the first memory substrate for computers). In 1847 English matemathician George Boole publishes 'Mathematical Analysis of Logic' and uses the idea of binary numbering to fuse logic with algebra. In 1936 matemathician Alan Turing puts together binary notation and Boolean logic to produce tests for mathematical probability. He proposes the 'Universal Turing Machine' a construct which contains all the logic and mathematical elements of modern analogue computer. Meanwhile, the mechanical computers benefited from the invention of the electricity and of the electro-mechanical devices, increasing computational throughput. The introduction of novel information processing devices with a reliable storage substrate enabled the manufacturability of programmable computers and their use during the World War II to decode encrypted messages from the enemy. Later, in 1947 the transistor was invented [1], and its use as the electrical equivalent of the relay gave a boost towards more performant switches [2]. It was then in 1958 that the integrated circuit was invented, enabling the integration of several transistors on a semiconductor substrate [3]. A few years later (in 1965) Intel co-founder Gordon E. Moore described how the number of components in an *Integrated Circuit (IC)* doubled every two years since the invention of the ICs, and that this trend would continue for at least another 10 years [4]. Such an exponential increase in computational throughput is still valid today, and this trend has gained the name of Moore's law [5]. Such achievements have led to more and more powerful electronic systems, and the transistor today is the most widespread human artifact, affecting any sector of the world's population. It enabled the diffusion of computers, the internet, smart phones, digital cameras, and practically any other electronic device. Nonetheless, in the last decade many declared that increased technological challanges would have caused a slowing down of the pace of scaling. Anyway such difficulties have been compensated by the increasing research efforts, especially from the semiconductor industries, at different levels of the IC integration. As the computational paradigm evolution can be splitted in at least three components, namely logic, memory and input/output interfaces, different care must be taken for the different components.

At the transistor level, for instance for logic, the happy scaling following Dennard's rules [6] has been facing the Boltzmann's tiranny, or, in other words, the limit of the subthreshold slope due to the thermal effects (around 60mV/dec at room temperature), as well as the static current leakage of thin SiO_2 gate dielectric, polydepletion, *Short Channel Effects (SCEs)*, *Drain Induced Barrier Lowering (DIBL)*, *Gate Induced Drain Lowering (GIDL)*. All these challanges have however found technological solutions, which are summarized in Table 1.1, and lead to non-planar construction of the MOSFET [7]. Novel materials and device configurations have recently became hot topics in the research community, as a passport for scaling prosecution. One example is the introduction of *Silicon Nanowire (SiNW) Field-Effect-Transistors (FETs)*. The SiNW channels have the advantage of better immunity toward *Short Channel Effects (SCEs)* mantaining a full compatibility with the current planar technology [8]. In addition,



(a) (b) (c)

(d) (e) (f)

Figure 1.2: Evolution of information processing. (a) One of the first example of writing: the proto-cuneiform. (b) The first written decimal system that includes the numeral zero. (c) A window pane printing press. (d) Babbage's difference engine. (e) The ENIAC computer. (f) The Intel's Ivy Bridge microprocessor.

nanowire channels can be configured in stacks for increased performance [9] or used for new functionalities [10]. The suspended channel enables the implementation of a *Gate-All-Around (GAA)* configuration that gives further benefits for the transistor scheme: we can think about engineered SiNW channels with increased performances [11, 12, 13] for instance by increasing the mobility by inducing strain [14], or exploit the quantum ballistic effects related to the one dimensional channel [15]. SiNW channels can also be used to build new logic architectures [16, 17] or as ultimate memory architectures for *Ultra-Large-Silicon-Integration (ULSI)* [18, 19]. The main advantages for the SiNW configuration is the possibily of ultimate scaling, thanks to the GAA structure. Moreover, quantum ballistic effects are envisaged as an opportunity for higher conductance operation, compared with the standard planar technology. This effect is related to the 1D confinement of the channel and it cannot be obtained with a different configuration. The best channel diameter dimension to operate in the 1D transport regime is believed to be 4nm for a circular SiNW. This small dimension has the disadvantage of low current drive so the use of parallel channels is of concern if ones would like to drive other devices, as it is normally required from a circuit designer.

At the same time, most of the circuit architectures that are now used for computation purposes show their performance limits in both the interconnection delay as well as in the power density generated by the devices. Since for high performance ICs an innovation breakthrough should make smarter use of the existing interconnection capabilities rather then pushing the operational frequency of the basic device, we should use the novel funcitonalities coming from

the SiNW channels to make more efficient computation. The GAA SiNW MOSFET is a suitable candidate for ultra low power operation since the gate dielectric layer can be scaled more easily, enabling a strong reduction of the static leakage that is a major contribution to the power dissipated by MOSFETs. At the same time doping levels in SiNWs can be relaxed, resulting in higher carrier mobilities. This intrinsic benefits of the SiNW GAA MOSFETs push the limit for scaling up to 5nm transistor gate length [20]. Then, depending on the wire diameter a certain number of quantum channels can partecipate to the conductance. However, carrier mobility suffers for a high number of quantum channels. Thus a parallel number of 1D SiNW channels should be used for high current and low leakage operation. In Fig. 1.3, the different strategies for MOSFET scaling are summarized [21].

Considering memory, nowaday different technologies are utilized for different applications, relying on magnetic, optical or charge-based type of storage [22]. It is anyway with the advent of semiconductor memories that high-density, high-speed and low-power become possible [23]. Semiconductor device memories can be classified into two main categories, *Random Access Memory (RAM)*, which can be re-written several times and *Read-Only Memory (ROM)*. The ROMs are non-volatile while RAMs can be either volatile or non-volatile type. Further classification can be made based on the technological implementation. As shown in Fig. 1.4, the volatile RAM is composed of two main categories, SRAM and DRAM. The SRAM is a logic cell consisting of at least *6 Transistors (6T)* and requires static power to keep the state, while the DRAM utilizes the charge stored in a capacitor to keep the state. Typical DRAM cells consist of *1 Transistor - 1 Capacitor (1T1C)*. Since the capacitor leaks charge though the transistor, the state of DRAM must be refreshed if needed over a period of time longer than a few seconds. Although SRAM and DRAM have the inconvenience of volatility, their advantage is speed, which surpasses any of the non-volatile memories. For this reason, SRAM are utilized as cache in microprocessors, while DRAM are utilized when density is more important for temporary information storage [24]. When considering non-volatile memories, the current driving market is FLASH[1], which is an evolution of the *Erasable Programmable ROM (EPROM)* and *Electrically Erasable PROM (EEPROM)*. The advantage of FLASH compared to the volatile memories is that their state can be stored for more than 10 years and that the density is the highest among all the semiconductor memories. The high density of FLASH is due to the 1T configuration, which makes a typical FLASH architectures with a feature size of $4F^2$ or lower when utilized as multi-bit FLASH. Nonetheless, the write/erase process in FLASH is quite slow compared to the volatile memories and this prevented their further diffusion. Interestingly, emerging non-volatile devices, such as *Ferroelectric RAMs (FRAM)*, *Magnetic RAMs (MRAM)*, *Phase change RAMs (PRAM)* or *Resistive RAMs (RRAM)* could compete with the SRAM and DRAM in terms of density while being faster than FLASH. The baseline and emerging semiconductor device memory parameters are summarized in Table 1.2 and Table 1.3, respectively.

[1] FLASH memory (both NOR and NAND types) was invented by Dr. Fujio Masuoka while working for Toshiba circa 1980. According to Toshiba, the name FLASH was suggested by Dr. Masuoka's colleague, Mr. Shōji Ariizumi, because erasure process of the memory contents reminded him of the flash of a camera.

Nevertheless, as the size of the transistor shrinks following Moore's Law, the increased delay of wires begin to outweigh the increased performance of small transistors. Decreasing the wire delay, e.g. by using the low-dielectric constant (low-κ) wiring materials releases the problem in 90nm; but for 65nm and beyond, ultralow-κ material is required. However, although this is technologically feasible, it may increase a lot the fabrication costs [25]. The interconnects requirements have been satisfied by introducing more and more metal layers and advanced flavors of BEoL technology. Nevertheless, interconnects scaling is facing fundamental barriers such as the low-κ, limited by the integration of air gaps, as well as worsened conductivity due to the larger line edge roughness impact on scaled interconnects and the interaction between the metal lines and the surrounding *InterLayer Dielectric (ILD)*. These fundamental issues are somewhat mitigated by the multi-core design, which enable the packing of more functinality at the system level.

In the International Roadmap for Semiconductors, the future of interconnects may lead to completely new concepts (see Table 1.4), either exploiting a totally different physics, such as wireless or optical/plasmonics [26] signalling or to a radical re-adaptation of the actual dual damascene Cu process into another one that employs innovative conductors, such as *carbon nanotubes (CNT)* [27, 28], nanowires or graphene. The different approaches points to deliver high performance by leveraging on specific advantages. For instance the optical signalling has the advantages of high bandwidth and no cross talk; the RF wireless invests on the possibility of interconnecting different components without the need of routing. In the case of nanotubes/nanowires/graphene, the intrinsic force as interconnect is an higher conductivity than Cu when properly engineereed. In this respect, it is worth mentioning the scalability of NiSi nanowires, which do not show degradation of resisitivity when scaled, and are expected to be competitive with Cu at the 11nm technology node. Moreover, since these innovative materials are also investigated for their promising properties as field effect transistors for future technology nodes, there is the likelyhood that these two branches of research, the one being on interconnects, and the other one being on devices, will one day led to a unique platform entirely based on nanowires/nanotubes technology [29].

Another promising interconnect strategy, which can be implemented while keeping the compatibility with the other BEoL solutions is 3D stacked integration. The 3D integration technology was proposed first in 1970's and foresee the scaling of the off-chip wiring to enable stacking of several IC dies. Several 3D circuit processing can be envisioned, perhaps creating additional semiconducting layers of silicon, germanium, gallium arsenide, or other materials on top of an existing device layer on a semiconducting substrate. There are several possible fabrication technologies to form these layers. The most promising near-term techniques are wafer bonding [30], silicon epitaxial growth [31], and recrystallization of polysilicon [32].

A near term goal, will be the integration of off-chip components by the development of disruptive 3D-stacking technology. To this respect, *Through Silicon Via (TSV)* can enable the integration of stacks of different layers, enhancing the communication performance and the integration of new functionality (see Fig. 1.5) [33].

Table 1.1: Challanges and Solutions to Future Logic Scaling following Moore's Law

Challanges	Solutions
Boltzamann's tiranny	Steep slope devices
Increased Current Leakage	high-κ and metal gate
Poly-depletion	Metal Gate
SCE, DIBL	pocket doping, halo doping
GIDL	retrograde doping, floating body channel

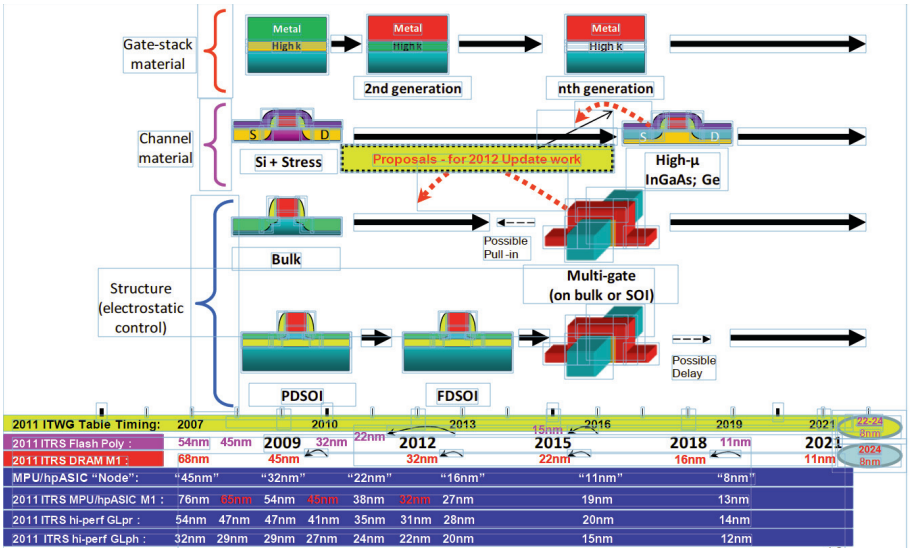


Figure 1.3: ITRS Executive Summary

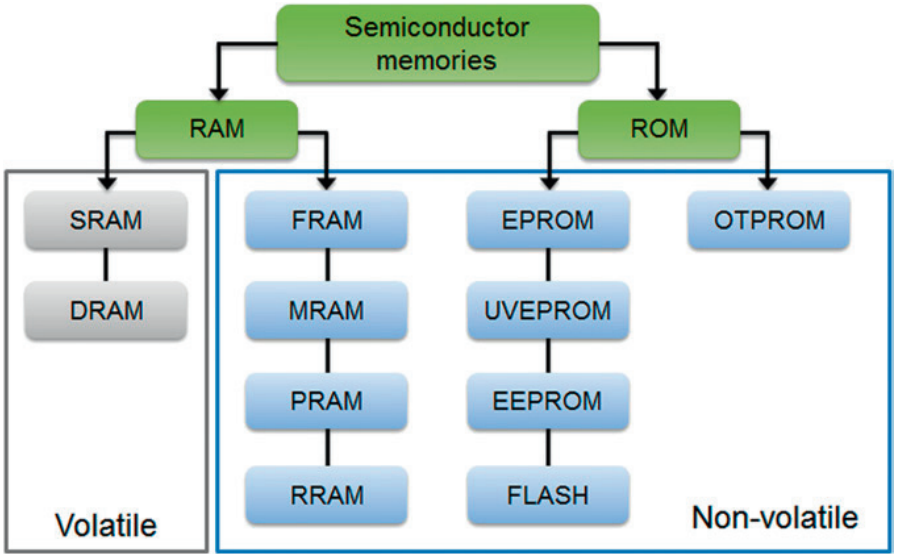


Figure 1.4: Classification of Semiconductor Device Memories

Table 1.2: Comparison of Baseline Memory Technologies

	Stand-Alone DRAM	**Embedded DRAM**	**SRAM**	**Embedded FLASH (NOR)**	**Stand-Alone FLASH (NAND)**
Cell Elements	1T1C	1T1C	6T	1T	1T
Cell Area	$6F^2$	$(12-30)F^2$	$140F^2$	$10F^2$	$4F^2$
Read Time	10ns	2ns	0.2ns	15ns	0.1ms
W/E Time	10ns	2ns	0.2ns	1μs/10ms	1/0.1ms
Retention Time	64ms	4ms	N/A	10y	10y

Table 1.3: Comparison of Emerging Memory Technologies

	FRAM	**MRAM**	**PRAM**	**RRAM**
Cell Elements	1T1C	1(2)T1R	1D1R	1D1R
Cell Area	$22F^2$	$20F^2$	$4F^2$	$4F^2$
Read Time	40ns	35ns	12ns	5ns
W/E Time	10ns	10ns	20ns/50ns	5ns
Retention Time	10y	10y	10y	10y

Table 1.4: Alternative Interconnect Technologies

Technology	**Advantages**	**Disadvantages**
Optical	High Bandwidth	Low density
Plasmonics	High Density	Low Distance
Wireless	Scaling compatible	Process Integration
Nanowires/Nanotubes	High Density	CMOS compatibility

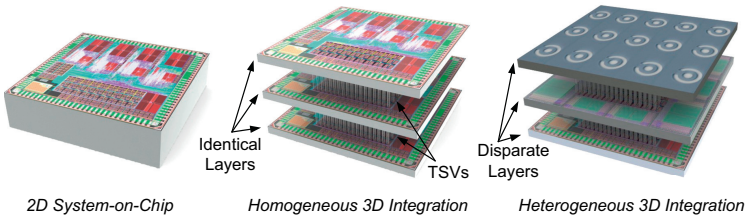


Figure 1.5: Illustration of conventional 2D, homogeneous 3D and hetherogeneous 3D integration.

1.1 Thesis Goals

This thesis focuses on the development of novel devices that bring additional functionality to the CMOS logic and memory, while keeping a CMOS-compatible top-down process flow. In particular, two features of the fabricated devices are investigated: *ambipolarity* in Schottky barrier Si nanowire transistors and *memristive functionality* in both transistors and two-terminal non-volatile transition-metal oxide RAMs. As it is discussed througout the thesis, ambipolarity can be utilized as a new state variable for computation, while the memory effects found in Schottky barrier Si nanowires can also be exploited for applications different than logic, such as volatile memory as well as sensing. It is worth mentioning that distributed memory elements finely integrated with logic can be utilized as bricks for More-than-Neumann architectures[2].

The generality of the memristive device framework enables to categorize the memory effects found for ambipolar Si nanowires and to include them in the large family of multi-terminal memristive devices. One hot topic belonging to the multi-terminal memristive devices family are the Resistive RAMs. In this thesis, Redox RAM based on transition metal oxides are discussed with particular emphasis on the applications for standalone memories, *Field Programmable Gate Arrays (FPGAs)* and TSVs.

1.2 Thesis Overview

Chapter Two

In chapter 2, top-down fabrication and electrical characterization of ambipolar Si nanowire devices is showcased. The chapter content flows from the early process flow, which is a method of fabrication of single nanowire field effect transistors, to more advanced versions, that enable vertically-stacked Si nanowire channels, the use of stencil lithography to pattern 3D gates with high-resolution, the compatibility with *Silicon-On-Insulator (SOI)* and with as made *Polysilicon-On-Insulator (POI)* substrates. In addition, a technique to form ultra-dense vertically-stacked Si nanowire arrays whose vertical and horizontal pitch is not limited by oxidation steps is discussed. Finally, electrical performance of as fabricated ambipolar Si nanowire transistors are discussed and prepare ground of further development, which is then discussed in the two applications chapters, chapter 4 and chapter 5.

Chapter Three

In chapter 3, a general overview of memristive devices, including resistive RAMs and Schottky barrier SiNW transistors is given. The memory effects found in nano-scaled devices are discussed in the frame of extension of the memristive device theory, including multi-terminal

[2] As More-than-Neumann architectures are meant systems for which the infomation processing througput is no more limited by the bandwidth between the data storage and the processing elements [21, 34]

devices. A classification of three-terminal memristive devices is attempted and specific examples are given. Finally, four-terminal Schottky-barrier Si nanowire devices are discussed with respect to the voltage-controlled and current-controlled operation. Further discussions on the applications of multi-terminal memristive devices are given in chapter 5.

Chapter Four

In chapter 4, applications of the ambipolar behavior of Schottky barrier Si nanowire transistors are discussed, and dedicated process flow steps for each application are included. As current CMOS computational throughput is mainly limited by the interconnects, logic blocks that can compute more efficiently are desired. To this respect, three main idea concerning ambipolar devices exploited for logic platforms different than CMOS are developed:

- **Ternary Logic:** ternary logic allows to economize number of digits and, theoretically, faster computation than binary logic [35]. However, the complexity hindered by ternary logic gates prevented the development of ternary logic architectures. Nevertheless, the ambipolarity of Si nanowire transistors can be exploited to build three-state logic, exploting two different ON currents and one OFF current levels. The three-state logic will then apply based on specific gate library which can do the logic translation for a ternary logic level platform.
- **Multi-Value Logic:** current-controlled ambipolar nanowire transistors can be utilized as threshold gates, whose threshold depends on the current bias. This feature is conveniently exploited in a hybrid Si nanowire/Boolean logic gate library to produce multi-level logic gates, such as the NMAX function.
- **Polarity-Controlled Logic:** the fact that ambipolar devices can be tuned to have relevant conductance with both electrons and holes under different gate bias conditions brought about the idea of engineering a device which polarity can be controlled by means of an additional gate. The use of Double-Independent Gate structure to control the polarity of a Schottky barrier transistor is discussed, and shows the potential of building several logic functions with the same device. In addition, the top-down fabrication of a Si nanowire polarity controlled transistor is a a first-time idea which paves the way to more complex polarity-controlled logic, compatible with CMOS and scalable to advanced technology nodes.

Chapter Five

In chapter 5, applications of multi-terminal memirstive devices are discussed. The chapter includes both two-terminal resistive RAMs as the two-terminal memristive devices and three- and four- terminal Schottky barrier memristive Si nanowire devices. As it will be developed in the chapter, the applications of memristive devices does not limit to memory but it can be extended to logic and sensing as well. In particular, the following applications are discussed:

- **Standalone Memories:** The use of resistive RAMs is not a novelty for standalone memory applications, and they can be classified as two-terminal memristive devices. The fabrication and characterization of several resistive RAM in passive crossbar array is discussed.

- **Generic Memory Structure for non-volatile FPGAs:** A new element realized with two bipolar resistive swiching resistive RAMs is discussed for non-volatile FPGA applications. In particular, the element can be utilized either as non-volatile memory element, thus substituting the power-hungry SRAM-based lookup tables, as well as replacement for the pass-gates needed to route the different resources on an FPGA.

- **Resistive Programmable TSVs:** The Through Silicon Via technology is a BEoL enabler for 3D stacked architectures, and it is seen as a performance booster for several applications. One of this could be a 3D-stacked FPGA architecture, for which also the TSV layers connecting among the tiers could be programmed. In this context, a programmable TSV technology is developed and discussed.

- **Sensing:** Multi-terminal memristive Schottky-barrier Si nanowire transistors can be utilized for sensing, thanks to the high sensitivity of the Schottky barriers to external electrical charges. More specifically, thermal sensing and bio-sensing techniques based on the dynamics of the electrical charge within multi-terminal SBFETs is developed and discussed.

Conclusions

In the final chapter the achievements and the original contributions of this work are summarized and a perspective on future work related to the different projects discussed in this thesis are given. Finally I conclude with some perspective future work that can be envisaged from the collective results gathered in this thesis.

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2 Ambipolar Si nanowire Field Effect Transistors

2.1 Introduction

Recently, there has been a huge interest in the physical properties of Si nanowires (SiNW) due to their excellent mechanical [1] and electrical properties [2]. The one dimensionality of SiNWs makes these structures excellent candidates for sensing [3] as well as channels for solid-state Field Effect Transistor (FET) devices [4]. Thus, reliable and inexpensive top-down fabrication methods of SiNWs are of huge interest for several applications. In this respect, stacking multiple layers of nanowires is emerging as potentially powerful approach for building high density systems [5].

One method, proposed by Javey et al. [6], relies on the iteration of contact printing and metallization techniques to stack several layers of nanowire-based circuits (see Fig. 2.1. The key advantage of the technique is that it can be applied to any type of nanowires grown by bottom-up approaches and it can be applied to any kind of substrates, including flexible plastics. However, the throughput of the method is limited by the number of steps and the use of different substrates for nanowire growth and pattern transfer.

Another method to produce vertically-stacked SiNWs is based on Si/SiGe epitaxy (see Fig. 2.2) and has been reported by several groups [7, 8, 9]. The epitaxial method allows for very tight control of the film thickness and therefore, of nanowire dimensions; however, it lacks fabrication compatibility with conventional CMOS processes. Indeed, the number of stacked SiNW levels on a wafer is fixed by the epitaxial layers and careful control on the stress-build up is required in order to obtain reproducible electrical characteristics [9].

A third method recently published [10, 11] leverage on the formation of $SiO_2 - Si_3N_4$ dielectric cavities in which ultradense polysilicon nanowires can be conformally grown and etched. In particular, in [11] low horizontal pitch of about 150 nm and a vertical pitch of 50 nm are demonstrated.

Another method uses *Time Multiplexed Alternating Process (TMAP)* etching, also known as

Deep Reactive Ion Etching (DRIE) or Bosch process in combination with high temperature oxidation to form vertical stacks of SiNWs. Several groups, including the authors, have reported on variations of the TMAP-DRIE process for the fabrication of vertically stacked SiNWs arrays for *Micro-Electro-Mechanical-Systems (MEMS)* [12] and FET devices [13, 14]. Nevertheless, the SiNW fabrication typically relies on thermal oxidation and/or hydrogen annealing techniques [7, 8, 15, 14] which increase the temperature budget.

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the planar transistor design [16, 17]. Considering novel device structures, multiple-gated transistors have been proved of better electrostatic control and larger drive current with respect to the traditional planar transistor design [18, 19]. These features are particularly attractive as enablers for further device scaling and have been already demonstrated circuit feasibility [20]. In fact, double-gate and finFET structures are the first non-planar 3D gate constructions being successfully employed into commercial products.

Nowadays, growing research efforts are spent with *Gate-All-Around (GAA)* constructions with sub-10 nm diameter nanowire (NW) channels, which enable better electrostatic control and performance [17]. Nevertheless, as the dimensions reduce and 3D structures are introduced, major difficulties arises due to the need of scaling while keeping large fabrication yields. The Si nanowire technology has been adopted for its compatibility with the standard CMOS fabrication processes; a remarkable feature with respect to the current trends of evoking revolutionary device concepts, such as spin FETs, carbon nano tube FETs, graphene transistors among others. In fact, if on the one hand Si-based technology has been claimed as to be coming to an end due to the inherent problems of scaling, on the other hand innovations have been brought inside the full hierarchy of CMOS chips, thus at any technology node application-specific issues could be solved so to keep the Si platform.

In order for a technology to be widely adopted, simplicity and cost-effectiveness are important parameters, and in this chapter, several top-down fabrication flows are discussed. Another aspect of research concerning the Beyond CMOS paradigm is the introduction of novel state variables, other than charge, for computation. In this thesis, one example in this direction is given by device ambipolarity. The ambipolar property can be described by the presence of two high conductance states for the same FET, each of these related to carriers of opposite charge values [21]. In Si devices ambipolarity typically emerges from un-doped junctions, and it can be eliminated also in nanowires by epitaxial deposition of doped contacts [22]. Preliminary works on device ambipolarity show how it can be used to compute more complex logic functions per chip [23]. Additionaly, however, in terms of process integration, a few technologies have the flexibility to be implemented within 3D integration schemes and, at the same time, offer the ambipolar property with good CMOS compatibility and electrical performance.

In this chapter, several approaches for CMOS-compatible top-down fabrication of single and

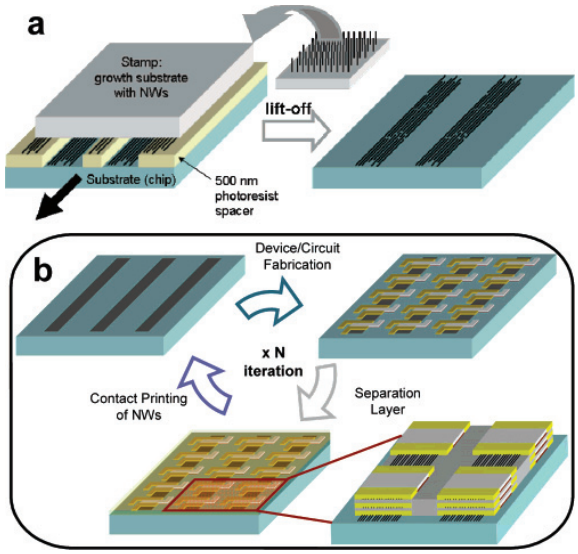


Figure 2.1: Bottom-Up nanowire assembly proposed by Javey et al. [6].

vertically stacked SiNW transitors are showcased and discussed, with considerations between the different technological solutions. Then, in Section 2.3, the electrical characterization is discussed and then, in section , a perspective analysis will guide the reader towards the applications of ambipolar SiNW transistors presented in chapter 4. Finally, in the conclusion section a wrap-up of the achieved results with perspective future work is given.

2.2 Fabrication of Si nanowire transistors

In this Section several top-down fabrication flows are discussed and ambipolar SiNW transistors are characterized. The following text is organized as follows: in Section 2.2.1 single Si nanowire transistor fabrication is discussed in detail. Then in Section 2.2.2 vertically-stacked Si nanowire transistor fabrication method by sacrificial oxydation method is presented. These fabricaton methods have been modified by introducing the nano-stencil lithography methods as explained in Section 2.2.3. Finally, an innovative process flow for the realization of ultra-dense vertically-stacked SiNWs also exploited for the fabrication of FET devices [24] is discussed in Section 2.2.4.

2.2.1 Single nanowire transistors

In the following paragraphs, a simple process flow for single nanowire transistors is presented. The fabrication utilizes optical lithography to define the channel area, and sub-lithographic features are achieved through an oxidation step. The oxidation reduces the dimensions of the Si, and a similar approach has been demonstrated to produce very narrow Si tips [25]. The advantage of this approach is the fabrication of Si nanowire transistors without the need of

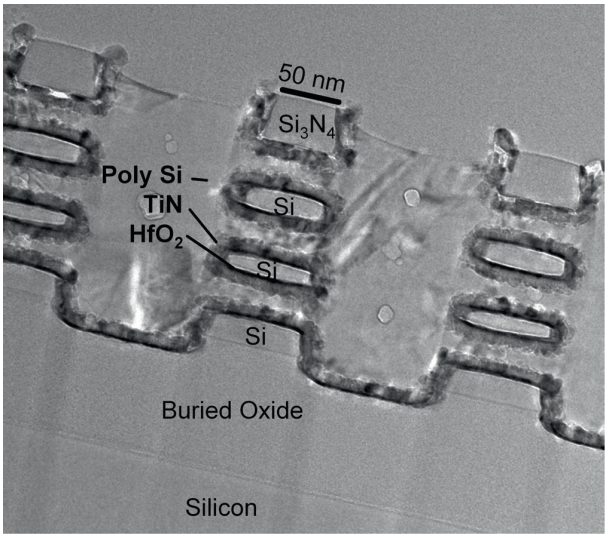


Figure 2.2: Top-Down fabrication of vertically-stacked Si nanowire arrays by epitaxy. [7].

expensive lithographic tools such as EUV or electron beam systems.

Bulk-Si wafers with low boron concetration ($N_A \sim 10^{15}$atoms/cm^3) have been selected as the substrates for solid-state fabrication. The low doping of Si is important in order to obtain mid-gap Schottky junctions, thus providing ambipolar functionality.

The patterning of the Si nanowires on the wafers is carried out by optical lithography with relaxed resolution capabilities ($1\mu m$ critical dimension). The optical mask is realized with an Heidelberg DWL200[1] laser scanner, which transfers the mask design onto a resist that coats a 5inches large Cr/glass mask. The resist is then developed and it is used as an etching mask to pattern Cr. Finally the resist pattern is transferred by structuring the Cr film. This procedure is repeated for each of the layers designed for the microfabrication flow. As a result, a set of Cr/glass masks is fabricated, each with a positive or a negative pattern reproducing one layer of the design.

The optical masks are then utilized to transfer the Cr pattern into photoresist spun onto the device substrates, through another sequence of optical lithography steps.

With the first mask a photoresist pattern is realized to define source/drain and active regions (see Fig. 2.3a). Then a dry Si etch carried out in a plasma etching tool (Fig. 2.3b) . The dry Si etch recipe consists of a plasma etching with a passivation step, defining scalloped trenches attached to Si pillars with high reproducibility. Thus a vertical modulation of the trench width is obtained, a feature that is then exploited to form the nanowire channel. As follows, a sacrificial oxidation is carried out with the double purpose of eliminating the Si where the trench is thinner, and also to reduce the surface roughness intruced by the etching (Fig. 2.3c). If the oxidation is carried out long enough, it can lead to the formation of suspended

[1] www.cmi.epfl.ch

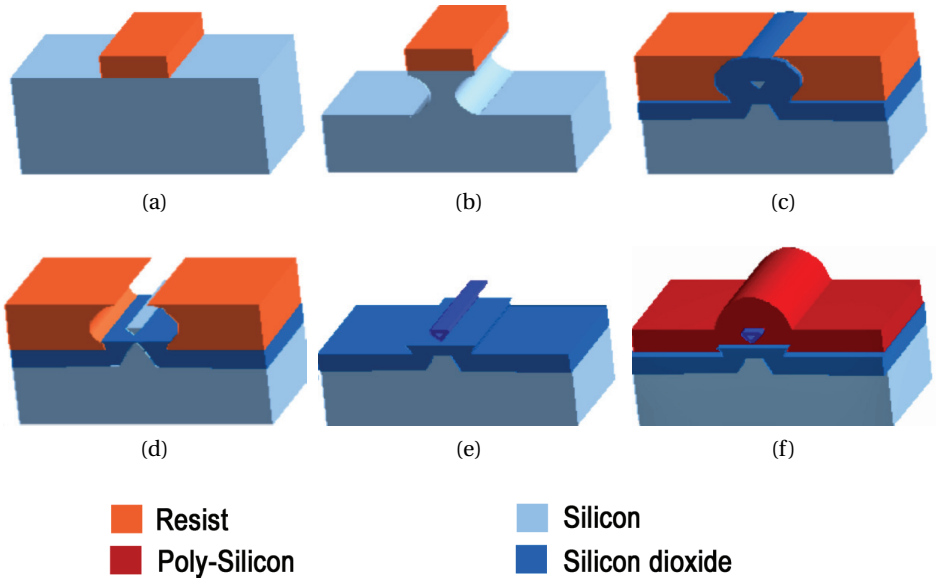
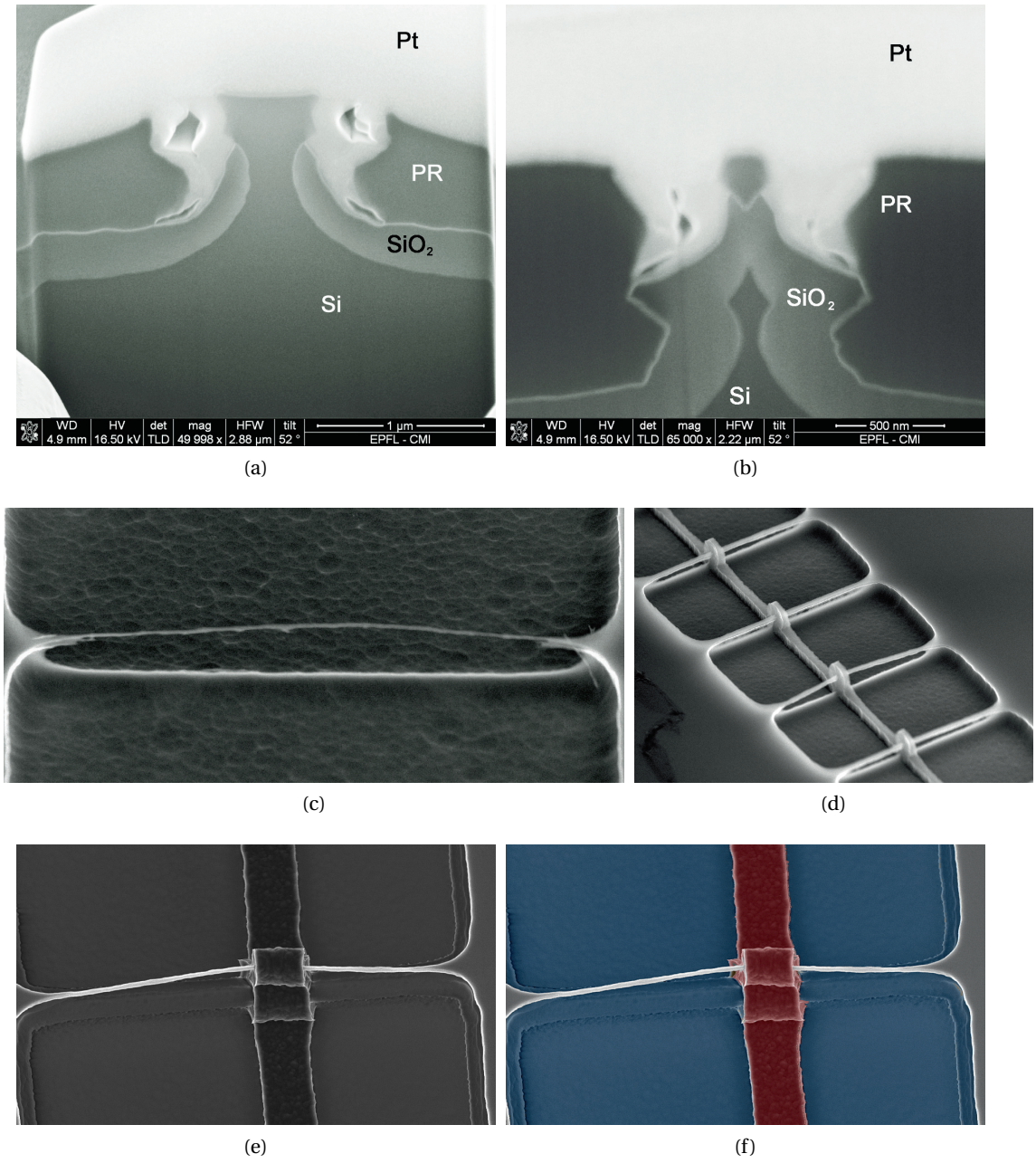


Figure 2.3: GAA SiNW SBFET process flow. (a) A photoresist line is defined for the definition of the nanowire position. (b) A DRIE etching step forms a trench with a scallop. (c) After wet oxidation, the Si trench reduced to a suspended nanowire. The caves are filled with photoresist and planarization is carried out by means of a CMP step. (d) Buffered HF selective oxide etching is stopped as the SiNW release. (e) Gate oxidation. (f) Poly-silicon is deposited and patterned as the gate of the device.

Si nanowire, as it is shown in Fig. 2.4a and Fig. 2.4b. Then a thick AZ9260 *Photo-Resist (PR)* is spin coated onto the substrate, filling the trenches. The resist is planarized by means of a 20seconds long *Chemical Mechanical Polishing (CMP)* step, leaving the sacrificial oxide exposed at the top. A buffered HF etch is carried out to release the single Si nanowire without removing the SiO_2 formed on top of the Si substrate (see Fig. 2.3d). Then, the resist is stripped with a combination of remover and plasma oxygen steps, and further cleaning is performed by the RCA sequence. Then the gate oxide is formed in a horizontal furnace with dry atmosphere (Fig. 2.3e). An example of suspended Si nanowire is shown in Fig. 2.4c, after the sacrificial oxide is removed. polysilicon is conformally deposited by *Low Pressure Chemical Vapor Deposition (LPCVD)* and doped with phosporous by means of a diffusion process. The n+ poly gate is then patterned with a combination of isotropic and anisotropic plasma etching steps (Fig. 2.3f). The resulting structure is a Si nanowire transistor with GAA polysilicon structure (see Fig. 2.4d). The transistor is well isolated from the substrate as it can be seen from the prototype shown in Fig. 2.4e or better in the colored Fig. 2.4f. Then Cr/Ni bilayers (10nm/50nm) are deposited by lift-off on top of the Si pillars, partially covering the SiNW at the anchor points (see Fig.2.5). A NiSi layer is formed by annealing the sample at 450°C for 20min. The Cr is used as adhesion layer for Ni and it moves towards the metal/air interface as silicidation occurs. As shown in Fig.2.5 silicidation of the nanowire starts from the Cr/Ni bilayer toward the gated region of the nanowire.



(a) (b)

(c) (d)

(e) (f)

Figure 2.4: (a) A *Focused Ion Beam (FIB)* cross-section of a Si trench after sacrificial oxidation and partial etching of the SiO_2 layer. The oxidation time of 1hour at 1000°C did not form a suspended SiNW. (b) An FIB cross-section of a Si trench after 2hours at 1000°C lead to the formation of a suspended Si nanowire with pentagonal shape, electrically isolated from a 400nm thick Si dioxide layer. (c) Single Si nanowire suspended at two anchor points after the removal of sacrificial oxide. (d) 4 parallel Si nanowire transistors with 500nm long GAA construction. (e) A suspended GAA Si nanowire transistor with local isolation. (f) Colored image showing the polysilicon GAA (red), the Si nanowire and the anchor points (gray) and the local isolation obtained from the wet oxide (blue).

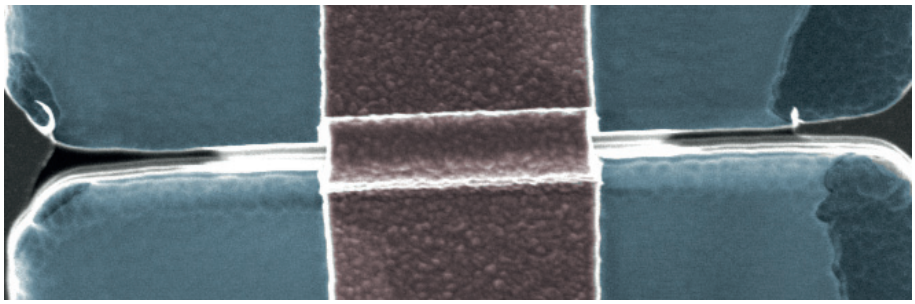


Figure 2.5: GAA SiNW SBFET with Cr/Ni source/drain after the lift-off process. The gate is 4μm long. The change in contrast on the NW channel is attributed to a difference between Si and silicided regions.

2.2.2 Vertically-Stacked Si nanowire transistors

In the following text, a prototypal process flow to fabricate vertically-stacked Si nanowires is presented. Moreover, the microfabrication steps discussed here enables top-down fabrication of Si nanowires at a pitch that is not limited by the lithographic resolution. This approach is utilized to obtain arrays of vertically-stacked Si nanowires by means of the scalloping effect generated by the DRIE technique. While the density of horizontal strands is limited by the lithographic pitch, each strand can be composed of several vertically-stacked nanowires by adjusting the number of cycles set in the DRIE process.

In [15], the process begins by defining a photoresist line on a p-type silicon bulk wafer (see Fig. 2.6a. This mask will be used as protective layer for the successive DRIE technique. This technique, that alternates a plasma etching with a passivation step, has been optimized to produce a scalloped trench in silicon with high reproducibility. Etching time, passivation time and plasma platen power can be changed in order to enhance the scalloping effect. The application of the DRIE technique gives a trench like the one depicted in Fig. 2.6b. The flexibility of the process allows us to change the number of scallops easily. After trench definition, a sacrificial oxidation step is carried out (see Fig. 2.7a). The effect of oxidation results in the total Si consumption of the thinner portions of the trench. The wider parts of the trench leave vertically-stacked Si nanowires embedded in the grown oxide (see Fig. 2.6c and Fig. 2.7b). Then the cavities produced by the etching are filled with photoresist (Fig. 2.6d). After a combination of CMP and BHF dip, the wet oxide is removed around the nanowires (see Fig. 2.6e). After removal of the resist, caves with stacks of several nanowires are freestanding on a layer of thick wet oxide, which is left to isolate the substrate from the successive processes (Fig. 2.6f) and it will later serve to reduce the effect of the parasitic bulk transistor. The nanowires are oxidized in O_2 atmosphere, to form a 10 - 20 nm higher quality oxide, as the dielectric for FET devices (Fig. 2.6g). Then between 200 nm and 500 nm of LPCVD polysilicon is deposited and doped with phosporous through a diffusion process (Fig. 2.6h). The LPCVD polysilicon layer has a conformal coverage of the 3D structure, enabling the formation of gate-all-around devices, such as FETs [15] or optical modulators [26, 27]. The GAA is patterned by means of

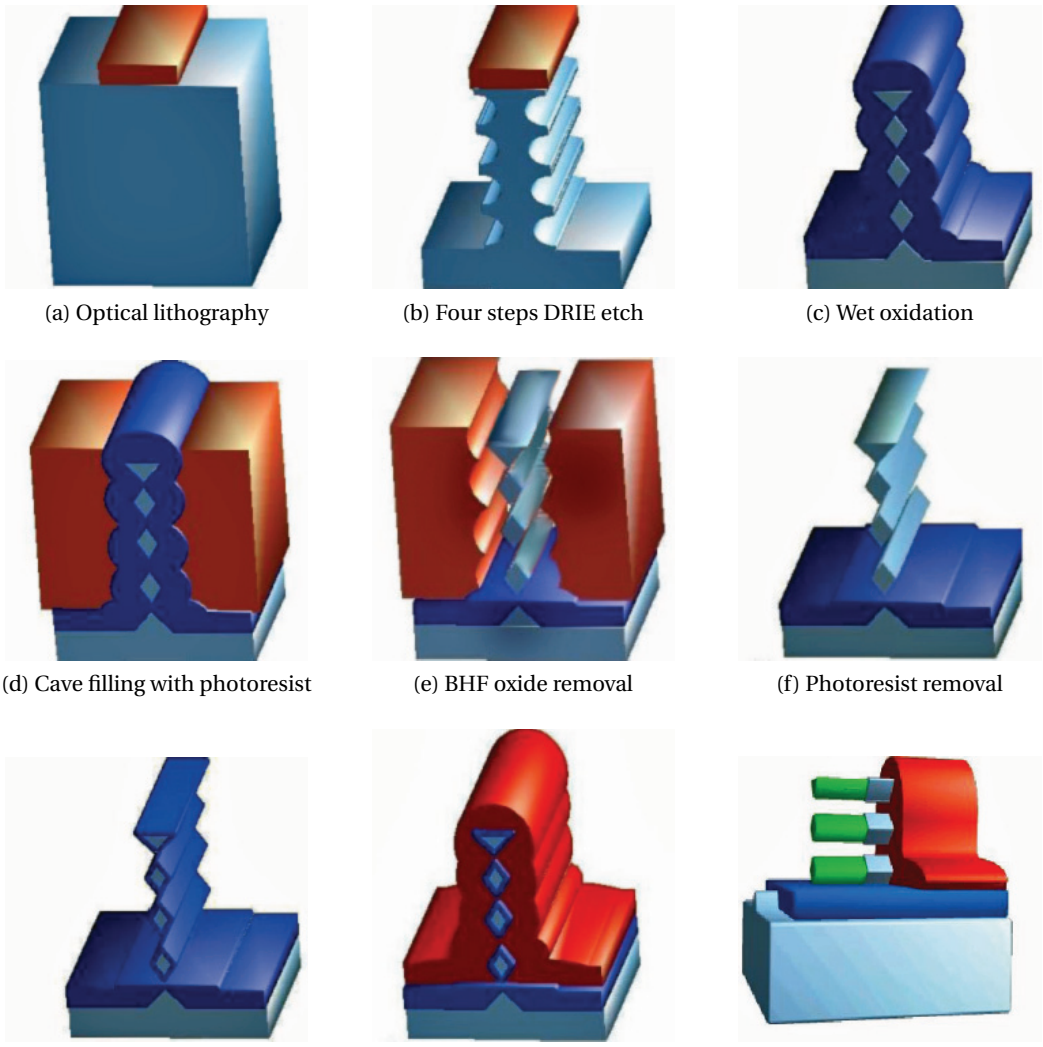
a combination of isotropic and anisotropic recipes, very similar to the DRIE sequence (see Fig. 2.6i). Depending then on the structure, implantation or metalization of the Si pillars can be carried out, so to produce MOSFETs or SBFETs respectively.

Examples of fabricated structures demonstrating arrays having from 3 up to 12 vertically-stacked Si nanowires are shown in Fig.2.7. In Fig. 2.8a, an array of vertically-stacked SiNWs with two parallel polysilicon lines is shown. An FIB cross-section of the gate stack demonstrate good coverage of the LPCVD polysilicon, leading to a conformal GAA construction (see Fig. 2.8b). Moreover, the local isolation tecnique with vertically stacked SiNWs is also demonstrated, as it can be seen in Fig. 2.8c. The rhombic shapes of the Si NWs are probably due to the effect of the stress-built during oxidation, due to the mismatch between the volume of the SiO_2 molecule and the Si [28]. Simulations of the oxide stress, show that oxidation reduces where stress is higher [29]. Indeed, as it can be seen in Fig. 2.9a and Fig. 2.9b, stress is higher at the convex regions than close to the thinner portions of the Si. This effect facilitate the formation of the nanowires. The obtained nanowires can be used to build GAA SINW FETs (see Fig. 2.8) interconnected through Si pillars. Initially, the formed SiNWs have diameters ranging from 70 nm to 200 nm, several techniques can be applied in order to refine the dimensions in a controlled manner. For instance, it has been demonstrated that the use of self-limiting oxidation is capable of producing channels with nanometer dimensions and good controllability [30, 31]. Surface irregularities of the suspended NWs can be improved either by means of a self-limiting oxidation or by hydrogen annealing step [32]. It was found that the proposed fabrication method consistently produces repeatable and very controllable dimensions of clearly separated NW stacks, by optimizing the etch oxidation conditions.

An improved version of the vertically-stacked SiNW formation has been developed in collaboration with M.Zervas on SOIs. By using an ebeam lithography system, *hydrogensilsesquioxane (HSQ)* lines are patterned for the SiNW strands as well as the Si pillars. A dedicated DRIE sequence is then performed, leaving vertically-stacked SiNWs with small diameters down to 20nm. The developed recipes has been tested for several design structures, demonstrating high yield on bulk-Si, SOIs and polysilicon on insulator substrates.

2.2.3 Focus on the Stencil lithography

In the following text, the fabrication of single and vertically-stacked SiNWs on polysilicon-on-insulator substrates is discussed. Moreover, high-resolution stencil lithography has been utilized to define the gate patterns. The stencil lithography is an innovative masking technique for micro- and nano-fabrication that does not require the use of intermediate resist patterning to structure substrates. A stencil mask is instead fabricated with high resolution (typically using ebeam lithography) and clamped with the substate. The stencil acts as a mask for the subsequent processing.

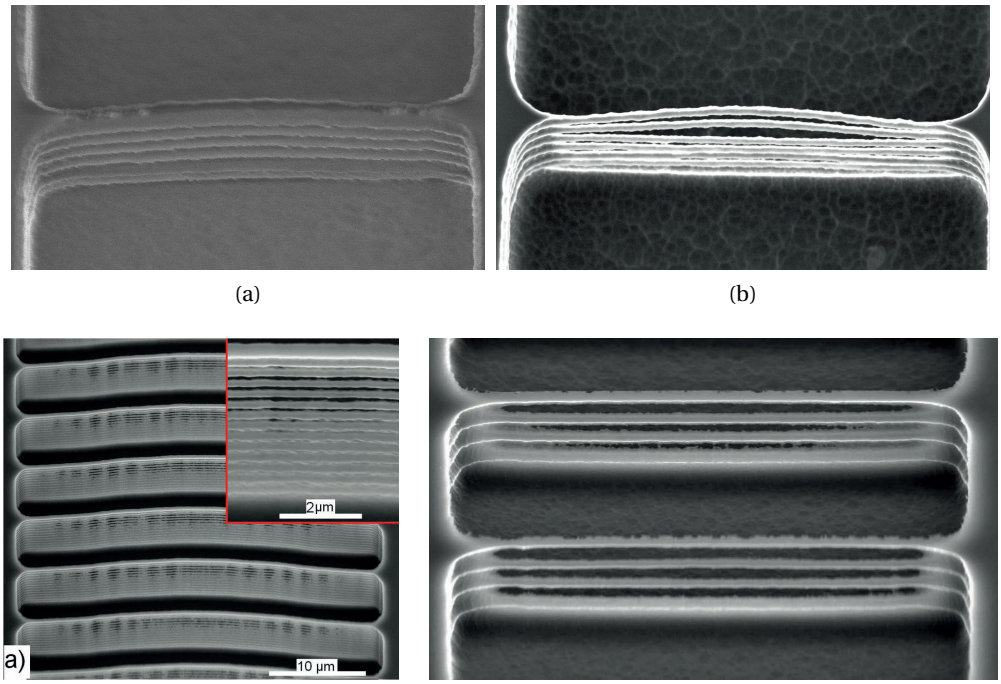


(a) Optical lithography (b) Four steps DRIE etch (c) Wet oxidation

(d) Cave filling with photoresist (e) BHF oxide removal (f) Photoresist removal

(g) Dry oxidation (h) Conformal LPCVD polysilicon deposition (i) polysilicon patterning

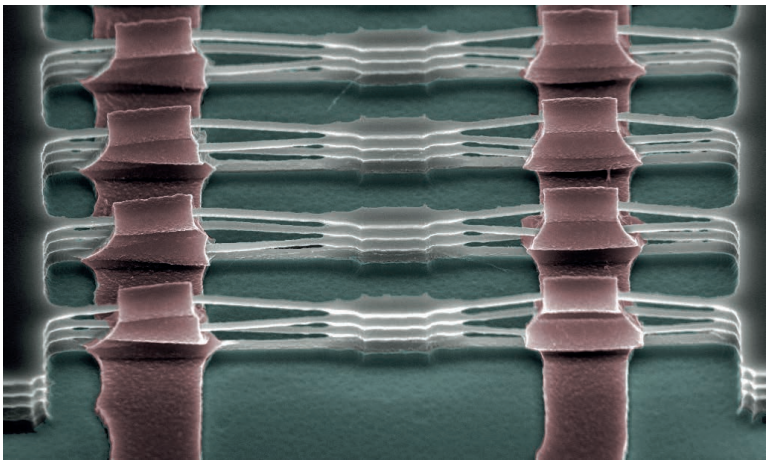
Figure 2.6: Vertically-stacked Si nanowire process steps.



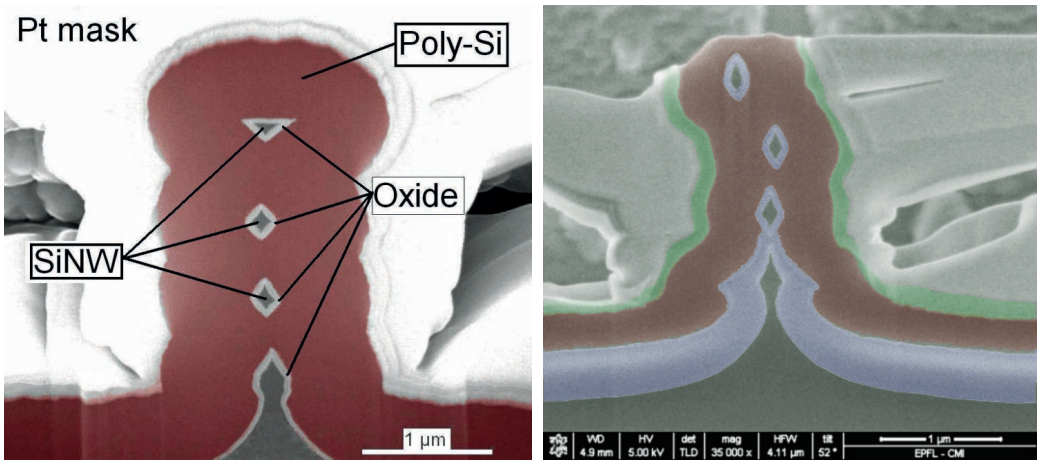
(a) (b)

(c) (d)

Figure 2.7: Arrays of vertically-stacked Si nanowires [15]: (a) A Si trench carved with DRIE process after sacrificial oxidation. (b) Vertically-stacked Si nanowires released after wet oxide removal. (c) Silicon nanowire arrays with 12 vertical levels. (d) Silicon nanowire arrays with 3 vertical levels.

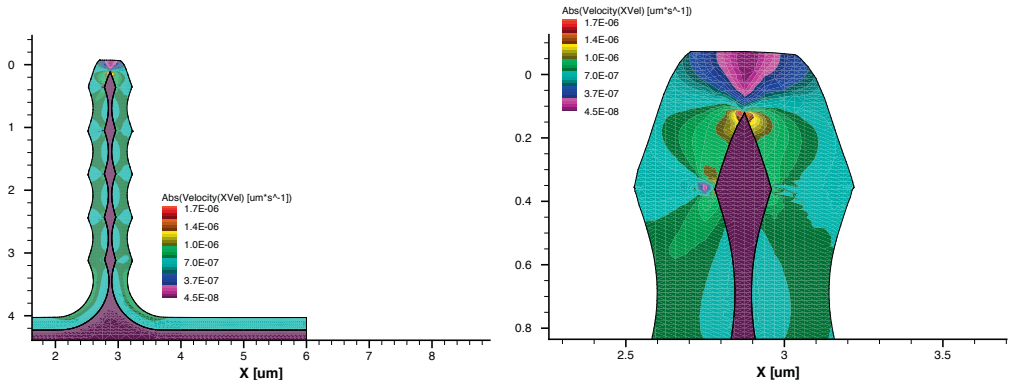


(a)



(b) (c)

Figure 2.8: Vertically-stacked Si nanowire transistors [15]: (a) Three horizontal Si nanowire strands with two parallel polysilicon gates. (b) FIB cross-section showing triangular and rhombic nanowires embedded in a gate-all-around polysilicon gate. (c) TEM lamellae of a device with 3 rhombic-shaped Si nanowires, LPCVD polysilicon GAA (red) and local SiO_2 isolation (blue). The thin green layer is a NiSi polycide formed toghether with the contacts.



(a) (b)

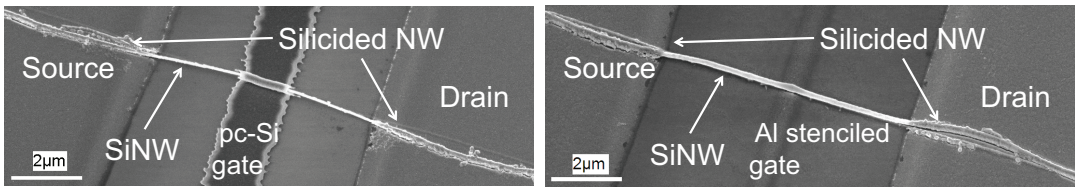
Figure 2.9: (a) Oxide flow rate of a scalloped Si trench. The oxide flow is slower around the regions with smaller radius. This effect explains the rhombic-shaped Si nanowire formation. (b) Oxide flow rate around the top portion of the scalloped trench.

Poly-SiNW transistor fabrication with stencil-lithography

FinFETs with stenciled Al gates are successfully co-fabricated with polysilicon gated devices achieving excellent performance. The difficulty of achieving high resolution gate patterning on non-planar devices is addressed for the first time by means of stencil metal deposition [33]. We envisage the use of this technique also for metal patterning on high aspect ratio FETs, such as vertically-stacked nanowire transistors [15]. It is worth noting that this process can be repeated several times, eventually being used for monolithic 3D integration.

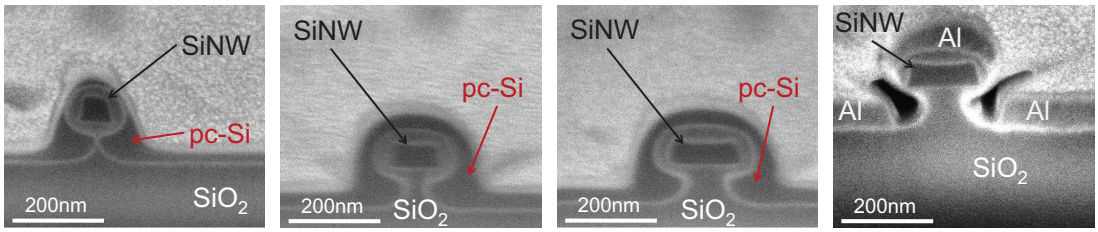
The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500nm thick wet oxide and a 100nm LTO layer. Then a 100nm *amorphous Si (a-Si)* film is deposited as the active layer. A 70nm thick dilution of HSQ is spin coated and patterned with e-beam lithography. Lines having widths ranging from 70nm to 250nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip buffered hydrofluoridric acid (BHF) step. The obtained a-Si nanowires are then covered by a 40nm dry oxide and a 50nm LPCVD polysilicon layers. Large 100μm × 100μm polysilicon pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, polysilicon Ω-gated FinFETs with gate lengths between 1μm and 10μm are obtained.

Then a bi-layer of 20nm Ti/55nm Ni is patterned with lift-off to form electrical contacts between the Si nanowires and the pads. A 400°C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been chosen for its mid-gap workfunction and for its use in a-Si metal induced recrystallization process [34]. Moreover, the contact annealing at temperatures from 400°C and above have been demonstrated to improve channel mobilities in ambipolar Si nanowire transistors [35]. The fabrication flow is completed by



(a) (b)

Figure 2.10: FinFETs with silicided nanowire portions at source/drain contacts:(a) polysilicon FinFET having 2μm long gate and 60nm x 65nm channel cross-section. (b) Al stenciled FinFET having 700nm gate length and 60nm x 140nm channel cross-section



(a) (b) (c) (d)

Figure 2.11: FIB cross-sections showing the nanowire channels embedded in 40nm oxide and gate materials:(a) polysilicon Ω -gate FinFET with 60nm×65nm section. (b) polysilicon Ω -gate FinFET with 60nm×110nm section. (c) polysilicon Ω -gate FinFET with 60nm×140nm section. (d) Al stenciled-gate FinFET with 60nm×140nm section

the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100nm thick SiN membranes with apertures having widths between 100nm and 1μm [36]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2μm [36] accuracy using a customized SUSS MA/BA 6 mask aligner [37]. The clamped substrate-stencil setup is placed in an evaporator where 100nm thick Al gates are deposited.

FinFETs and inverters with up to 62μm nanowire length were fabricated. An example of a 2μm long polysilicon gate FinFET having 100nm × 65nm Si nanowire channel is shown in the SEM tilted view of Fig. 2.10a. In Fig. 2.10b, a Si nanowire transistor with 130nm × 65nm channel (see Fig. 2.11d) cross-section and 700nm large stenciled Al gate is shown. FIB cross-sections (see Figs. 2.11(a)-(c)) demonstrate nanowire channels sections having widths between 65nm and 130nm. The total Si thickness is reduced from the intial value of 100nm to 65nm due to processing. Narrower nanowires (the expected nanowire size was around 35nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

Vertically-Stacked poly-SiNW transistor fabrication with stencil-lithography

The fabrication starts with the substrate preparation for the two separate wafer batches. Bulk-Si wafers are oxidized in wet atmosphere to form 500 nm thermal oxide. Then either 50 nm or 350 nm thick LPCVD polysilicon is deposited as the device layer to build finFETs or vertically-stacked SiNW FETs, respectively. Individual or arrays of lines of widths of 50 nm and length of 8 μm are patterned with diluted HSQ using EBL (see Fig. 2.12a). The HSQ is then used as hard mask for the fins and the vertically-stacked SiNWs etching (Fig. 2.12b). For the fin formation, a Cl_2 based plasma etching is used to obtain vertical sidewalls, whereas for the vertically-stacked SiNWs the etching consists of 3 cycles of passivation and etching steps, alternating low frequency pulses of C_4F_8 and SF_6 plasmas. The etching technique used for the stacked SiNW formation has been calibrated from the recipes previously described for the formation of vertically-stacked SiNWs in crystalline Si substrates [38]. Next, a 10 nm dry oxidation followed by a 100 nm LPCVD polysilicon deposition form the gate stack (see Fig. 2.12c). At the same time a low stress SiN nanostencil mask has been patterned with the gate design. The fabrication details of the nanostencil are described by the authors in a different publication [39].

The nanostencil is made of 100 nm thick LPCVD low stress Si_xN_y. The gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows. Then the nanostencil mask is aligned with a dedicated optical alignment tool and mechanically clamped with the device substrates. After loading the substrates with the nanostencil into a commercial e-beam evaporator, 40 nm Al are deposited, leaving an Al hard mask reproducing the gate design on top of the polysilicon layer (Fig. 2.12d). The Al mask gives better selectivity than SiO_2 hard maks for dry Si etching, thus enabling the patterning of higher aspect ratio structure. Hence, polysilicon gates are etched and Si_xN_y spacers are formed to provide good isolation barrier between the gate and the source/drain regions (Fig. 2.12e). This step is thus used to form pad areas for electrical characterization as well as polysilicon gates with lengths between 100 nm and 500 nm. Finally, a 30 nm thick Ni layer is deposited on the substrates, and a thermal annealing process at 400°C is utilized to form a stoichiometric 1:1 NiSi phase on top of the gates and to metallized source/drain regions. The unreacted Ni that was lying either on top of SiO_2 BOX layer or onto the spacers has been removed with a selective Piranha solution. Thanks to the self-alignment of the Si_xN_y spacers with the gates, self-aligned source/drain regions are formed and the devices are ready for electrical characterization.

The fabricated devices included FETs or inverters designed with different number of channels, having either 1 to 11 parallel SiNWs for the finFETs. For the vertically-stacked SiNWs the same design is used, nevertheless, thanks to stacking 3 levels, the same devices have 3 to 33 parallel SiNW channels. Another difference among finFETs and vertically-stacked FETs is notably the gate structure, which are tri-gates and GAA, respectively. In Fig. 2.13, a finFET with 11 parallel SiNWs and tri-gate construction is shown. The SiNWs are interconnected every 500nm in order to improve the mechanical stifness and so to avoid bending. In Fig. 2.14, a vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter and GAA construction is

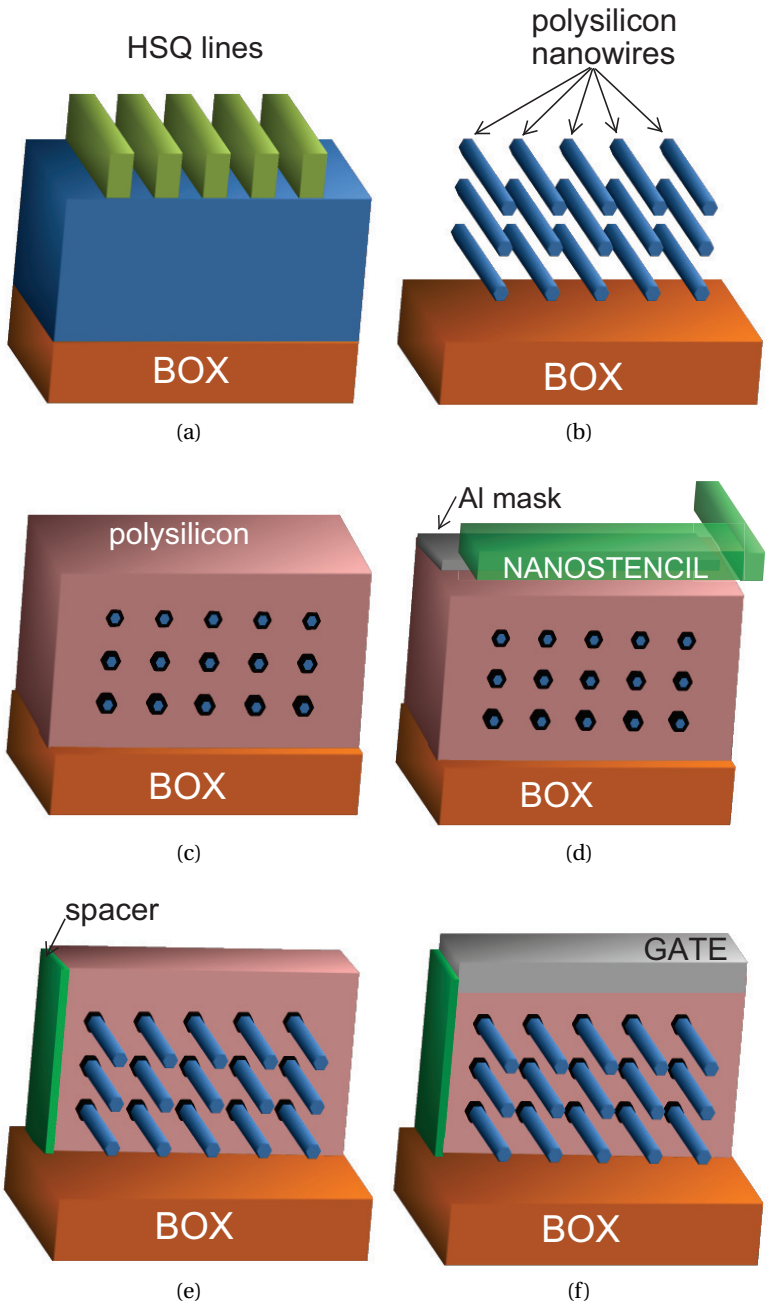


Figure 2.12: Fabrication flow of the vertically-stacked GAA FETs. (a) HSQ lines are patterned with EBL. (b) A DRIE etching process is tuned to form 3 levels of stacked SiNWs. The nanowires are attached to polysilicon pillars at their extremes (not shown). (c) 10 nm dry oxide and 100 nm LPCVD polysilicon are deposited to form the gate stack. (d) A nanostencil mask is aligned and mechanically clamped with the substrate, serving as evaporation mask for Al deposition. The Al is then used as mask to pattern the gate.(e) After gate patterning a Si_xN_y spacer is formed on vertical sidewalls. (f) After Ni blanket deposition and a thermal annealing at 400°C, a Piranha wet etching is used to remove unreacted Ni from either BOX and spacer regions, thus forming self-aligned NiSi source/drain and gate areas.

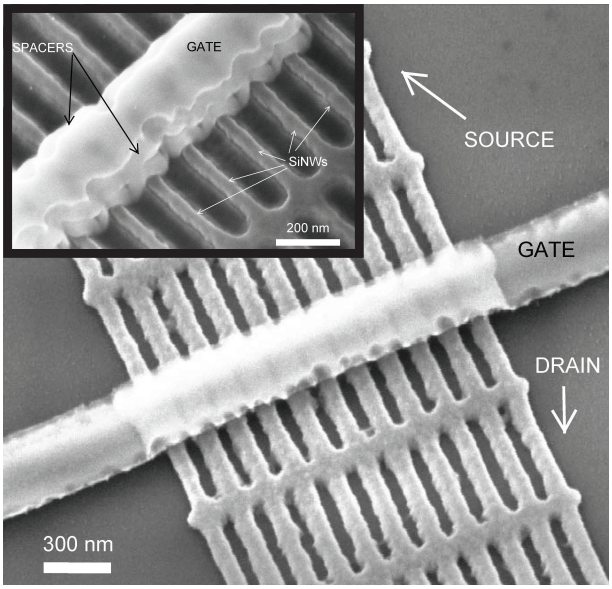


Figure 2.13: Si nanowire FET with 11 channels with 50 nm times 50 nm channel cross-section, 350 nm long polysilicon gate. The nanowires are connected at regular intervals of 500nm in order to improve the stiffness of the structure. In the inset a magnified and tilted SEM view shows the nitride spacers and the SiNWs around the gate structure.

shown. In the inset, conformal coverage of 10nm thick SiO_2 dielectric and LPCVD polysilicon gate is shown.

In all substrates, the design included 150 FETs and 150 inverters, for which the fabrication yield has been checked. In Table 2.1 fabrication yields larger than 70% are reported, showing excellent reproducibility, considering the experimental nature of the process. Moreover, the failing sites have been observed the same for all the substrates, regardless of the process flow. This is the reason for the very similar yield reported for finFETs and vertically-stacked FETs. It is worth noticing that failing devices are mainly related with defects in the mask design, and that this aspect of the work has not been optimized. Thus, the main limitation on the fabrication yield is related with systematic errors in the design. For instance, one of the major fabrication issues is the mechanical stability of the nanostencil, whose robusteness is crucial for the correct patterning of the Al mask. If we consider the device subset of finFET inverters, the the larger yield of 85% is mainly attributed to the lower number of defective nanostencil patterns. Using a smaller size for the nanostencil, which would be a natural consequence when fabricating more scaled devices, improves stability and, at the same time, reduces the frequency of defective patterns. Hence, there is indication that fabrication yields larger than 85% with this process flow is possible with relatively little effort in the mask design.

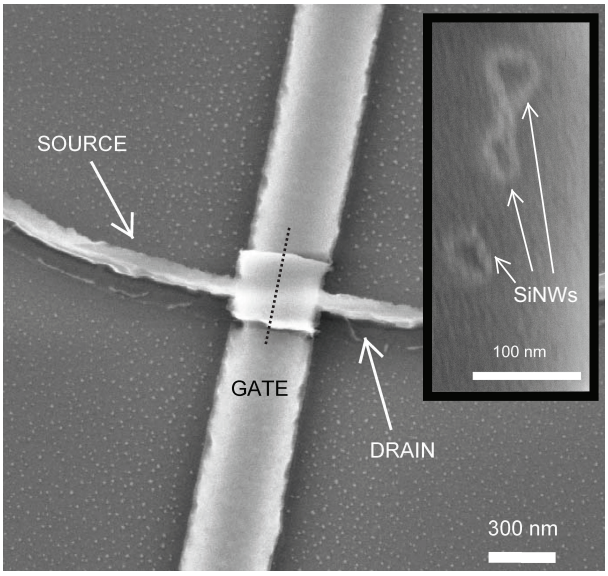


Figure 2.14: Si nanowire FET with 3 vertically stacked single-stranded 30 nm diameter channels. In the inset, a FIB cross-section of the gate shows 3 SiNWs surrounded by 10 nm SiO_2 dielectric and 100 nm LPCVD polysilicon. Gate length is 350 nm.

Yield	finFETs	vertically-stacked FETs
FETs	70%	70%
inverters	85%	84%

Table 2.1: Fabrication Yield measured for the 4 device types.

2.2.4 Ultra-dense Vertically-Stacked SiNWs

Introduction

This section focuses on the top-down fabrication of ultra-high density vertically-stacked SiNWs arrays with sub-50 nm diameter from a single etching step with low thermal budget, without the need for thermal oxidation or hydrogen annealing techniques. For instance, since all processing steps are performed at room temperature,this feature can be used in CMOS post-processing or for flexible polymeric substrates [40], for which temperatures lower than 200°C are needed. Very-high horizontal and vertical SiNWs density is demonstrated for curved and straight geometries with edge-to-edge SiNW spacings down to 60 nm for a cross-sectional density of $2 \cdot 10^{10}/\text{cm}^2$. The etching recipes are optimized to obtain either round- or rhombic-shaped SiNWs. Si fins are also fabricated. Additionally, the number of vertically placed SiNWs in-a-stack can be easily tuned from 1 up to 6.

Fabrication

The process starts with a bulk-Si wafer. The wafer is dipped for 60 s in tetramethylammonium hydroxide (TMAH) for priming the Si surface for hydrogen silsesquioxane (HSQ) coating, after it is dehydrated on a hot plate at 180°C for 10 min. A 150 nm thick HSQ layer is spin coated at 4000 rpm. Then single lines (Fig. 2.15a) and dense arrays (Fig. 2.15b) are patterned using Vistec EBPG5000 e-beam lithography system. Typical HSQ lines are written with 50 nm width with line distance from 50 nm up to 500 nm. After exposure the wafer is developed in TMAH and rinsed in water, acetone and IPA, in order to lower surface tension and avoid stiction. After the exposure the wafers are processed in Alcatel AMS200 DSE Fluorine etcher using different TMAP recipes. Four process parameters are tuned; flow rate, step time of SF_6 and C_4F_8 gases and one design parameter, the distance of the nanowire to the sidewall and pitch for the arrays. In particular, round (see Fig. 2.15c and Fig. 2.15d) and rhombic (see Fig. 2.15e and Fig. 2.15f) cross-sections can be obtained using optimized recipes.

Results and Discussion

The presented work is based on time multiplexed alternating process (TMAP) [41, 42], also known as DRIE or Bosch process. The more advanced etching recipes presented in this work target scallops dimension between 20 and 30 nm, to allow the formation of stacks of nanowires from mask line widths of 50 nm and below. Four technological parameters were adjusted in order to obtain a stable and slow etch rate: flow rate and time step of SF_6 and C_4F_8 gases. The etching rate and profile are mainly determined by three key phenomena:

- Loading effect [43].

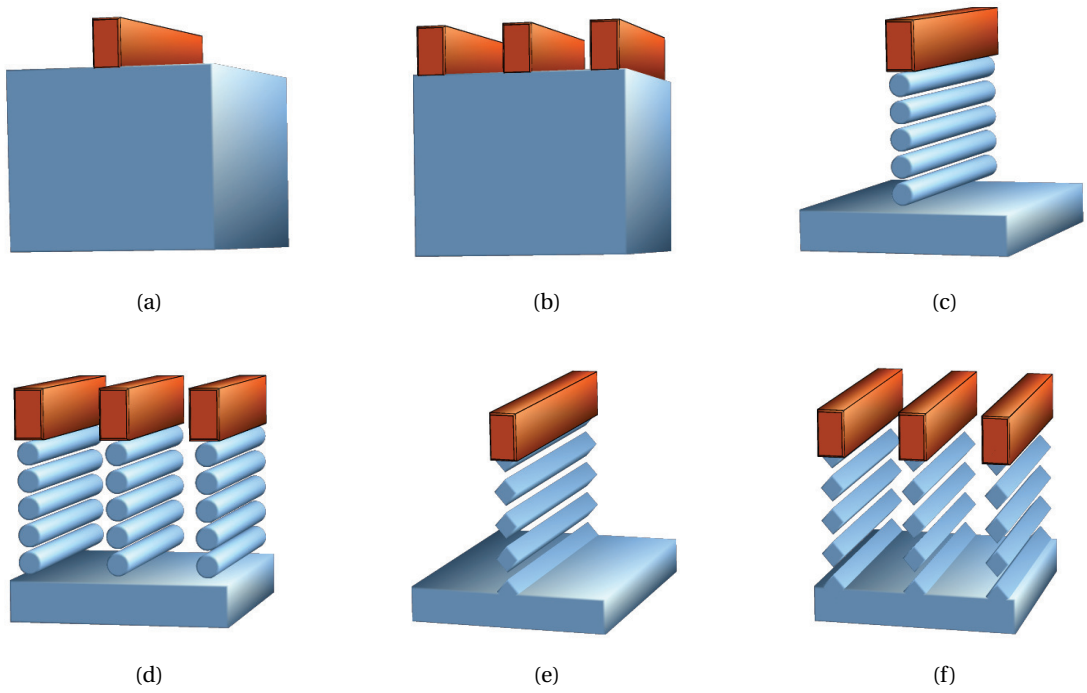


Figure 2.15: Fabrication flow. (a) Single HSQ line patterned on Si substrate. Typical HSQ width is 50 nm. (b) Dense HSQ line arrays. (c-d) After etching with recipe (2) as reported in Table 2.4. (e-f) After etching with recipe (3) as reported in Table 2.4.

- Microloading effect [43, 44].
- Ion induced defluorination of the passivation film (IIDPF) [45, 46].

A quick summary of design and process parameters dependencies with these physical phenomena is given in Table 5.1. More details are explained in the following paragraphs.
The loading effect [43] is the decrease of the etching rate of the reactive ion etching due to the increased area exposed to the SF_6 plasma. In our test structures more than 90% of total wafer area is exposed. In case the pattern is required to cover more than 50% of the total wafer area then the loading effect can not be used as part of the strategy to lower the etch rate.

A special case of the loading is the microloading effect. The microloading effect is the etching rate degradation due to the high density of a pattern, the main mechanism for microloading is, etchant depletion [43, 44]. Etchant depletion happens inside an etching trench and it is due to the difficulty for the etchant species to be replenished, as the etching opening reducing. The smaller the nanowire pitch, the lower the etch rate. Microloading can be controlled by flow rate. Thus, reducing the flow rate it reduces the rate at which the etchants are replenished leading to etchant depletion, magnifying the microloading effect.

The TMAP consists of the alternation of etching and passivation steps. At the beginning of each etching cycle the plasma needs to remove the passivation at the bottom, deposited at the passivation cycle. The time needed for the passivation removal is a function of its thickness, which in turns is controlled by C_4F_8 flow rate and time step. The time needed to clear the passivation is very short in standard TMAP processes. However, this effect is not negligible for nano-scale etching, as the passivation etching time becomes comparable with the total SF_6 time step. Similarly, thicker passivation films reduce the Si etching rate [41] since a larger fraction of the SF_6 step is needed to remove the passivation.

To keep the etching rate low, the time step and flow rate of SF_6 needs to be kept as low as possible. Thin passivation layers should be used in order to avoid micrograss formation [41]. The downside of very thin passivation layers is that ion induced defluorination, the ion bombardment assisted desorption of fluoride from the carbofluride film, creates chemical species in the passivation film that etches away the underlying Si [45, 46]. The favorable aspect of low SF_6 flow rate is reduced roughness due to higher local plasma uniformity [44].

This effect can be exploited to affect the cross-section of the nanowires with the following mechanism: (1) The diameter of the nanowire is reduced isotropically (2) Sharp points and low dimension features are removed first, creating an elliptical shape.

The etching of vertically stacked SiNW arrays is investigated for the following designs:

Phenomena	Design variation	Process variation	Common problems	Effect
Loading [43]	Reduce exposed area	N/A	N/A	Reduced etching rate
Microloading [43, 44]	Denser patterns.	Reduce SF_6 1) Flow rate 2) Time step	1) Micrograss [41] 2) Formation of fins instead of SiNWs	1) Reduced etching rate. 2) Reduced roughness [44]
IIDPF [45, 46]	N/A	Reduce C_4F_8 1) Flow rate 2) Time step	Complete etched away structures	Alter cross section from rhombic to elliptical

Table 2.2: Experimental design and process parameter dependencies with the main physical phenomena affecting the nano-scale TMAP process.

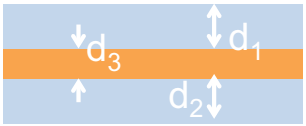
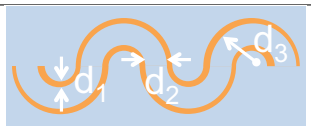
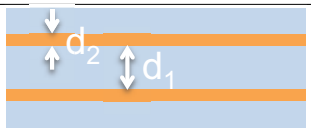
Mask design	Top View	d_1	d_2	d_3
Straight-line nanowire stacks		trench opening: 100, 200, 500 nm	trench opening: 100, 200, 500 nm	nanowire width: 50, 100, 150 nm
Curved-line nanowire stacks		trench opening: 200 nm	nanowire width: 50 nm	outer diameter: 250, 450, 850 nm
Ultra-high density arrays		pitch: 50, 60, 75, 100, 200 nm	nanowire width: 50 nm	N/A

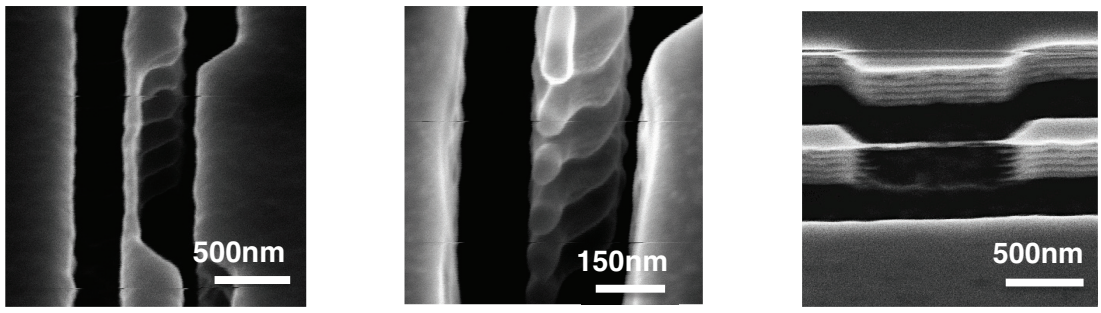
Table 2.3: Mask design parameters for straight lines, curved lines and dense array nanowire structures.

- Straight-line nanowire stacks.
- Curved-line nanowire stacks.
- Ultra-high density arrays.

Process development has been carried out by parameterizing individual device design in order achieve a high repeatability and fabrication yield. In Table 2.3 the design parameters are listed. In the following sections each device type is addressed separately.

Process recipes	SF_6 [cm^3/min]	SF_6 [s]	C_4F_8 [cm^3/min]	C_4F_8 [s]	Mask design (see Table 2.3)
(1)	300	3	150	1	straight-line nanowire stacks
(2)	200	2.5	150	1	curved-line nanowire stacks, ultra-dense arrays (d_1 = 75, 100, 200 nm)
(3)	200	2.5	100	1	ultra-dense arrays (d_1 = 50, 60, 75 nm)

Table 2.4: Recipes overview optimized for different mask designs. The substrate temperature is kept at 20°C.



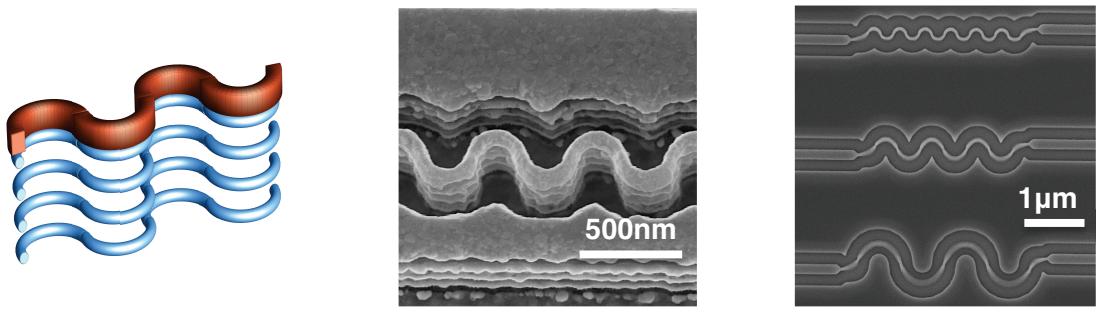
(a) (b) (c)

Figure 2.16: Vertically stacked 50 nm diameter for straight-line nanowires carved inside a 200 nm narrow trench. (a) Bird's eye view. (b) Cross-section. The etching parameters are 300 cm^3/min and 3 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (c) Tilted view of a straight-line nanowire stack carved in a 500 nm wide trench. Due to a reduced etchant depletion effect, all the nanowires but the top one are overetched.

Straight-line nanowire stacks

Lines widths of 50 nm, 100 nm, 150 nm are written with lengths 100 nm, 200 nm, 0.5 μm, 1 μm, 2 μm. The patterns are placed inside a trench to reduce and control the etching rate through microloading. Trench opening of 100 nm, 200 nm and 500 nm are designed. Flow rate used are 300 cm^3/min for SF_6 and 150 cm^3/min for C_4F_8 with step times have 3 s and 1 s respectively. The process can achieve very good repeatability, with a wire diameter variation of less than 10 nm. The smallest fabricated structures for the straight-line design are nanowires obtained from 50 nm mask line width, 200 nm trench opening and of independent length. In Fig. 2.16a and Fig. 2.16b a stack of six nanowires is shown in bird's eye view and cross-section, respectively.

The importance of the trench opening dimension is established by the observation that, for 500 nm trench opening nanowires are not formed (see Fig. 2.16c) while for 200 nm trench opening, while using the same process, 50 nm nanowires are fabricated (as shown in Fig. 2.16b). The trench opening etching rate dependence can be explained by the microloading effect causing local etchant depletion.



(a) (b) (c)

Figure 2.17: (a) Concept view of vertically-stacked curved nanowires. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (b) Bird's eye view of the nanowire stack covered by a 50 nm thick Pt layer for conformal PtSi silicide formation. (c) Top view of the three curved nanowire design.

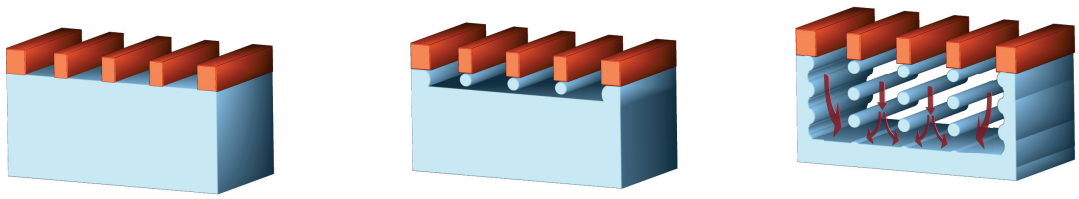
Curved-line nanowire stacks

Curved line nanowires are patterned with a line width of 50 nm. The patterns are carved into Si as for the case of straight-line nanowires, as depicted in Fig. 2.17a. The trench opening is kept constant at 200 nm. The pattern consists of semi-circles connected in a serpentine fashion. Three circle diameters are explored: 200 nm, 400 nm, and 800 nm, as shown in Fig. 2.17c. In Fig. 2.17b a bird's eye view of a stack of three nanowires with 200 nm circle diameter encased in Pt is shown.

A drawback of the design is that the trench opening cannot be kept constant in case the circle diameter is double the trench opening, as can been seen from Fig. 2.17c by comparing the designs with 200 nm and 800 nm diameter. Etching rate is faster where trench opening is wider, again due to microloading effect. To reduce the etching rate created by the irregular trench openings a reduced flow rate recipe is used. Flow rate of 200 cm^3/min for SF_6 and 150 cm^3/min for C_4F_8 were used where step times are 2.5 s and 1 s respectively.

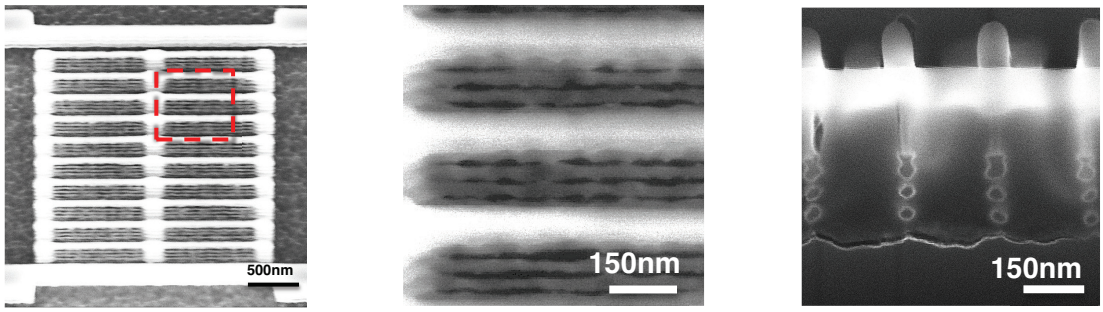
Ultra-high density arrays

Dense array designs for 50 nm line widths and pitches ranging from 100 nm to 300 nm were explored for lengths from 100 nm up to 50 μm. The array pattern was etched faster than the reference case of the straight line nanowires explained in Section 2.2.4. This could be due to the vertical nanowire separation that alters the etchants flow once the nanowire is released as illustrated in Fig. 2.18, countering this effect is microloading that slows down etching rate the denser the array gets. Two recipes are selected: the first is optimized for 200 nm trench opening and it uses 200 cm^3/min for SF_6 in 2.5 s time steps and 150 cm^3/min for C_4F_8 in 1 s time steps. In Fig. 2.19 a stack of 3 nanowires, which is fabricated with the first recipe, is shown in bird's eye view and cross-section. Average diameter of the SiNWs is 30 nm and pitch is



(a) (b) (c)

Figure 2.18: (a) Dense array before etching. (b) Nanowire formation at etching time step t_1. (c) After 4·t_1 3 levels of SiNWs are obtained and a fourth one begins to form. The arrows indicate the plasma flow directions.



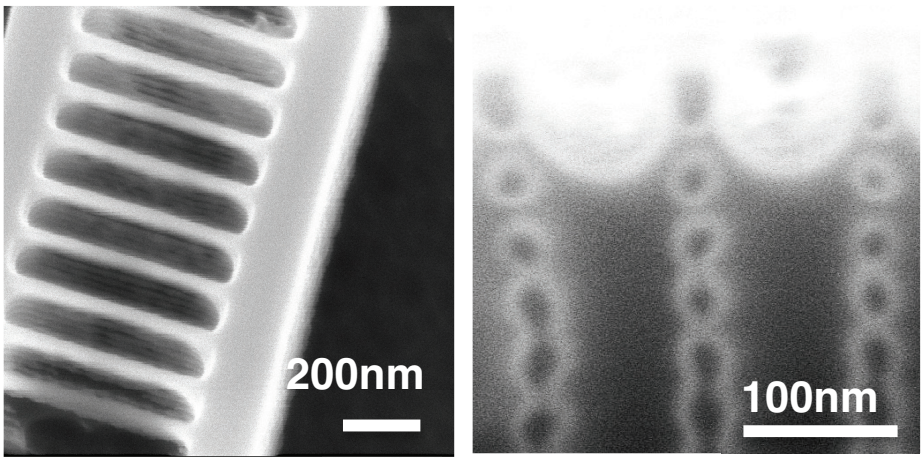
(a) (b) (c)

Figure 2.19: Examples of nanowire arrays with 200 nm pitch, 1 μm length and 30 nm average diameter. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 150 cm^3/min and 1 s for C_4F_8. (a) Bird's eye view. (b) High magnification showing the vertical stacks. (c) Cross-section of the vertically stacked array.

200 nm. The length of the nanowires is 1 μm. The same recipe is used to fabricate a stack of six round SiNWs with pitch of 75 nm and 300 nm long (Fig. 2.20a) and SiNW diameters of 20 nm (Fig. 2.20b), producing repeatable SiNW structures with minimal diameter variation. The second recipe is designed for denser arrays and uses 200 cm^3/min for SF_6 for 2.5 s and 100 cm^3/min for C_4F_8 for 1 s. A stack of six rhombic SiNWs with pitch of 75 nm (Fig. 2.21a) is fabricated for 75 nm horizontal and 60 nm vertical spacings. Typical SiNW diameter is 10 nm with lengths of up to 550 nm, yet diameter variability is larger compared to earlier examples. Higher density arrays lead to the formation of scalloped fins, as shown in Fig. 2.21b.

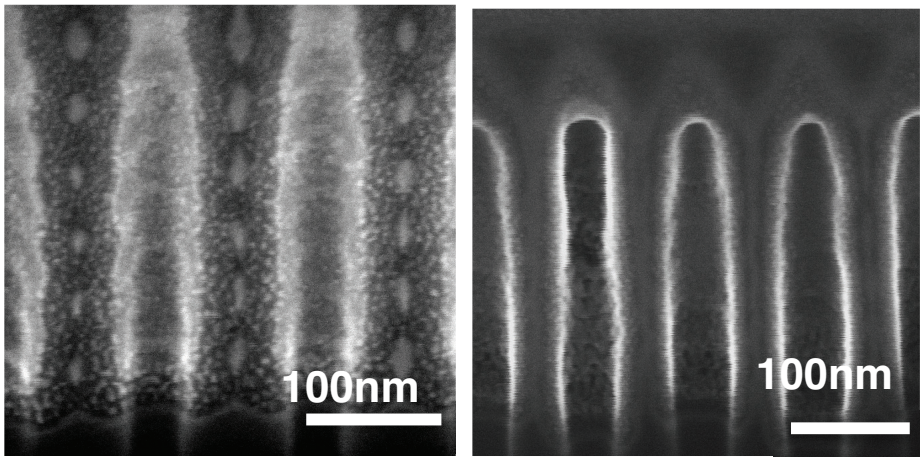
Summary

Vertical stacks of SiNWs with round or rhombic shapes of diameters down to 10 nm are fabricated using a simple TMAP process in bulk Si with very-low thermal budget. To our knowledge, the cross-sectional nanowire density of $2 \cdot 10^{10}/cm^2$ result is among the highest for top-down fabricated SiNWs arrays reported in literature. Moreover, SiNWs arrays with lengths from 50 nm up to 1 μm and horizontal inter-wire spacing ranging between 50 nm and 200 nm



(a) (b)

Figure 2.20: Examples of dense nanowire arrays. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 150 cm^3/minand 1 s for C_4F_8. (a) Bird's eye view of a 550 nm long wires with 200 nm pitch cut with FIB. (b) Cross-section for an array with 300 nm long wires and 100 nm pitch. The average nanowire diameter is 25 nm.



(a) (b)

Figure 2.21: Examples of dense nanowire arrays. Etching parameters are 200 cm^3/min and 2.5 s for SF_6, 100 cm^3/min and 1 s for C_4F_8. (a) Cross-section showing 18 SiNWs (3 parallel stacks with 6 levels each) having 75 nm horizontal spacing and 60 nm vertical spacing, with rhombic cross-sections. Average diameter is 25 nm. (b) Cross-section showing scalloped fins for 50 nm horizontal spacing (dimension d_1 for dense array design as in Table 2.3).

are demonstrated. The technique is presented in terms of its potential use for the fabrication of a broad range of nano-scale devices, from NEMS, to nano-electronics and sensing.

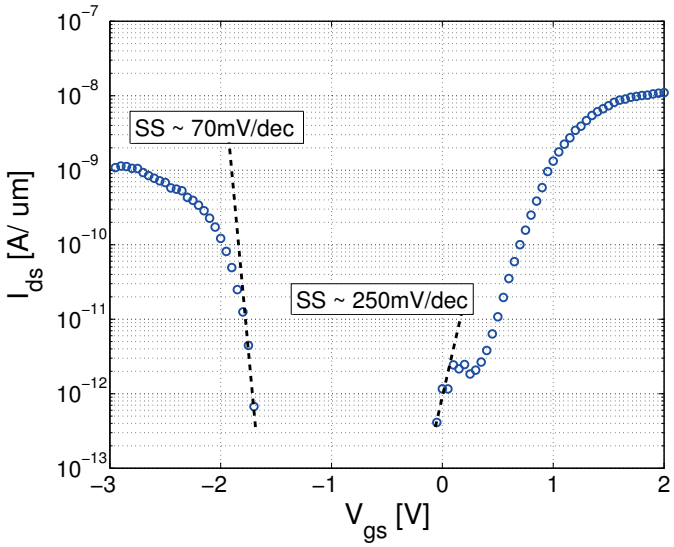


Figure 2.22: Ambipolar $I_{ds} - V_{gs}$ curve at V_{ds}=1V.

2.3 Electrical Characterization

All the devices presented in this chapter presented ambipolar conductance, according to the expectations for Schottky barrier SiNW devices. In this section, electrical results concerning SiNW SBFETs are presented and discussed.

2.3.1 SiNW transistor on SOI

The earliest example, showed ambipolar conductance with good performance of both the n- and p-branches (see Fig.2.22). The device was fabricated on SOI and had 5μm long gate and 930nm wide channel. The impact of the source/drain junction distance with the gated region is observed on a different device, for which the gate to junction distance is about 1μm. As presented in Fig.2.23, the $I_{ds} - V_{gs}$ curve shows larger SS, which is attributed to the partially-gated regions of the channel. Comparing Fig.2.22 and Fig.2.23, it emerges that the non-gated portions of the channel in SBFETs are very sensitive to the fringing field generated by the gate, and that this feature can be exploited to control the polarity of the device with a second gate.

2.3.2 Poly-SiNW FETs with Stencil Gate

Then, a second batch with poly-Si nanowire channel has been fabricated and characterized on insulating substrates. FinFETs with stenciled Al gates are successfully co-fabricated with poly-crystalline Si (polysilicon) gated devices achieving excellent performance. The $I_{ds} - V_{gs}$ curve of a polysilicon Ω-gate FinFET has a typical ambipolar behavior, with a higher conductance

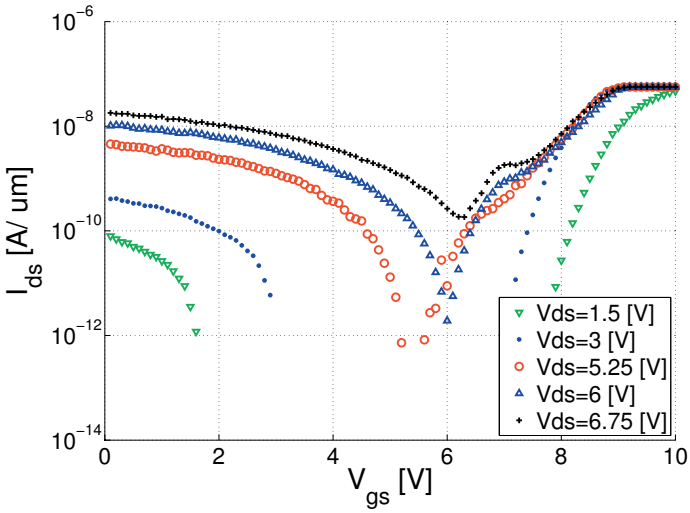


Figure 2.23: Ambipolar $I_{ds} - V_{gs}$ curve at V_{ds}=1V.

for holes (at negative V_{gs} voltages) than for electrons (Fig. 2.24a). In the holes-conductance regime, a subthreshold slope SS $\approx$ 420mV/dec is observed, while a larger SS is observed for the electron-dominated current. The gate misalignment error is source of variation for the channel series resistance which in turn impacts the overall current conductance. Nevertheless, the main limiting factor for the current conductance is the injection of carriers over the Schottky barrier, and the series resistance is considered to play a minor role. This aspect is confirmed by the observation of a lower I_{ON} for electrons than holes over a large number of samples. In Fig. 2.25, the average I_{ON} for holes and electrons is shown. The I_{ON} increase linearly with the channel width, which is calculated as the perimeter of the SiNW, since volume inversion effect are negligible for SiNW-channel diameters larger than 10nm.

Conversely, Al-gated devices show a p-type conductance mainly (see Fig. 2.24b), which can be explained with Al contamination at pad regions due to the stencil process. This is also reflected in a SS $\approx$ 200mV/dec, indicating that doping can effectively be used to improve SS by suppressing the ambipolar conductance. In both devices, I_{ON}/I_{OFF} ratios of more than 6 orders of magnitude are observed. The lower current for the n-branch in the Al gated devices might be due to metal gate-induced doping. The transfer characteristic of polysilicon Ω-gate inverters show (Fig. 2.26) an output voltage range V_{out} compatible with the input voltage range and a gain of $\Delta V_{out}/\Delta V_{in} \approx 4$. Thus, polysilicon gated inverters are suitable elements for cascading additional devices, enabling the construction of more complex circuits. Similarly, a current bias scheme for FinFETs can be used to obtain pseudo-inverter operation, which consist in using a current bias scheme as depicted in Fig. 2.27. For pseudo-inverter operation a triangular voltage transfer characteristic is obtained, with very low power consumption (≤1.2pW). Data from different dies on the wafer show stability of the V_{in} value for which inversion occurs (V_{th}) under different current bias (see Fig. 2.28a). Moreover, as it is shown in Fig. 5.24b, the maximum of V_{out} increases linearly with the current bias.

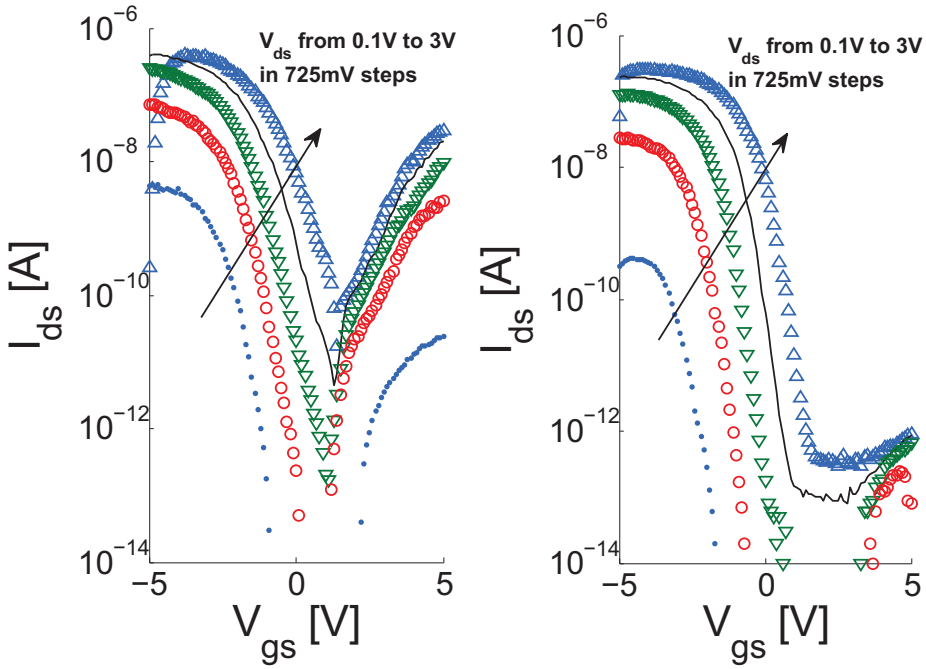


Figure 2.24: (a) Ambipolar $I_{ds} - V_{gs}$ curve of a polysilicon Ω-gated FinFET having 1μm gate length and 60nm × 110nm nanowire section. (b) Ambipolar $I_{ds} - V_{gs}$ curve of a stenciled Al-gate FinFET having 1μm gate length and 60nm × 110nm nanowire section.

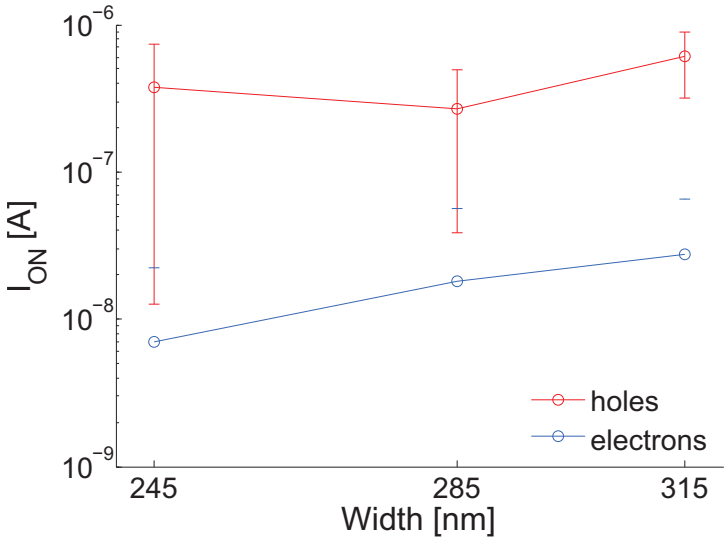


Figure 2.25: Average I_{ON} for holes and electrons of polysilicon Ω-gated FinFETs of different widths. The error bar represents the standard deviation over a sample of 8 devices.

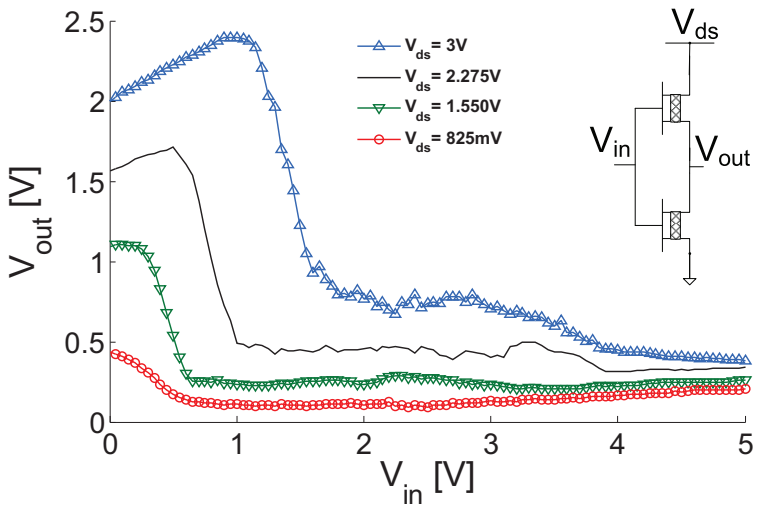


Figure 2.26: Voltage transfer characteristic of a 2 in series connected polysilicon Ω-gate FinFETs on-a-wire and biased as for inverter operation. The insets represents the inverter bias scheme. Two ambipolar polysilicon FinFETs are connected in series.

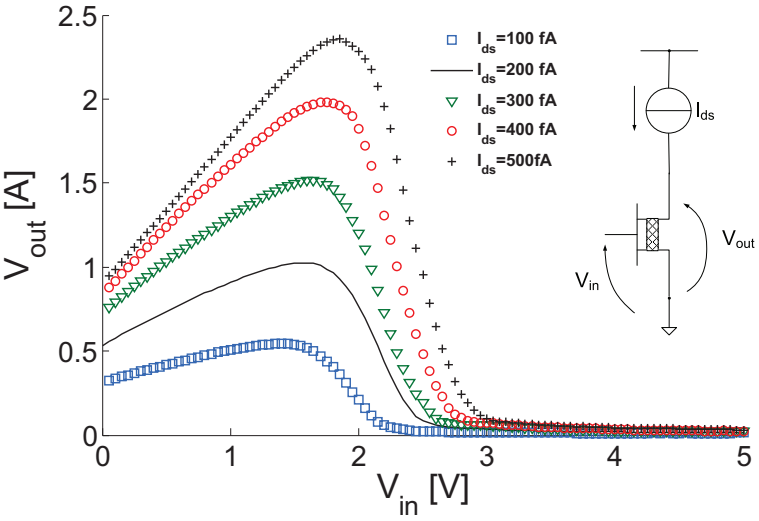
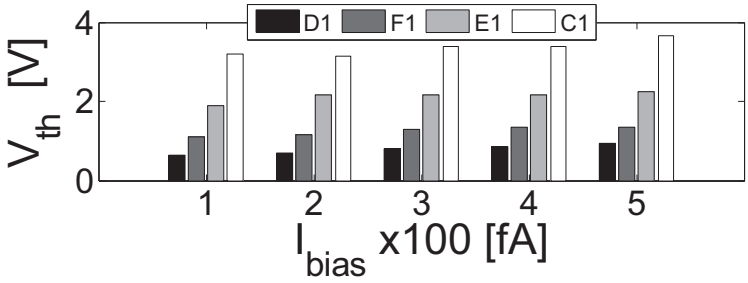
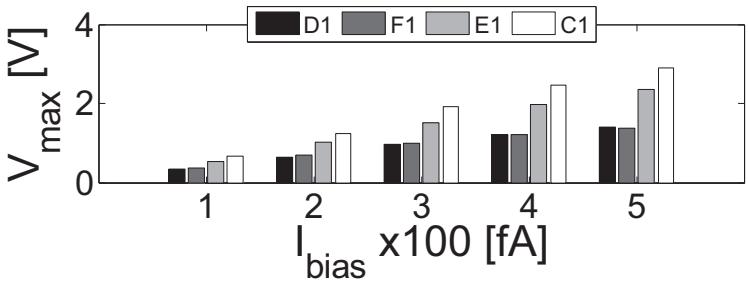


Figure 2.27: polysilicon FinFET biased for pseudo-inverter operation having 2μm gate lengths and 60nm x 110nm channel cross-section. The insets shows the pseudo-inverter bias scheme using a single polysilicon FinFET and a current source.



(a)



(b)

Figure 2.28: (a) Threshold voltage (V_{th}) values for the polysilicon gated pseudo-inverters. The inversion voltages are stable under different current bias. (b) Maximum output voltages values for the polysilicon gated pseudo-inverters. The V_{max} values tend to increase linearly with I_{bias}

2.3.3 Vertically-Stacked polysiliconNW FETs with Stencilled Gate

Electrical characterization is carried out with a manual probe station connected to a Agilent B1500 semiconductor parameter analyzer. Tungsten tips are put in contact with the polysilicon source/drain pads and on the Al/polysilicon gate pad. Typical $I_{ds} - V_{gs}$ curves are first measured for finFETs which show large inverse subthreshold slopes of about 1500 mV/dec and average $I_{ON} - I_{OFF}$ ratio of 3 orders of magnitude. These results are then compared with the electrical performance measured for the vertically-stacked GAA NW FETs. The $I_{ds} - V_{gs}$ curves (Fig. 3.11b) for the vertically-stacked FETs with 3 stacked SiNWs show typical device ambipolarity with inverse subthreshold slopes for n- and p- branches up to 300 mV/dec and up to 1300 mV/dec, respectively. Notice the strong dependence of the p-branch with applied V_{ds}. This undesired behavior is largely compensated for, in the devices with 3 times 11 parallel fingers, as shown in Fig. 2.30. The apparent robustness with respect to short channel effects is attributed to the different geometry of the 3D mesh with respect to the single stranded stacked SiNWs.

Another interesting result is the hysteresis observed for $I_{ds} - V_{ds}$ curves (see Fig. 3.12). The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward V_{ds} sweep is not identical to the same curve for backward V_{ds} sweep. This behavior can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [47]. More detailed explanation of the memristive electrical behavior can be found for

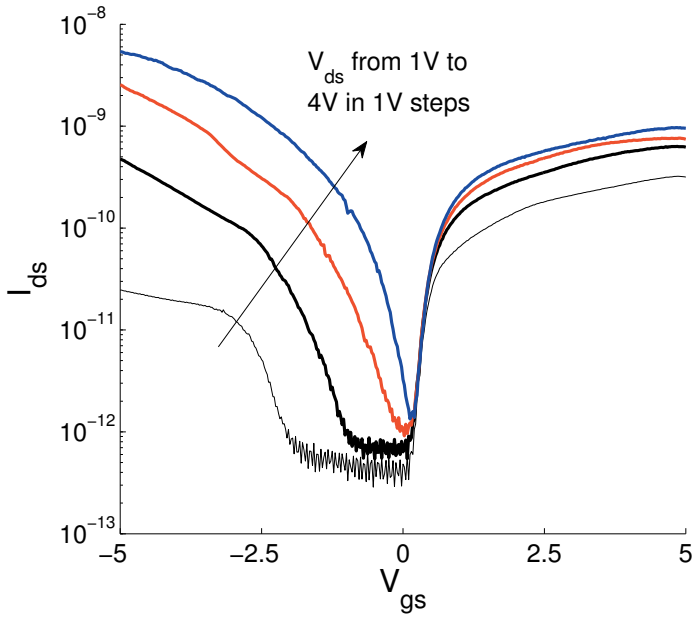


Figure 2.29: $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 stacked channels. Measured minimum inverse subthreshold slopes for electrons (n-branch) and holes (p-branch) are 300 mV/dec and 1300 mV/dec at $V_{ds} = 4V$.

similar, previously reported devices [48].

Finally, inverter and logic NAND operation have been performed using a current biasing scheme. In Fig. 2.32, a current bias from 5 pA to 15 pA in 5 pA steps has been utilized. As shown in the graph, the inversion voltage saturates at $V_{in} \approx 1.2V$ with a gain $\Delta V_{out}/\Delta V_{in} \approx 14$. Moreover, by using two vertically-stacked FETs in series connection, NAND functionality can be achieved by measuring the voltage drop across while sweeping the gate voltages of the two devices. With this method, typical NAND functionality is obtained, as shown in Table 2.5.

V_1[V]	V_2[V]	V_{out}[V]
0 (logic 0)	0 (logic 0)	≈ 4 (logic 1)
0 (logic 0)	2 (logic 1)	≈ 3 (logic 1)
2 (logic 1)	0 (logic 0)	≈ 5 (logic 1)
2 (logic 1)	2 (logic 1)	≈ 0.5 (logic 0)

Table 2.5: Logic NAND functionality obtained with two vertically-stacked FETs in series connection. V_1 and V_2 correspond to the voltages applied to the two independent gates of the NAND circuit. V_{out} corresponds to the total voltage drop of the series. Current bias is 5 pA.

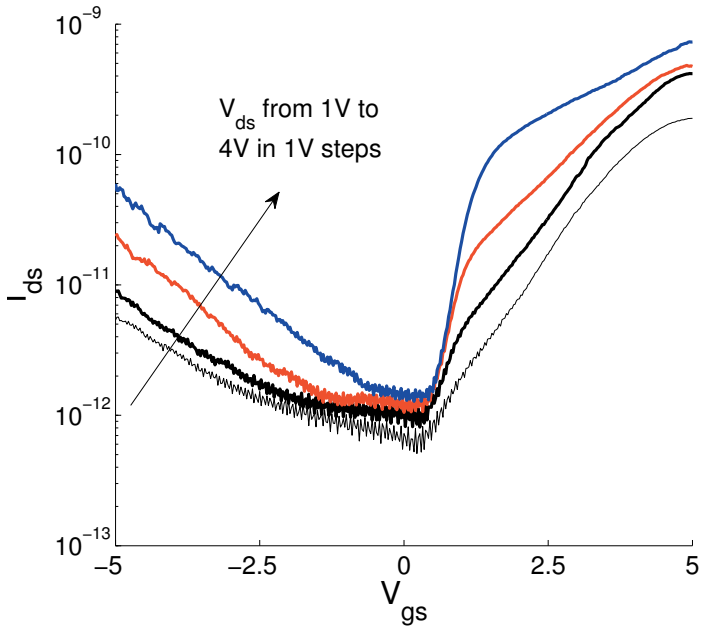


Figure 2.30: $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 times 11 channels. Measured minimum inverse subthreshold slope for electrons is 350 mV/dec. Notice that the holes conduction is effectively suppressed due to the 3D nanowire mesh.

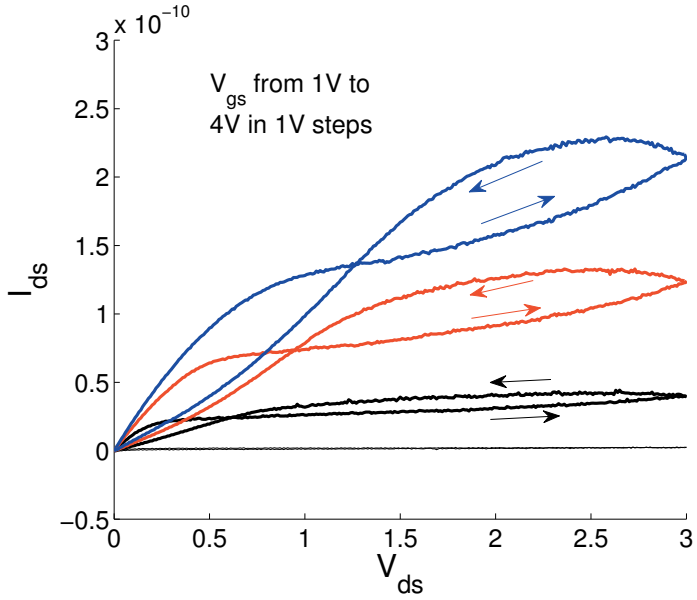


Figure 2.31: $I_{ds} - V_{ds}$ memristive/hysteresis curve for vertically-stacked SiNW GAA FET with 3 stacked channels. The hysteresis lead to different saturation threshold due to the dynamics of charges with interface states at either the Shottky junctions or at the polysilicon grain boundaries.

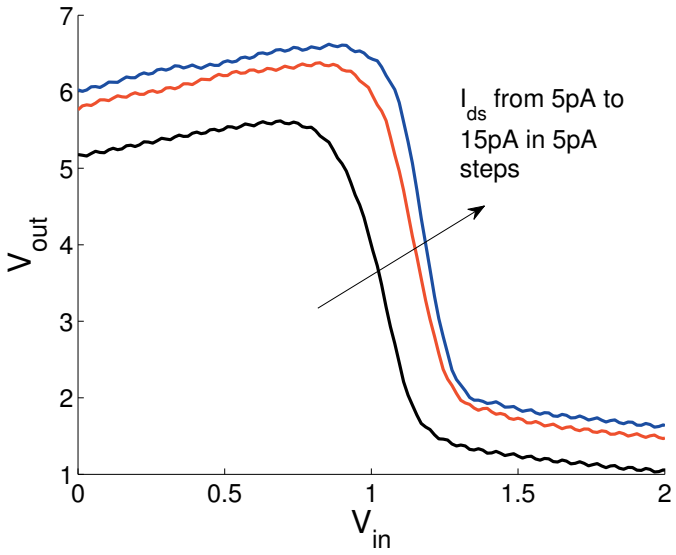


Figure 2.32: Inverter operation obtained by biasing a FET with constant current. The $V_{out} - V_{in}$ characteristics switched from high to low V_{out} at $V_{in} \approx 1\ V$.

2.4 On the design with Vertically-Stacked Si nanowire transistors

2.4.1 Introduction

In this section the newly introduced vertically-stacked silicon nanowire gate-all-around field-effect-transistor technology and its advantages for higher density layout design are discussed. The vertical nanowire stacking technology allows very-high density arrangement of nanowire transistors with near-ideal characteristics, and opens the possibility for design optimization by adjusting the number of nanowire stacks without affecting the footprint area of the device. Several libraries for combinational logic synthesis have been designed and implemented for the synthesis of carry-lookahead adders, using the vertically-stacked nanowire technology. The reduction in silicon active area occupancy of vertically-stacked gates are envisaged of great significance for regular cell mapping, in disruptive future applications based on nanowire transistor arrays.

2.4.2 Overview on Vertically-Stacked nanowire technology

Vertically-stacked Si nanowire (SiNW) technology makes use of smart processing to fabricate transistors having parallel SiNW channels or *fingers*. As depicted in Fig. 2.33 the basic device is composed of a stack of SiNW channels embedded in a polysilicon GAA structure. Each channel forms a unit width transistor. The process allows for easy tuning of vertical and horizontal separation between channels as well as the number of channels to be used for a certain device. All the channels are anchored to source/drain regions. Due to stacking, the SiNW channels will have different values of access resistance. One advantage of this technology is that the width of

the transistor is wrapped around the stacked SiNW channels, thus reducing the silicon estate of the active area. In addition, the versatility of stacking a variable number of fingers reduces the active area occupancy even more. Besides, due to the one dimensionality of the channels, specific technology boosters such as strain [26] can be envisaged, enhancing the performance compared with planar SOI technology.

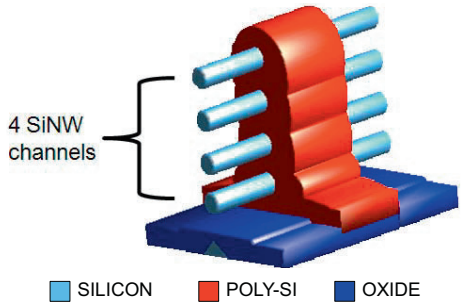


Figure 2.33: Vertically-stacked transistor in GAA configuration. The stack is composed of 4 SiNW channels (fingers). The total width of the transistor is the sum of all channel widths. The ends of the SiNW channels composing the stack are electrically connected to form source/drain regions.

Inverter construction

The vertically-stacked transistor technology presented in the previous section can be used to implement different logic gates, with a reduced active area. For instance, an inverter can be fabricated as depicted in Fig. 2.34. In this construction either the pull-up or the pull-down networks are made of SiNW transistors anchored to source/drain pillars. Source/drain electrical contacts are made with metal via, to reduce the access resistance of bottom channels. This configuration with metal via will be used to assess the total effective resistance of the vertically-stacked transistors in next section. A fabricated example of the inverter is shown in Fig. 2.35. In this example pull-up and pull-down networks are composed of three parallel SiNW stacks each of these composed of 4 SiNW channels.

CMOS logic-on-a-wire

Silicon nanowire MOSFETs can be used to build more complex gates. For instance, two Ω polysilicon gates have been used to fabricate (at CMI, EPFL)[2] an inverter (see Fig. 2.36) on a Si rib [49]. A similar approach can be used to build complex gates on a suspended wire. For instance, a SiNW pseudo-NMOS NAND can use 2 parallel gates placed side-by-side (see Fig. 2.37a and Fig. 2.37b). The same structure can be used to build an inverter on a suspended SiNW (see Fig. 2.38). Similar constructions can be made using a set of rules for design of other CMOS gates (Fig. 2.39a to Fig. 2.39d. For instance a 2-inputs NAND (see Fig. 2.39a would use 2

[2]Center of Micro and Nanotechnology, Ecole Polytechnique Federale de Lausanne

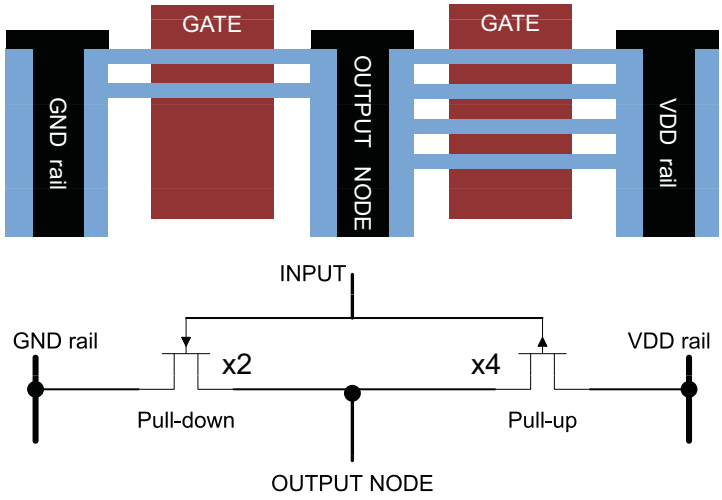


Figure 2.34: Vertically-stacked inverter structure with SiNW channels anchored to Si pillars with GAA configuration. The electrical equivalent circuit is a CMOS inverter with double drive. The number of SiNW channels is double for pull-up network compared with the pull-down network.

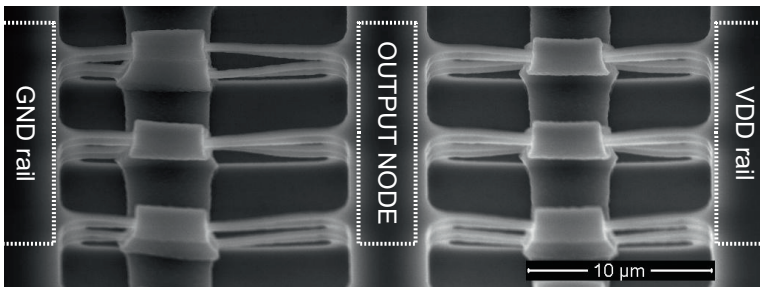


Figure 2.35: Tilted *scanning electron micrograph (SEM)* view of an inverter construction composed of 3 parallel stacks each composed of 4 SiNW channels. In this case pull-up and pull-down transistors have 12 unit width each.

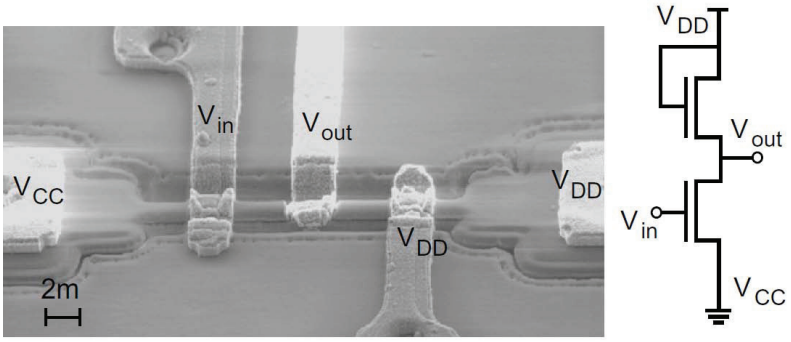
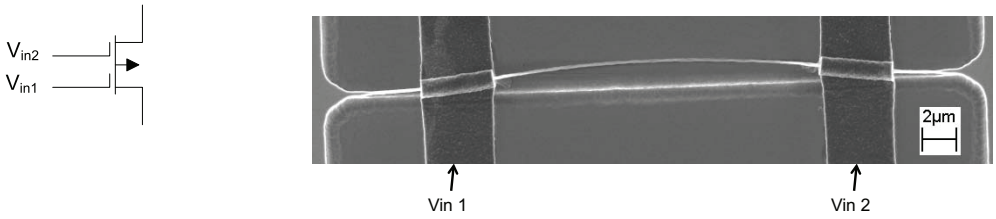


Figure 2.36: An inverter-on-a-wire configuration. The nanowire rib is body tied to the bulk, and the electrical connections is the one of a pseudo-NMOS inverter. The pull-up NMOS is always ON (tied to Vdd) [50].



(a) (b)

Figure 2.37: A NAND-on-a-wire configuration equivalent to the pull-down network of a standard CMOS 2-inputs NAND. This construction can be used for pseudo-NMOS ratioed logic, using a pull-up device that is always conducting. (a) NAND schematic; (b) practical realization.

separate nanowire arrays for the pull-down and the pull-up networks.

2.4.3 Combinational logic design

To assess the performance of complex logic circuits using the vertically-stacked nanowire technology, we perform combinational logic synthesis of carry-lookahead adders that are then mapped with vertically-stacked nanowire libraries. The vertically-stacked transistor electrical behavior was modeled as a switch in series of a resistance, which include both access and channel resistance. An estimation of the total diffusion capacitance is also carried out. Then performance and active area estimation are calculated for different combinational logic gates. Finally different libraries of logic gates are built varying both design and technology parameters of the basic transistor cell.

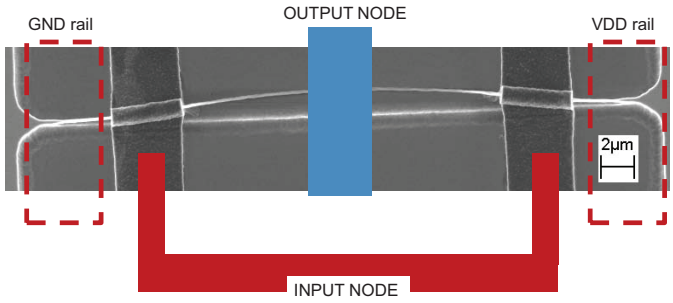


Figure 2.38: A CMOS inverter-on-a-wire can use the same construction of the pull-down network of a NAND-on-a-wire. The two input gates would be connected together, the middle portion of the nanowire would be used for the output electrical connection and the pillars used as V_{DD} and GND rails.

Basic assumptions

The configuration of channels of a vertically-stacked transistor can be generalized into a 3D matrix construction. We introduce the general construction to evaluate the total effective resistance, R_{tot} of the transistor (see Fig. 2.40). Since the topmost SiNW in the stack is closer to the via contacts than the other wires, its resistance is simply modeled as the channel resistance, $R_{channel}$. The other SiNWs in the stack will have an additional contribution due to the access resistance. Then, each additional channel carries a resistance calculated as follows:

$$R = R_{channel} + 2 \cdot R_s = \alpha \cdot R_{channel} \tag{2.1}$$

where $R_{channel}$ is the resistance of the single SiNW transistor, R_s is the series resistance path between the end of the SiNW channel and the via contact, $\alpha = \frac{2 \cdot R_s}{R_{channel}} + 1$ expresses the ratio between the topmost SiNW resistance and any of the other SiNWs composing the stack. We assume $R_{channel} \simeq 2.5\, k\Omega \cdot \mu m$ [51]. Since the top wire has less access resistance compared to the other wires in its stack, the total effective resistance can be reduced by using parallel stacks of fingers. Then, depending on the channel configuration (see Fig. 2.40) we get a general formulation of the total effective resistance:

$$R_{tot} = \frac{\alpha \cdot R_{channel}}{(\alpha + 1) \cdot k + n} \tag{2.2}$$

where k is the total number of stacks placed in parallel along the horizontal direction and n is the total number of channels composing the transistor. The total effective resistance of planar SOI transistors was calculated with formula 2.2 assuming $\alpha = 1$ and $k = 0$.

The same 3D matrix configuration of Fig. 2.40 is used to calculate the value of input and diffusion capacitances. We assume that each channel has the same contribution to the total diffusion capacitance, C_d thus the total diffusion capacitance of a single gate become:

$$C_{d,tot} = C_d \cdot n \tag{2.3}$$

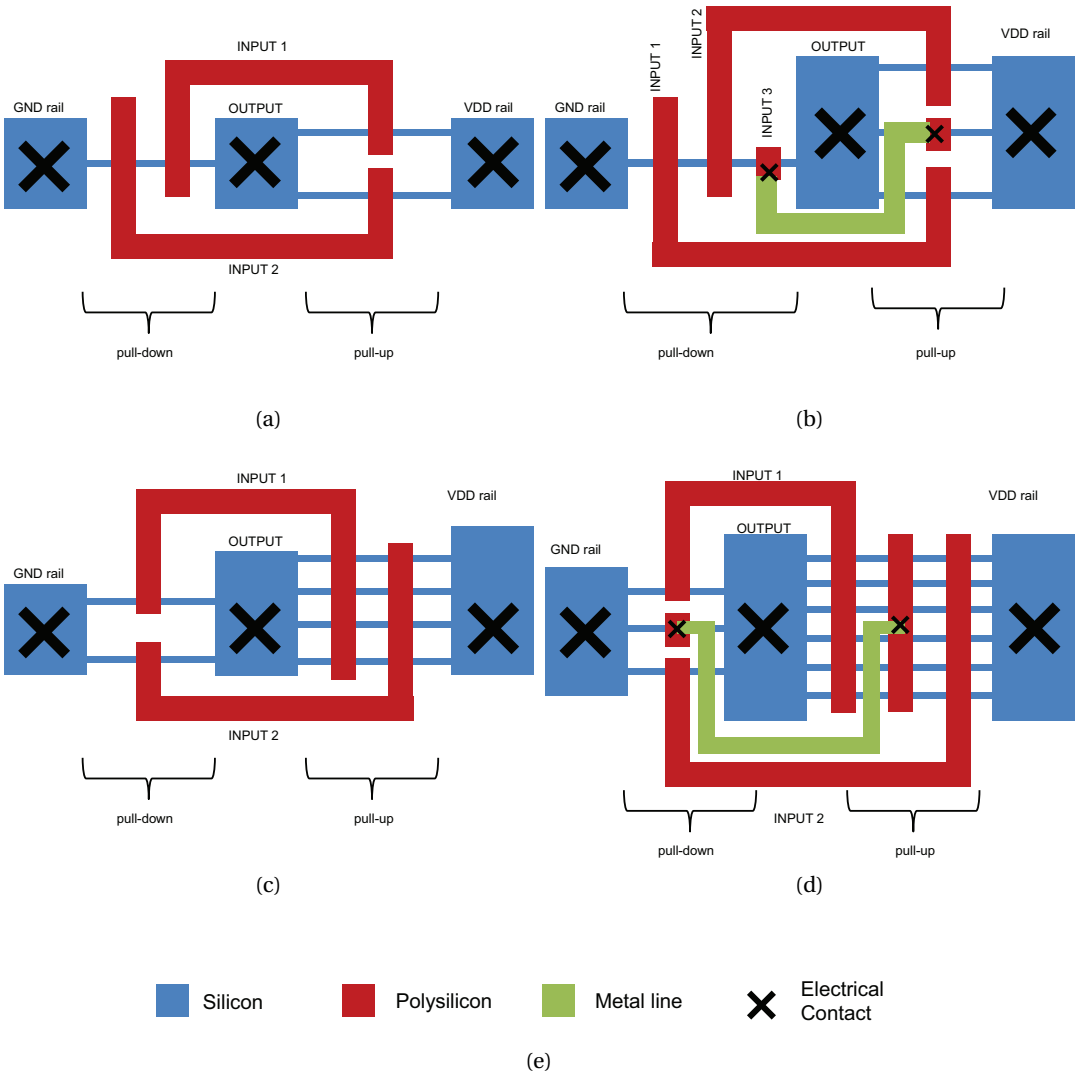


Figure 2.39: Basic stick diagrams of single SiNW CMOS gate layouts: (a) 2-inputs NAND; (b) 3-inputs NAND; (c) 2-inputs NOR; (d) 3-inputs NOR.

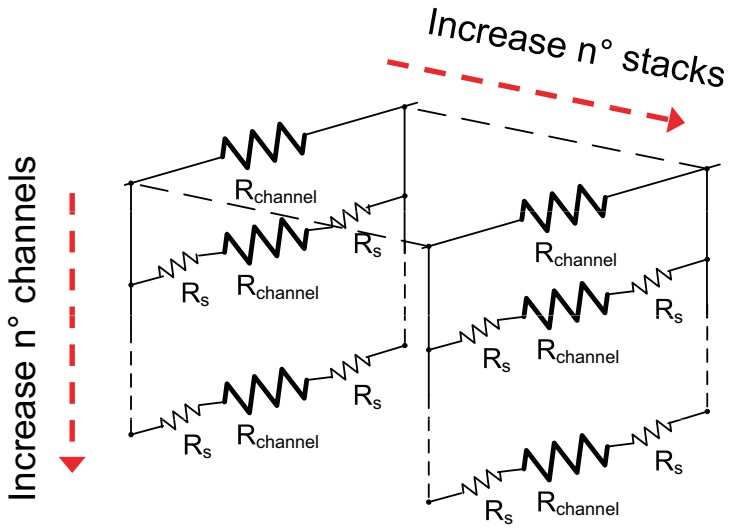


Figure 2.40: Resistive network construction representative of the channel 3D matrix composing a transistor.

The number of wires that compose the channel depends on the drive required by the transistor which in turn determines $C_{d,tot}$. The gate input capacitance, C_{in} is expected to grow linearly with the number of SiNW channels . In order to assess the impact of capacitances on gate delay, we assume equal C_{in} and $C_{d,tot}$ [51]. A common value for the capacitances that is used in linear delay modeling is $C_d \backsimeq 2\,fF/\mu m$ [51].The interconnect contribution is not considered here. Thus $C_{d,tot}$ corresponds to the parasitic output load of a transistor and to its input capacitance.

Gate modeling and libraries

We considered 9 different combinational logic gates that are listed in Table 2.6. We implemented 14 libraries, listed in Table 2.7; every one of them being formed by these 9 logic gates. The libraries include a planar SOI technology and 13 different SiNW technology libraries. These latter are obtained by varying two technology parameters: the access resistance (represented by R_s) and the strain (represented by the actual channel resistance, and a design parameter: the number of nanowire stacks). We designed the 9 logic gates in every library using the linear switch model [51], which assumes that every logic gate is driving the same current as a unit inverter, when it switches. We therefore obtained the required characterization in terms of area and delay. The latter was estimated as the *fanout-of-four (FO4)*, assuming that every gate drives its own intrinsic delay and a loaf of 4 instances of itself. The obtained area, FO4 delay and input capacitance for 3 different sample libraries are illustrated in Table 2.6.

2.4.4 Synthesis/mapping results

The ABC tool from Berkeley [52] was used to generate CLAs of 8, 16, 32 and 64 bits. Fast and efficient synthesis with the designed libraries is achieved by DAG-aware rewriting of the

Table 2.6: Gate parameters of three different libraries reporting active area occupancy, FO4 delay and capacitive input load.

Gate	planar SOI			L06 : SiNW, single stack			L07: SiNW, double stack		
	Active Area [units]	FO4 delay [ps]	C_{in} [C units]	Active Area [units]	FO4 delay [ps]	C_{in} [units]	Active Area [units]	FO4 delay [ps]	C_{in} [units]
INV	3	75	3	2	125	5	3	75	3
NAND2	8	110	4	4	220	7	4	110	4
NAND3	15	145	5	6	315	11	7	195	7
NAND4	24	180	6	8	410	14	10	280	10
NOR2	10	130	5	4	280	11	7	170	7
NOR3	21	185	7	6	435	17	13	315	13
NOR4	36	240	9	8	590	23	19	460	19
MUX2	24	180	6	8	420	14	10	300	10
MUX4	72	240	6	24	560	14	10	400	10

Table 2.7: Library list obtained varying series resistance, number of horizontal stacks and $R_{channel}$ reduction due to strain booster.

Library	$\frac{R_s}{R_{channel}}$	n° of stacks	$\frac{R_{channel,strained}}{R_{channel}}$	add8b		add16b		add32b		add64b	
				Area [units]	Delay [ns]	Area [units]	Delay [ns]	Area [units]	Delay [ns]	Area [units]	Delay [ns]
planar SOI	0%	-	100%	601	1.87	1265	3.87	2593	7.87	5249	15.87
L01	0%	1	100%	302	1.87	638	3.87	1310	7.87	2654	15.87
L02	25%	1	100%	302	2.44	638	5.08	1310	10.36	2654	20.92
L03	25%	2	100%	595	1.97	1267	4.13	2611	8.45	5299	17.09
L04	50%	1	100%	302	2.95	638	6.15	1310	12.55	2654	25.35
L05	50%	2	100%	571	2.02	1211	4.26	2491	8.74	5051	17.7
L06	100%	1	100%	302	3.92	638	8.24	1310	16.88	2654	34.16
L07	100%	2	100%	570	2.17	1210	4.65	2490	9.61	5050	19.53
L08	50%	1	80%	302	2.07	638	4.31	1310	8.79	2654	17.75
L09	50%	2	80%	586	1.61	1211	3.37	2491	6.89	5051	13.93
L10	100%	1	80%	302	2.49	638	5.21	1310	10.65	2654	21.53
L11	100%	2	80%	571	1.66	1211	3.5	2491	7.18	5051	14.54
L12	100%	1	60%	302	2.12	638	4.44	1310	9.08	2654	18.36
L13	100%	2	60%	597	1.29	1261	2.73	2589	5.61	5245	11.37

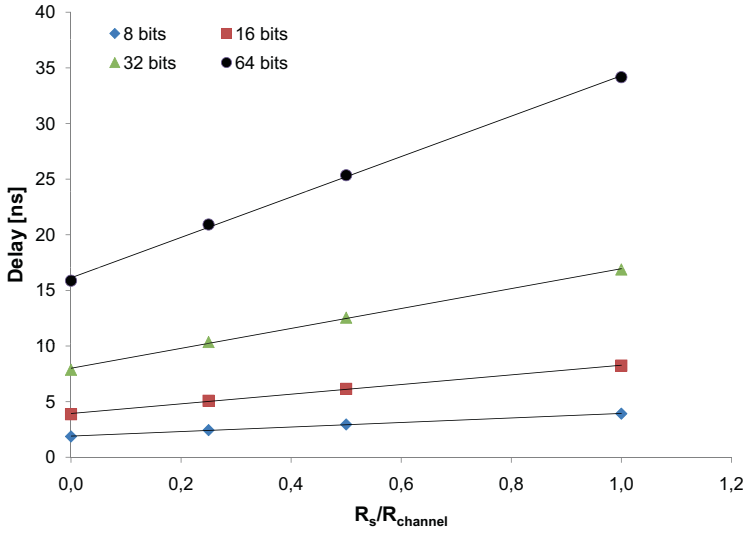


Figure 2.41: Effect of series resistance on delay. The values shown in the graph are obtained after mapping of carry-lookahead adders.

and-inverter-graph (AIG) representation of the adder network. We used the script $resyn2$ for synthesis, which consist of an alternation of network rewriting and balancing algoritms that reduce the AIG size and the number of AIG levels. The optimized network was then mapped with the different libraries (see Table 2.7). The impact of the different design and technology parameters on mapped CLAs is analyzed in the following.

Impact of series resistance on delay

In Fig. 2.41 the impact of series resistance on FO4 delays is shown. The data refers to CLAs with different number of bits mapped with single stack configuration. As expected, the FO4 delay linearly increases with series resistance. This behavior is enhanced for adders with more inputs, due to the use of more complex gates. Data points at $\frac{R_s}{R_{channel}} = 0$ correspond to a FO4 delay that is the same of the planar SOI case.

Impact of pararellizing stacks on delay and area

The detrimental effect of series resistance can be counterbalanced by using more stacks instead of a single one, thus reducing the effect of R_s on R_{tot} which in turn is reflected on the delay. For instance a 64 bits carry-lookahead adder synthetized with 2 stacks shows an evolution of FO4 delay with series resistace that is 6 times lower than the configuration which uses 1 stack (see Fig. 2.42). The speed-up achieved by the double stacking costs additional active area occupancy. However, the total active area occupancy remains lower than the planar case. For instance, the 64 bits CLA with single stack would reduce occupancy area of 49% compared with the one mapped in planar technology. The use of double stack will still reduce occupancy area of 4%. However, the improvement in delay get by using double stack is bigger than the additional cost on area.

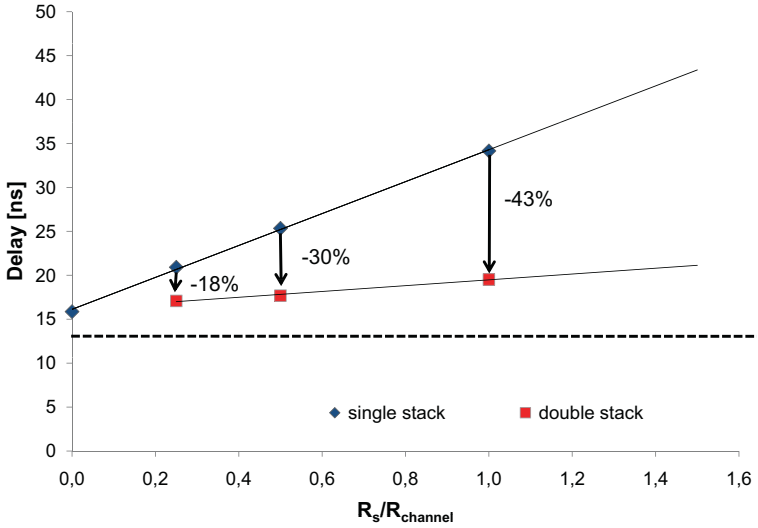


Figure 2.42: Evolution of 64 bits carry-lookahead adder delay with increasing series resistances (R_s as depicted in Fig. 2.40). Dashed horizontal line represent delay of planar technology. The use of a double stack significantly reduces the impact of series resistances.

Impact of strain on delay

More significant performance improvement can be achieved by using strained nanowires. The impact of strain was evaluated varying α within single or double stack configurations. By comparing FO4 delays (Fig. 2.43) we see that strain can effectively counterbalance the effect of series resistance, eventually outperforming planar technology.

2.4.5 Opportunities

The presented architecture can be employed for standard cell libraries with minimum sized gates. Alternatively, the vertical-stacking of channels can be used to increase the area density of regular array architectures such as for *programmable logic array (PLA)*. One example are nanowire crossbars, which are promising architectures for their higher density and their fault-tolerance due the reconfigurability [53, 54]. As a matter of fact, combinational logic functions can be expressed in terms of sum-of-products canonical form, which can be mapped onto a PLA. In general, the PLA construction uses AND and OR planes that can be programmed to give a certain combinational logic funtion. For instance an adder can be built using a PLA architecture (see Fig. 2.44a). The PLA planes can be implemented with different logic gates. The smallest possible PLA design makes use of NORs and inverters to construct the AND and the OR planes. The implementation of the planes using vertically-stacked technology would drammatically improve the density (see Fig. 2.44a).

2.4.6 Summary

In this paper we reported on the vertically-stacked Si nanowire technology assessment for combinational logic circuit design. The synthesis of CLAs of different sizes were mapped

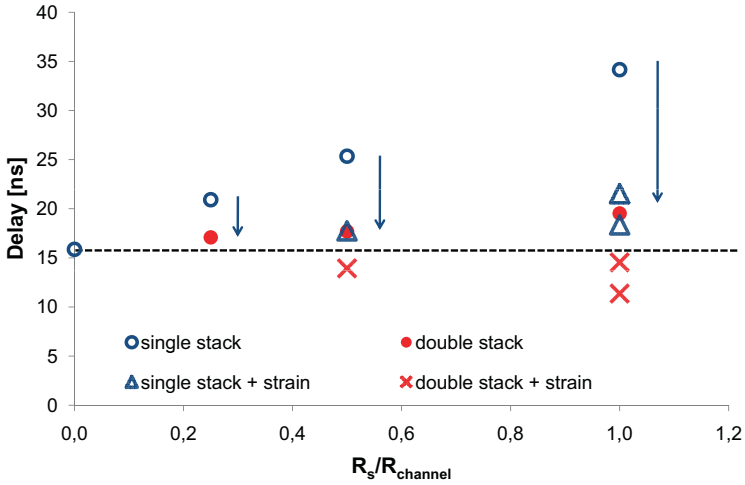
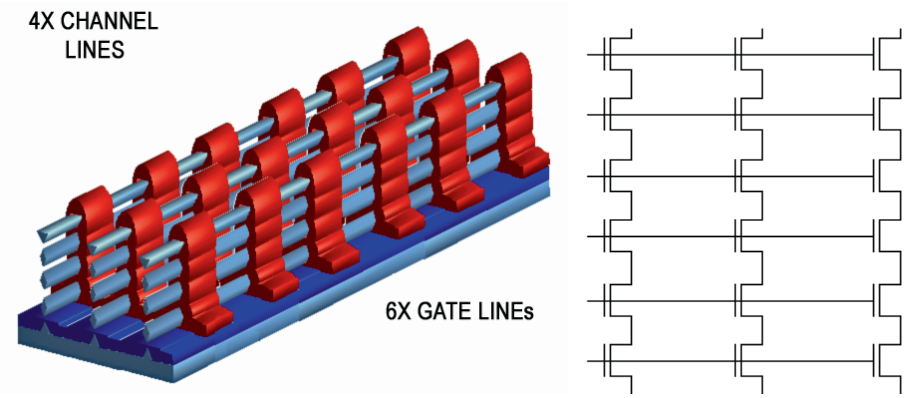


Figure 2.43: Effect of strain on delay (64 bits carry-lookahead adder data). Dashed horizontal line represent delay of planar technology. The plot shows that either using double stacks and/or strain improve delay. Notice that strained nanowires with double stacking outperform planar Si technology.



(a) (b)

Figure 2.44: (a) Nanowire based pseudo-NMOS PLA with NOR structure example showing 6 parallel gate line construction, 4 levels of stacked nanowires and 3 parallel channel stacks. Adjusting the threshold voltage of the channels would result in a ROM construction of the PLA. (b) Schematic representation of the NOR PLA.

with vertically-stacked nanowire libraries. We showed that the vertically-stacked nanowire technology can effectively reduce the active area of gates from 4% to 49% compared with planar SOI technology. Moreover, the additional series resistance could be counterbalanced by means of specific technology boosters which are peculiar of SiNW channels. Finally, we introduced the conceptual idea of using vertically-stacked nanowire technology as a way to enhance the density of PLA regular architectures.

2.5 Chapter Summary and Conclusions

In this chapter several micro-fabrication methodologies for a variety of Si substrates have been presented and discussed. In particular, the fabrication of gate-all-around vertically-stacked Si nanowire transistors has been achieved with a low cost-method that uses standard optical lithography to define nanowires of sizes 10 times smaller than the critical dimension of the photoresist. This technique, which is based on DRIE and sacrificial oxydation has been validated for a variety of substrates, including bulk-Si, Silicon-On-Insulator, polysilicon-On-Insulator.

The sacrificial oxydation technique has been proven to provide smooth vertically-stacked Si nanowire formation and, it can be utilized also to form a local insulating layer, removing the contribution of the parasitic substrate transistor in parallel with the nanowires. Additionally, an innovative process flow that includes the use of stencil lithography for the definition of the gate stack has been explored for the first-time, allowing faster prototyping and removing the 4:1 aspect ratio constraints for the definition of 3D structures.

The main limitations of the presented approaches lie in the limited alignment capabilities of the manual optical aligners available in CMi and on the pitch constraints of the vertically-stacked nanowires. In order to improve that, an optimized process flow for the fabrication of ultra-dense vertically-stacked SiNWs has been co-developed in collaboration with my colleague Michael Zervas. The optimized fabrication enables the formation of vertically-stacked nanowires with sub-20nm diameters without the need of sacrificial oxydation as well as pitch density that are limited only by the ebeam pitch (in the horizonal plane) and by the scalloping dimension (in the vertical plane).

New design opportunities inferred from the achieved fabrication results of vertically-stacked Si nanowire transistors are discussed and design synthesis of vertically-stacked Si nanowire CMOS technology leads to clear advantages in terms of area and performance.

In the last part of the chapter, electrical results of the fabricated ambipolar SiNW transistors and inverters are discussed. These electrical results will be the base for the next chapters. In particular, the hysteretic behavior will be discussed more in detail in the memristive device chapters, while the ambipolar feature will be exploited by dedicated device structures targeting specific applications.

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3 Memristive Devices and Systems

3.1 Introduction

The main source of the CMOS success lies in the exponential increase of device density that the silicon industry kept true for more than 40 years reducing the unit cost of integrated circuits. Recently, the pace of scaling has been slowing down due to approaching fundamental limits at the device level. While the paradigm of scaling is still alive, researchers are striving to follow Moore's law by focusing on new materials, new device structures and new state variables. The basic building block for circuits has always been the four-terminal planar transistor but new versions of the MOSFET structure such as the double-gate FET, the FinFET, the gate-all-around nanowire FET can be found in commercial products.

Due to the natural limitations of materials, future nano-scale circuits will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages an end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. A long list of fundamental state variables other than charge includes the spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states [1]. Technologies using new state variables would have to be implemented within a completely new technological platform, and cannot be seen as CMOS-compatible alternatives.

The recent realization of devices by Stanley Williams and his team [2] gave new push to solid state research for logic and memory applications. For instance, ultra-dense crossbar memristive memory arrays can be made thanks to the compactness of the two terminal junction. Complementary logic based on two-terminal memristive devices (see Fig. 3.1a) or ultra-dense crossbar arrays with memristive cross-points (see Fig. 3.1b) can dramatically improve device density up to 10^{11} bits per square centimetre [3]. Moreover, the use of memristive effects as new state variables for computation can be exploited to build new types of functional devices with three- or four-terminals (see Fig. 3.1c and Fig. 3.1d, respectively).

The physical realization of the memristor, whose behavior was postulated by Leon Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6]. It is worth noting that, a generalized model for memristive systems can be implemented under DC, small signal and sinusoidal excitation [5].

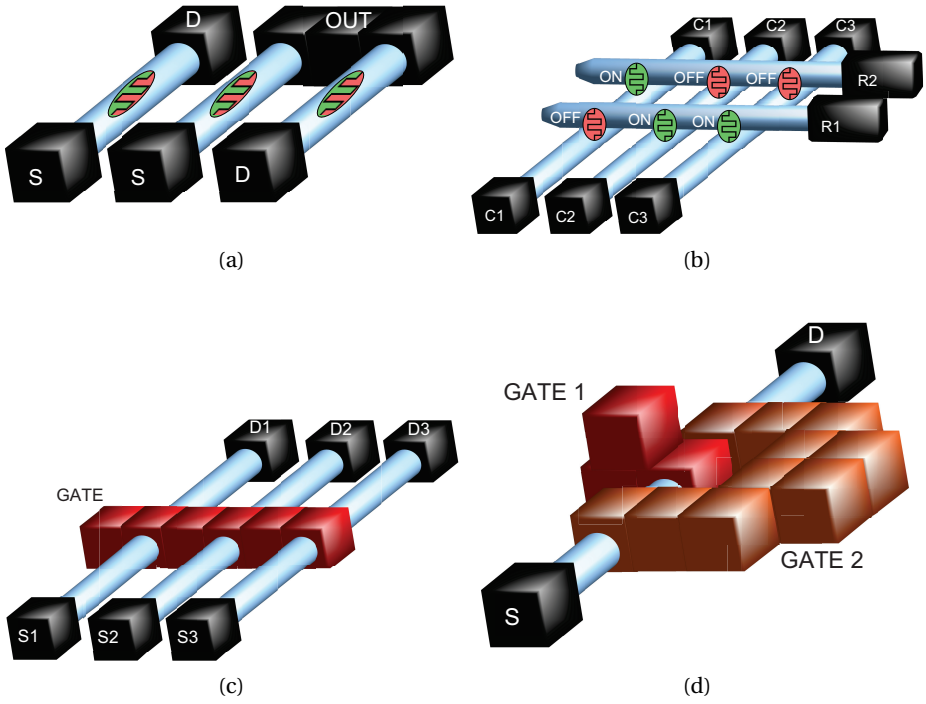


Figure 3.1: (a) Parallel nanowire two-terminal memristive devices. (b) Crossbar array consisting of memristive cross-points (two-terminal). (c) Gate controlled three-terminal nanowire memristive device. (d) Double-gate four-terminal nanowire memristive devices.

The implications of such modeling is linked with the observation of memristive functionalities over a broad range of technologies based on nanoelectronic and nanoionic behaviors.

The content of this chapter is organized as follows. First, a generalization of memristive devices is given (Section 3.2). Then two-terminal devices with memory are discussed in Section 3.3, while a broader chategorization and discussion on multi-terminal memristive devices is given in Section 3.4. Finally the original contributions of this chapter are summarized in Section 3.5.

3.2 Generalization of the Memristive Devices

The memristive functionality is not a unique property of two-terminal passive devices but mainly a memory effect related to internal state variable changes. For instance, the memristive functionality can also arise from a delayed switching response of a Zener diode [7]. As described by Di Ventra et al. [8], the memory effects in nanoscaled devices can be generalized for resistance, capacitance and inductance to their time dependent and non-linear responses. If *u(t)* and *y(t)* are two complementary constitutive circuit variables, denoting the input and the output of the system, respectively, and x is a n-order vector of internal state variables, the existance of a n-th order u-controlled memory element as that defined by:

$$\begin{cases} y(t) = g(x,u,t)\,u(t) \\ \dot{x} = f(x,u,t) \end{cases} \tag{3.1}$$

where g is a generalized system response and f is a continuous n-dimensional vector function. As described in [8], the relation between current and voltage defines a *memristive system*, while the relation between charge and voltage defines a *memcapacitive system* and the flux-current relation defines a *meminductive system*. The Equations 3.1 can be further generalized for cases where the internal state is described by a continuous function or functions instead of discrete variables as well as cases for which the internal state variables follow a *stochastic differential equation* rather than a deterministic one. In the next sections, we review some of the two-terminal passive devices that can be modeled as memristive. The memristive functionality is seen as arising from different physical mechanism for different device classes. Thus, three- and four-terminal devices that show memristive functionality can be used for electrical control signals (either voltage or current). It is important to remember that a device showing a "pure" flux-charge relationship has not been found yet. Conversely, internal state variables can provide a stimulus response that can be modeled as memristive, thus adding more degrees of freedom for circuit designers.

3.3 Two-terminal Devices with Memory

3.3.1 Mem-Resistive Switching Devices

A mathematical definition of two-terminal passive mem-resistive devices has been formulated by Chua and based on this interpretation a mem-resistive device would present three fingerprints:

- pinched hysteresis loop in the *i(t)-v(t)* plane;
- passive: *i=0* when *v=0*;
- frequency dependence with the input signal *u(t)*

However, many electronic devices that were previously classified as *"memristors"* have been recently re-classified as their actual behavior requires an extension of the memristive theory. [9]. Nevertheless, by looking at these three fingerprints, it has been recently reported that mem-resistive behavior has been noticed in several electric devices in the past two centuries [10]. More specifically, a predominance of mem-resistive behavior seems to be linked with an electric discharge phenomena, and as such it is believed that the first memristor was actually found in 1899 by Herta Ayrton (see Fig. 3.2). Later on the solid-state realization of devices by Stanley Williams and his team [2] which showed mem-resistive fingerprints gave new push to research on nano-scaled mem-resistive devices. It has been stated that the mem-resistive "fingerprints criteria" are satisfied by several resistive switching materials, and as such it becomes clear that the mathematical formulation of memristors and memristive devices does not necessarily link to a specific physical phenomenon. Considering resistive switching materials, a classification based on physical phenomena has been provided by Waser (see Fig. 3.3) [11].

Two-terminal memristive devices can be based on metal/oxide switches, such as for SiO_2, HfO_2 [12], CuO [13], NiO [14], ZnO [15], Al_2O_3 [16], VO_2 [17], $SrTiO_3$ [18]. These devices behave as solid-state electrochemical switches, whose resistance is defined by a metallic filament formation mechanism related to the solid-state redox reactions stimulated by the polarity of the applied electric field [19]. One example is the CuO-based ReRAM of Dong et al. [13], that shows repeatable resistive switching at very low voltages.

The well known TiO_2-based ReRAM [20, 21] seems to be based on a different mechanism, which is attributed to the vacancy/dopant diffusion in the oxide layer. The re-distribution of oxygen vacancies into the TiO_2 depends on the polarity of the applied voltage, and it causes the switching between a semiconductor state into a metallic one. Typical ReRAM functionality of the TiO_2-based ReRAM is shown in Fig. 3.4 [22], with the resistivity switching by 5 orders of magnitude.

Another type of two-terminal memristive device is the *phase change (PC)* RAM [23]. The main switching mechanism is based on phase transition between an amorphous and a crystalline type due to Joule heating effects controlled by a voltage pulse. For instance, Si nanowires can be engineered such that melting and solidification processes can be iterated, thus giving rise to alternate resistance states [24].

Another class is based on polymers [25]. Several memristive switches can be build by interposing a bio-molecule layer with properties ranging from molecule-dependent switching, such as rotaxanes [3], or more in general on inter-locked molecules [26] but also on molecule-independent switching, where a filament formation mechanism through the molecular layer is involved [27].

A fifth class belongs to spintronics [28]. The spin-transfer induced domain wall motion in a spin valve structure is by nature a memristive effect and is confirmed by some recently

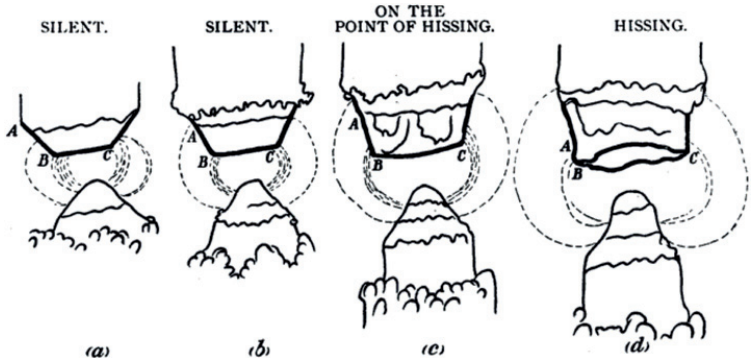


Figure 3.2: The "hissing of the electric arc" as presented to the Institution of Electrical Engineers in 1899 by Hertha Ayrton. The image is taken from [10].

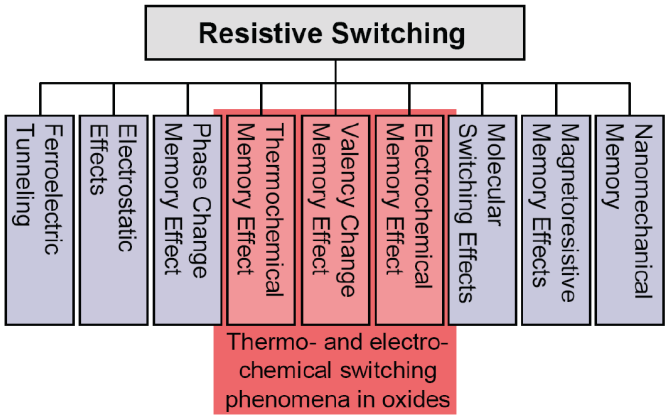


Figure 3.3: A classification of resistive switching devices depending on the underlying physical mechanisms as provided by Waser [11].

published results [29]. Moreover, Pershin et al. demonstrated that electron-spin polarization controlled by the external voltage applied to a spintronic device, acts as a state variable that can be modeled as memristance [30].

In all these devices the amplitude and frequency of the input signal contribute in the formation of a so called pinched hysteresis loop, whose salient feature is its zero crossing property [5], which is critical for ultra low power operation.

3.3.2 Mem-Capacitive Switching Devices

As per two-terminal memristive devices, two-terminal memcapacitive devices can be based on several mechanisms. A classification has been given by Pershin et. al [8], and it is divided mainly in two categories: geometrical and permittivity-related memcapacitors.

An example of mem-capacitive switching device based on geometrical effects consists of a capacitor with a movable plate, whose movement depends on the applied electric field [31]. One

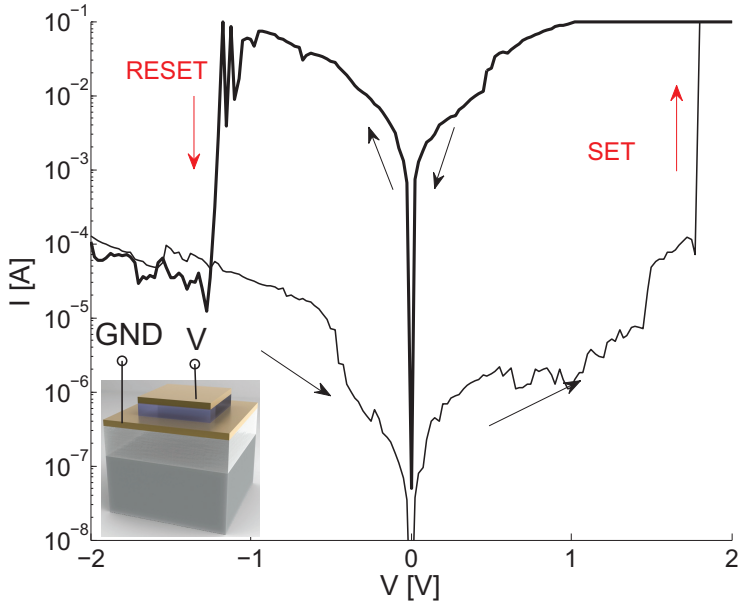


Figure 3.4: Resistive switching through I-V sweeps for planar $Pt/TiO_2/Pt$ [22]. The inset shows the $Pt/TiO_2/Pt$ ReRAM sandwich layer on top of an insulated substate with the two terminal electrical contacts.

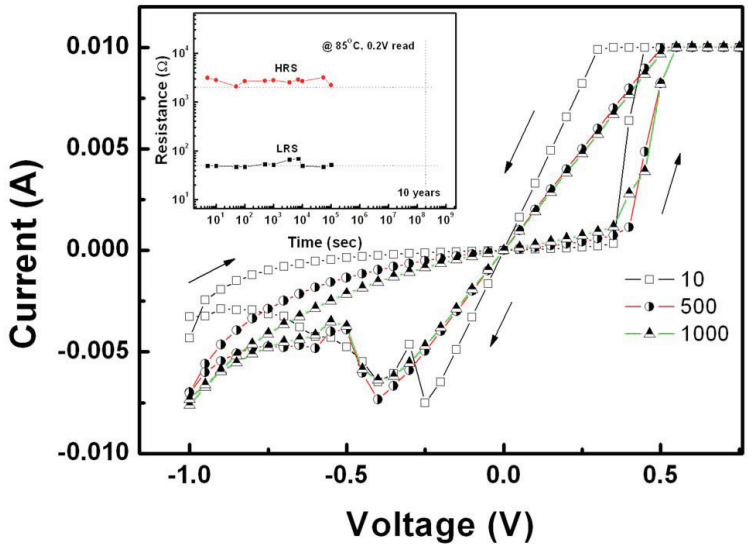


Figure 3.5: Switching mechanism of a CuO-based ReRAM. The image is taken from [13].

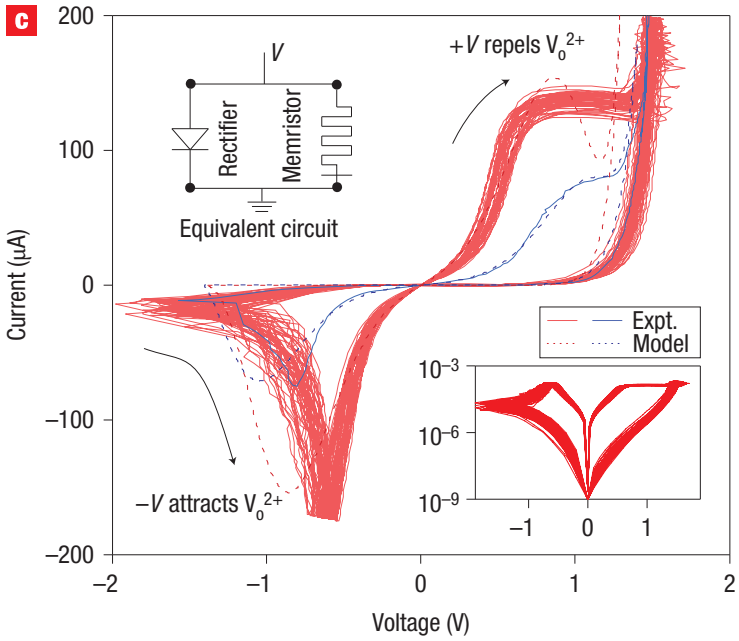


Figure 3.6: Pinched hysteresis loop from a $Pt/TiO_2/Pt$ memristive junction. The image is taken from [20].

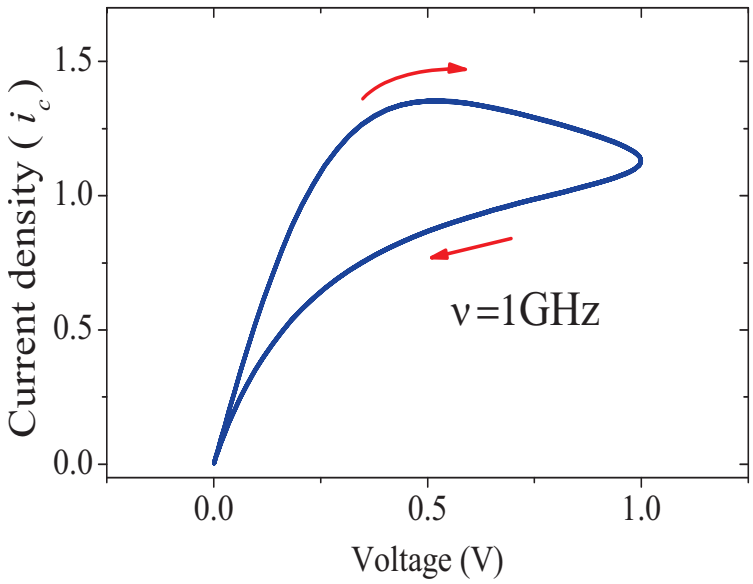


Figure 3.7: Unipolar I-V simulation for a semiconductor spintronic system. The image is taken from [30].

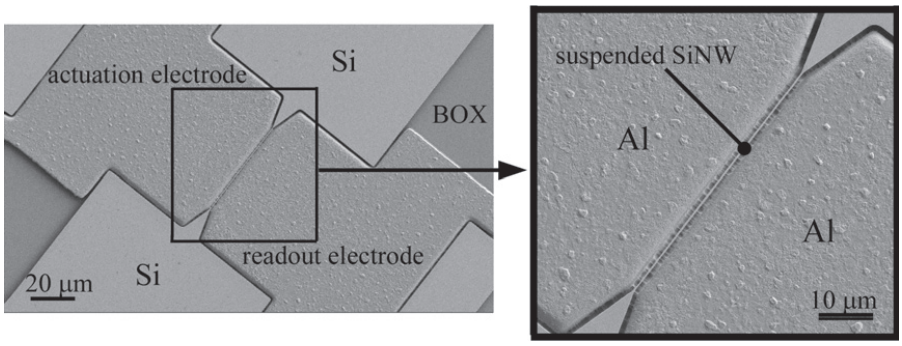


Figure 3.8: NEMS resonator consisting of a SiNW and two Al side-electrodes. A two-terminal memcapacitor configuration can be obtained by using the elastic SiNW and either one of the Al pads as the electrodes. The image is taken from [32].

such device would be a capacitor having one of the electrodes being elastic. If a voltage pulse is applied across the capacitor, the elastic plate moves towards the other electrode, in response of the electric field, thus modifing its capacitance. One possible realization of the geometrical mem-capacitor can be obtained from a *Nano Electro Mechanical System (NEMS)* resonator configuration. Such devices can be, for instance, fabricated with a CMOS compatible process flow on SOI substrates. As depicted in Fig. 3.8, a NEMS device consisting of a suspended SiNW and Al metal electrodes can be utilized as a geometrical-effect memcapacitor. In this device, the SiNW in the middle is utilized as an elastic electrode [32]. It is worth mentioning that the NEMS resonator can also be utilized as resistive switching device, but this does not represents a case of two-terminal memristive device because its pinched hysteresis loop does not depend on the frequency of actuation, as it results on the absolute value of the DC signal (see Fig. 3.9).

A second example is a device whose permittivity modifies upon the application of a voltage bias. A memcapacitor proposed by Di Ventra et al [33], consists of a parallel plate capacitor with additional floating plates in between, separated by dielectrics. The internal charge can move between the different plates and its polarization can screen the electric field applied at the external plates. This way, based on the distribution of the charges in the polarized plates, a memcapacitive behavior is obtained [33].

Another memcapacitive device has been demonstrated with a III-V diode and high-κ dielectrics [34].

3.3.3 Mem-Inductive Switching Devices

Similarly to the memcapactive devices, geometrical effects [35] and permeability-related effects [36] can lead to an inductive system showing memory, thus forming a mem-inductive device. Several properties, including mechanical, electrical, magnetic and thermal were discussed by Pershin et al. [8] as possible mechanisms that can be exploited in a mem-inductive system.

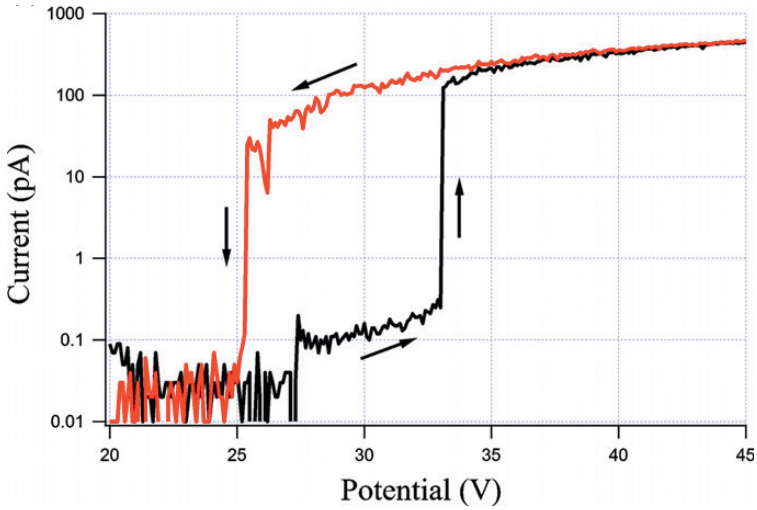


Figure 3.9: Resistive switching characteristic of SiNW NEMS [32]. The hysteresis arise from the var-der-Walls forces that retain the SiNW at pull-out. Since the hysteresis does not depends on the actuation frequency, this resistive switching mechanism cannot be considered as mem-ristive.

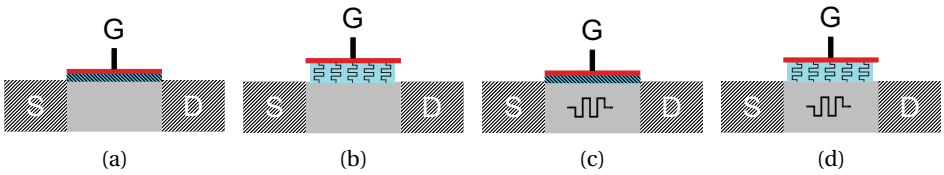


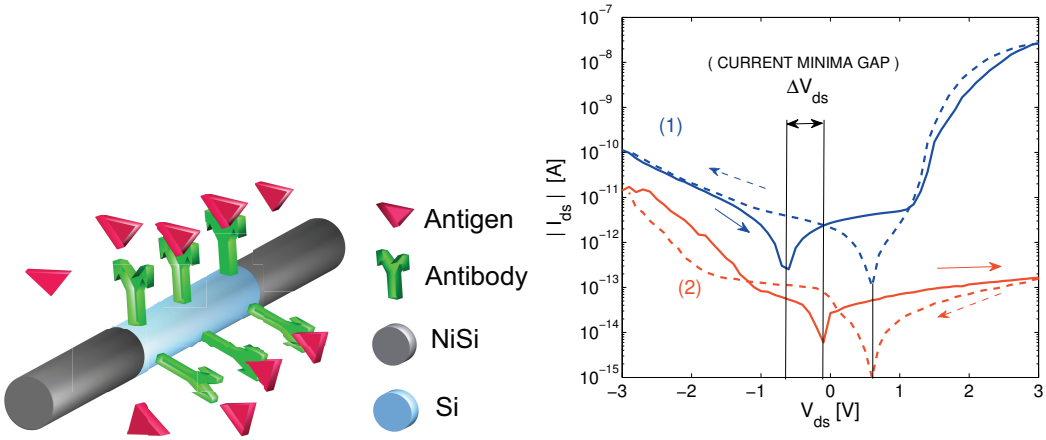
Figure 3.10: Categorization of FETs with memristive functionalities: (a) Conventional FET. (b) FET with memristive gate dielectric. (c) Gated memristor (memristive channel). (d) Gated memristor with memristive dielectric.

3.4 Multi-terminal nanowire memristive devices

3.4.1 Three-terminal memristive devices

The new concept of three-terminal memristive device is presented in terms of memristive functionality for logic and memory applications. Examples of three-terminal memristive devices are the electrochemical organic memristor [38], the solid-electrolyte nanometer switch [39], the ferroelectric FET [40], non passivated transistor devices (here cite the non-passivated CNT and graphene transistors), Carbon Nanotube and/or graphene transistors and the ambipolar Si nanowire Schottky barrier FET [41, 42].

A classification of three-terminal memristive devices can be based from the general concept of the FET structure (see Fig. 3.10a) in which memristive functionality can be inserted either by engineering the gate dielectric or by gating a memristive channel. For instance, trap charging dielectric layers inserted between the channel and the gate fall into the category of FET with capacitive memory storage (Fig. 3.10b). One example in this category can be the flash memory



(a) (b)

Figure 3.11: (a) Suspended functionalized Si nanowire with NiSi extremities. The functionalized layer is capable of trapping antigen molecules which in turn affects the memristive hysteresis behavior, giving a new method for bio-sensing [37]. (b) A typical memristive hysteresis is observed; the blue curve (1) is measured after drying the sample from de-ionized water. The red curve (2) is measured after dipping in 5 pM antigen solution and drying. The measured ΔV_{ds} is proportional to the concentration of antigen [37].

for which the trap charging into the gate dielectric influences the transconductance state of the channel [43]. Thus a first category that exploits the operation of writing/erasing cycles into the gate dielectric will be a generalization of the flash memory concept, for which volatility of the charges that are injected into the trap charging layer can be tuned accordingly to a desired frequency response. Such a device has been recently demonstrated by Ziegler et al. [43] by using a FLASH transistor in a two-terminal configuration. As depicted in Fig. 3.13, the device can be operated such that a bipolar resistive switching behavior is measured and non-volatility is a consequence of trap-charging into the floating gate. Another example can be the *zero-capacitor RAM (ZRAM)* and the *twin-transistor RAM (TTRAM)*, which rely on floating body effects in SOI transistor to provide a volatile hysteresis effect [44, 45].

A second category is the one of the gated memristor (Fig. 3.10c). A few examples are the electrochemical organic memristor [38], the bio-memristive nanowire [37] and the solid-electrolyte nanometer switch [39]. In the electrochemical organic memristor the gate potential is represented by the potential of the bath, which is used to transfer positively charged Rb^+ ions into a polyaniline (PANI) layer [46]. The conductivity change can be iterated by switching the polarity of the bath potential, thus giving rise to a unipolar I_{ds}-V_{ds} curve that can be modeled as a memristor. In this case the device can be set into either memristive or diode functionality. Similarly, a novel method for bio-sensing that has been recently proposed exploits the memristive effect to detect low concentration of bio-molecules [37]. The device consists of a NiSi/Si/NiSi nanowire structure coated with antibody layer (see Fig. 3.11) shows memristive behavior. The hysteresis loop of this device has been demonstrated for detection of low concentrations of bio-molecules (antigen) in a dry environment (see Fig. 3.11b). Conversely, the three-terminal solid-state electrolyte nanometer switch shows a typical bistable resistance

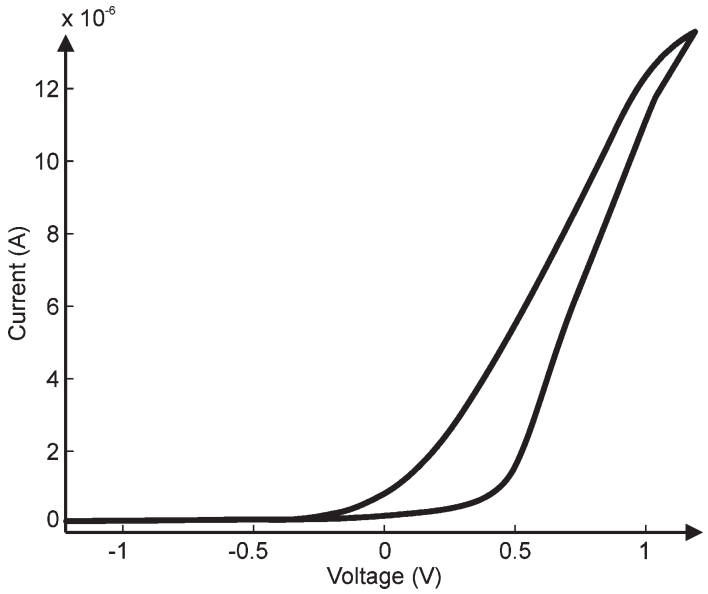


Figure 3.12: Cyclic voltage measurement showing bistable memristive behavior. The image was taken from [38].

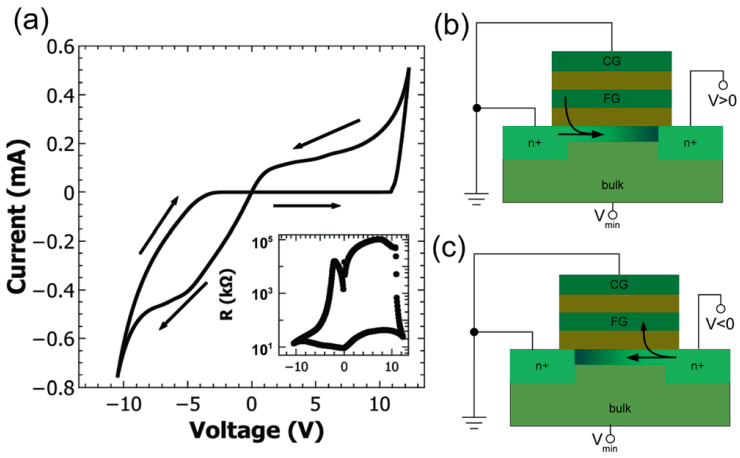


Figure 3.13: Two-terminal memristive configuration of a FLASH memory cell. Depending on the polarity of the applied voltage, trap charging dynamics of electrons to and from the floating gate and dielectric is responsible of the hysteresis. The image was taken from [43].

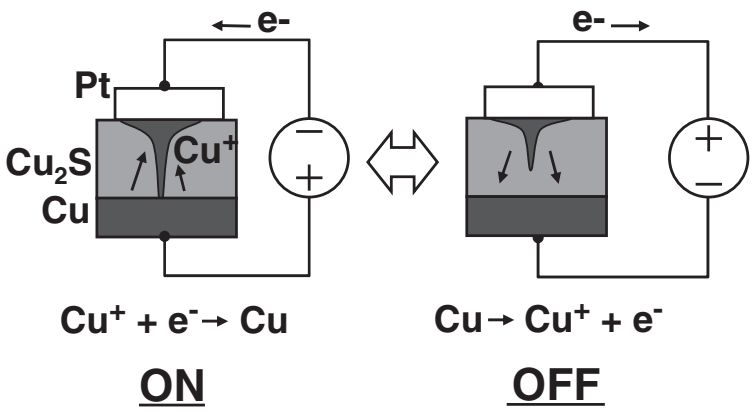


Figure 3.14: Controlled filament formation of the three-terminal nanobridge device. The image was taken from [47].

state but using 100 times less current than standard two terminal operation [47]. This device is based on controlling the filament formation mechanism using the voltage of a gate terminal (see Fig. 3.14).

The ambipolar SB FET with SiNW channel reported in [48] (see Fig. 3.10d), falls in both categories of gated memristor and trap charging dielectric, as it shows dynamic trap charging mechanisms at the Schottky junctions and in the gate dielectric insulator. The result depicted in Fig. 3.15 shows a hysteretic behavior that is reminiscent of a two-terminal monolithic memristive device [49]. The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward V_{ds} sweep is not identical to the same curve for backwards V_{ds} sweep. It can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [50]. First, two-terminal measurements are performed. The drain-source current I_{ds} is measured vs. the drain-source voltage V_{ds} at constant $V_{gs} = 5\ V$. The device is equivalent to two back-to-back Schottky diodes. The two diodes operate in opposite regimes: for negative V_{ds}, the source-to-channel diode is reversely biased while the drain-to-channel diode is forward biased. For positive V_{ds} both diodes invert their respective bias conditions. In either case, I_{ds} is limited by the current flowing in the reverse-biased diode. The reverse current of a metal-insulator-semiconductor diode has been observed to be very sensitive to charge trapping at the metal/semiconductor interface [16]. The large current value in the range of mA is most likely due to the large parallel parasitic structure in the bulk. In an ideal Schottky diode, the current is given by:

$$I = I_S \cdot e^{-\phi_B q/kT}(e^{Vq/kT} - 1) \tag{3.2}$$

with I and V the diode current and voltage respectively, ϕ_B the Schottky barrier, k the Boltzmann constant, q the elementary charge and T the absolute temperature. From the measured hysteretic behavior, it seems that the diode curve is modified as follows:

$$I = I_S \cdot e^{-\phi_B q/kT}(e^{(V-V_0(V))q/kT} - 1) \tag{3.3}$$

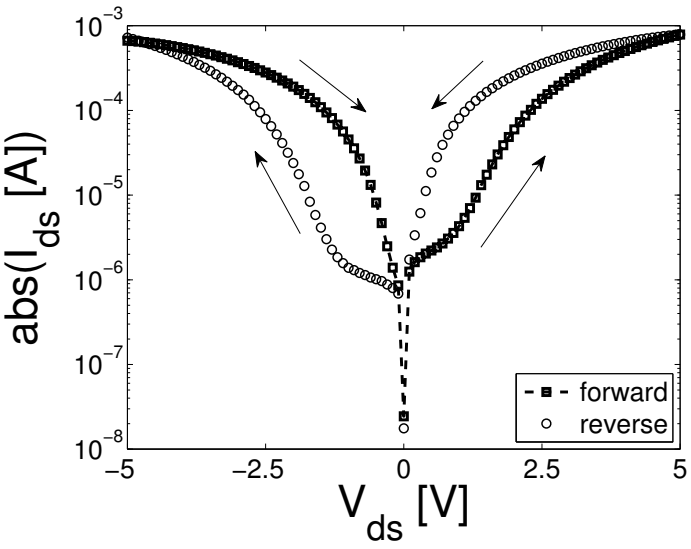


Figure 3.15: $I_{ds} - V_{ds}$ characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 SiNW in parallel. The forward sweep curve has a symmetrical correspondence with the reverse sweep curve, showing the respective Schottky barrier modulation. A current ratio of about 50 is found at either $V_{ds} = \pm 1$V. This behavior is typical of two-terminal memristive devices for ReRAM applications.

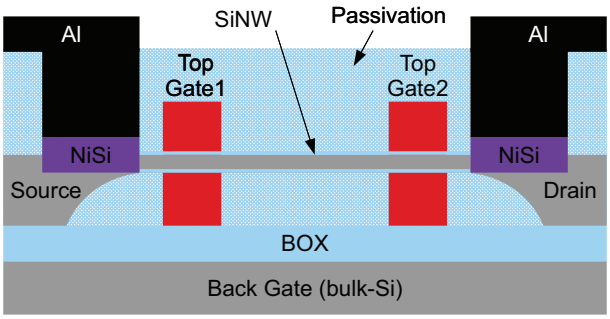
with V_0 a built-in voltage at the Schottky contact that is positive for a positive V sweep and negative for a negative V sweep.

3.4.2 Four-terminal memristive devices

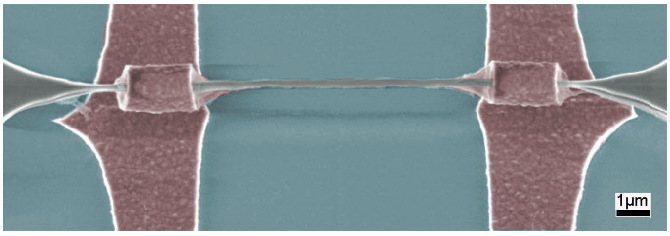
Memristive functionality can be seen as state variable that can be used for more expressive logic gates [6]. The memristive behavior reported in Section 3.4.1 for the SB SiNW FETs can be tuned by operating on the polarity of the gate voltage. This type of behavior is linked with the double conductance, for holes and electrons. As described in [51] for SB *Carbon-Nanotube (CNT)* FETS, the ambipolarity can be controlled by using an additional control gate, such that it blocks one type of carrier conductance. Following this principle, four-terminal memristive SB SiNW FETs can be built (see Fig. 3.16). In the following, two modes of operation are reported, depending on the nature of the controlling signal applied at the Si nanowire channel.

Voltage-controlled 4-T memristive device

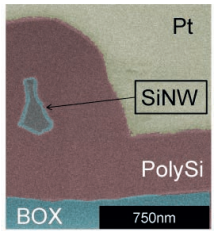
A voltage-controlled four-terminal memristive Schottky barrier SiNW FET is obtained by using a dual gate configuration such that one of the two gate is controlling a portion of the channel that is between the source/drain contacts and the main gate. This configuration is exploited to control the ambipolarity imbalance, such as for CNT FETs [51]. Since the back-gate voltage modifies the ambipolar conductance, this fact can be used in ambipolar memristive devices to limit the current levels for one of the carriers. A fixed back-gate voltage $V_{bg} = 0$ V



(a)



(b)



(c)

Figure 3.16: (a) Schematic cross-section of a dual gate device with NiSi source and drain regions on SOI substrate. (b) A 20 μm long SiNW with 2 parallel GAA polysilicon gates having 4 μm gate lengths. (c) A FIB cut cross-section image showing the SiNW channel surrounded by a 500 nm polysilicon top gate.

leads to imbalanced bistable hysteresis loops under different V_{gs} voltages. By applying a negative V_{bg}= −5V this imbalance is toggled to the negative side of the characteristics, giving a complementary effect (Fig. 3.17). Finally, a V_{bg}= +5 V levels off the conductances of electrons and holes, giving a fairly symmetric hysteresis.

Current-controlled 4-T memristive devices

A current-controlled version of the four-terminal memristive Schottky barrier SiNW FET is obtained by using a current I_{ds} bias instead of a V_{ds}. The output voltage is then compared with V_{gs} (Fig. 5.24a). The obtained hysteresis can be used as a latch device, whose position in the $V_{out} - V_{in}$ plane can be adjusted by using a different value of the current bias. A similar behavior has been exploited with three-terminal Schottky-barrier polysilicon nanowire FETs circuits to build a new logic family based on precharge and evaluation scheme [52]. Moreover, a similar scheme has been demonstrated for DRAM type of memory [53] and for pA current and temperature detection [54]. Similarly, SB Si nanowire transistors fabricated with a low termal budget process and biased in current-controlled mode shows a similar hysteresis. Moreover, polycrystalline SiNWs SB FETs can give an hysteretic transfer characteristic (Fig. 3.19) very similar to the one reported for crystalline SiNW SB FETs fabricated with a low thermal budget process [55]. As it is shown in Fig. 3.19 the maximum output voltage in the transfer characteristics increases with the I_{ds} bias current. From Fig. 3.19(a)-(c) the sweep time is reduced. Similarly to what was discussed for the three terminal SB SiNW FET memristive device, the sweeping time impacts on the amount of charge that traps at the gate

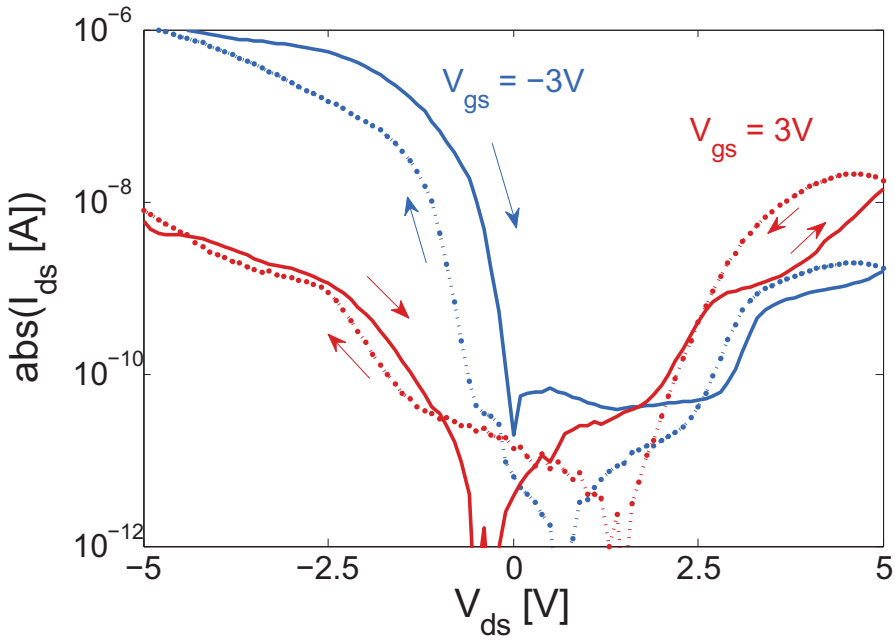


Figure 3.17: Controlled memristance for fixed top and back gate voltages $V_{bg} = -5$V.

oxide/channel interface, thus influencing the conductance state of the nanowire channel. A faster sweeping time outbalances the charge trapping/detrapping mechanism, resulting in lower output voltages (see Fig. 3.19(a)-(b) compared with Fig. 3.19(c)).

3.5 Chapter Summary and Conclusions

A general overview on multi-terminal memristive devices is reported. The functionality of the devices can be used for logic, memory and sensing applications. Ultra-dense memristive ReRAMs crossbar arrays can be used for ultra-dense non-volatile memory storage. It was shown that three- and four-terminal memristive devices can be used for both logic and memory applications. In particular, Schottky-barrier silicon nanowire FETs are very interesting devices due to their CMOS-compatibility and ease of fabrication. Disruptive applications exploiting the high expressive power of four-terminal memristive devices arranged in crossbar arrays are foreseen as a significant advance in the electronic computation.

The two-terminal memristive behavior concerning bipolar resistive RAM application will be further developed in Chapter 5, for several applications examples. Moreover, the unique features of the multi-terminal memristive Si nanowire transistors will also be discussed in more detail with focus on specific applications.

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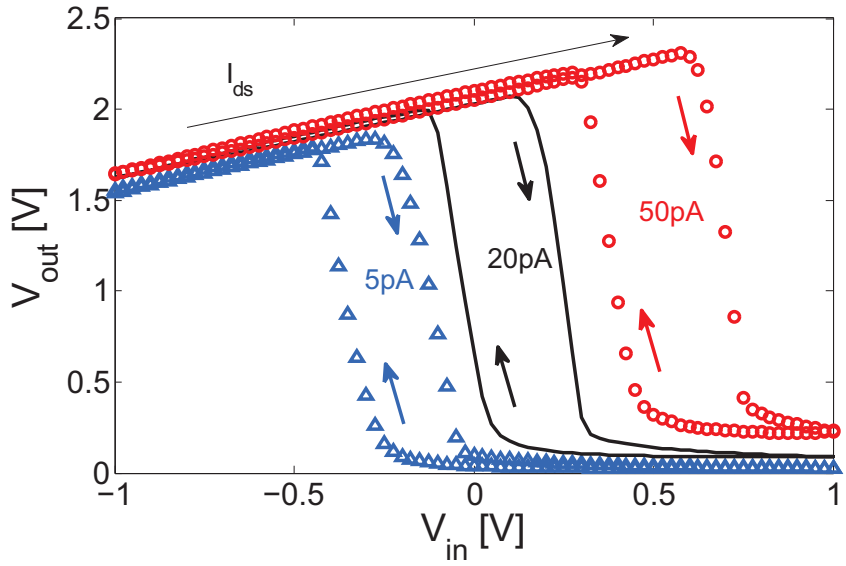


Figure 3.18: Current-controlled memristive Schottky barrier SiNW FET hysteresis loop.

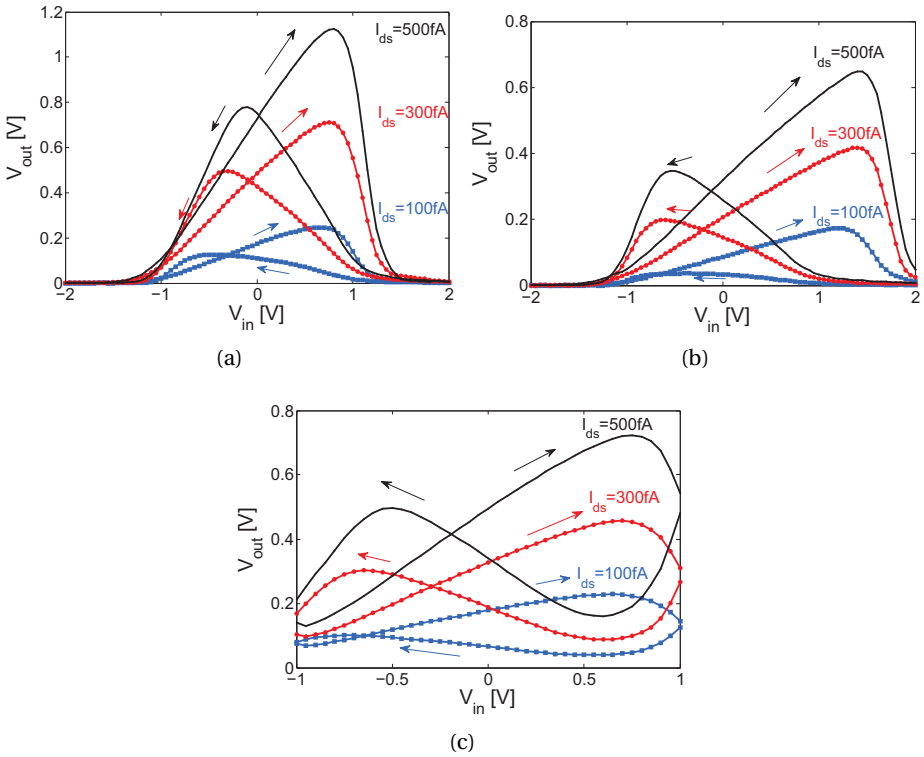


Figure 3.19: V_{out} voltages for increasing with I_{ds} current bias. In all the figures I_{ds} bias values are 100fA, 300fA and 500fA. Notice the output voltage hysteresis narrows for increasing frequency sweep: (a) 24sec. (b) 6sec. (c) 0.5sec.

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4 Applications of Ambipolarity

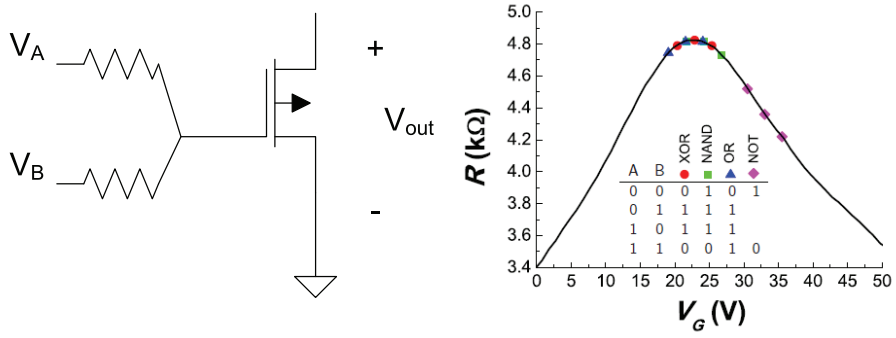
4.1 Introduction

In this chapter several examples on the use of the ambipolarity as computational variable are showcased. Quasi-static measurements of Schottky barrier FETs having SiNW channels has lead to ambipolar $I_{ds} - V_{gs}$ characteristic. This behavior can be explained with the physics of the metallic/semiconductor junctions at the source and drain of the devices. The Schottky barriers that characterize the fabricated FETs has a mid-gap profile, enabling either holes or electron current flows. In particular, with a negative (positive) gate voltage holes (electron) conductance occurs. Depending on the relative barrier heigths for electrons or holes and the mobility of eitheir of the carriers a certain level of ON current will be exploited to switch on the device.

A recent work of Sordan et al. [1] demonstrated the possibility to use the ambipolarity of a graphene based FET to compute different logic functions. The proposed prototype exploits the V-shaped resistance-voltage characteristic of the graphene channel to perform two input NOT, NAND, OR and XOR logic functions. However, the same principle can be applied to any ambipolar device, such as *Carbon Nanotubes (CNT)* FETs, *Thin-Film Transistors (TFT)* or undoped SiNW FETs with Schottky barrier source/drain. The logic biasing extended to the fabricated SiNW FETs are particularly attractive due to their CMOS-compatibility. The biasing scheme for two input logic functions is reproposed in Fig. 4.1. The versatility of this scheme enables the possibility to build more complex logic functions, using this device as building block.

Another possibility is to use ambipolar Si nanowire FETs to build ternary logic elements, thanks to the different conductance of the holes and the electrons in the same device. Alternatively, a current bias scheme of ambipolar Si nanowire FETs can be combined with standard binary Boolean logic elements to buid multi-valued logic circuits.

Another scheme utilizes an ambipolar SiNW FET with 2 gates to program the polarity of the device. This type of device has already been demonstrated for ambipolar CNT FETs [2] as well as for graphene ambipolar FETs [3] and for SiNW FETs [4, 5]. The polarity control can be exerted by means of a second gate to control the portions of the SiNW between a central gate and the sorce/drain regions. The control gate is held to a fixed voltage, depending on



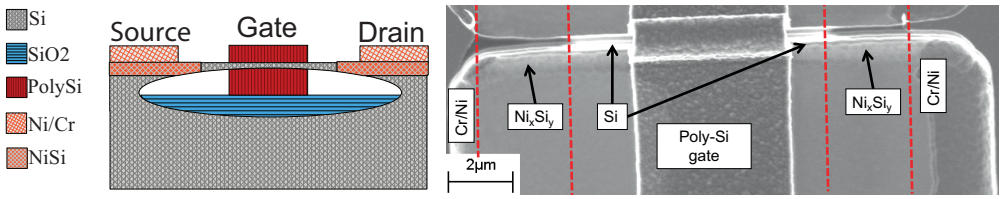
(a) (b)

Figure 4.1: (a) An ambipolar Schottky barrier FET with resistive biasing scheme from reference [1]. (b) The voltage partitioning scheme at the gate electrode is utilized to drive the device. Depending on the input voltages, XOR, NAND , OR and NOT operations can be performed.

which type of carrier is required for the same device. The main, central gate is then used to switch the device ON and OFF. This scheme allows to operate the FET either as a p- or a n-type device, depending only on the control gate voltage. Such a device would increase the required interconnects to operate the same but it gives the functionality of setting its polarity.

The use of ambipolar gates for logic circuits has many interesting opportunities. One should notice that a perfectly symmetric ambipolar device has to deal with both the carrier mobility and the Schottky barrier heigth for electrons and holes. For instance, an ambipolar device having equal carrier mobility for electrons and holes must build an equal Schottky barrier heigth with both carriers. However, this is often not the case, considering the limited choice of materials that are CMOS-compatible. In addition, Si has a lower mobility for holes than electrons. Hence, to produce a symmetrical ambipolar conductance it is necessary to use different channel widths or different channel lengths for p- and n-type devices. On the one hand using different lengths has the detrimental effect of increasing the device dimensions. Moreover, compact layouts are more difficult to design if the pull-up devices utilize different channel lengths with respect of the pull-down devices. On the other hand for nanowire channels the width is fixed, and only integer multiples of the single nanowire width are feasible. In the case of the logic-on-a-wire construction, the increase of the device width can be achieved adding the nanowires horizontally. However this approach has the drawback to reduce the device density significantly.

In Section 4.2 the ambipolar conductance of Schottky barrier Si nanowire FETs is discussed for ternary logic applications. Then, in Section 4.3, the possibility to utilize ambipolar SiNW FETs as threshold gates is discussed for its potential in multi-value logic. Then, the use of a double independent gate construction for logic is discussed in Section 4.4. Finally, a summary and the original contributions of this chapter are given in Section 4.5.



(a) (b)

Figure 4.2: (a) SiNW SB FET with NiSi source/drain and polysilicon GAA configuration. (b) Fabricated device having $8\mu m$ SiNW length and $3\mu m$ gate length. Ni_xSi_y source/drain extensions observable by the contrast difference.

4.2 Ternary Logic

4.2.1 Introduction

One way to improve the computational througput can be achieved by moving toward a ternary-logic paradigm. It can be shown that the most efficient radix for computation is ϵ, which makes the integer number 3 the best integer value [6]. For instance, if ternary logic elements could switch as fast as binary logic elements, then a 15-decimal digit number may be processed 57% faster if ternary circuits are used. In literature, different technologies can be utilized to build ternary logic elements, a few examples exploit bi-photons [7], ambipolar CNTs [8] or other semiconductor devices [6]. Nevertheless these approaches are still difficult to implement as these technologies are not as mature as the CMOS fabrication paradigm. In this section a new approach based on a Schottky barrier Si nanowire FET configuration has been investigated. The devices are built with a fabrication flow similar to what has been discussed in chapter 2. This device combines the memristive functionality of a Si nanowire SB FET originating from the charge trapping of the MOS oxide layer and ambipolar conductance. It is shown that a range of different functions can be achieved with this device, and how this can be applied to build ternary logic elements.

4.2.2 Device Fabrication

Recently, a CMOS-compatible process for SB SiNW FETs was proposed [9]. The devices consists of undoped SiNW channel with GAA polySi configuration (see Fig. 4.2.a). The source/drain regions consist of Ni_xSi_y, which has the property to form a mid-gap SB when put in contact with undoped Si. Contact regions for measurements are then obtained through Cr/Ni bilayer deposition and lift-off. An SEM picture of an SB FET device with $8\mu m$ SiNW length and $3\mu m$ gate length is shown in Fig. 4.2.b. A typical channel diameter in tested devices is of the order of 100nm.

4.2.3 Electrical Characterizations

The device construction generally leads to an ambipolar V-shaped $I_{ds} - V_{gs}$, as reported previously [9]. However, this time the devices were not annealed, thus avoiding the removal

of free charges from the gate oxide layer. The trapped charges have been observed to play a major role in the electrical behavior of the device, leading to a hysteretic $I_{ds} - V_{gs}$ characteristic (Fig. 4.3). Depending on the duration of the measurement (sweep time), a cumulative injection of holes (electrons) into the gate oxide layer can be obtained. In Fig. 4.3.a the long duration of the measurement is such that the free charges in the gate oxide layer are neutralized, and the electrical behavior follows the ambipolar characteristic of a mid-gap source/drain FET. The hysteresis is due to the direction of the measurement and consists of a lateral shift of the $I_{ds} - V_{gs}$ as for charge-based non-volatile memories [10]. In Fig. 4.3.b and Fig. 4.3.c the measurement duration is reduced, thus charge neutralization cannot completely occur during the forward regime. This produces an enlargement of the hysteresis window. Increasing further the measurement frequency (Fig. 4.3.d) inhibits the charging/discharging of the oxide layer making the device insensitive to the applied V_{gs}. A fast measurement is suitable for the reading operation. This behavior opens the possibility to program the device with a low (high) precharge phase. Reading can be performed in a subsequent phase of shorter period. Another effect is obtained when maintaining the same sweep time for different values of V_{ds}. Increasing V_{ds} at constant sweep time leads to an exponential increase of the current during forward sweep measurement (Fig. 4.4a). Applying $V_{ds} = 2$V and a sweep time of 512s leads to a channel resistance hysteresis (Fig. 4.4a) with three resistance states. As depicted in Fig. 4.4b, the channel resistance R_{ds} increases with the gate voltage when in forward regime. Measuring with decreasing V_{gs} leads to a different curve, due to the incomplete charge (discharge) of the gate oxide layer. The three resistance states can be computed using the scheme depicted in Fig. 4.5. A constant I_{ds} current bias of 2μA is applied. A *Low Resistance State (LRS)* can always be read at $V_{gs} = -10$V. A *Middle Resistance State (MRS)* is read when $V_{gs} = 10$V. Finally, an *Hiigh Resistance State (HRS)* can be read at $-1\text{V} < V_{gs} < 5\text{V}$ after an high precharge phase (which sets the device to work in the reverse regime).

A circuit can be built using two devices connected as depicted in Fig. 4.6. In Fig. 4.6 an output set of three values is expected using an high precharge phase for device A and a low precharge phase for device B. Reading consists of evaluating the output resistance with a certain combination of input values, L (-10V), M (1V) or H (+10V). The circuit shows three possible combinations of low/high precharge phases making device A and B to work into either forward or reverse mode. Table 4.1 reports the possible output states depending on the combination of reading signals. Depending on the precharge phases, 2, 3 or 4 resistance states can be stored and read.

Ratioed ternary-logic shifter

The difference in the conductance coming from an asymmetric ambipolar SiNW FET can be used for ternary-logic circuits, for which the input signal can assume three states to drive the current to three different values. A basic device would consist of an ambipolar SiNW FET with a pull-up resistor (see Fig. 4.7). The pull-up resistor would be of the value of the MRS of the SiNW FET and always conducting. The 3-valued conductance of the asymmetrical ambipolar FET would make the output node to assume 3 values of voltage, depending on the input voltage. The voltage divider circuit composed of the pull-up resistor and the pull-down device would make the output voltage to make a shift of the input voltage. This shifting can be applied multiple times, by cascading the devices as depicted in Fig. 4.8. At each stage, the

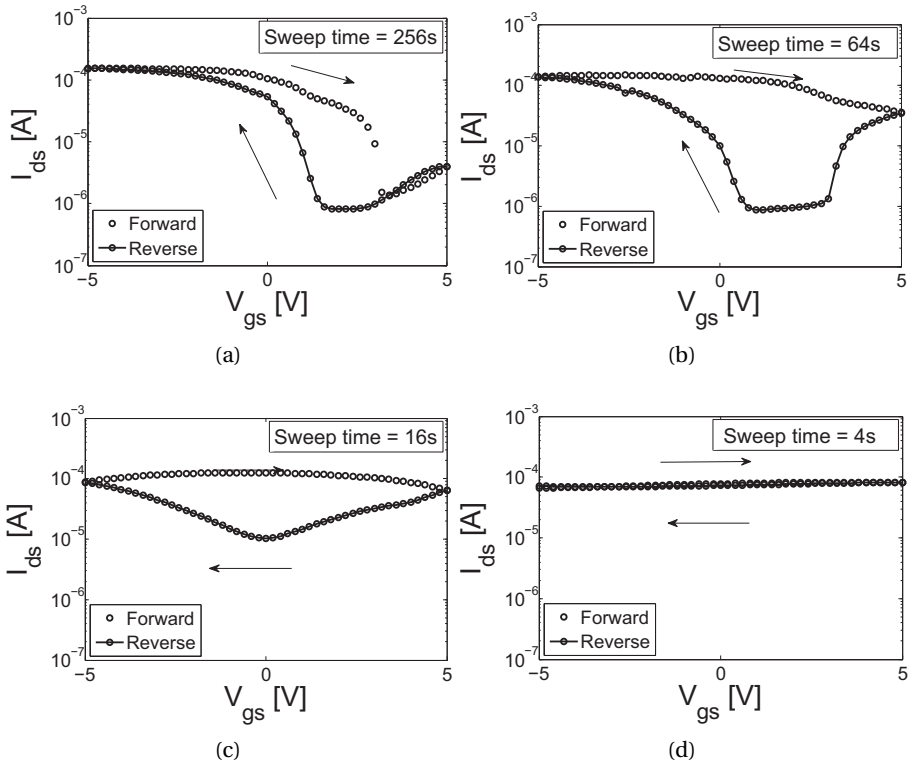


Figure 4.3: Hysteretic dependence with the measurement (sweep time) duration. From (a) to (d) the sweep time is reduced, thus a longer time is needed to program the device and a shorter time would be used to measure the programmed current.

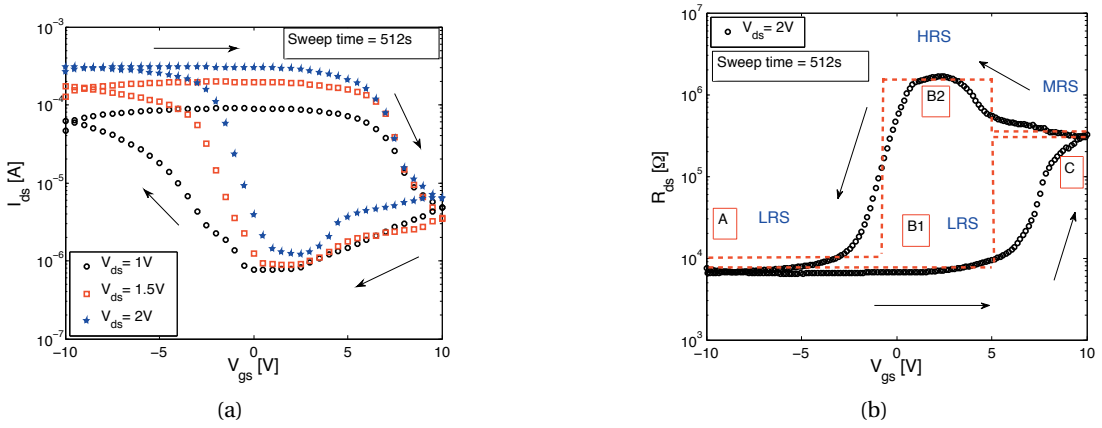


Figure 4.4: (a)Dependence of the measured current and the hysteresis loop on the V_{ds} voltage. For this plot, the device dimensions are different from those of Fig. 4.3. (b) Measured resistive hysteresis characteristic of the device at V_{ds}= 2V. The hysteresis shows three main plateau: (A) LRS at V_{gs}= −10V ; (B1) LRS when V_{gs}= 0V and forward regime; (B2) HRS when V_{gs}= 0V and reverse regime; (C) MRS at V_{gs}= 10V . Dashed lines indicates the idealized hysteresis characteristic.

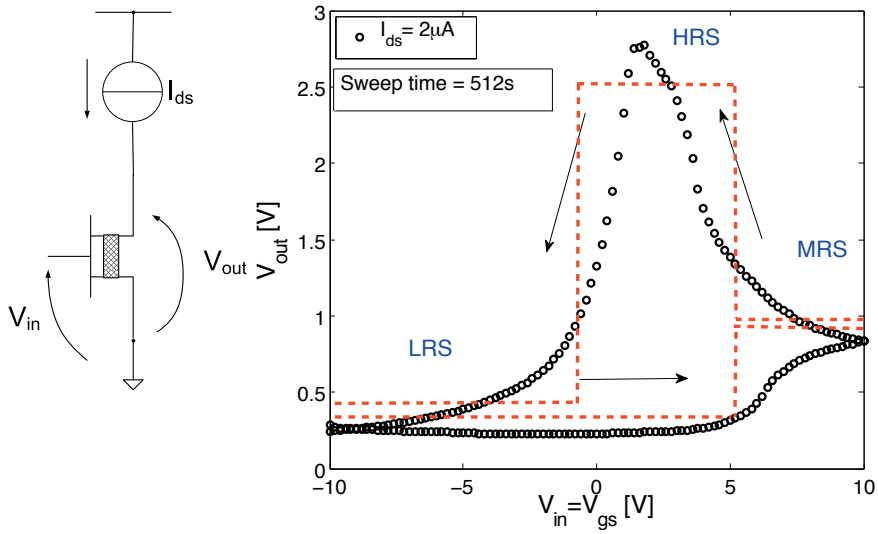


Figure 4.5: $V_{out} - V_{in}$ transfer characteristic of the device with constant current bias and constant sweep time.

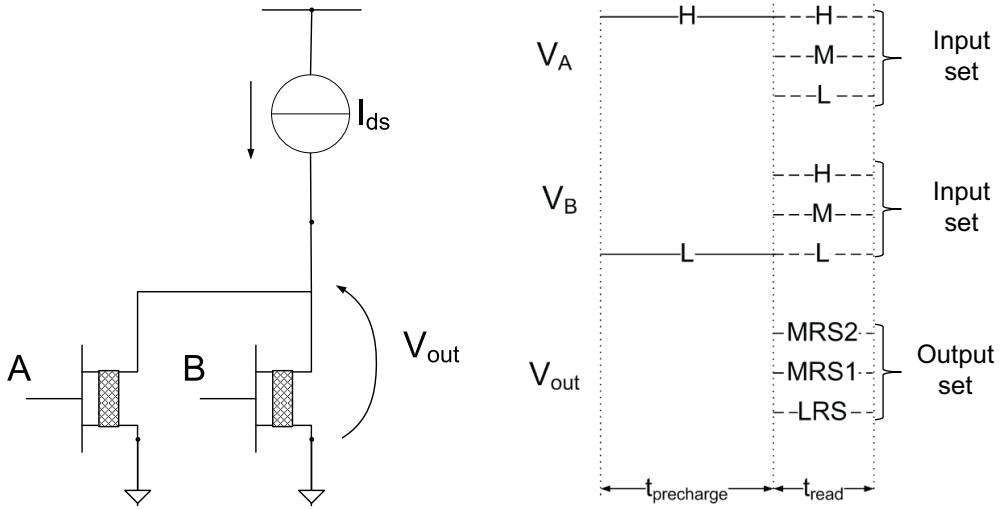
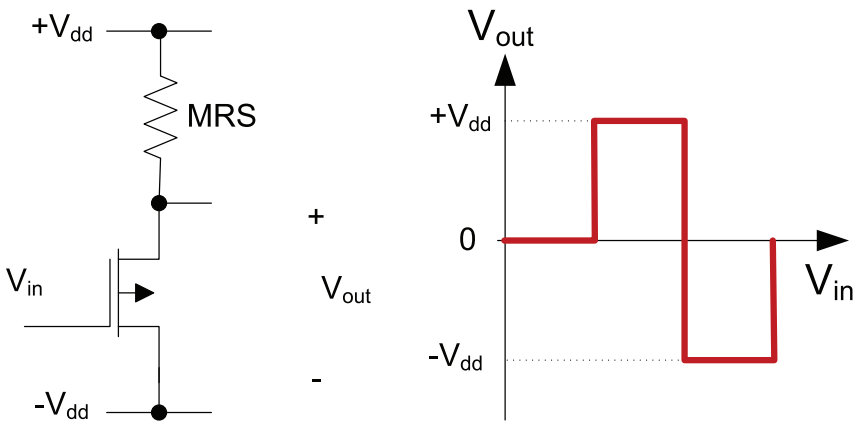


Figure 4.6: Proposed ternary logic circuit element and expected output when high precharged V_A and low precharged V_B are used.



(a) (b)

Figure 4.7: The ternary-logic device can combined with a pull-up resistance to obtain a three-state logic device.

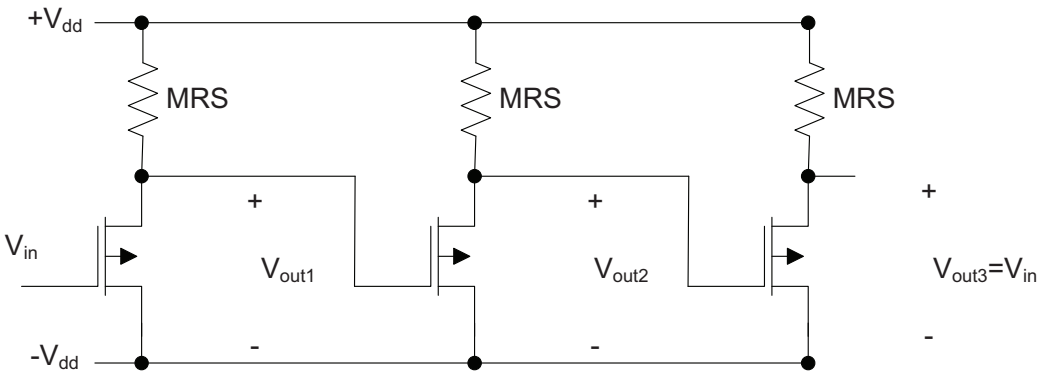
Table 4.1: Expected resistance states for the proposed circuit of Fig. 4.6.

IN		OUTPUT		
A	B	Low A and B	Low A, High B	High A and B
L	L	LRS	LRS	LRS
L	M	LRS	LRS	LRS
L	H	LRS	LRS	LRS
M	L	LRS	LRS	LRS
M	M	LRS	LRS	HRS
M	H	LRS	LRS	MRS2
H	L	LRS	LRS	LRS
H	M	LRS	MRS2	MRS2
H	H	MRS1	MRS1	MRS1

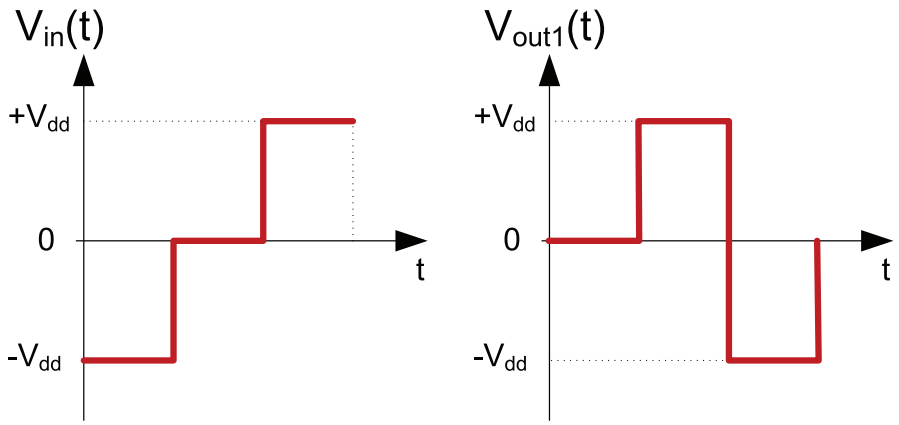
ternary-logic device makes a shift of the input states. Thus, an equivalent of the binary logic buffer can be obtained by cascading three ternary-logic devices.

4.2.4 Summary

The operation of an ambipolar SiNW SBFET for both memory and computation applications in multi-value circuitry has been demonstrated. Retention times longer than 4 seconds makes the device suitable for DRAM applications. The combination of two or more devices can be used to build multi-bits logic and memory. In addition, the technological process used for the SiNW structure is compatible with 3D ultra-high dense crossbar configuration, with projected cross-point density of $5 \cdot 10^{11}/\text{mm}^2$, which is based on the vertically-stacked SiNW technology demonstrated by the authors [9] (Fig. 4.9). The combination of high-dense arrays with multi-bits operations is envisaged for ultimate performance logic/memory circuits.

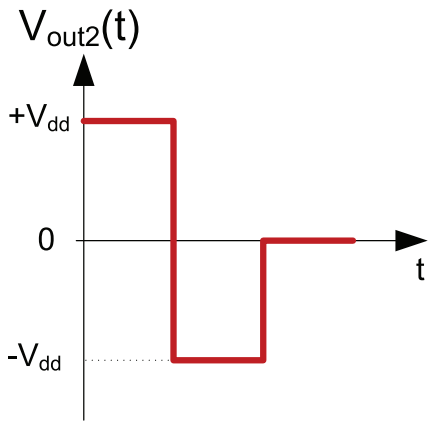


(a)

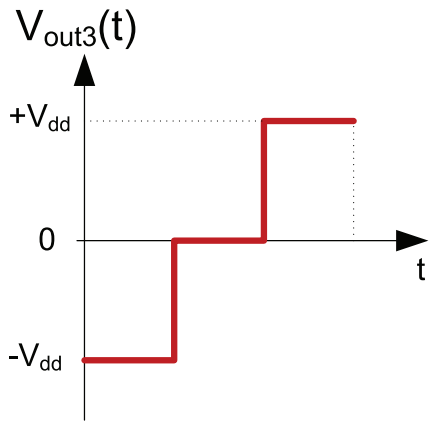


(b)

(c)



(d)



(e)

Figure 4.8: Cascading the ternary logic device can be used to make three-value shifter. At each stage, the ternary-logic device makes a shift of the input states. Using three devices in cascade makes the equivalent of the buffer for ternary-logic.

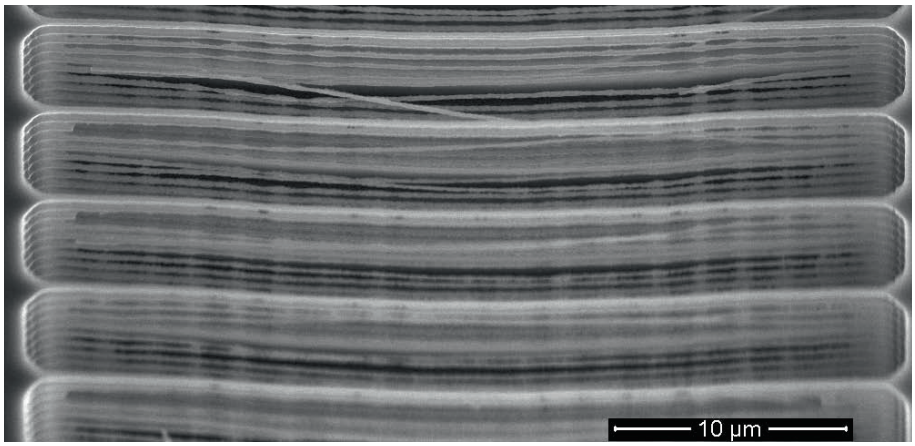


Figure 4.9: High density array produced with a CMOS-compatible top-down approach [9] consisting of multiple parallel strands of vertically-stacked SiNWs, each with a diameter of <100nm. The structure is suitable for ultra-high dense 3D crossbar arrays of ternary logic/memory elements.

4.3 Multiple valued logic functions based in Si nanowire Threshold gates

Multiple-valued logic (MVL) is a candidate circuit design technique to replace traditional Boolean logic based on CMOS [11]. One dimensional devices exploiting novel functionalities are the most credible candidates for future nanosystems [4, 12]. Recently, a fully-CMOS compatible process flow has been proposed for the fabrication of vertically-stacked SiNW GAA SBFETs showing ambipolar behavior [9]. Ambipolarity has been envisaged as a way to build gates capable of exploiting denser logic functions [13], and here we originally propose to exploit the Schottky barrier for *Threshold Logic (TL)* gates, enabling the constructions of MVL functions. In this paper a completely new SB crystalline SiNW device for the implementation of MVL functions is proposed, characterized and studied over a broad range of temperatures. A single SiNW FET implementing TL functionality, without the need of the large number of transistors as in capacitive TL is demonstrated with ultra-low power consumption.

4.3.1 Device Fabrication

The device fabrication is similar to what has been described in chapter 2 and here a quick summary of the clean room processes are given. The device scheme consists of a SiNW having NiSi source/drain contacts with 2 parallel polysilicon gates with GAA configuration. A slightly p-doped SOI wafer is used as the substrate. Then a DRIE technique is adapted to form a single suspended Si ribbon over the BOX. The 1μm wide Si nanoribbon anchored to 2 Si pillars is smoothed and thinned down to a 100nm diameter cross-section by means of a 500nm sacrificial oxidation step. A 20nm dry oxidation is performed followed by a 500nm LPCVD polysilicon layer. The patterning enables a device construction having two parallel polySi gates over 20μm long SiNWs. A passivation layer of 1μm sputtered SiO_2 is deposited and used as hard mask for the metallization phase. The self-alignment of the via openings with the

lift-off is then exploited for the definition of 50nm thick contact areas at the anchor points of the devices. This first metallization layer consists of a 50nm Ni + 10nm Al deposited by a standard e-beam evaporation tool. The Al is used as a cap layer to prevent Ni oxidation during the silicidation and to provide a good interface with final metallization. Then a dual step silicidation annealing has been performed in a standard horizontal wall furnace to form NiSi source/drain regions. Finally, 1μm thick Al is patterned for electrical characterizations.

4.3.2 Electrical Characterization

An ambipolar V-shaped $I_{ds} - V_{bg}$ can be observed with similar ON currents for both hole and electron conductances; $I_{ON}^{h+} / I_{ON}^{e-} \leq 10$. Moreover, increasing positive V_{gs} voltage produces a shift of the curve toward negative V_{bg} voltages. This effect is explained by the increasing effort required by the back gate voltage to counteract the top gate electric field. An Arrhenius plot has been extracted by means of $I_{ds} - V_{gs}$ measurements at $V_{ds} = 100$mV and low gate voltages in the temperature range between 25°C and 115°C. The conductance of the device is attributed to different regimes, which are due to thermionic emission and tunneling through the Schottky barrier. From this data, an average effective barrier of $E_a = 450 \pm 5$meV is found for $V_{gs} \geq 0.2$V. However, since the device in this regime has both thermionic and tunneling components, a better estimation of ϕ_{Beff} is obtained from the maximum at $V_{gs} = -0.45$V, as suggested by Svensson et al. [14]. Either the ambipolar $I_{ds} - V_{gs}$ characteristics and the activation energy plots confirm the mid-gap nature of the Schottky barrier. This is exploited in a pseudo-inverter configuration, using a current source for the pull-up network in order to generate the inverter transfer characteristics of Fig. 4.10a at room temperature. By increasing the current bias, the switching point can be shifted toward more positive input voltages, Vin. Moreover in Fig. 4.10a, three different thresholds are obtained by means of current values between 20pA and 90pA which is compatible with ultra-low power consumption in the order of tens of pWs. The functionality of the device is preserved at temperatures as high as 115°C with good inverter gain (see Fig. 4.10b. A two-device cascading with buffer-like functionality is shown in Fig. 4.10c, demonstrating that more complex circuits can be built using this nanowire technology.

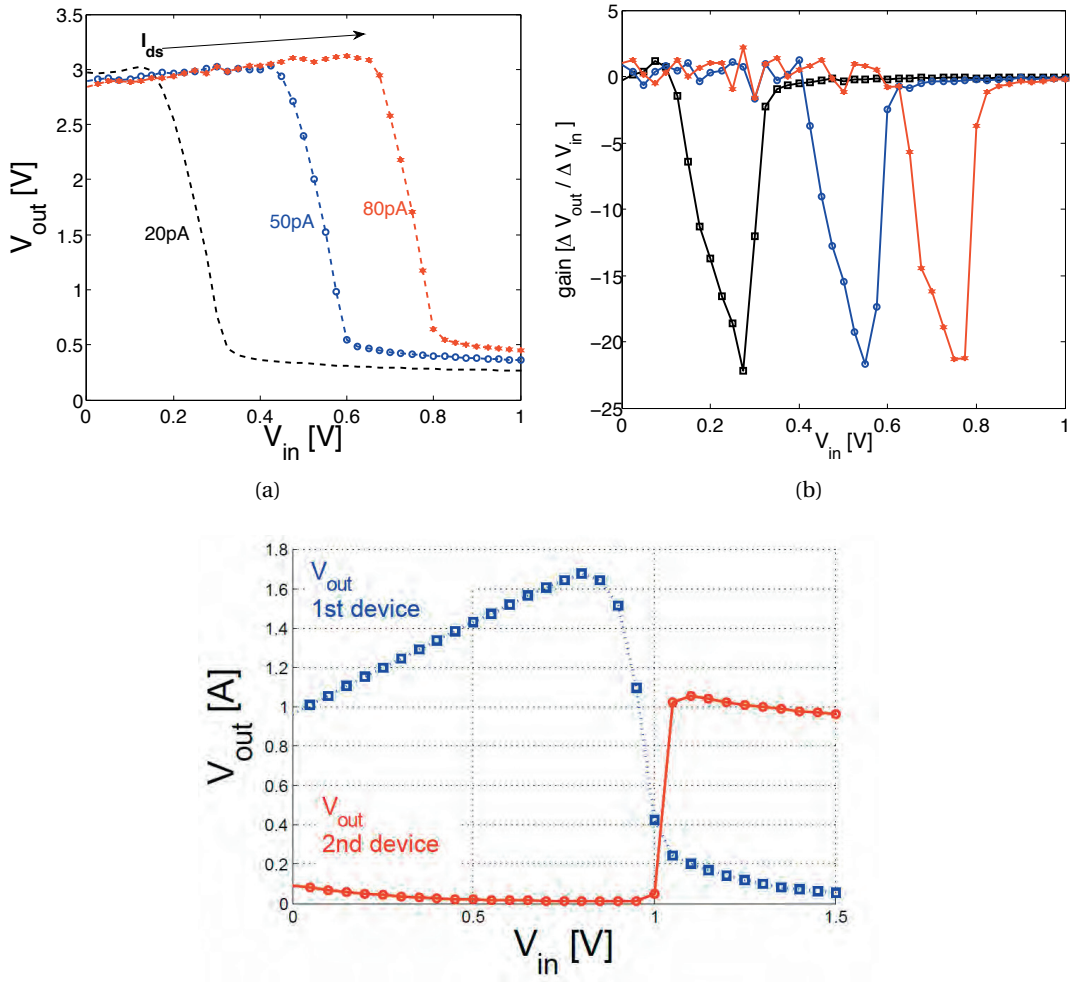
4.3.3 Threshold gates for multiple valued logic

Threshold Logic (TL) gates are implemented exploiting the shift of the inversing point of the devices by changing the current bias. A set of three threshold gates having threshold voltages of 0.25V, 0.5V, 0.75V are obtained by using bias currents of 20pA, 35pA and 50pA respectively. A one-variable literal function using an AND gate and 2 TL gates having opposite polarities and thresholds at 0.5V and 0.75V is shown in Fig. 4.11a. A two-input MVL function can be obtained by connecting a two-input Boolean function with 2 TL gates. By using an AND gate we obtain a MVL-AND function (Fig. 4.11b), whereas a NOR gate is used to implement a MVL-NOR function (Fig. 4.11c). More complex combinations are possible, and a proposed MVL function is depicted in Fig. 4.11d, where MVL-NOR and MVL-NAND gates are combined with a Boolean INV and AND. The surface plot of Fig. 4.11d shows how a function can be mapped inside a two-variable input space. Some of the most commonly used functions in MVL are the MIN and MAX operators. A three-layer arrangement consisting of a first layer of TL gates, a second layer of Boolean logic gates, and a third layer of level recovery allows the construction of the

MVL-NMAX or MVL-NMIN operators (Fig. 4.12a). The 3D staircase output representation of the MVL-NMAX function is shown in Fig. 4.12b.

4.3.4 Summary

The proposed nanowire-based device proves to be a versatile TL block for the synthesis of several MVL functions. The excellent input/output voltage ranges observed experimentally enable cascaded operation of TL nanowire gates with Boolean gates. A reset signal is required to set the device threshold before using it for MVL logic circuit operation.



(a) (b)

(c)

Figure 4.10: (a) Transfer characteristics of pseudo-NMOS inverter configuration. Pull-up PMOS is substituted by a current source. The increase of current bias is reflected into a shift of the switching threshold toward more positive values. This behavior can be exploited to implement a threshold gate out of a single device. (b) Threshold gate gain of the pseudo-inverters for different current biases. (c) Voltage signals of two devices in cascade. The voltage ranges are compatible for driving more complex gates. Threshold voltage is set at 1V.

4.4 Logic functions with polarity controllable devices

An ambipolar SiNW FETs with *Double Independent Gate (DIG)* structure enable the use of polarity control signals as a method toward Si circuits with increased logic expressive power. Moreover, the use of polarity control leads to improved performance in terms of $I_{ON} - I_{OFF}$ ratio and inverse subthreshold slopes with respect to the ambipolar behavior.

4.4.1 Device Description

The device consists of a 20μm-long crystalline SiNW attached between two Si pillars on a SOI wafer (see Fig. 5.19a). The SiNW is then covered by two independent n++ polysilicon gates with this scheme: a main central gate (gate 1) of 7.5μm length and a second gate (gate 2) that is used to control the SiNW portions between the main gate and source and drain regions, respectively.

4.4.2 Fabrication

First, a low doping p-type ($N_A \approx 10^{15}$atoms/cm^2) SOI wafer with 1.5μm device layer is spin coated. The photoresist is then patterned in 1.5μm wide lines (see Fig. 5.19b) and used as mask for a next isotropic Si etching. A Si plasma etching recipe is tuned to form a triangular 75nm wide SiNW lying on top of the BOX layer (Fig. 5.19c. Then a 30nm thick gate oxidation and a 150nm polysilicon layer are deposited with LPCVD method to form a main gate with 7.5μm length (gate 1, Fig. 4.13d). The main gate is then isolated by a 300nm LPCVD LTO. A second 500nm polysilicon layer is then deposited. Then a thick photoresist is spun over the wafer and planarized using a chemical mechanical polishing procedure similar to the one previously described by the authors in [9]. This method leaves a protective polymer layer that is used to etch a second polysilicon gate self-aligned within the cavity thanks to the topography (see gate 2 in Fig. 4.13e). After standard cleaning steps, one additional patterning of gate 2 is performed to remove the unnecessary polysilicon and to form areas for the contacts (see the top view of the device in Fig. 5.19a). In Fig. 4.13f, a focused ion beam cross-section of the triangular SiNW channel with the DIG stack is shown. Then source/drain contacts are formed by means of NiSi silicidation in a horizontal wall furnace in forming gas at 400°C. Finally Al metal lines and pad area are defined for the electrical characterization.

4.4.3 Device Operation

The source/drain regions after NiSi silicidation have a mid-gap Schottky barrier contact with the SiNW, thus both electrons and holes can contribute to the current flow. The use of the two gates enables the selection of which carrier species shall prevail in the conduction. In the following discussions, the voltage applied to gate 1 is defined as V_{gs}, while the voltage applied to gate 2 V_{bg}. This scheme was proposed by Lin et al. [15] for the control of polarity of CNT FETs. As depicted in Fig. 5.5a, positive back gate voltage V_{bg} enable electron flow, while holes current is blocked. Similarly, (Fig. 5.5b) negative V_{bg} makes the opposite selection: holes current is enabled while the electron flow is blocked.

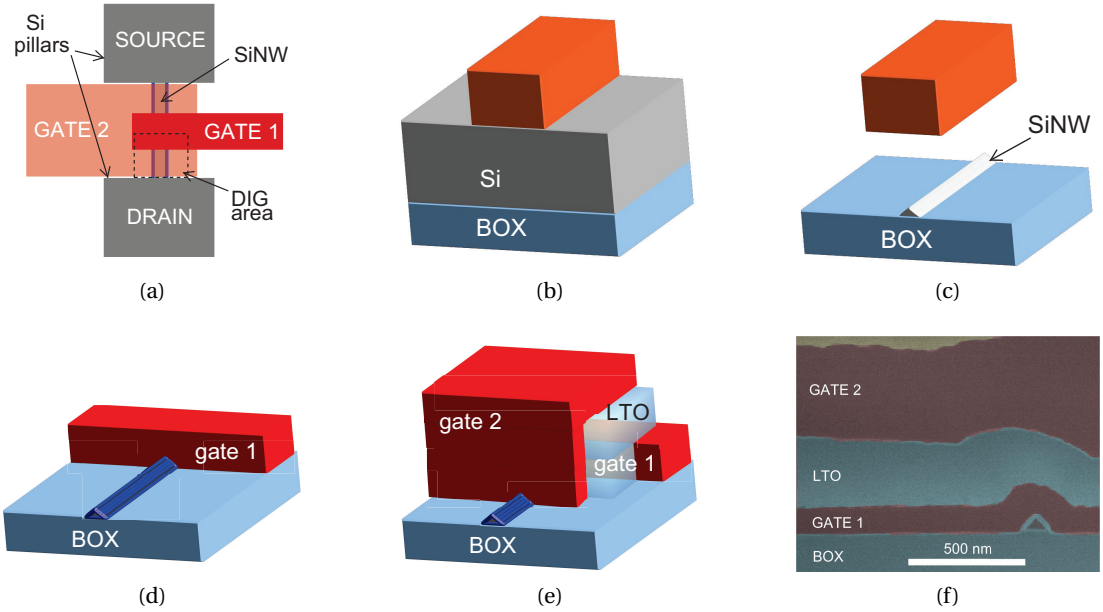


Figure 4.13: Fabrication flow. (a) Top view of the dual-gate device. The next steps focuses on the DIG area construction. (b) Photoresist mask is patterned. (c) After isotropic etching of Si a triangular-shaped SiNW is formed. (d) Gate oxidation and LPCVD polysilicon are deposited and patterned to form the main, central gate stack. (e) A LTO inter-poly dielectric is deposited and a second polysilicon gate is made self-aligned with the nanowire. (f) Focused ion beam cross-section showing a triangular SiNW channel with two 75nm sides and 100nm base. The gate 1, gate 2 and the LTO inter-poly dielectric have 150nm, 500nm and 300nm thicknesses, respectively. Gate 1 dielectic is 30nm thick.

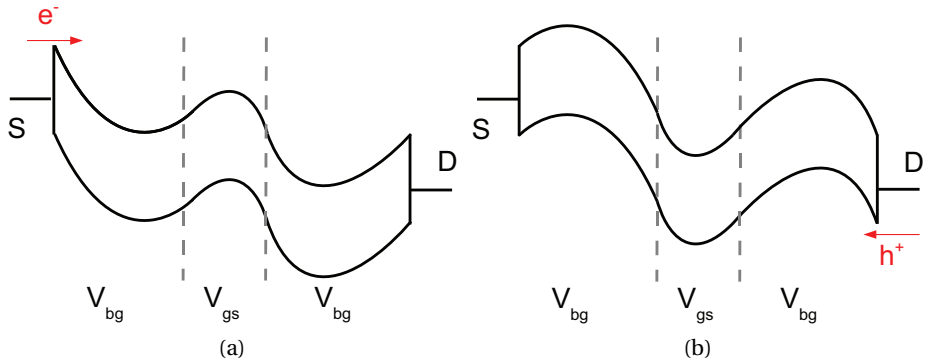


Figure 4.14: (a) Conceptual band diagram for n-type operation. A positive V_{bg} is used to block the flow of holes from the drain. (b) Conceptual band diagram for p-type operation. A negative V_{bg} is used to block the flow of electrons from the source.

V_{bg}[V]	$\frac{I^{h+}_{ON}}{I_{OFF}}$	$\frac{I^{e-}_{ON}}{I_{OFF}}$	SS^{h+}[mV/dec]	SS^{e-}[mv/dec]
+10	50	250	1000	600
+7.5	N/A	2000	N/A	250
+5	N/A	1000	N/A	250
+2.5	N/A	1000	N/A	325
0	1000	600	475	750
-2.5	1000	N/A	375	N/A
-5	5000	N/A	250	N/A
-7.5	10000	N/A	300	N/A
-10	30000	N/A	300	N/A

Table 4.2: Obtained electrical behavior for different V_{bg} voltages.

4.4.4 Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer in dark at room temperature. In Table 5.1 the effect of V_{bg} on the inverse subthreshold slopes (SS^{h+}, SS^{e-}) for hole and electron conduction branches depicts a trend for improved SS^{h+} and SS^{e-} when increasing V_{bg} voltages of negative and positive polarities are applied, respectively. Similarly, improved $I_{ON} - I_{OFF}$ ratio ($\frac{I^{h+}_{ON}}{I_{OFF}}$, $\frac{I^{e-}_{ON}}{I_{OFF}}$) is observed when larger V_{bg} voltages are applied. The improved performance is related with a reduced I_{OFF} current due to the screening of one of the two types of carriers for the conduction. As better shown in Fig. 5.26b, positive or negative V_{bg} voltages can be used to obtain n-type or p-type $I_{ds} - V_{gs}$. Moreover, a symmetrical ambipolar $I_{ds} - V_{gs}$ is obtained for $V_{bg} = 0$V. This functionality allows for increased expressive logic power with a single FET. For instance, the two voltage signals, V_{gs} and V_{bg} can be coded to make logic XOR operation with the device of Fig. 5.26b; an operation that would require more transistors in standard CMOS technology. In Table 4.3, V_{gs} and V_{bg} voltage values are encoded into logic levels 0 and 1 to map into four binary logic operations: XOR, NAND, AND and NOR, while using the data plot in Fig. 5.26b. The result of the logic operation are summarized in Table 4.4. Logic 0 and logic 1 outputs are represented by light and dark gray, respectively. Another solution that can be envisaged can use the same logic levels for both gates in order to save space for external encoding circuits. This solution will become a most desirable one by optimizing the thickness of the two gate dielectrics, which in the current implementation lead to a more effective electric field density for gate 1 than for gate 2. In future designs, this technological issue might be overcome by optimizing the dielectric thickness for the two gates and/or in combination with dopant segregation techniques to balance the Schottky barrier heights for holes and electrons. Moreover, gate workfunction engineering can be used to code the threshold voltage of the device, thus addressing the different logic 0/1 voltages needed for a specific logic function. Thanks to these technological options, dense arrays of ambipolar DIG FETs can be envisaged as basic building blocks to map complex logic circuits. The AC characteristic of the proposed device concerning delay and power will depend, among other factors, on the capacitive coupling between the two gate electrodes. However, this parasitic coupling is estimated to be of the same order of magnitude of the source/drain to gate capacitance, and giving the fact that the fabricated device performs a more expressive logic functionality, this additional coupling is not expected to be a limiting factor.

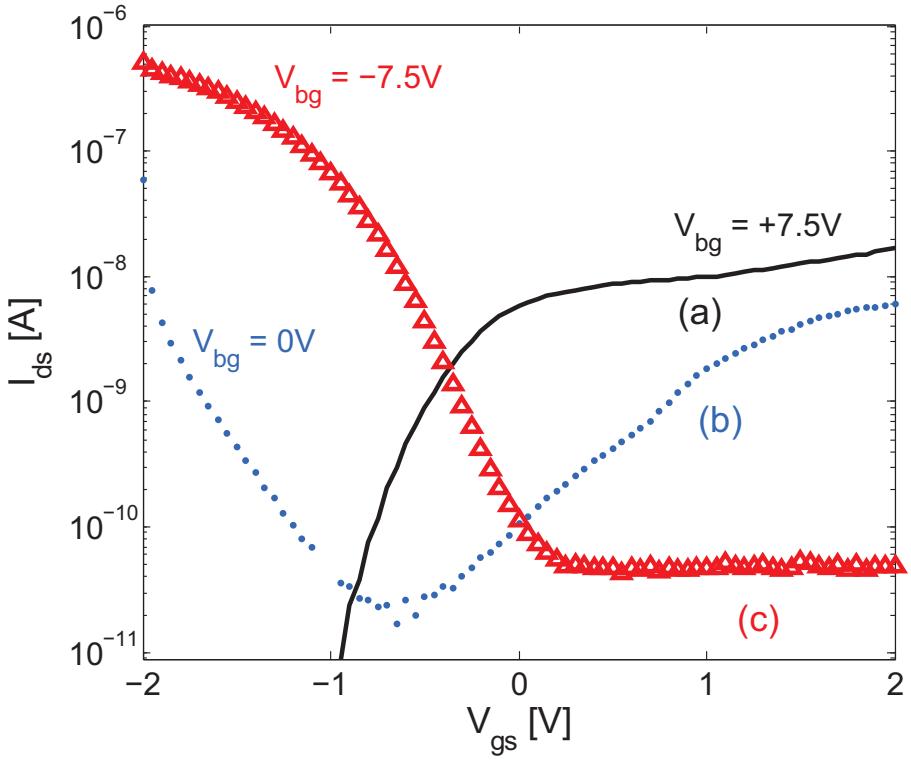


Figure 4.15: Controlled ambipolar $I_{ds} - V_{gs}$ characteristics at different V_{bg} back gate voltages. (a) A positive $V_{bg} = +7.5V$ is used to obtain a n-type characteristic. (b) A $V_{bg} = 0V$ gives ambipolar $I_{ds} - V_{gs}$. (c) A negative $V_{bg} = -7.5V$ is used to obtain a p-type characteristic.

CODE	XOR		NAND		AND		NOR	
	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]
logic 0	+1	-7.5	-0.5	+7.5	0	0	0	+7.5
logic 1	-1	+7.5	+1	-7.5	-1	-7.5	-1	0

Table 4.3: Binary logic - voltage signals coding for XOR, NAND, AND and NOR operation.

logic values		XOR	NAND	AND	NOR
gate 1	gate 2	I_{OUT} [A]	I_{OUT} [A]	I_{OUT} [A]	I_{OUT} [A]
0	0	$4 \cdot 10^{-11}$	$2 \cdot 10^{-9}$	10^{-10}	$6 \cdot 10^{-9}$
0	1	10^{-8}	$2 \cdot 10^{-9}$	10^{-10}	10^{-10}
1	0	$7 \cdot 10^{-8}$	10^{-8}	10^{-11}	10^{-11}
1	1	10^{-11}	$4 \cdot 10^{-11}$	10^{-7}	$5 \cdot 10^{-11}$

Table 4.4: Output current levels for the 4 logic operations: XOR, NAND, AND, NOR.

4.4.5 Summary

In this study a new device structure exploiting a double independent gate configuration with SiNW and top-down fabrication flow has been demonstrated as useful building block for ambipolar-controlled logic operation. All the $I_{ds} - V_{gs}$ characteristics, defining n-type, p-type and ambipolar behavior have been obtained with good $I_{ON} - I_{OFF}$ ratio of up to 4 orders of magnitude and inverse subthreshold slopes close to state-of-the art Schottky barrier FETs. In addition, a single device can be used to perform any of the XOR, XNOR, NAND, AND and NOR binary logic operations depending on the input signals encoding. The proposed integration scheme is envisaged for logic circuits exploiting the improved logic expressive power of ambipolar-controlled SiNW devices, which is enabled by the reliability of Si fabrication technology.

4.5 Chapter Summary and Conclusions

In this chapter applications of ambipolar devices have been discussed. In particular, asymmetric ambipolar devices can be exploited for ternary logic, as they provide two ON state conductance (one for electrons and one for holes) and one OFF state. This feature can be exploited to build ternary logic gates. Another interesting feature of ambipolar SiNW transistor is the possibility of building precise threshold gates by using a current biasing scheme. Then, the threshold gates can be utilized to build generic multi-value logic gates, as the base for more complex multi-value functions such as NMAX. Finally, the use of double independent gate construction enables the control of the electric field at the Schottky junctions, independently from the gate built around the central portion of the channel. This feature can be exploited to compute boolean logic functions with a single device and paves the way for more complex logic circuits exploiting the ambipolarity as a computational state variable.

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5 Applications of Memristance

5.1 Introduction

Very different applications belonging to signal processing, memory and sensing are envisaged for multi-terminal memristive devices. The possibility to build very dense crossbar arrays of two-terminal memristive devices is often seen as a disruptive technology for ultra-dense ReRAM or *Write-at-Once Memory (WORM)* storage [1]. In this concern, all the non-volatile two-terminal memristive technologies are suitable candidates to replace flash memory in the future, given their higher density storage per cost. This feature is especially interesting because it can be utilized to stack non-volatile memory elements in the BEoL, increasing both density and access speed among logic and memory layers. Good examples are the recently proposed hybrid semiconductor/nanowire/molecular (CMOL) integrated circuits [2], as well as 3D *Field Programmable Gate Arrays (FPGA)* architectures with programmable *Through Silicon Vias (TSVs)* [3] (see Fig. 5.1). The two-terminal memristive crossbars can also be integrated into programmable logic array architectures to compute Boolean logic functions. The memristive crossbar architecture can be exploited to re-program itself. For instance in [4], a very dense nanowire crossbar with TiO_2 memristive junctions was used to perform logic functions and to store the result into another portion of the same crossbar. Moreover, memristive switches can be used to perform material implication function [1] and exploited to build latches that use resistance in place of voltage or charges as physical state variable [5]. Another application that can exploit the memristive functionality is related to the design of Cellular Neural Networks [6]. The Hodgkin-Huxley model for the synapse was one of the earlier examples reported by Chua and Kang [7] of systems that can be modeled with the memristor. Recently, the use of two-terminal memristive devices in combination with digital to analog converters demonstrated a way of reproducing the associative memory of animals [8]. The modification of the memristive characteristic to environmental conditions can also be utilized for different types of sensing. For instance, functionalization of nanowires with redox active molecules give rise to the typical memristive pinched hysteresis loop [9]. Another example can be the sensing of temperature with spintronic memristor [10]. The temperature change can cause a variation of the domain-wall mobility that in turns is sensed thanks to a positive feedback loop electronics. This type of sensor has been reported to be

[1] Here, the material implication is used for a fundamental Boolean logic operation on two variables p and q such that pIMPq is equivalent to (NOTp)ORq

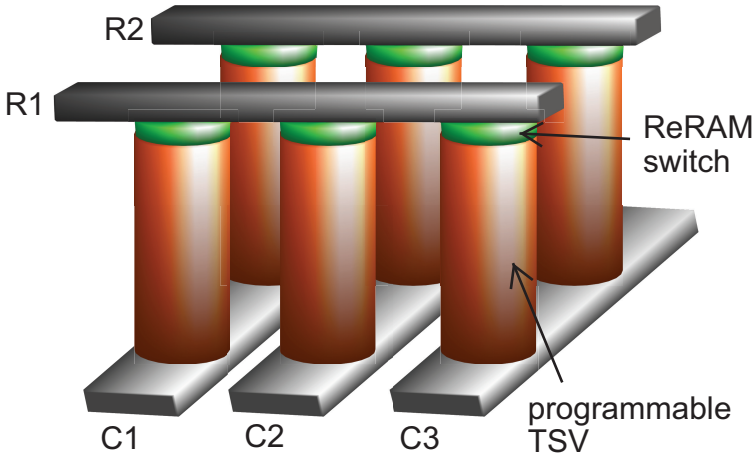


Figure 5.1: A crossbar architecture with programmable TSVs made of ReRAM stacks [3].

very compact ($\leq$1 μm^2 cell size) and to operate with very low power.

Multi-terminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [11] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for bio-molecule detection in dry environment [12]. More specifically, in [12] the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all-around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authours [13]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [14]. For instance in [14], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing an hysteretical negative differential resistance [15]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel. In chapter 3, it has been shown that a similar hysteresis can also be obtained independently on the phase state of the Si nanowire channel. Similarly, the same structure can exploit the functionality of an additional gate to tune the polarity of a SB SiNW FET, thus giving even more functionality, as described in the previous chapter. A very high expressive power architecture can be made of four-terminal memristive devices arranged in a crossbar implementation that exploits the high-density of the SiNW arrays (Fig. 5.2).

In this chapter applications for two-terminal memristive devices, and specifically bipolar resistive RAM are discussed. In Section 5.2 an example of fabrication and characterization of bipolar resistive RAM based on Al_2O_3 and Ta_2O_5 is discussed. Then a *Generic Memory Structure (GMS)* made of two resistive RAM devices is presented and discussed for FPGA applications (Section 5.3). Another example of resistive RAM application is given in Section 5.4. Then in Section 5.5 applications for multi-terminal memristive SiNW devices are showcased. Finally,

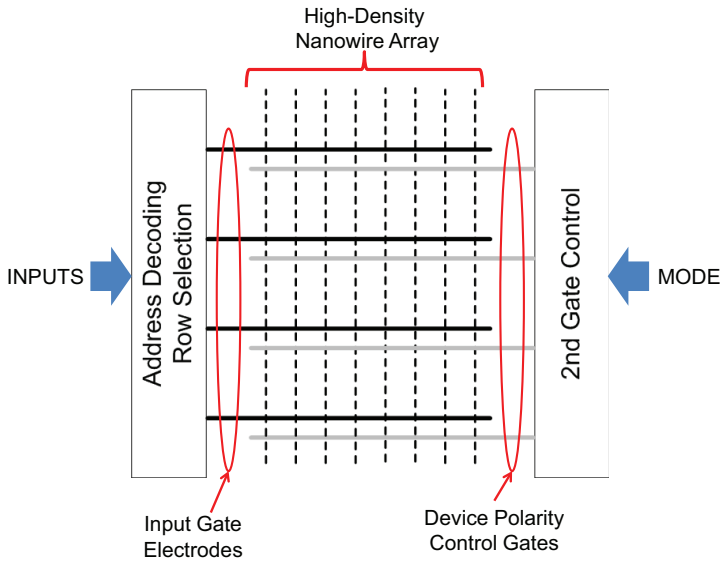


Figure 5.2: A crossbar architecture with polarity control and address decoding made with high-density 4-T memristive SiNW arrays.

in Section 5.6 the original contributions of this chapter are summarized.

5.2 Standalone Memories

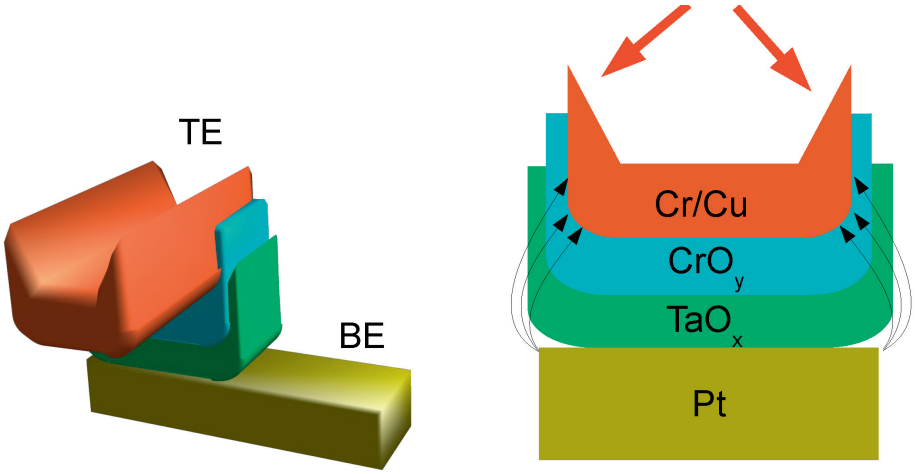
5.2.1 Introduction

Future deeply scaled circuits will see their performances limited by the physical limitations of the materials. To keep pushing the performance of computation and the density of storage, the microelectronics industry envisages using more efficient state variable than the electronic charge. In this sense, the memristor is an attractive candidate for both computation and memory, thanks to its programmable resistive state. When considering the Resistive RAM (ReRAM) memories, which can be classified as memristors, excellent scalability and programming time can be obtained if compared to traditional Flash, which make ReRAMs suitable candidates for standalone memory applications.

In this section, a ReRAM technology demonstrating a *Multi-Level (ML)* forming-free $Pt/TaO_x/CrO_y/Cr/Cu$ crossbars built with low thermal budget ≤200°C is discussed. The devices show excellent scalability down to $2.5x10^9 bit/cm^2$ with device half-pitch of 100nm with projections of practical storage density of up to $10^{12} bit/cm^2$ at the 10nm technology node [16].

5.2.2 Fabrication

The basic device concept is a ReRAM composed of 2 metal lines crossing orthogonally and a transition metal oxide stack in between (see Fig.5.19a). Moreover, the shape of the *Top Electrode (TE)* has been fabricated such that corners are smoothed (Fig.5.19b). This feature



(a) (b)

Figure 5.3: (a) 3D cross-point ReRAM concept with fence-like Top Electrode (TE) shape. (b) Lateral cross-section view of Pt/TaO_x/CrO_y/Cr/Cu cross-point ReRAM device. The fence-like TE enables better scalability of the cross-point device thanks to a reduction of the intense electric field distribution at the corners.

reduces the fringing field intensity at the wire ends, thus improving both reliability and scalability of the devices. Two different ReRAM (Pt/TaO_x/CrO_y/Cr/Cu and Al/TiO_2/Al with the Bottom Electrode/Transition Oxide/Top Electrode order) stacks have been built and compared in terms of performance. Both stacks have forming-free property and as such they do not require special forming steps to form the devices. This is a considerable advantage for actual implementation on chip. Several devices have been built in a passive crossbar array fashion as explained in the following text. Si bulk wafers are first isolated by depositing 100nm thick Al_2O_3 with *Atomic Layer Deposition (ALD)* (Fig. 5.20a). Then, PMMA bi-layers are patterned with e-beam lithography as lift-off masks for 10nm/80nm Pt *Bottom Electrodes (BE)* deposition (Fig.5.20b). In the next step, a second lift-off mask is defined and 15nm TaO_x oxide layer (Fig.5.4c) is deposited by sputtering from a Ta_2O_5 target with increasing RF power in Ar/O_2 atmosphere (Fig.5.4e). Finally, 50nm/100nm thick Cr/Cu bi-layers TE are deposited by e-beam evaporation (Fig.5.4d). For Al/TiO_2/Al devices, the Al electrodes are deposited with e-beam evaporation while 10nm thick TiO_2 is deposited by ALD. In Fig.5.5a and 5.5b SEM images of 100nm wide BE lines and 64bit passive crossbar are shown, respectively. In Fig.5.5c, a 3D reconstructed AFM profile is shown. About 250 individual Pt/TaO_x/CrO_y/Cr cross-points for area sizes varying from 100nm x 100nm to 1μm x 1μm, and 64bit crossbars with half-pitch varying from 100nm x 100nm to 500nm x 500nm are built on the same sample following the proposed fabrication steps. In Fig.5.6a and Fig.5.6b, a tilted SEM view, and a 3D reconstructed AFM profile of a cross-point device with fence-like TE are shown, respectively.

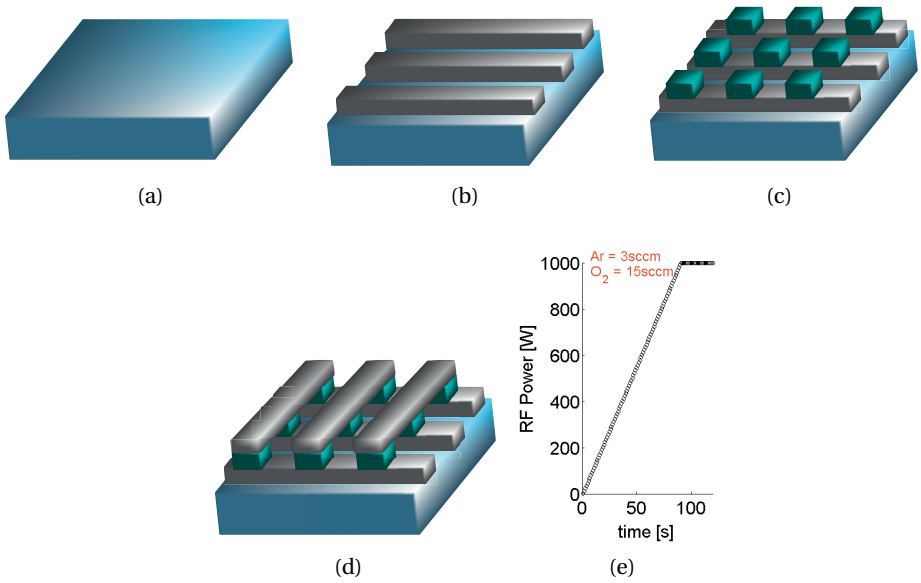


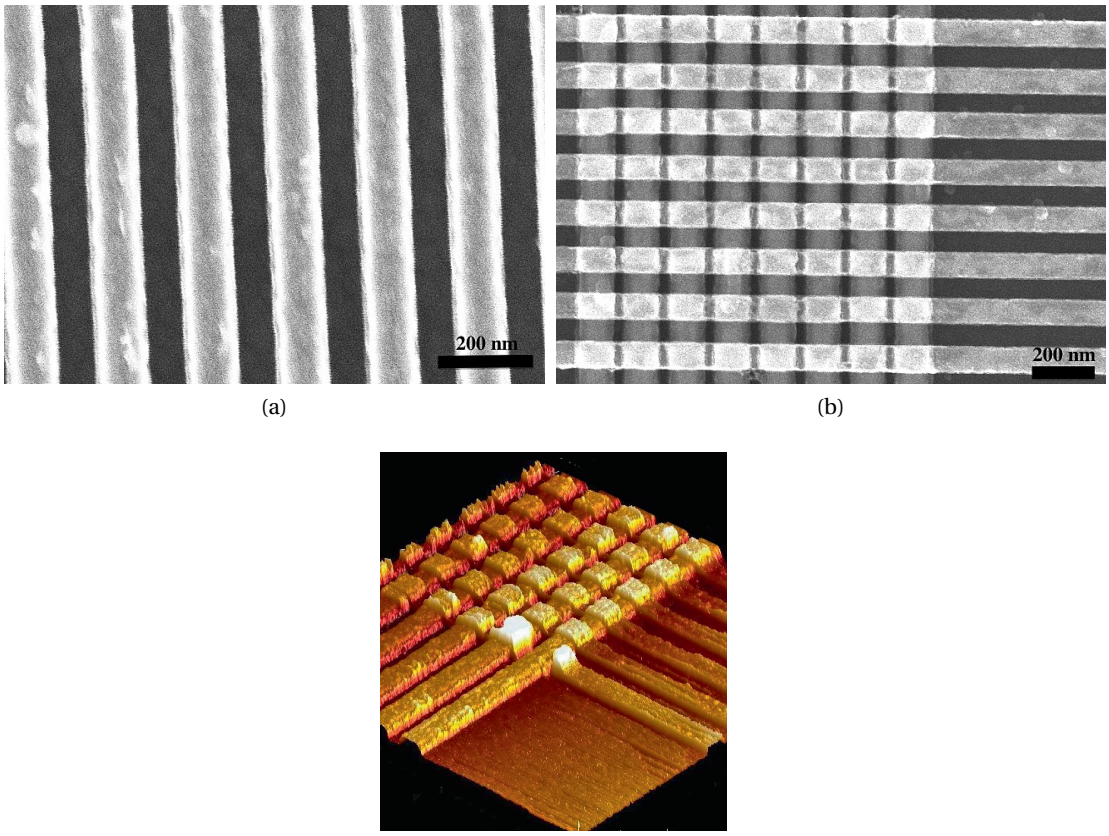
Figure 5.4: Process Flow. (a) Insulated Si substrate; (b) Pt bottom electrode lift-off; (c) TaO_x sputtering deposition; (d) TE lift-off (e) Sputtering parameters of TaO_x, with increasing RF power and constant 3sccm/15sccm Ar/O_2 flows.

5.2.3 Electrical Characterization

Electrical measurements are carried out with an Agilent B1500 semiconductor device analyzer. Pulse mode sweeps with pulses of 500μs demonstrate forming-free *Bipolar Resistive Switching (BRS)* for $Pt/TaO_x/CrO_y/Cr/Cu$ (Fig.5.21c). The BRS is obtained for a voltage range of less than 1V with pristine ON state in the same range of the *Low Resistance State (LRS)*. This is an important advantage compared with non forming-free ReRAM devices, because the forming operation requires higher voltages. A forming voltage of -3.4V has indeed been necessary for the $Al/TiO_2/Al$ (Fig.5.7b), that then show similar performance as the $Pt/TaO_x/CrO_y/Cr/Cu$ devices. In Table I structural and electrical parameters of the different cells are reported.

5.2.4 Discussion

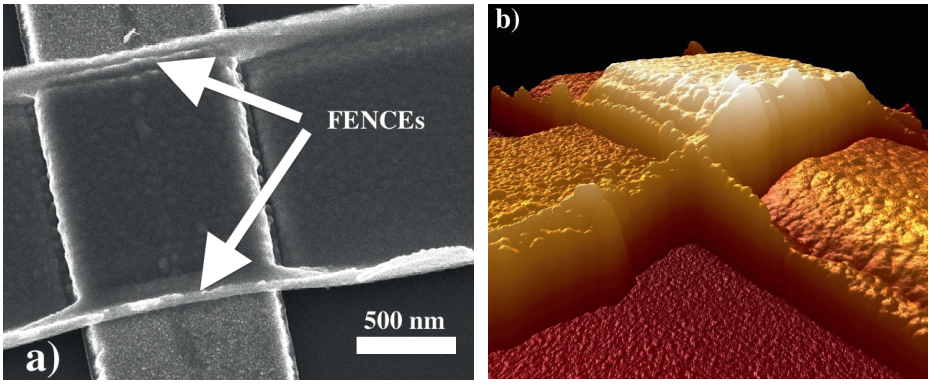
Material characterization has been carried out to understand the pristine ON state of the $Pt/TaO_x/CrO_y/Cr/Cu$ device. The X-ray diffraction pattern of Fig.5.8a shows peaks from the TE and the Si substrate. The absence of any Ta_2O_5 or TaO_2 peaks indicates that the material is in amorphous state, due to the low deposition temperature. The visible peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. The pristine ON state excludes the conductive filament mechanism and observing the double logarithmic plot of the *I-V* curve (Fig.5.9a), quasi-Ohmic regimes with slopes $\approx$1 are obtained for regions far from the SET condition. Typical trap-assisted *Space-Charge-Limited-Conduction (SCLC)* is observed close to the SET condition. The SCLC conduction is also observed for $Al/TiO_2/Al$ devices (Fig.5.9b) whose slopes indicate a more abrupt distribution of trap density, which can be



(a) (b)

(c)

Figure 5.5: Top SEM view of: (a) bottom electrode lines; (b) complete 64bit crossbar array of devices with 100nm half-pitch; (c) reconstructed 3D image from AFM profile.



(a) (b)

Figure 5.6: Pt/TaO_x/CrO_y/Cr/Cu cross-point device with 900nm x 900nm cross-point area. (a) Tilted SEM image view. Notice the fence-like structures at the edges of the TE line. (b) Reconstructed 3D AFM image of the pristine cross-point device. Average roughness on TE is $\sigma \approx$42.6nm.

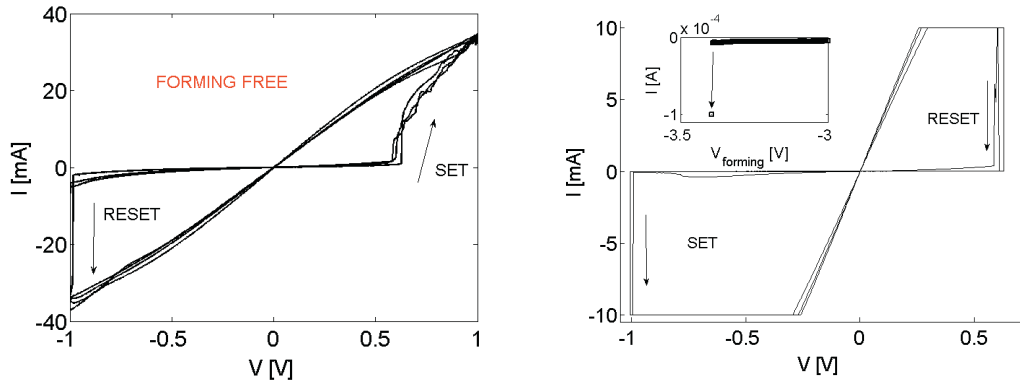
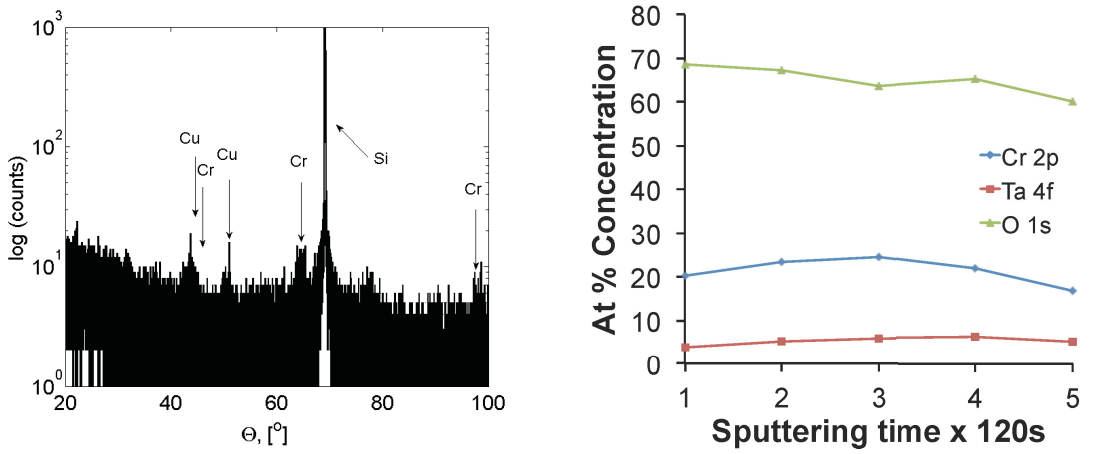


Figure 5.7: (a) Typical I-V characteristic of the Pt/TaO_x/CrO_y/Cr/Cu ReRAM cell showing resistance ratio of 10^4. Notice very low V_{SET} = +0.8V and VRESET=-1V. After fabrication the devices are forming-free and in the ON state. (b) Typical *I-V* characteristic of the Al/TiO_2/Al ReRAM cell after forming with $V_{SET} = -1V$ and $V_{RESET} = +0.8V$. Inset shows $V_{FORMING} = -3.4V$.

related to the different deposition methods. In both devices, the resistive switching mechanism can be attributed to Redox reaction linked with the motion of oxygen-vacancies [17, 18]. Moreover, structural modification is observed from the roughness profile of Pt/TaO_x/CrO_y/Cr/Cu cross-point after 100cycles. As shown in Fig.5.10a and Fig.5.10b, the Pt/TaO_x/CrO_y/Cr/Cu average roughness (Ra) measured above the TE broadens. The Ra changes from a pristine 100nm variation into a 200nm broad window, indicating structural modification by the motion of oxygen vacancies upon switching. In addition, XPS-depth analysis (Fig.5.8b) confirms that $Ta_2O_{5-\delta}$ and $TaO_{2-\gamma}$ phases are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE that is consistent with the Redox switching mechanism.

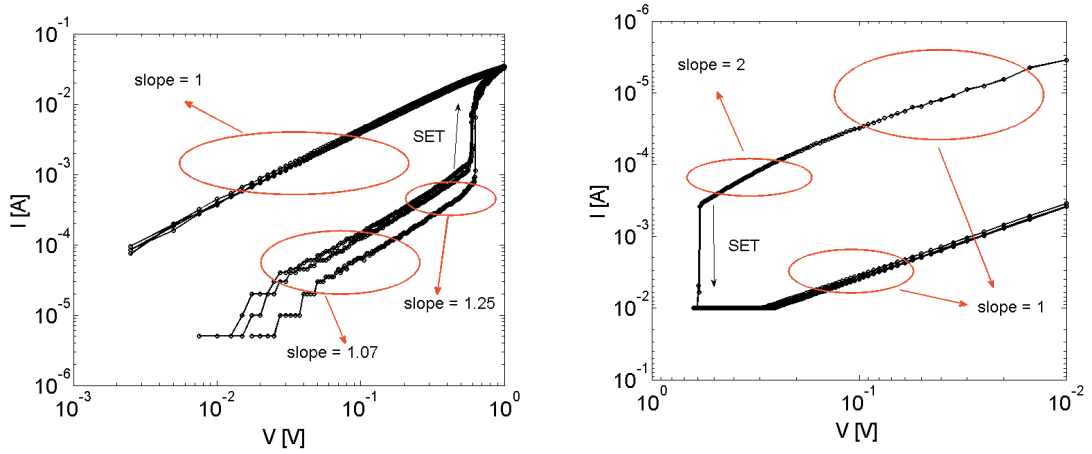
High Density Multi-Valued Crossbars

Several resistance levels of Pt/TaO_x/CrO_y/Cr/Cu devices can be programmed. As shown in Fig.5.11a, four levels of resistance (encoding 2bits) are found within a 4 orders of magnitude range. A larger resistance window of 1bit is found for Al/TiO_2/Al devices, which show a LRS around 30Ω and an HRS at 1M Ω within 2 orders of magnitude variation (see Fig.5.11b). The Al/TiO_2/Al show stable LRS and HRS in a large V_{READ} voltage range (Fig.5.12a). The Pt/TaO_x/CrO_y/Cr/Cu devices demonstrate excellent scalability, as the HRS/LRS ratio improves for smaller device sizes (Fig.5.12b). For instance, 2bit can be written in a Pt/TaO_x/CrO_y/Cr/Cu by using shorter SET pulses in order to program the cell in one of the stable *Intermediate Resistance (IR)* states. An example of 2bit storage using LRS, HRS and 2 IRs is demonstrated in Fig. 5.13, each level is separated of about one order of magnitude from each other for various V_{READ}. The devices could be easily assembled into dense 2.5x10^9bit/cm^2 passive crossbar arrays whose storage density improves to 10^{10}bit/cm^2 thanks to ML capability of Pt/TaO_x/CrO_y/Cr ReRAMs.



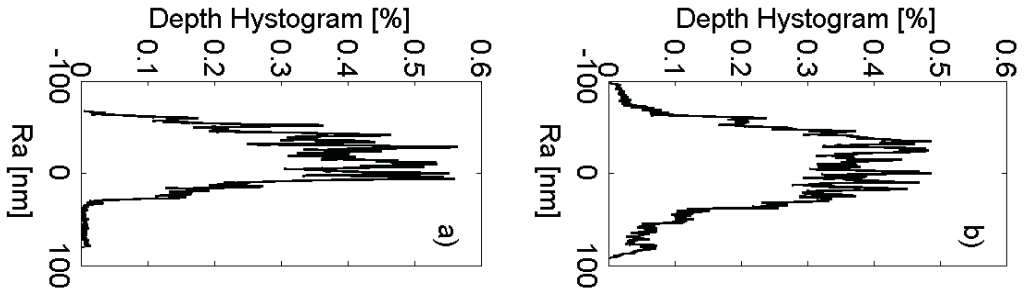
(a) (b)

Figure 5.8: (a) X-ray diffraction pattern on a Si wafer demonstrating amorphous TaO_x/CrO_y. The peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. (b) XPS depth profile analysis showing the presence of both Cr and Ta in oxidized states. Both $Ta_2O_{5-\delta}$ and$TaO_{2-\gamma}$ are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE.



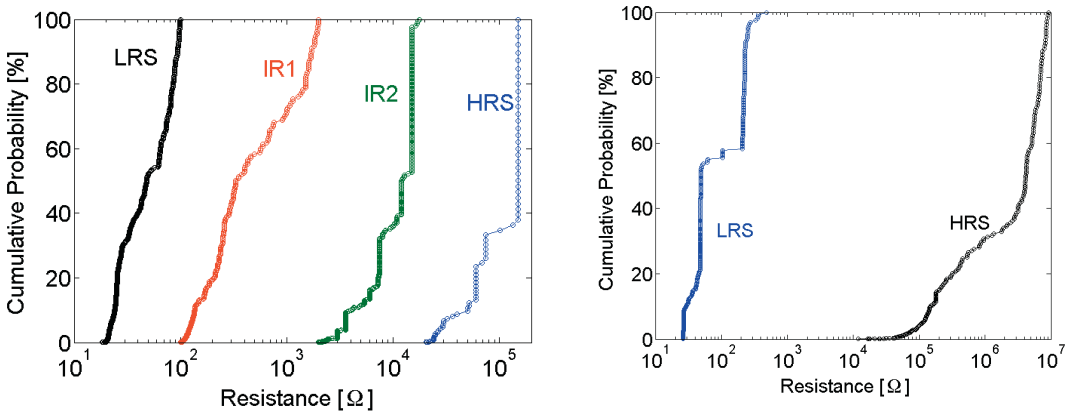
(a)

Figure 5.9: (a) The log(I)-log(V) plot of $Pt/TaO_x/CrO_y/Cr/Cu$ shows typical trap-controlled conduction of *Space-Charge-Limited-Conduction (SCLC)* before SET. In the SET region, the slope is about 25 and it is indication of gradual distribution of defects. (b) The log(I)-log(V) plot of the $Al/TiO_2/Al$ shows typical trap-controlled conduction of SCLC with quadratic V dependence before SET condition, thus following Child's law dependence. In the SET region, the slope is about 50, and it is indication of an abrupt distribution of defects.



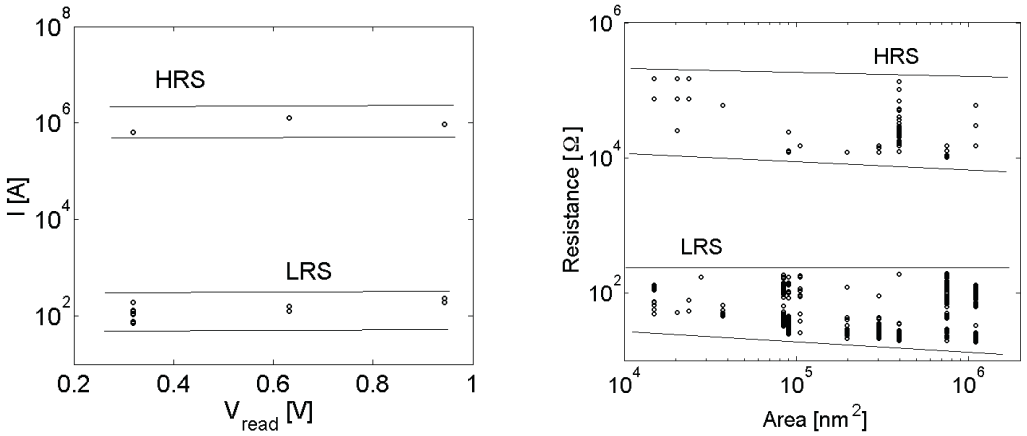
(a) (b)

Figure 5.10: Average roughness profiles for TaO_x cross-points: (a) $\sigma \approx 42.6$nm after fabrication; (b) $\sigma \approx 56.3$nm after 100 cycles. The broadening is attributed to the structural change induced by the motion of oxygen-vacancies upon cycling.



(a) (b)

Figure 5.11: (a) Cumulative probability of *Low Resistance State (LRS), Intermediate Resistance states 1 (IR1) and 2 (IR2)* and *High Resistance State (HRS)* for $Pt/TaO_x/CrO_y/Cr$ devices are shown. The LRS, IR1 and IR2 are obtained by using SET pulses of 2ms, 1ms and 500μs at 1V, respectively. The HRS is obtained with a 500μs RESET pulse at -1V. (b) Cumulative probability of LRS and HRS for $Al/TiO_2/Al$ devices are shown. The LRS and the HRS are obtained by using SET and RESET pulses of 500μs at -1V and +1V, respectively.



(a) (b)

Figure 5.12: (a) LRS and HRS resistance distributions for increasing V_{READ} of the Al/TiO_2/Al cell. The 10^4 resistance ratio is constant over a large range of reading voltage. (b) Measured HRS and LRS values for the Pt/TaO_x/CrO_y/Cr cell devices with different cross-point area demonstrating excellent scalability, indicating local switching at the nanoscale.

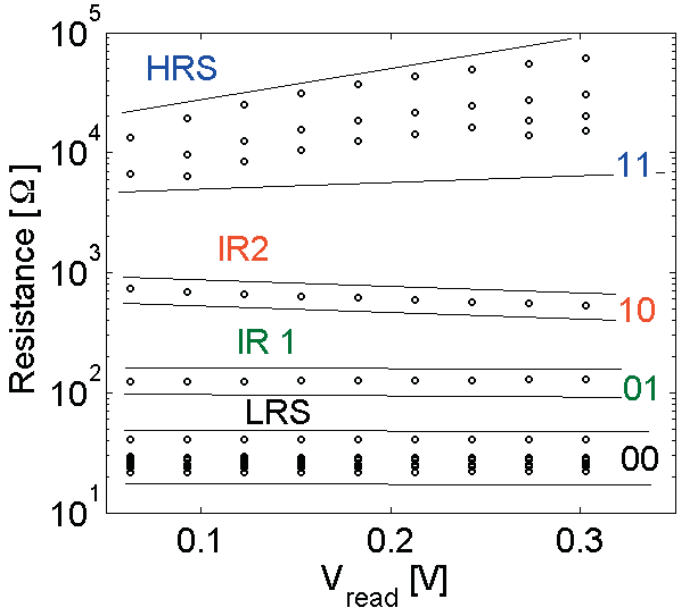


Figure 5.13: Resistance distributions for multi-value storages vs. increasing V_{READ} of the Pt/TaO_x/CrO_y/Cr cell. The HRS, IR2, IR1, LRS are encoded in 2bit.

5.2.5 Summary

Bipolar Resistive Switching Pt/TaO_x/CrO_y/Cr/Cu and Al/TiO_2/Al devices built with thermal budget ≤200°C have been fabricated and characterized. Very large storage density of TaO_x/CrO_y based ReRAMs is demonstrated up to 10^{10}bit/cm^2 thanks to the excellent scalability of the fence-like top electrode lines.

5.3 Generic Memory Structure (GMS) for non-volatile FPGAs

5.3.1 Introduction

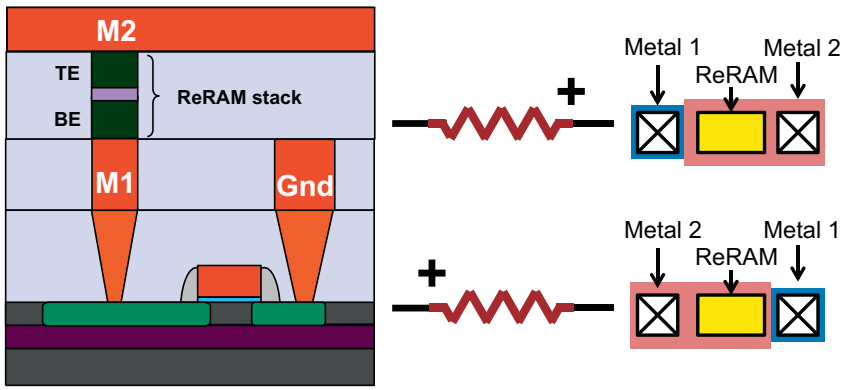
While a lot of research effort targets high density ReRAM-based standalone memories [19], the focus of this work is the usage of ReRAMs for FPGAs. The reason behind this choice is that in reconfigurable logic, up to 40% of the area is dedicated to the storage of configuration signals [20]. Traditionally, the configuration data is serially loaded in SRAM cells, distributed throughout the circuit [21]. As a consequence, power up of the circuit is limited by the slow serial configuration. To overpass SRAM volatility and loading time issue, Flash NVM have been proposed [22]. Nevertheless, the use of an hybrid CMOS-Flash technology results in high fabrication costs. Conversely, ReRAMs are fabricated within the Back-End-of-the-Line (BEoL) metal lines, moving the configuration memory to the top of the chip and reducing the area utilization [23]. Similarly, the ReRAM cells can be utilized in combination with TSVs, enabling 3-D stacked FPGA architectures [3]. In this paper, we propose a complete proof of concept of an ReRAM-based *Generic Memristive Structure (GMS)* circuit for FPGAs from technology development to architectural evaluation. The main idea is to replace the pass-transistors in SRAM-based FPGAs by ReRAMs. Hence, the ReRAMs store the information in their resistive states and can be either used to route signals through lowresistive paths, or to isolate them by means of high-resistive paths. Such a functionality is envisaged either to build routing Multiplexers (MUXs) or configuration nodes. In order to keep the programming complexity in the same range of SRAM-based FPGAs, we propose an efficient methodology based on the inherent GMS complementary programming. The proposed methodology, with GMS-based complementary programming has been validated by electrical measurements on a fabricated device.

5.3.2 BEoL integration of ReRAMs

As per the previous section, ReRAMs can be fabricated within the BEoL processing. Hence, it is possible to fabricate them between two metal layers (e.g. in between Metal 1 and Metal 2). Because of the BRS of the ReRAMs of this study, depending on the forming polarity, either the Metal 1 or the Metal 2 terminal can be utilized as the positive electrode of the memory, giving two possible configurations (see Fig.5.14a).

5.3.3 Device Description

In the GMS, two ReRAMs are interconnected as shown in Fig.5.15a. The positive terminal of the top memory is connected to the negative terminal of the bottom memory. This arrangement



(a) (b)

Figure 5.14: Cross sectional schematic showing the integration of a ReRAM integrated between the M1 and M2 interconnection levels in the back-end-of-line. (a) The bottom electrode is thus directly connected to a MOSFET selector (bottom) forming a 1-Transistor 1-Resistor (1T1R) memory node. (b) ReRAM polarity selection by physical design.

enables complementary programming of the two ReRAMs composing a GMS. We call the concurrent programming of the GMS a complementary programming operation. A similar programming scheme was previously used for low power crossbars [24]. Fig.5.15b illustrates the programming of the top path (i.e. left to right arrow in the programming graph shown in Fig. 5.15d). R_1 and R_2 are switched simultaneously to R_{OFF} and to R_{ON} respectively. This operation is achieved by grounding the common right terminal and biasing the left terminal to $-V$th (which corresponds to the SET voltage $-V$th for R_1 and to the RESET voltage $+V$th for R_2). The programming of the bottom path (see Fig.5.15c) is obtained by inverting the $-V$th and the GND (which corresponds to the RESET voltage for R_1 and to the SET voltage for R_2). In addition to speed up the programming operation, due to the complementary scheme, only two voltages are needed (GND and Vth).

The complementary programming operation has been validated by electrical measurements, while the MUX performances have been extracted by electrical simulations. Fig.5.16 depicts the resistance values of R_1 and R_2 of an GMS-based MUX21. Resistances are read at V_{READ}= +0.1V.

After a preliminary forming step, R_1 and R_2 are set to R_{ON}. The devices are then read for 10 cycles, showing a stable non-volatile resistance. Hence R_1 and R_2 are switched using the complementary programming operation presented in the previous section. During the first writing operation SET and RESET events are induced on R_2 and R_1, respectively (see Fig.5.15c) by applying a voltage pulse for 500μs. After reading the resistance values for another 10 cycles, again validating the non-volatility of the resistance states, a second complementary switching operation is performed. Now the resistance states of R_1 and R_2 are complementary switching, as seen in the reading sequence of Fig.5.16. As can be noticed the resistance values of R_1 and R_2 do not exactly match. This is due to the different ReRAM geometries and to the large variability of the cells utilized for the demonstrator. Nevertheless, improved variability of one order of magnitude has been demonstrated for ReRAM prototypes fabricated with industrial

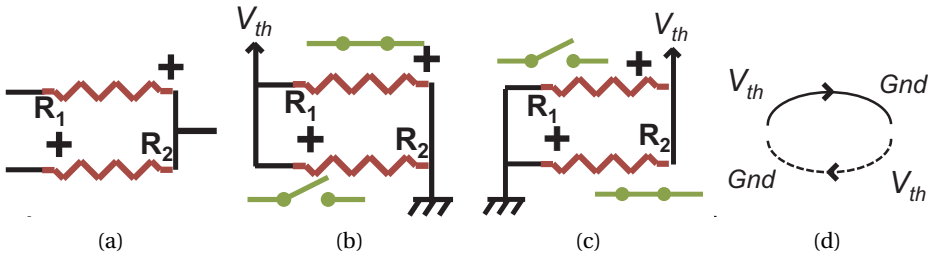


Figure 5.15: GMS complementary programming. (a) Two BRS resistive RAMs are in series connected after forming. (b) When V_{th} is applied, R_1 switches ON, while R_2 switches OFF. (c) When $-V_{\text{th}}$ is applied, R_1 switches OFF, while R_2 switches ON. (d) Graph representation of the complementary switching operation.

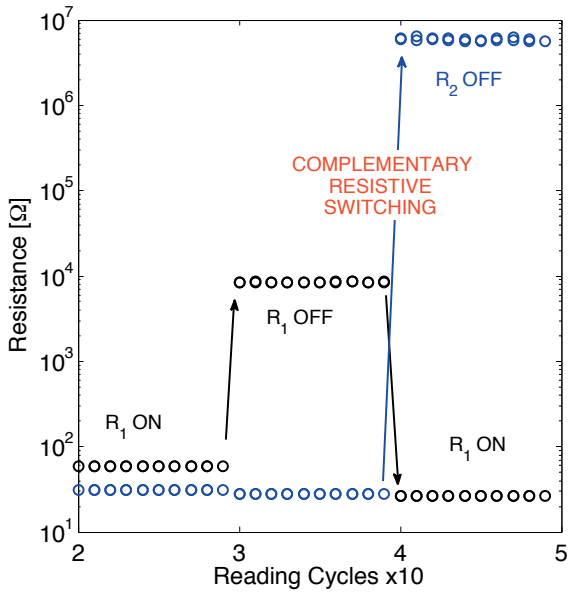


Figure 5.16: Complementary switching operation for the ReRAM-based GMS.

methods [25].

5.3.4 GMS memory node

In this section, we present an elementary circuit used to move most of the configuration part of reprogrammable circuits to the back-end, reducing their impact on front-end occupancy. Such a memory node is dedicated to drive LUT inputs. The memory node is based on a unique GMS node and provides intrinsically the retained information as a voltage level. Furthermore, it shall allow a layout efficient line sharing.

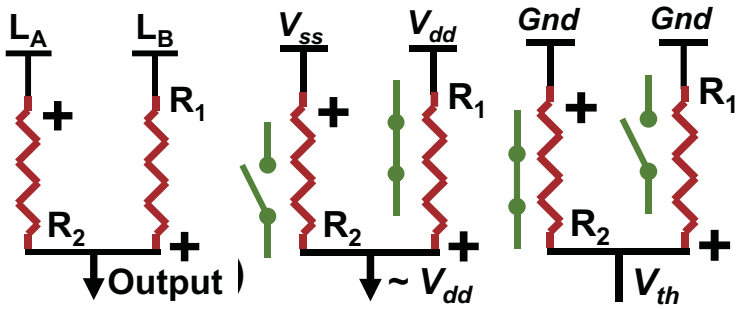


Figure 5.17: GMS complementary programming: (a) Two in-series connected BRS RAMs forming a voltage divider between 2 metal lines, LA, LB. (b) Voltage distribution to program a logic 1 into the GMS cell. (c) Voltage distribution to program a logic 0 into the GMS cell.

Overall Structure

The basic memory node is presented in Fig. 5.17c . The circuit consists of 2 ReRAMs connected in a voltage divider configuration between 2 fixed voltage lines (LA and LB). The memories are used in a complementary manner, in order to improve reliability. Reliability is required as far as the output is not restored by an inverter for compactness purpose. The output is designed to place a fixed voltage on a conventional standard cell input. Read operations are intrinsic with the structure, while programming is an external operation to perform on the cell.

Read operation

A voltage divider is used in this topology to intrinsically realize the conversion from a bit of data stored in the variable resistance to voltage level. Fig. 5.17b presents a configuration example where the node stores a '1'. Voltage lines LA and LB are respectively connected to VSS and VDD. For the sake of example, consider that the resistive memory R_1, connected to the VDD line, is configured to the low resistivity state. The other memory R_2, connected to VSS, is in the high resistivity state. As a consequence, a voltage divider is configured and the output node is charged close to the voltage of the branch with a high conductivity.

Write Operation

Fig. 5.17c presents the programming phase of the node. First, the lines LA and LB are disconnected from the power lines and connected to the programming signals. The programming signals are chosen according to the GMS programming scheme. Fig. 5.18 presents the programming circuits required to program an array of GMS-based configuration memories. To provide individual access, each GMS has its own selection transistor. Thus, the different lines can be shared in a standalone-memory-type architecture, yielding an efficient layout strategy. The different modes and programming signals are selected by line-driving multiplexers.

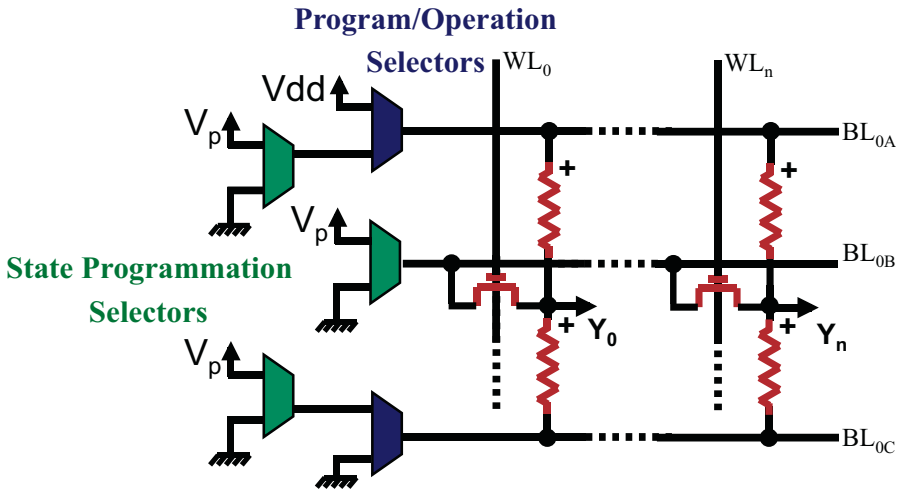


Figure 5.18: Complementary switching operation for the ReRAM-based GMS.

5.3.5 Summary

This paper introduced a novel design, called GMS, based on resistive memories, designed to replace traditional routing resources in reconfigurable logic circuits. Resistive RAM memories combined into a complementary switching GMS cells were used to reduce the footprint and to improve the electrical performances of the data path. The GMS cell can also be used to replace standalone memories, leading to more compact LUTs and steering logic, due to the BEoL integration of ReRAMs.

Thanks to ReRAMs, the area and the delay are reduced by 7% and 58% respectively due to the compactness and the low on-resistance of ReRAMs.

5.4 Resistive Programmable TSVs

In this section, BEoL technology for 3D interconnects is addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in *three-dimensional (3D)* wafer/chip stacking solutions utilizing *Through Silicon Vias (TSVs)* [26] as well as in reconfigurable interconnect fabrics. The discussed BEoL demonstrate the co-integration of TSVs with ReRAM stacks, offering a new path for re-programmable 3D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3D chip interconnects. the fabrication and characterization of titanium dioxide (TiO_2)-based *resistive RAM (ReRAM)* co-integration with 380 μm-height Cu *Through Silicon Via (TSV)* arrays for programmable 3D interconnects is discussed. Non-volatile resistive switching of Pt/TiO_2/Pt thin films are first characterized with resistance ratio up to 5 orders of magnitude. Then co-integration of Pt/TiO_2/Pt or Pt/TiO_2 memory cells on 140 μm and 60 μm diameter Cu TSV are fabricated. Repeatable non-volatile bipolar switching of the ReRAM cells are demonstrated for different structures.

5.4.1 Fabrication

Planar ReRAM devices

First, high resistivity p-type ($N_A \approx 10^{15}$atoms/cm^2) bulk-Si wafers are prepared by 500nm thermal oxidation in H_2O atmosphere. Then the deposition of the resistive switching materials is performed by sputtering of Pt/TiO_2/Pt layers with 270nm/80nm/270nm thicknesses. A conceptual picture is shown in Fig. 5.19a. The top electrode area of 100μm by 100μm squares were patterned by standard lithography and etched by ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

TSV devices

The resistive switching materials were integrated with TSVs producing two different devices:

- 140μm TSV diameter in 380μm thick wafer, using Pt/TiO_2/Pt memory stack
- 60μm TSV diameter in 380μm thick wafer, using Cu/TiO_2/Pt memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

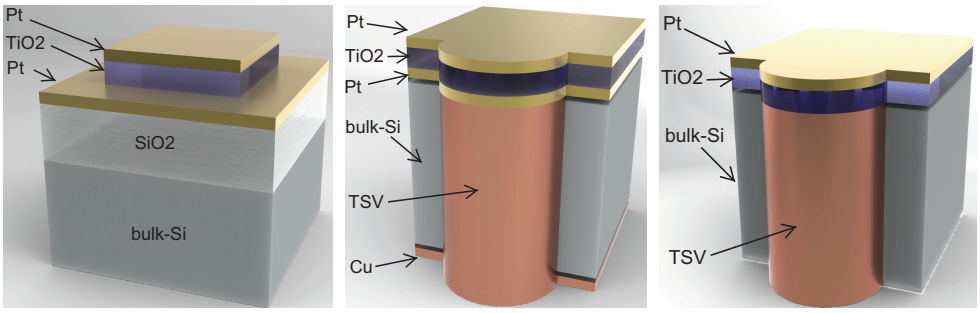
The TSVs are fabricated using the same process in both cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through wafer etch, RCA wafer cleaning and thermal oxidation in water atmosphere to grow a 3μm thick oxide. A 750 nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

TSV with Pt/TiO_2/Pt ReRAM

For the first type of devices, once the TSVs are fabricated the front side of the wafer is processed with *Chemical Mechanical Polishing (CMP)* technique to form a flat surface. The Pt/TiO_2/Pt stack is sputtered with layer thicknesses 270nm/80nm/270nm accordingly. A concept picture of the fabricated structure can be seen in Fig. 5.19b.

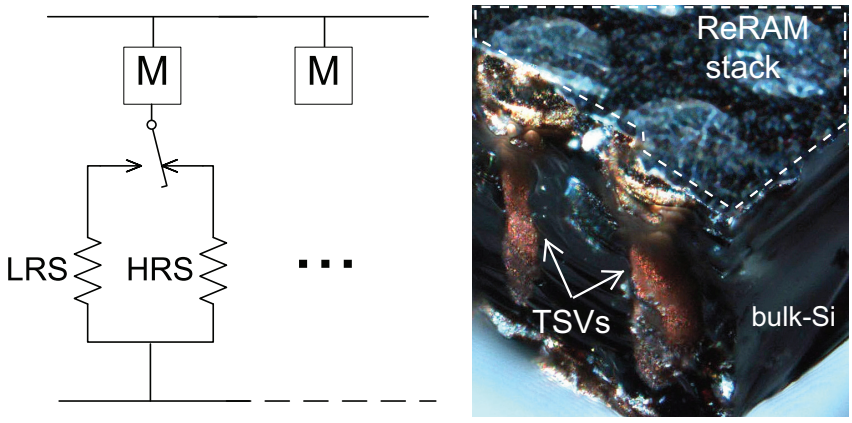
TSV with Cu/TiO_2/Pt ReRAM

For the second type of devices the wafer is polished using CMP on both sides to remove the seed layer and to planarize the surfaces. The Cu was then cleaned using a $NH_4 : H_2SO_4$ etching solution at room temperature for 10 minutes. Then the wafer was loaded into a vacuumed sputtering chamber and a TiO_2/Pt layer was deposited with thicknesses of 80nm and 270nm respectively. The Cu of the TSV is acting as the bottom electrode of the ReRAM (see Fig. 5.19c). Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Fig. 5.20a and 5.20b, respectively.



(a) (b) (c)

Figure 5.19: (a) Concept image of planar ReRAM made of $Pt/TiO_2/Pt$ stack. (b) Concept image of the ReRAM-TSV using $Pt/TiO_2/Pt$ programmable fuse. (c) Concept image of the ReRAM-TSV using $Cu/TiO_2/Pt$ programmable fuse.



(a) (b)

Figure 5.20: (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element M). (b) Reconstructed 3D photograph of the TSV – $Cu/TiO_2/Pt$ device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

5.4.2 Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station in dark conditions. For electrical contacts, standard tungsten needles with 15μm apex diameter were placed on the top electrode area very softly, since a dependence of the switching with needle pressure has been observed, similarly to the observation of local pressure modulated conductance with AFM tips [27]. Then double $I-V$ DC sweeps have been used to investigate the resistive switching behavior. In all the cases, bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table 5.1.

5.4.3 Planar ReRAM devices

First the planar Pt/TiO_2/Pt are characterized and it showed stable and repeatable bipolar switching behavior between 10 Ω and 1MΩ read or measured at +1V (see Fig. 5.26a). Originally the devices are in the high resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low resistance state (LRS) occurs at +1.8V. After the SET event, the voltage sweep continues until +2V and then move backward toward negative voltage region. When −1.3V is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about 5 orders of magnitude is read at +0.5V.

5.4.4 TSV − Pt/TiO_2/Pt devices

Next, TSV − Pt/TiO_2/Pt with the same layer thicknesses are measured, showing resistance switching below ± 1V (see Fig. 5.26b). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks as well as to surface states acting as dopants for the TiO_2 [28]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only +0.6V, while the RESET voltage is measured at −0.5V. Using a reading voltage of +0.2V, an HRS of 2MΩ and a LRS of 665Ω, with resistance ratio of 3000 are measured.

5.4.5 TSV − Cu/TiO_2/Pt devices

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the TiO_2 layer [29, 30], that is a n-type semiconductor, an alternative device is obtained by depositing TiO_2 and Pt directly on top of the Cu − TSV. Thus, thanks to a larger Schottky barrier height at the Cu − TiO_2 interface, a larger programming window is obtained (Fig. 5.21c). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. A HRS of 500MΩ and LRS of 5kΩ are read at +1V.

Device	SET	RESET	HRS	LRS	HRS/LRS	Reading
Planar $Pt/TiO_2/Pt$	+1.8V	−1.3V	10MΩ	10Ω	10^5	+1V
$TSV-Pt/TiO_2/Pt$	+0.6 V	−0.5V	2MΩ	665Ω	3003	+0.2V
$TSV-Cu/TiO_2/Pt$	−4.2V	+5V	500MΩ	5Ω	10^5	+1V

Table 5.1: Obtained ReRAM electrical parameters for the different devices

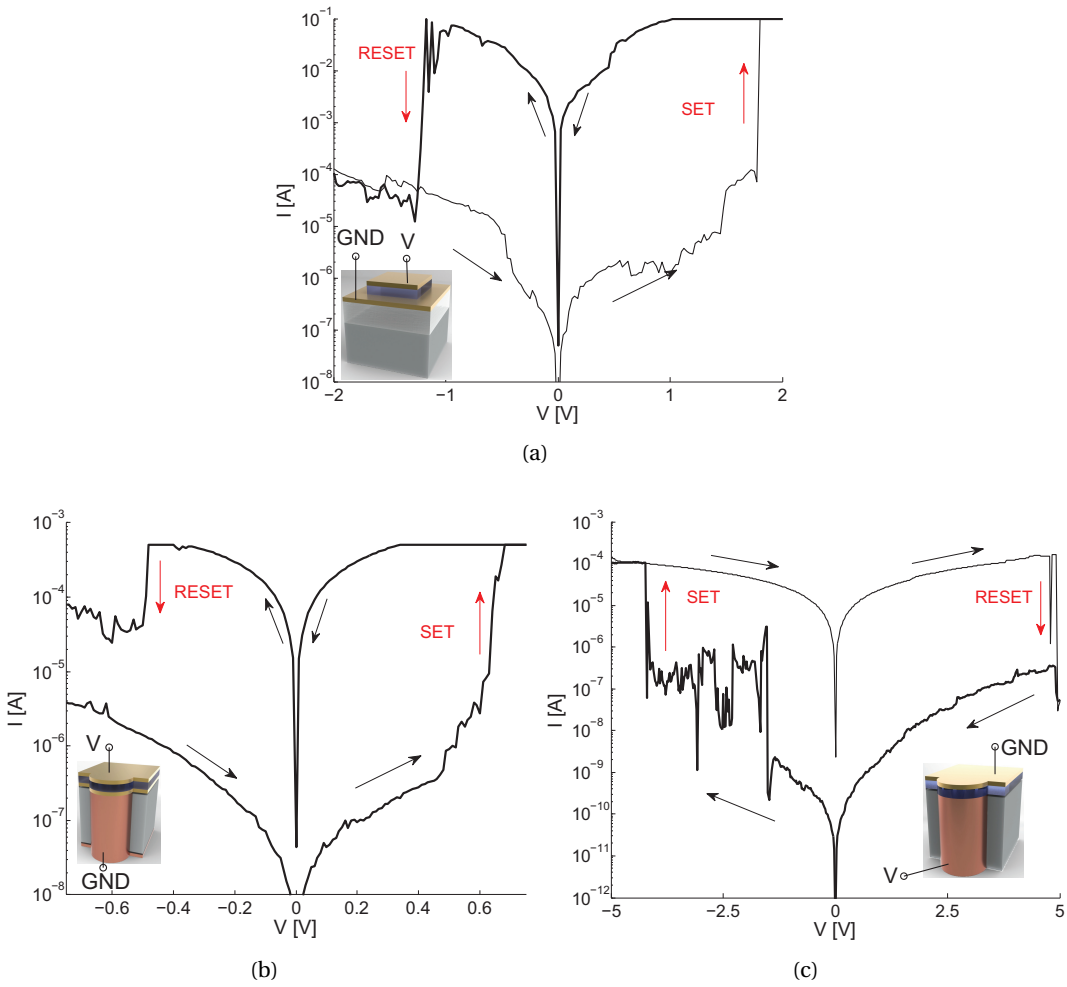


Figure 5.21: (a) Resistive switching through $I-V$ sweeps for planar $Pt/TiO_2/Pt$. (b) Resistive switching through $I-V$ sweeps using $TSV-Pt/TiO_2/Pt$ programmable fuse. (c) Resistive switching through $I-V$ sweeps using $TSV-Cu/TiO_2/Pt$ programmable fuse.

5.4.6 Summary

In this study, Pt/TiO_2/Pt obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with LRS to HRS resistance ratio up to 5 orders of magnitude. The device is successfully integrated on top of 140μm and 60μm TSV arrays either in the full Pt/TiO_2/Pt stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The co-integration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3D chip interconnects.

5.5 Sensing

5.5.1 Temperature sensing with Ambipolar Si nanowire transistors

This section reports on the fabrication and characterization of a pA current and temperature sensing device with ultra-low power consumption based on a Schottky barrier silicon nanowire transistor. Thermionic and trap-assisted tunneling current conduction mechanisms are identified and discussed on the base of the device sensitivity upon current and temperature biasing. In particular, very low current sensing properties are confirmed also with previously reported polysilicon-channel nanowire Schottky barrier transistors. demonstrating that these devices are suitable for temperature and current sensing applications. Moreover, the process flow compatibility for both sensing and logic applications makes these devices suitable for heterogeneous integration. In this work we extend the application of Si nanowires to temperature sensing. A range of device operation conditions are investigated, showing how an ambipolar device can be used for different applications, the only requirement being the biasing condition.

Device Description

The device scheme consists of a suspended Si nanowire having NiSi silicide source/drain junctions with 2 parallel polysilicon gates having gate-all-around (GAA) configuration on a SOI substrate. Typical Si nanowire with drop-like cross-section shape has an average diameter of 100nm.

Device Fabrication

The process flow is based on a previously reported technique utilized for the fabrication of vertically-stacked Si nanowire FET arrays [31]. Here a deep reactive ion etching technique is adapted to form a single suspended Si ribbon over the buried oxide. A sacrificial oxidation is performed to reduce the cross-section down to a 100nm. Then a 20nm dry oxidation is performed followed by a 500nm polysilicon layer deposited by low pressure chemical vapor deposition. Contact regions are etched in a low temperature oxide passivation layer. Then a 50nm Ni + 10nm Al bi-layer is evaporated and annealed to form a silicide/Si mid-gap Schottky junction. The Al is used as a cap layer to prevent Ni oxidation during the silicidation step and to provide a good interface with final metallization. Finally, 1μm thick Al is patterned for

electrical characterizations.

I-V dependence

For Schottky barrier FETs, Ids can be described by the sum of a tunneling I_{tunnel} and a thermionic-emission I_{th} component [32]:

$$I_{\text{ds}} = I_{\text{th}} + I_{\text{tunnel}} \tag{5.1}$$

$$I_{\text{th}} = A_C A^* T^2 e^{\left(-\frac{\phi_{\text{Beff}}}{kT}\right)} \left\{ e^{\left(-\frac{\phi_{V\text{a}}}{kT}\right)} - 1 \right\} \tag{5.2}$$

$$I_{\text{tunnel}} = A_C \frac{q^2 F^2}{8\pi h \phi_{\text{Beff}}} e^{\left(-\frac{8\pi}{3hqF}\sqrt{2m(q\phi_{\text{Beff}})^3}\right)} \tag{5.3}$$

Where A_C is the contact area of the source to channel junction, F the electric field across the Schottky barrier, A^* the Richardson's constant, h the Plank's constant, m the electron rest mass, q the elementary electron charge, ϕ_{Beff} the effective Schottky barrier height, T the temperature, V_{a} the applied voltage across the Schottky junction, k the Boltzmann's constant.

Temperature dependence

The $I_{\text{ds}} - V_{\text{gs}}$ dependence with T is mainly attributed to the I_{th}, however T also influences the I_{tunnel} since hotter carriers pass through a narrower Schottky barrier, leading to an increasing current level [32]. The I_{OFF} current is increasing exponentially with temperature and, as suggested by Eq. 5.2, its main contribution is a thermionic emission component. A different behavior has been observed for the I_{ON} current. Increasing the temperature makes the I_{ON} current to decrease until the temperature reaches 55°C and then it rise exponentially with linear increase of T. At lower temperatures tunneling and trap-assisted tunneling are more important than thermionic emission. Rising T up to 70°C makes the charges trapped into the gate oxide to un-trap, reducing the I_{tunnel} component. A different behavior is observed for the I_{ON} currents for 70°C≤T≤115°C. In this range, the I_{ON} exponentially increases with T. This effect is evidence of two main current components, for which the I_{ON} changes from a tunneling to a thermionic emission dominated regime. A set of $I_{\text{ds}} - V_{\text{ds}}$ curves (Fig. 5.22a) taken at different temperatures at constant V_{ds} = 100mV and V_{bg} = 5V are used to extrapolate the Arrhenius plot shown in Fig. 5.23a. The constant V_{bg} = 5V is used to set the device operation more favorable for electron conductance at low V_{gs}. Constant subthreshold swings ≈ 110mV/dec are observed independently from the temperature (see Fig. 5.22b). Low negative V_{gs} voltages ranging from −1V to 0V show an almost linear slope with inverse of temperature and can be correlated to a thermionic-emission regime. However, for this V_{gs} range the current level is on the order of fAs, which is comparable to the background noise, and it cannot be used to extrapolate the Schottky barrier height. Another distinct regime is observed for $-0.3\text{V} \leq V_{\text{gs}} \leq -0.5\text{V}$, for which the slopes are greatly affected by tunneling. This regime shows a dominant tunneling component for the two lowest temperatures. Finally, an exponential

dependence with T is observed again for $V_{gs}\geq$0V with the exception of the lower temperature. All these regimes demonstrate that the current in our device is mainly thermionic for $T\geq$ 70°C and that the tunneling contribution is trap assisted. The slopes from the Arrhenius plot are then used to extract the effective Schottky barrier height ϕ_{Beff} with the activation energy E_a method. As shown in inset A of Fig. 5.23b, an average effective barrier height $E_a\approx 450\pm 5$meV is found over a large range of $V_{gs\geq 0.2V}$. However, these values cannot be taken as Schottky barrier height since in this regime the device has both tunneling and thermionic components. As suggested by Svensson et al. [33], a better evaluation of the Schottky barrier height can be taken at the maximum of E_a for low current levels. As shown in the inset B of Fig. 5.23b, this maximum corresponds to $V_{gs}=-0.45$V and gives a $\phi_{Beff}=$ 525meV, confirming the mid-gap Schottky barrier height.

Current sensing

Current biasing the devices with a constant Ids current makes the device to behave as a pseudo-inverter configuration with hysteretic transfer function. Thanks to the ambipolarity, the $V_{out}-V_{in}$ curves shift linearly with the applied current bias. For instance in Fig. 5.24a, low pA current levels can be either read from the high-to-low or the low-to-high transition voltage with sensitivities of 17mV/pA. A similar biasing scheme for polysilicon nanowires has been previously characterized by the authors show a similar trend. In Fig. 5.24b, forward and reverse threshold voltages for currents between 100fA and 500fA show a linear increase with current.

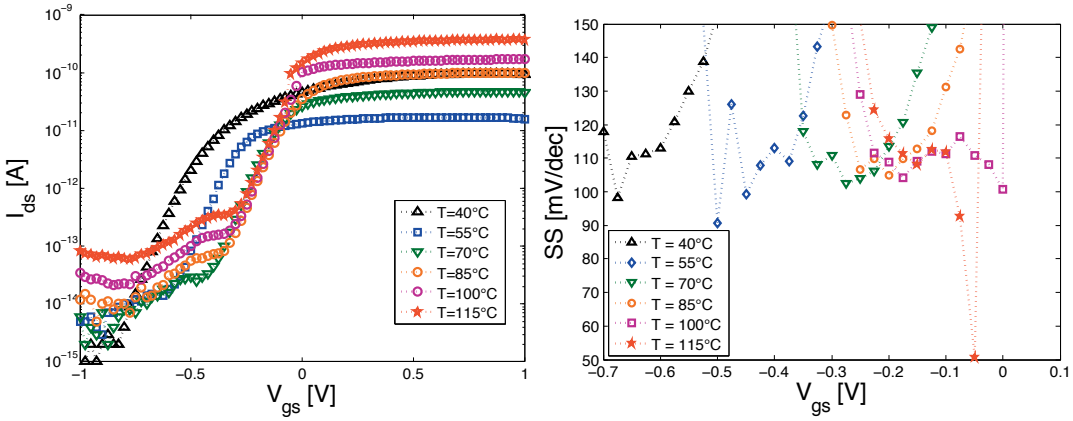
Temperature sensing

Upon application of increasing temperature of operation, the hysteresis window observed in pseudo-inverter biasing scheme shrinks. The crystalline Si nanowire Schottky barrier FET shows different sensitivities at different temperature regimes, depending on which mechanism dominates the conductance. Since the hysteresis is attributed to the storage of charges in either gate oxide and/or at the Schottky barrier junctions [34], an increased hysteresis window is expected for the lowest temperatures. The highest sensitivity of 40mV/°C is found in the T range around 40°C at which the trap tunneling mechanisms dominates. For temperatures higher than 55°C the sensitivity tends to saturate according to the dominance of thermionic current contribution, leading to lower sensitivity of 10mV/°C. In Fig. 5.24c the hysteresis window shrink for increasing T when 70°C≤T≤100°C is shown.

5.5.2 Bio-sensing with memristive ambipolar Si nanowires

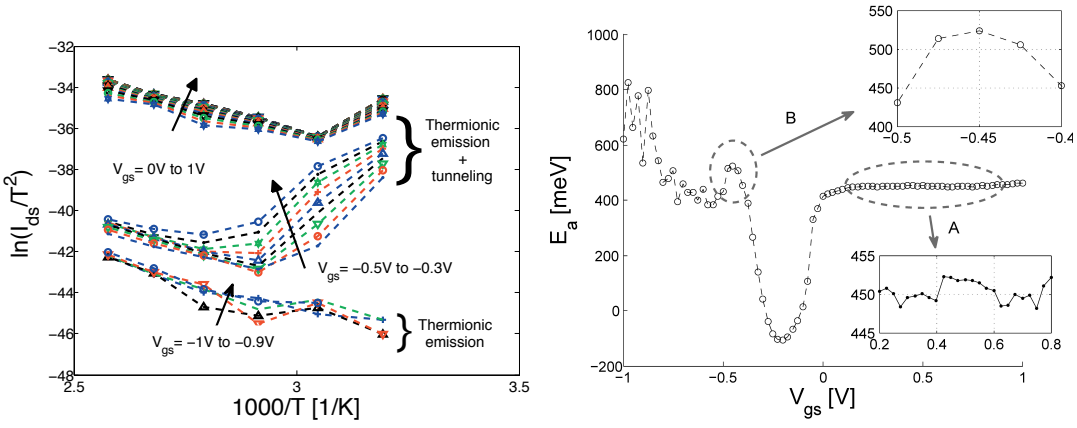
Introduction

Recently, there has been an increasing interest in nano-bio-sensing applications, due to possibility for minimal invasive, real-time monitoring for preventive treatments and therapy personalization [36]. In particular, one-dimensional silicon nanowires are good candidates for sensing devices due to their very large surface-to-volume ratio and quantum properties [37]. However, the sensing with nanowires is only exploited by the ion-sensitive field-



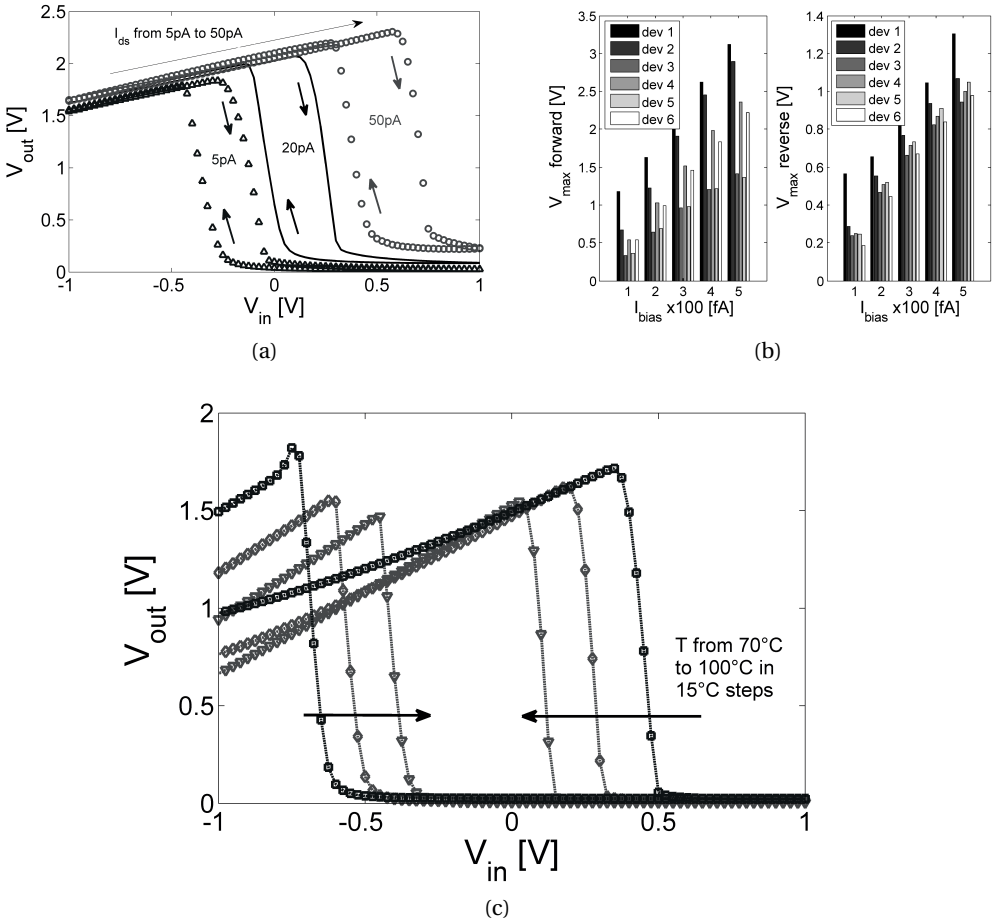
(a) (b)

Figure 5.22: (a) Effect of the temperature on the ambipolar I_{ds}–V_{gs} at V_{ds} = 100mV. (b) Subthreshold swings associated with the I_{ds}–V_{gs} plots. Very low swing minima are measured at 100°C and 115°C close to threshold voltages. Notice the voltage shift with temperature increase and the extremely low minima of 50mV/dec for the highest temperature.



(a) (b)

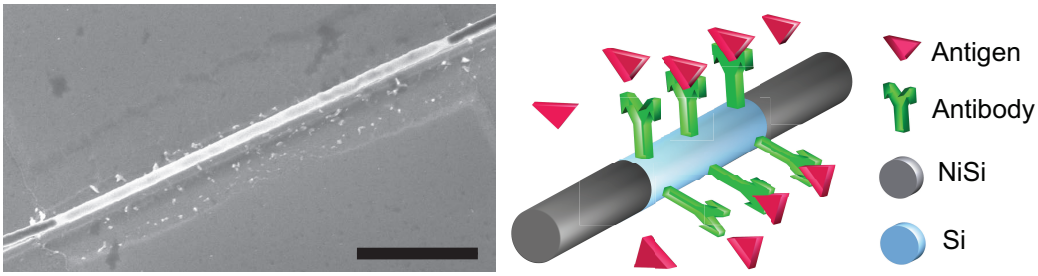
Figure 5.23: (a) Arrhenius plot for different V_{gs} extracted from the plots of Fig. 5.22b showing both thermionic emission and tunneling mechanisms. The linear decreasing slopes are associated with thermionic emission regimes. (b) Extracted E_a over a large range of V_{gs} . The inset A shows a constant $E_a = 450 \pm 5$meV over $-0.2\text{V} \leq V_{gs} \leq -0.8\text{V}$. Inset B shows the maximum of E_a = 525meV which is associated to the ϕ_{Beff}.



(a) (b)

(c)

Figure 5.24: (a) Measured input-output transfer characteristics of a hysteretic inverter based on a single Si nanowire FET with low current bias, showing current-dependent thresholds. (b) Forward and reverse threshold voltages for polysilicon Schottky barrier FETs under constant current biasing from 100fA up to 500fA (adapted from ref. [35]). (c) The hysteresis window shrinks with increasing temperature. Within this T range, the temperature sensitivity of 10mV/°C is related with the thermionic current regime.



(a) (b)

Figure 5.25: (a) Suspended functionalized silicon nanowire with NiSi extremities. Scale bar is 4 μm. (b) Concept model.

effect-transistor paradigm [38]. Due to the nano-scale of the fabricated geometries [39], the recent discovery in solid-state devices of the memristive effect has been source of renewed research efforts in applications for high-density memory device [1]. The physical phenomena governing the memristive behavior are attributed to the change of an internal state variable, which modifies the conductance in a non-volatile manner [7]. As reported by Duan et al., memory devices are possible also with molecule-gated nanowire transistors by using redox active molecules [9]. In here, we report on the first evidence of unexpected new insights for a novel molecular sensing in dry conditions based on nanofabricated memristors functionalized with bio-molecular thin films.

Device Nano-Fabrication

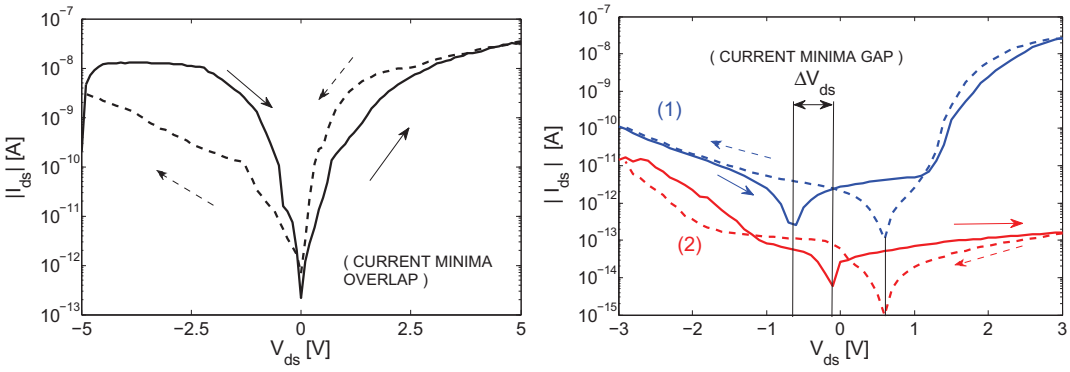
The fabrication method utilizes some of the steps that were previously reported [34] for memristive Schottky-barrier silicon nanowire field-effect-transistors. The process starts from low resistivity Silicon-On-Insulator substrates, with 1.5 μm device layer and 3 μm SiO_2 insulating layer. After standard lithography, the silicon nanowire is carved anchored at the top of two silicon pillars. Then, Ni is deposited on top of the pillars with overlap on the outer portions of the silicon nanowire. Hence, an annealing step at 450°C in a horizontal wall furnace forms NiSi contacts. Fig. 5.25a shows a nano-fabricated memristive silicon nanowire with NiSi contacts.

Biomolecule self-assembly

The silicon nanowire surface was derivatised with 3-glycidoxypropyltrimethoxysilane GPTS [40] and functionalized by covalent attachment of anti-rabbit polyclonal antibodies (AB) [41]. Antigen (rabbit antibodies, AG) interact with the functionalized wire as depicted in Fig. 5.25b.

Results and Discussion

Electrical measurements are carried out in a shielded probe station connected with HP4615C Semiconductor Parameter Analyzer and in dark, to avoid any photo-generated currents. Before functionalization with the AB layer, $I_{ds} - V_{ds}$ curves taken for forward and backward sweep do



(a) (b)

Figure 5.26: $I_{ds} - V_{ds}$ curves: (a) before functionalization with AB bio-layer. A typical memristive hysteresis is observed, with no ΔV_{ds} gap between I_{ds} minima in forward and backward regimes; (b) the blue curve (1) is measured after drying the sample from de-ionized water. The red curve (2) is measured after dipping in 5 pM AG solution and drying.

show a typical memristive behavior (see Fig. 5.26a), where the current minima always occur for $V_{ds=\ 0\ V}$; consistently with previously reported measurements [34] on non-functionalized devices. Conversely, functionalized silicon nanowires show different positions of the current minima for backward or forward regimes. This effect is observed after drying from: (a) de-ionized H_2O solution and (b) 5 pM AG solution. The $I_{ds} - V_{ds}$ curve before AG up-take shows an hysteresis (curve (1) in Fig. 5.26b) due to charge trapping mechanisms at the Schottky junctions. The binding of an AG with the functionalized wire is responsible for a modification of the hysteresis (curve (2) in Fig. 5.26b), in particular to a reduction of the current minimum gap between forward and backward V_{ds} sweeps. Coherently, the up-take of increasing amounts of AG (in the pM range) results on a further diminishing of this gap.

5.6 Chapter Summary and Conclusions

In this chapter several applications of two-terminals and multi-terminal memristive devices are discussed. Specifically, fabrication of resistive RAM memories have been presented for their potential for standalone memories. The resistive RAM can also be exploited for increased FPGA functionality, such as lookup tables, datapath routing. In here we propose the use of a generic memory structure to replace the pass-transistor in SRAM-based FPGAs. Another application envisages the use of ReRAM on top of Through Silicon Via for fully-3D programmable interconnects. A low thermal budget fabrication scheme of resistive programmable TSV has been developed and discussed. In the last section of the chapter, three-terminal memristive SiNW devices are exploited for sensing physical and biological quantities. Moreover, an innovative device exploting the hysteresis of functionalized Si nanowires is a first-time approach for bio-sensing in a controlled dry environment.

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6 Conclusions and Outlook

In this thesis several devices were developed and discussed. The main goals focused on enabling new functionalities for logic, memory and sensing applications. Such goals have been achieved by exploiting two phenomena that are typically disregarded in conventional nanoscale devices: ambipolar conductance and memory effects. Starting from the evidence that both phenomena are likely to increase as the scaling progresses, this these focused instead on making use of these rather than suppressing them. By relaxing these constraints on nanoscaled devices, additional functionality can be brought about several applications which are developed through the chapters.

In Chapter 1, fabrication methodologies for ambipolar Si nanowire devices are discussed. The methods enable the *top-down fabrication of vertically-stacked Si nanowires* of sub-lithographic dimensions, with sub-10nm nanowire sizes reachable out of a single sequence of optimized DRIE dry etching, without the need of additional oxidation steps. Such achievements are interesting for several applications, for instance advanced logic design, nanowire resonating structures, ultra-dense FLASH, new PLA architectures. Indeed logic design of *Carry Lookahead Adders* with vertically-stacked CMOS Si nanowire technology demonstrate additional benefits due to higher density and performance than planar CMOS gates.

The ambipolar conductance of the Schottky-barrier SiNW FETs has been exploited in several logic applications as a feature to perform more powerful computation. *Ternary logic gates* have been built from Schottky barrier Si nanowire FETs, by exploiting the ambipolar conductance. At the same time, ambipoalr Si nanowire FETs can also be utilized to obtain compact *threshold logic gates*, by means of a current-biasing scheme. The threshold can be precisely controlled by the amount of current and, combined with standard boolean logic circuits, enables multi-valued logic functions. Nevertheless, there are difficulties related to the compatibility between the input and output voltages and the usefuleness of such approach yet has to be demonstrated. Moreover, *ambipolar Double Independent SB SiNW FET* can be utilized as polarity-control device to build several Boolean logic functions with a single device. In addition, an optimized implementation demonstrated its potential for large logic circuits exploiting the ambipolarity as a computational state variable [1]. In this respect, *Sea-of-Tiles* architectures have been envisaged to fully exploit the potential of polarity-controlled devices [2].

As memory effects arise naturally from nanoscale systems, many applications ranging from

standalone memories, non-volatile FPGA, programmable interconnects, as well as sensing have been envisaged. In this thesis, *multi-value ReRAM* devices arranged in dense-crossbar are demonstrated with a top-down process flow compatibile with BEoL post-processing due to the low thermal budget (T < 200°C). Preliminary results on a CMOS chip demonstrate the feasibility of BEoL post-processing, opening new possibilities for FPGAs, standalone memories, ultra-low power analog design, neuromorphic architectures. In particular, ReRAMs with bipolar resistive switching mechanism can be arranged to form an equivalent of the pass-gate devices with the advantage high-density and very-low energy consumption. This feature can be exploited in the proposed *Generic Memory Structures (GMS)* that can be beneficial for either routing Multiplexers or configuration nodes in FPGAs.

In addition, memory effects in ambipolar SiNW SBFETs can be exploited for additional functionality. One possibility will be to exploit the retention of the memristive SBFETs to build a new type of DRAM. As the same structure can be utilized for both memory and logic, architectures based on distributed elements of memory and logic can be envisaged. Moreover, the hysteresis dependence over the current-bias and over the temperature have been exploited to sense these physical quantities. Moreover, as the hysteresis depends on the trap charging into the dielectric and the body of the nanowires, such dynamic can be effected by the presence of bio-functionalization layers. This is exploited in a novel device based on ambipolar Si nanowires for *bio-sensing* applications.

In future work, a platform hosting both logic and memory elements developed througout this thesis would enable new architectures either as a standalone platform or in the framework of CMOS post-processing, eventually generating novel research ideas. For instance, neuromorphic architectures can benefit from the *threshold function* of the ambipolar Si nanowire FETs with the current-biasing scheme as it is one of the elements in the *Perceptron model of the neuron* as well as from the non-volatility and density of the resistive RAM crossbars, whose electrical behavior can emulate the *synaptic interconnections* or, in other words, the weighted links in some of the *Artificial Neural Networks* architectures.

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A Process Flow Steps

A.1 ebeam lithography

The e-beam lithography is carried out with a VISTEC EBPG5000 providing a 100keV electron acceleration voltage. Negative tone Hydrogen SilsessQuioxane (HSQ) XR-1514 2% dilution from Dow Corning™ has been used as hard mask for the patterning of Si nanowires, while positive tone resist ZEP based on Styrene Methil Acrylate polymer is utilized for the patterning of the gates.

A.2 Si dry etching

The etching steps are carried out in an Alcatel Adixen AMS200 and it is operated with pulsed Low Frequency (LF) wafer biasing with alternative SF_6 and C_4F_8 gas flows for controlled Si etching. On SOI substrates an End Point Detection mechanism is utilized to verify that the Si device layer is correctly etched. This process has also been utilized to produce vertically-stacked SiNWs after the NiSi regions were formed on an SOI device layer (an example is shown in false colors in Fig. A.1).

A.3 Sacrifical wet oxydation

In the early examples, Si nanowires have been obtained by means of sacrificial oxydation steps. This method has also the purpose of forming a thick isolation layer at the bottom of the Si trenches.

A.4 Gate Stack

A.4.1 Polysilicon Gate Stack

After the nanowire formation process a Si oxydation in O_2 atmosphere is carried out. Different recipes were utilized and for thin nananowires a self-limiting oxydation at 850°C is carried out. Since the oxydation is carried out below the viscosity transition temperature of Si/SiO_2

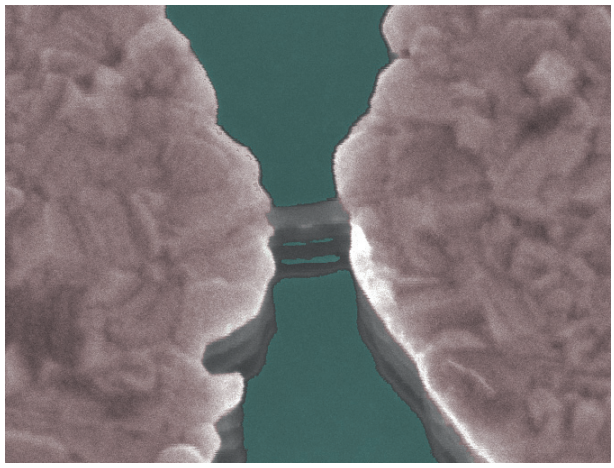


Figure A.1: 100nm long vertically-stacked SiNWs formed after the NiSi regions by DRIE. The etching has been performed after Ni lift-off and annealing. The NiSi source/drain regions then served as etching layer.

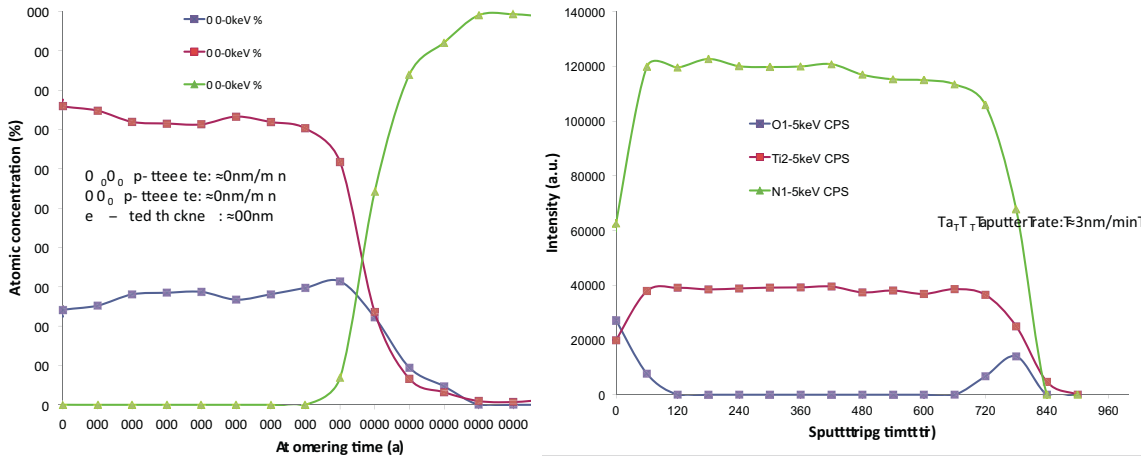
(960°C), compressive stress builds up and slows the oxydation rate. This phenomena can be exploited to achieve a good control of nanowire diameters. Typical SiO_2 thicknesses for Si nanowire transistors are between 5nm and 20nm. Then polysilicon layers of thickness between 50nm and 500nm were deposited by LPCVD, giving excellent conformality.

A.4.2 High-κ/Metal Gate

The High-κ/metal gate stack has been deposited by ALD. In particular, HfO_2 and TiN have been choosed for their thermal stability with Si. Concerning the resistive RAM development, TiO_2 stochiometry and the quality of the TiN are also important, and as such, the ALD deposition quality of TiO_2 and TiN at CMi has been checked with AES (see Fig. A.2a) and XPS (see Fig. A.2b) profiles, respectively.

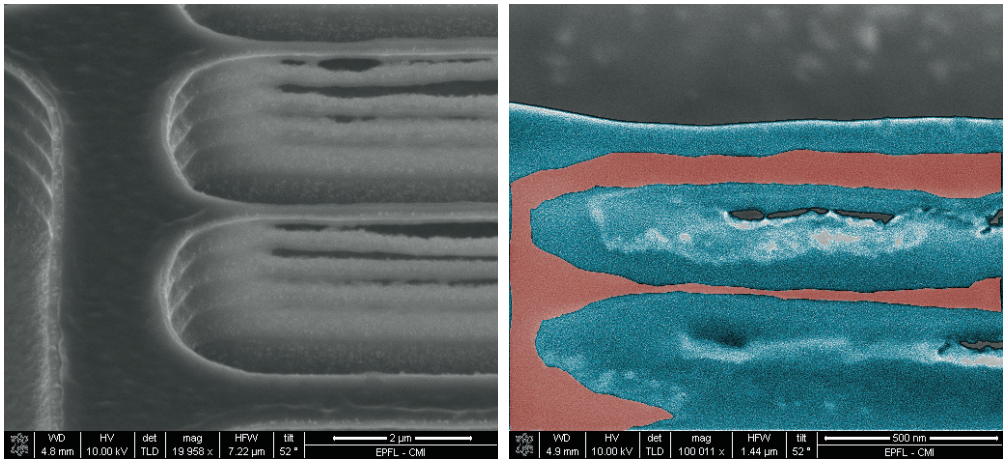
A.5 NiSi silicidation

A 30nm thick Ni layer is deposited by e-beam evaporation in Alcatel EVA600 evaporation system in vacuum level of $5 \cdot 10^{-7}$mbar. The substrate is quickly loaded into EVA600 just after a short BHF step to remove native oxide from the Si surface. In this way the formation of a fresh SiO_x layer that can prevent NiSi formation is limited. The EVA600 has been chosed because it can provide a uniform coverage of Ni all-around the nanowires. This feature has been tested on arrays of vertically-stacked Si nanowires and characterized by FIB cross-section after Ni silicidation (see Fig. A.3. After the Ni deposition, the substrate are loaded into a furnace for NiSi formation. The NiSi recipe has been carried out by a triple-step thermal annealing of a Ni layer in forming gas in a horizontal wall furnace. The three-step annealing refers to three plateau temperatures, each corresponding to a specific NixSiy phase (see Fig.A.4. At 200°C Ni-rich phases are formed. Then a second plateau at 300°C is exploited so that a Ni_2Si phase is obtained. Finally a 400°C plateau is kept for 20min to produce the Ni_1Si_1 phase required



(a) (b)

Figure A.2: Characterization of the ALD-deposited TiO_2 and TiN: (a) XPS profile of TiO_2, showing a 1:2 Ti:O stochiometric ratio. (b) AES profile of TiN showing a little oxide layer at the surface and at the bottom of the layer, which should be minimized to reduce resistivity.



(a) (b)

Figure A.3: NiSi nanowires after annealing in forming gas: (a) SEM tilted view. (b) FIB cross-section. The central Si section has been colored in red, while NiSi is colored in blue.

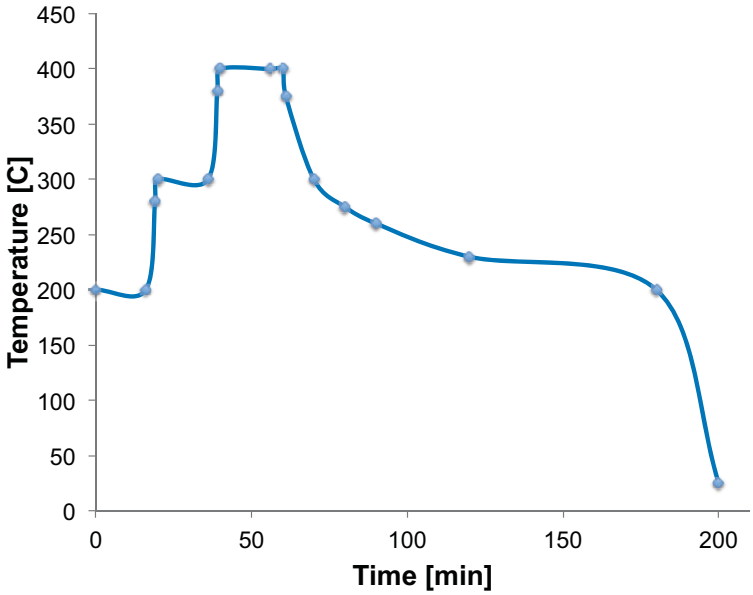


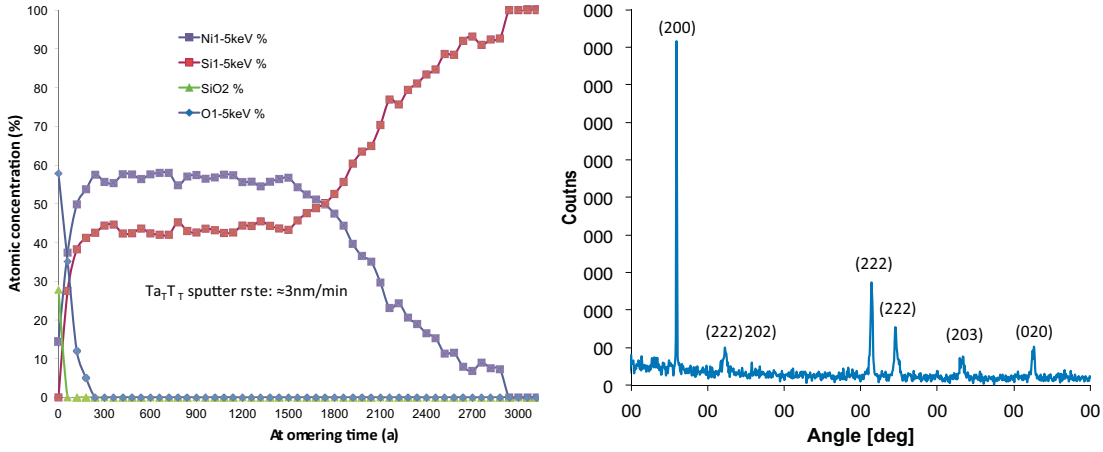
Figure A.4: Temperature-Time chart of the NiSi triple-step annealing. The substrates are loaded at 200°C (the furnace has been pre-heated) and after a 5min purge phase with 20slm N_2, $N_2 : H_2$ forming gas is injected while temperature is kept constant for 20min at 200°C. Then a second temperature plateau is reached at 200°C and kept for another 20min. Finally, the NiSi phase is obtained by increasing the temperature up to 400°C for 20min. Then the substrates are slowly cooled down, to avoid any thermal stress that might generate defects and unwanted interfacial states at the NiSi/Si junction. At 200°C the H_2 flux is stopped and the substrates are removed from the furnace.

for a mid-gap Schottky barrier contact. The Ni_1Si_1 phase is also chosen because it has been proven to be among several silicides to be the one with lowest resistivity. All thermal steps above 200°C are carried out in forming gas consisting of 9:1 N_2:H_2 mixture with a total flow rate of 100sccm/min.

The correct formation of NiSi has been checked with Auger Electron Spectroscopy (AES) and X-ray diffraction. The XPS/AES analysis has been carried out in a XPS/ESCA KRATOS AXIS ULTRA and in-depth profiling of NiSi layer has been carried out by Argon sputtering. The XRD tests were carried out in a Θ-2Θ X-ray diffractometer, and the instrument has been calibrated exploiting the position of the 400 Si peak.

A.6 BEoL post-processing

The development of a process flow compatible with CMOS Back-End-of-Line is fundamental for providing large access to this novel technology with a limited development costs. The main objective is to develop some integration techniques that allow to efficiently process ReRAM stacks on top of dies, processed by conventional CMOS foundries. One of the big advantages of ReRAM technology is its CMOS-compatibility. Indeed, the materials involved in ReRAMs are deposited at low temperature, compatible with metal line process. Different integration



(a) (b)

Figure A.5: Characterization of the NiSi thin-films after annealing: (a) Auger Electron Spectroscopy profile. Notice the Oxygen content at 0sec of sputtering, which is probably due to a thin native oxyde at the surface of NiSi. (b) X-ray Diffraction.

options might then be envisaged. First, it is possible to deposit the ReRAMs on the last metal layer of conventional process flow and add a final top cap layer that provides access to the top terminal of the ReRAMs. As an illustration, a schematic cross section and a temptative process flow of a co-integrated ReRAM-CMOS BEoL are shown in Fig. A.6.

The proposed solution illustrates a very conventional integration, that requires three lithographic steps. Additional lithographic steps increase the cost of the whole integration process, and decrease the reliability of the fabricated dies. To reduce the number of lithography steps, a second solution, using only a unique step, will be developed. As shown in Fig. A.7, the CMOS die is fabricated such that the last CMOS BEoL includes patterns that can be used as a mask for the definition of top electrodes. At the same time, the lower metal layers in the BEOL are exploited as bottom electrode lines, in this way the post-processing scheme is dramatically simplified as it requires only one lithography for the passivation opening. Finally, a third solution (Fig. A.8) envisages additional one or two lithographic steps in order to obtain a ReRAM stack in between the last metal layer and the last via layer. This solution is the most compact one and it also offer the flexibility for the implementation of top and bottom electrodes of different materials.

A.6.1 On going post-processing

A first CMOS chip with cross-bar arrangement of 32x32 rows and columns has been designed with pass-gates and decoder for the addressing. The design of the basic cell of the arrays is exploiting the presence of an MMC layer, which will be utilized as the upper electrode. Since the distance between the MMC electrode and the bottom metal (metal 5) is only 35nm, the current post-processing involves the etching of the ILD and the deposition of a *Resistive Switching Material*. In Fig. A.9a a tilted SEM view shows the basic cell with metal 6, MMC and

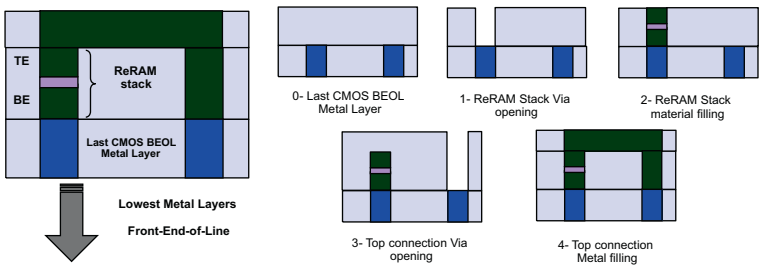


Figure A.6: Cross-sectional schematic and associated process flow showing the integration of a ReRAM device (on the top of a pro-processed CMOS die. The device is including a oxide layer between bottom (BE) and top (TE) electrode contacts and is integrated between the last metal layer and an additional one patterned on top of the existing die.

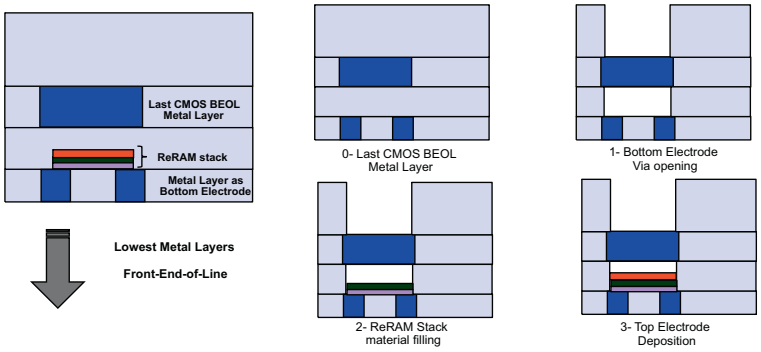


Figure A.7: Cross-sectional schematic and associated process flow showing the integration of a ReRAM device with an alternative process. Since the last CMOS BEOL metal is utilized as shadow mask for top electrode patterning, this scheme of ReRAM co-integration only use 1lithographic step for patterning, allowing for a more precise alignment of the different parts.

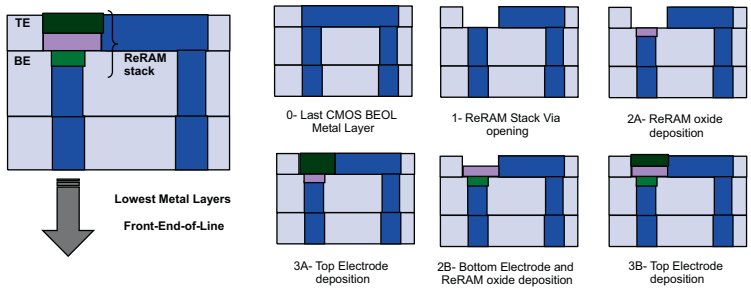


Figure A.8: Cross-sectional schematic and associated process flow showing the integration of a ReRAM device with an alternative process. In here, two (three) lithographyc steps are needed, allowing for the integration of top (top and bottom) electrodes of different materials.



(a) (b)

Figure A.9: (a) Tilted SEM view of a MMC cross-point. The MMC layer is colored in blue. Metal 5 is colored pink while metal 6 is colored brown. The bright parts of the image are due to charging of the dielectric layers. (b) FIB cross-section of the MMC electrode (in blue) with a bottom metal 5 electrode (brown color). A 35nm dielectric layer electrically separates the MMC and the metal 5.

metal 5 after the ILD etching.

Fabrication and Characterization of Vertically Stacked Gate-All-Around Si Nanowire FET Arrays

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***Abstract*— We describe the fabrication of vertically stacked Silicon Nanowire Field Effect Transistors (SiNW FETs) in Gate-All Around (GAA) configuration. Stacks with the number of channels ranging from 1 to 12 have been successfully produced by means of a micrometer scale lithography and conventional fabrication techniques. It is shown that demonstrator Schottky Barrier (SB) devices fabricated with Cr/NiCr contacts present good subthreshold slope (70mV/dec), I_{ON}/I_{OFF} ratio $\geq 10^4$ and reproducible ambipolar behavior.**

***Index Terms*— nanowire, FET, multichannel, ambipolar, vertical integration**

I. Introduction

Continuing efforts in Complementary-Metal-Oxide-Semiconductor (CMOS) research have lead to the exponential increase of device integration density during the last 40 years. More recently increasing fabrication costs and increasing overall variability have become an obstacle for the scaling trend. In order to overcome such limitations, considerable research is dedicated for instance to the use of new materials (such as high-κ dielectrics with metal gates), dual-gate devices, novel isolation techniques that make use of Silicon-On-Nothing (SON) or Silicon-On-Insulator (SOI) substrates [1]. In particular, dual-gate technology in conjunction with the geometry of the device can enhance the control over the transistor channel. In this sense, further improvements can be achieved with tri-gate, omega-gate or Gate All-Around technologies (GAA) [2].

Recent works explored the vertical stacking of SiNWs as channels for FET devices [3], [4]. The vertically stacked SiNWs represent channels of the same SiNW FET, whose electrostactic control can be enhanched by using a GAA configuration [5]. In addition, SiNW FETs can also be used to build new logic architectures [6], [7] or as ultimate memory architectures for Ultra-Large-Silicon-Integration (ULSI) [8], [9].

In this work we discuss novel and promising fabrication method for vertically-stacked SiNW FETs with different number of channels on bulk Si wafers. The reported method has also been applied to fabricate single channel devices that demonstrate excellent reproducible performance.

II. Related Work

Recently, a multichannel structure with GAA configuration has been proposed as a candidate for high-performance devices. Its implementation has the advantage of enhanced on-current (I_{ON}) along with low leakage as well as a small footprint for multi-finger (multi-channel) devices [10], [4]. The fabrication process described in [10], [4] is based on creating epitaxial layers to alternate Si and SiGe layers one on top of each other. A vertical trench is etched in the grown structure. A successive SiGe selective etching leaves vertically-stacked Si nanowires. Hydrogen annealing is then used to change the SiNW shapes from rectangular to circular, thus yielding channels with less surface roughness and improved controllability.

An alternative approach for the fabrication of vertically-stacked SiNWs [11] is based on producing a scalloped trench in bulk silicon by means of Deep Reactive Ion Etching (DRIE). Sacrificial oxidation steps are performed to reduce the dimensions of the trench. Thanks to scalloping, the Si trench is totally consumed in its thinner parts, leaving a vertical stack of suspended SiNWs. Although the DRIE process defines trenches of micrometer dimensions, the iteration of oxidation steps is capable for reducing the structures to suspended nanowires with of 20 nm in diameter [11]. This approach has also been demonstrated to be suitable for producing vertically stacked SiNW with small dimensions and different section shapes [12], yet it has not been used so far for GAA FET fabrication.

III. Device fabrication

In our work we produce vertical SiNW arrays by means of optical lithography with 1 μm resolution limit. Sub-micrometer features are obtained through sacrificial oxidation steps. Although the integration density would have been further increased by means of advanced lithography, the developed process already allows us to produce very high channel densities without making use of non standard fabrication steps.
We start by defining a photoresist line on a p-type ($N \sim 10^{15}$) silicon bulk wafer (see Fig. 1.a). Then a DRIE technique (also called Bosch process) is performed. This technique, that alternates a plasma etching with a passivation step, has been optimized to produce a scalloped trench in silicon with high reproducibility. Etching time, passivation time and plasma platen power have been optimized in order to enhance the scalloping effect. The application of the DRIE technique gives a trench like the one depicted in Fig. 1.b. The flexibility of the process allows us to change the number of scallops easily. After a wet oxidation step (see Fig. 1.c) vertically stacked SiNWs are formed. Then the cavities produced by the Bosch process are filled with photoresist. After a combination of chemical mechanical polishing (CMP) and BHF dip, the wet oxide is removed around the NWs (see Fig. 1.f). The oxide at the bottom of the cavity is left to isolate the substrate from the successive processes. The vertical structure obtained is then oxidized to produce a high quality dry oxide (20 nm thick, see Fig. 1.g) as gate dielectric. Then between 200 nm and 500 nm of Low Pressure Chemical Vapour Deposition (LPCVD) polysilicon is deposited (Fig. 1.h). The polysilicon gate is patterned by means of a combination of isotropic and anisotropic recipes (see Fig. 1.i). A final field oxide isolation and Al or Cr/NiCr patterning make the external electrical connections.

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A SOI wafer has been used to fabricate demonstrator devices with single channel layer. In this case we patterned Cr/NiCr through a lift-off technique to form source and drain. An advantage for using Ni is that it can easily form silicides with mid-gap workfunctions at low temperature, thus allowing the fabrication of FETs in few process steps and with a low thermal budget [13]. However, the main difference with FETs defined by implantation is the formation of Schottky Barrier (SB) source/drain thus leading to a device with ambipolar characteristic. The ambipolarity refers to the $I_{ds} - V_{gs}$ electrical characteristic of a transistor having both p- and n-type behaviour [13]. A double step annealing (at 200°C and 400°C, respectively) has been choosen to form silicided regions. This annealing process has been seen as good choice in terms of I_{ON}/I_{OFF} ratio improvement [14]. After the annealing steps, the unreacted Cr/NiCr parts were removed in wet etchant. Finally a 1 μm thick layer of Al has been patterned after via opening on the field oxide.

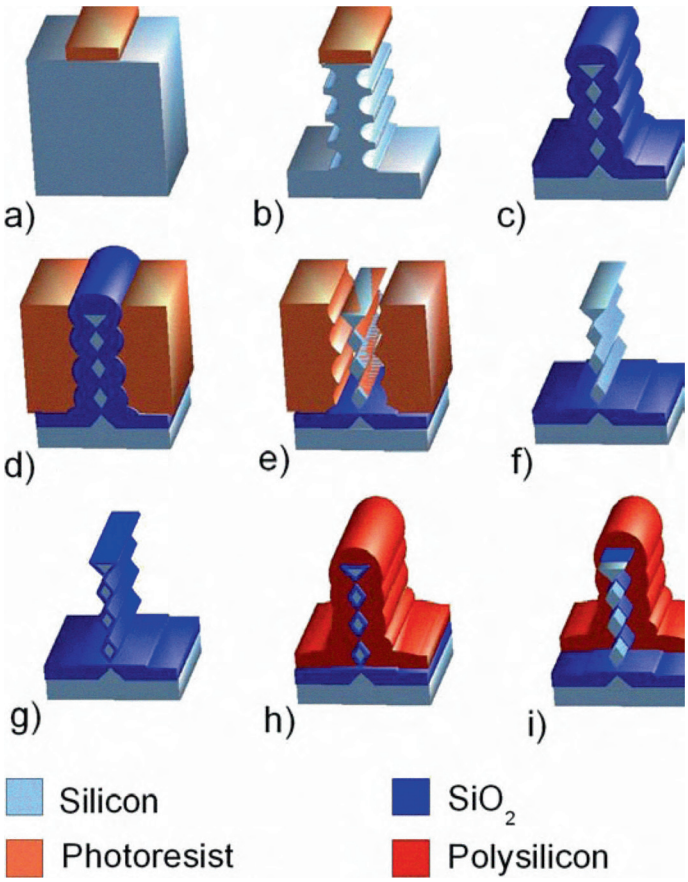


Fig. 1. Process flow of vertically stacked Si-NW FET. a) A photoresist line is defined on the Si wafer. b) A Bosch process is performed to produce a scalloped trench. c) Wet oxidation. d) A 5 μm thick photoresist is spin-coated in order to fill the cavities formed around the trench. e) The oxide removal step free the SiNWs withouth removing the oxide at the bottom of the cave. f) SiNWs are vertically stacked and electrically isolated from the substrate. g) A high quality dry oxide is formed. h) LPCVD polysilicon deposition. i) Gate patterning

IV. Discussion on the fabricated structures

Three dimensional SiNW FET arrays have been fabricated in vertical stacks with the number of channels varying between 1 and 12 (see Fig. 2). Initially, the formed SiNWs have diameters ranging from 70 nm to 200 nm, several techniques can be applied in order to refine the dimensions in a controlled manner. For instance, it has been demonstrated that the use of self-limiting oxidation is capable of producing channels with nanometer dimensions and good controllability [4], [15]. Surface irregularities of the suspended NWs can be improved either by means of a self-limiting oxidation or by hydrogen annealing step [10]. It was found that the proposed fabrication method consistently produces repeatable and very controllable dimensions of clearly separated NW stacks, by optimizing the etch/oxidation conditions. A uniform and thin gate oxide is formed around the suspended NWs by dry oxidation in a horizontal furnace under 10 slm O_2 flux. By combining isotropic and anisotropic etch techniques, polysilicon gate lengths down to 200 nm (see Fig. 3.a) were produced using 1 μm lithography. It can be seen that the polysilicon gate completely surrounds the suspended NW segment without any gaps, and that the silicon NW is covered by a 20nm thick gate oxide (Fig. 3.b). The proposed GAA device fabrication technique has also been succesfully applied for NW stacks with 3 suspended channels (Fig. 4). Fig. 4.a shows a structure with two parallel polysilicon gates, and Fig. 4.b shows the cross-section of the structure where individual wires and the surrounding polysilicon gate are clearly visible. Note that the cross-section of each suspended NW (with the exception of the top wire) has a well-defined rhombic shape that is dictated by the successive etching/oxidation steps used to produce the wire stacks. The top wire has a triangular profile that is also defined by the process. Schottky-barrier (SB) SiNW FETs demonstrator devices in GAA configuration have also been fabricated successfully on SOI, and shown in Fig. 5. In this particular example, the suspended NW segment has a trapezoidal cross-section.

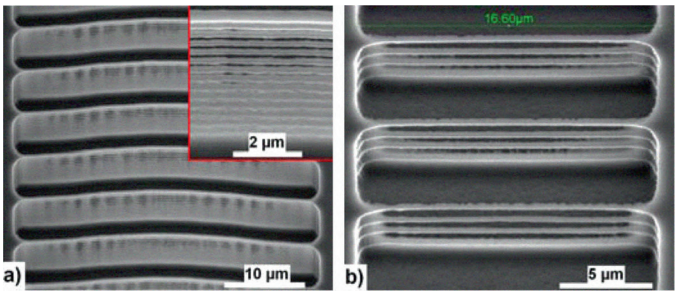


Fig. 2. a) Vertically stacked SiNWs in array configuration after oxide removal. The nanowires are free and sligthly bent due to residual stress. In this sample the number of vertically stacked nanowires amounts to 12. b) Another array with 3 vertically stacked SiNW channels.

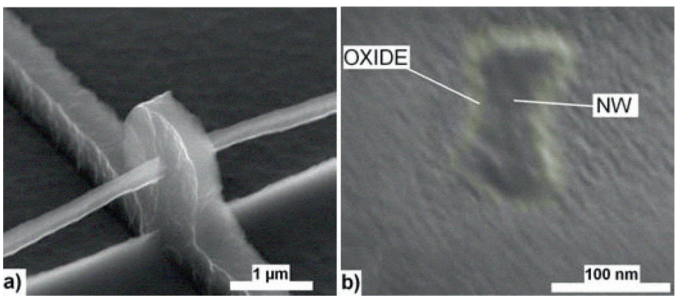


Fig. 3. a) Single nanowire surrounded by 500 nm thick polysilicon gate; $L_g \sim 200$ nm. b) Gate stack cross-section showing the Si core surrounded by 20 nm gate oxide and polysilicon.

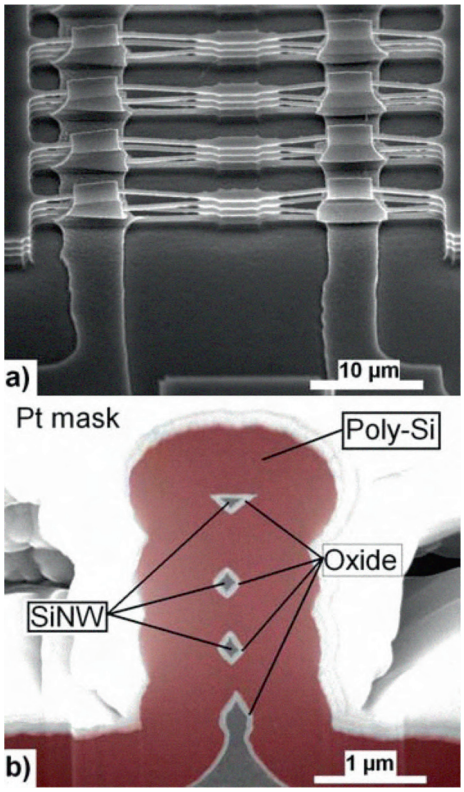


Fig. 4. a) Long nanowire channels with two parallel gate construction. b) Gate stack crossection showing three SiNW channels.

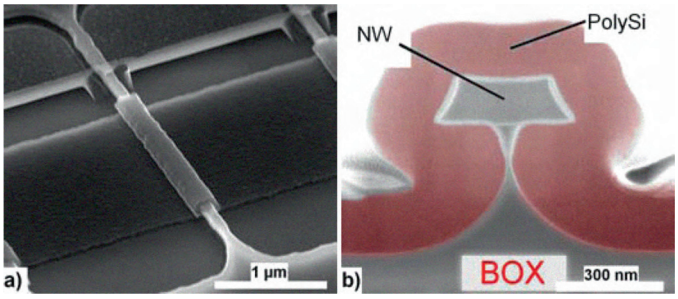


Fig. 5. a) Single GAA-NW device with polysilicon gate. b) Gate stack cross-section and highlight on different stack materials.

V. Electrical Measurements

The measured electrical performance of two SB SiNW FET devices with single SiNW channel in the stack are reported in the following. Each NW channel have $5\,\mu m$ gate length and an effective width of $930\,nm$. Since the NW cross-section is trapezoidal, the effective channel width is the perimeter of the NW. The devices (see Fig. 6) show an ambipolar behaviour with good performance of both p- and n- branches. Table I reports the device (device A) parameters demonstrating device ambipolarity, I_{ON}/I_{OFF} ratio $\geq 10^4$ and a subthreshold slope (SS) lower than 70 mV/dec for the p-type portion of the curves ($V_{gs} > V_{th}^{h^+}$ for h^+), and around 250 mV/dec for the n-type part ($V_{gs} < V_{th}^{e^-}$ for e^-). The $I_{ds} - V_{ds}$ curves have been measured for positive V_{gs} (Fig. 7.a) and negative V_{gs} (Fig. 7.b). The device behavior in the "triode" region indicates very distinct gate control over the drain current. The plots also show a Negative Differential Resistance (NDR) region when the channel is in inversion mode.

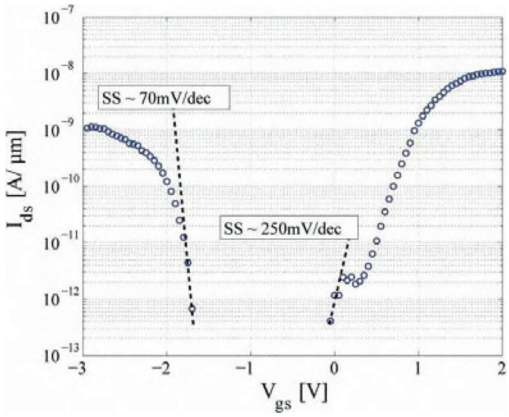


Fig. 6. Device A: $I_{ds} - V_{gs}$ curve for $V_{ds} = 1\,V$. The observed ambipolarity is typical for the metallic source and drain MOSFETs. Note the very high subthreshold slopes in both modes.

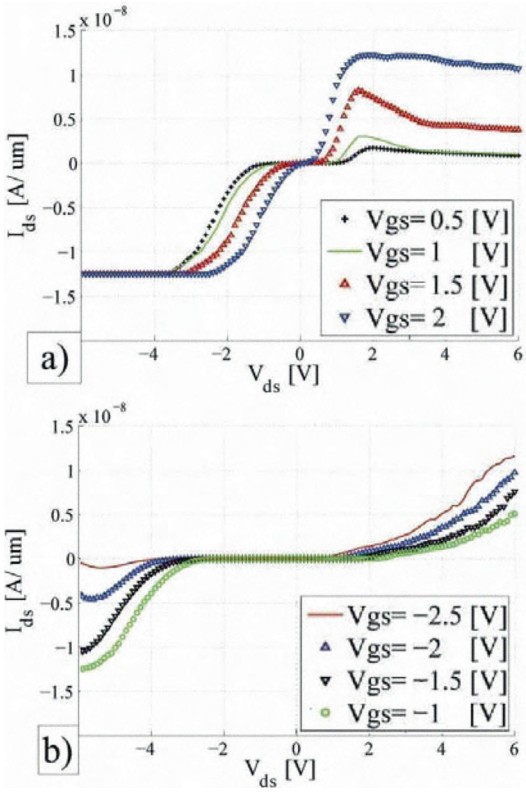


Fig. 7. Device A: $I_{ds} - V_{ds}$ curves showing negative differential resistance when the channel is at the inversion: a) for $V_{gs} \geq 0\,V$ channel in inversion mode for positive V_{ds} and in accumulation mode for negative V_{ds}. b) For $V_{gs} \leq 0\,V$ the channel is in inversion mode for negative V_{ds} and in accumulation mode when V_{ds} is positive.

TABLE I
Device A: SB SiNW FET parameters.

	$\frac{I_{ON}}{I_{OFF}}$	V_{th}^{+} or $V_{th}^{e^-}$ [V]	SS $[\frac{mV}{dec}]$	$I_{ON}^{h^+}$ $[\frac{nA}{\mu m}]$	$I_{ON}^{e^-}$ $[\frac{nA}{\mu m}]$
h^+	2900	−2	< 70	12.5	-
e^-	31000	1	250	-	2

A partially gated device (source and drain have been designed 1 μm far away from the gated channel) shows ambipolar behaviour (see Fig. 8). The extracted parameters for this device (device B) are reported in Table II. The high V_{gs} required for the onset of conduction is believed to be due to the non controlled portion of the channel. This behaviour is confirmed in [16]. Moreover, in [16] the possibility of making the device unipolar by using a dual gates was discussed as well. A dependency of the I_{OFF} on the applied V_{ds} is found (see Fig. 9).

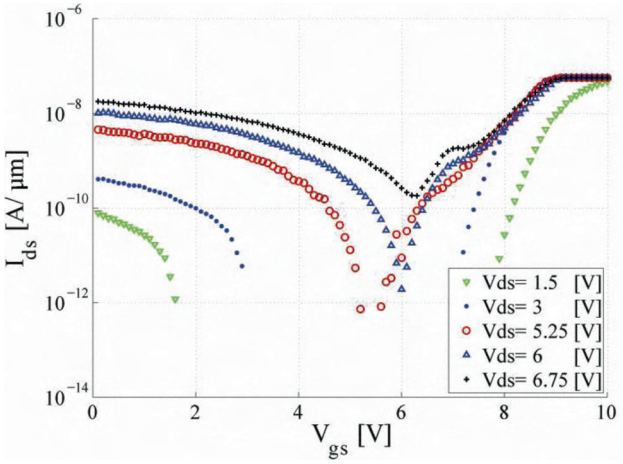


Fig. 8. Device B: $I_{ds}-V_{gs}$ curves for a partially gated device showing ambipolar behaviour and dependence to the applied V_{ds} .

TABLE II

DEVICE B: AMBIPOLAR BEHAVIOUR PARAMETERS FOR POSITIVE GATE VOLTAGES AFTER TWO STEP SILICIDATION ANNEALING.

V_{ds} [V]	$I_{OFF}^{h^+}$ [$\frac{pA}{\mu m}$]	$I_{OFF}^{e^-}$ [$\frac{pA}{\mu m}$]	$\frac{I_{ON}}{I_{OFF}}^{h^+}$	$\frac{I_{ON}}{I_{OFF}}^{e^-}$	SS^{h^+} [$\frac{mV}{dec}$]	SS^{e^-} [$\frac{mV}{dec}$]
1.5	1	8	300	7500	400	250
3	6	10	333	6000	700	350
5.25	0.7	0.7	10000	85700	200	300
6	2	2	10000	30000	200	200
6.75	200	200	150	300	N/A	N/A

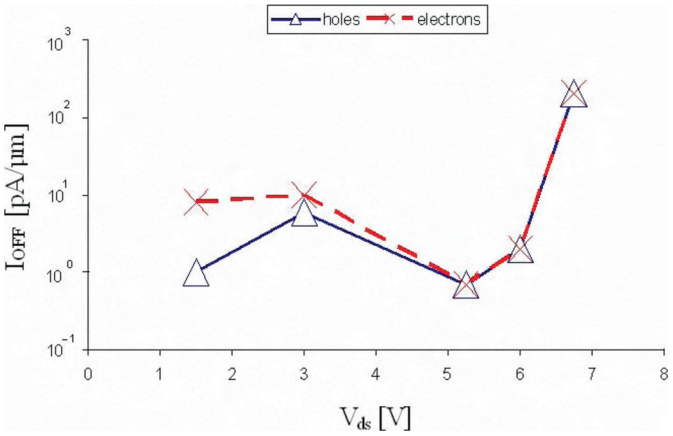


Fig. 9. Device B: I_{OFF} for holes (p-type portion of the $I_{ds} - V_{gs}$ curve) and electrons (n-type portion of the $I_{ds} - V_{gs}$ curve) conduction at different V_{ds}.

VI. CONCLUSIONS

High channel density SiNW GAA FETs have been fabricated by means of a DRIE technique for the first time. The same low cost top-down approach has been succesfully deployed to fabricate vertical SiNW stacks with different number of SiNW channels; i.e. the number of channels composing the vertical stack could be easily tuned from 1 to 12. Moreover, the process can be easily adopted for different substrates (bulk or SOI wafers) without any additional complexity. Finally, SB SiNW devices fabricated with good repeatability show excellent performance (the measured $SS < 70\,mV/dec$ is close to the optimal value for SiNW devices for room temperature operation) making the approach suitable for further investigations.

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Ambipolar silicon nanowire FETs with stenciled-deposited metal gate

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ABSTRACT

We report on a fully CMOS compatible fabrication method for ambipolar silicon nanowire FinFETs. The low thermal budget processing, compatible with monolithic 3D device integration, makes use of low pressure chemical vapor deposition (LPCVD) of amorphous Si (a-Si) and SiO_2 layers as well as metal gate patterning using stencil lithography, demonstrated for the first time. FinFETs with stenciled Al gates are successfully co-fabricated with polycrystalline silicon Ω-gated devices. Stencil lithography is envisaged as a key enabler for gate patterning on 3D structures, such as vertically stacked nanowire transistors.

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1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures or different state variables other than charge [1]. All these approaches will lead to significant modifications of the traditional planar transistor design. Considering novel device structures, the nanowire (NW) channel transistor with FinFET construction has been demonstrated to be one of the best in terms of electrostatic control, thus enabling further device scaling [2]. Another example can be the monolithic 3D integration, a process integration scheme that achieves higher device density by stacking p-type FETs on top of n-type FETs [3]. In terms of state variables, one example is given by device ambipolarity. The ambipolar property can be described by the presence of two high conductance states for the same FET, each of these related to carriers of opposite charge values [4]. Preliminary works on device ambipolarity show how it can be used to compute more complex logic functions per chip [5]. However, in terms of process integration, a few technologies have the flexibility to be implemented within 3D integration schemes and, at the same time, offer the ambipolar property with good CMOS compatibility and electrical performance.

We report on a fully CMOS compatible fabrication of ambipolar SiNW FinFETs by means of amorphous Si (a-Si) and low temperature oxide (LTO) deposited with low pressure chemical vapor deposition (LPCVD) technique. FinFETs with stenciled Al gates are successfully co-fabricated with polycrystalline Si (pc-Si) gated devices achieving excellent performance. The difficulty of achieving high resolution gate patterning on non-planar devices is addressed for the first time by means of stencil metal deposition [6]. We envisage the use of this technique also for metal patterning on high aspect ratio FETs, such as vertically stacked nanowire transistors [7]. It is worth noting that this process can be repeated several times, eventually being used for monolithic 3D integration.

In Section 2 we present the fabrication steps to build the devices. Then in Section 3 the fabricated structures are shown and described. In Section 4 we describe the electrical behavior of the two types of FinFETs fabricated and on the pseudo-inverter operation of pc-Si FinFETs. Finally, in Section 5 we draw the conclusions.

2. Process flow

The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500 nm thick wet oxide and a 100 nm LTO layer. Then a 100 nm a-Si film is deposited as the active layer. A 70 nm thick dilution of hydrogen silsesquioxane (HSQ) is spin coated and patterned with e-beam lithography. Lines having widths ranging from 70 nm to 250 nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip buffered hydrofluoridric acid (BHF) step. The obtained a-Si nanowires are then covered by a 40 nm dry oxide and a 50 nm LPCVD pc-Si layers. Large 100 μm × 100 μm pc-Si pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, pc-Si Ω-gated FinFETs with gate lengths between 1 μm and 10 μm are obtained.

Then a bi-layer of 20 nm Ti/55 nm Ni is patterned with lift-off to form electrical contacts between the Si nanowires and the pads. A 400 °C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been

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chosen for its mid-gap work function and for its use in a-Si metal induced recrystallization process [8]. The fabrication flow is completed by the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100 nm thick SiN membranes with apertures having widths between 100 nm and 1 μm [9]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2 μm [9] accuracy using a customized SUSS MA/BA 6 mask aligner [10]. The clamped substrate–stencil setup is placed in an evaporator where 100 nm thick Al gates are deposited.

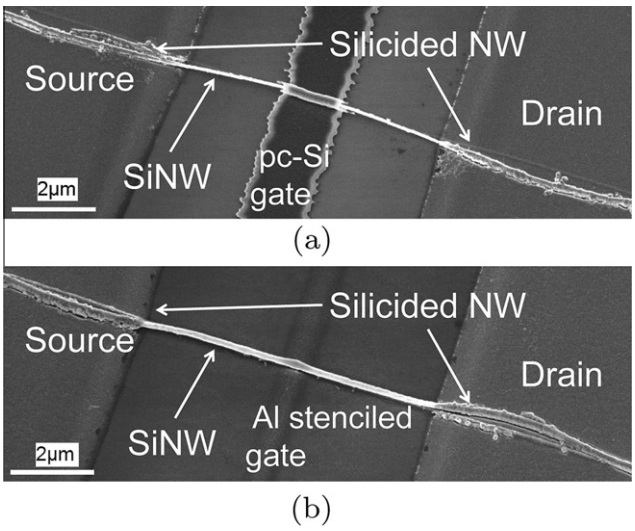


Fig. 1. FinFETs with silicide nanowire portions at source/drain contacts: (a) pc-Si FinFET having 2 μm long gate and 60 nm × 65 nm channel cross-section. (b) Al stenciled FinFET having 700 nm gate length and 60 nm × 140 nm channel cross-section.

3. Fabricated structures

FinFETs and inverters with up to 62 μm nanowire length were fabricated. An example of a 2 μm long pc-Si gate FinFET having 100 nm × 65 nm Si nanowire channel is shown in the SEM tilted view of Fig. 1(a). In Fig. 1(b), a Si nanowire transistor with 130 nm × 65 nm channel (see Fig. 2(d)) cross-section and 700 nm large stenciled Al gate is shown. Focused ion beam (FIB) cross-sections (see Fig. 2(a)–(c)) demonstrate nanowire channels sections having widths between 65 nm and 130 nm. The total Si thickness is reduced from the initial value of 100 nm to 65 nm due to processing. Narrower nanowires (the expected nanowire size was around 35 nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

4. Electrical measurements and discussion

The I_{ds}–V_{gs} curve of a pc-Si Ω-gate FinFET has a typical ambipolar behavior, with a higher conductance for holes (at negative V_{gs} voltages) than for electrons (Fig. 3(a)). In the holes-conductance regime, a subthreshold slope SS ≈ 420 mV/dec is observed, while a larger SS is observed for the electron-dominated current. The gate misalignment error is source of variation for the channel series

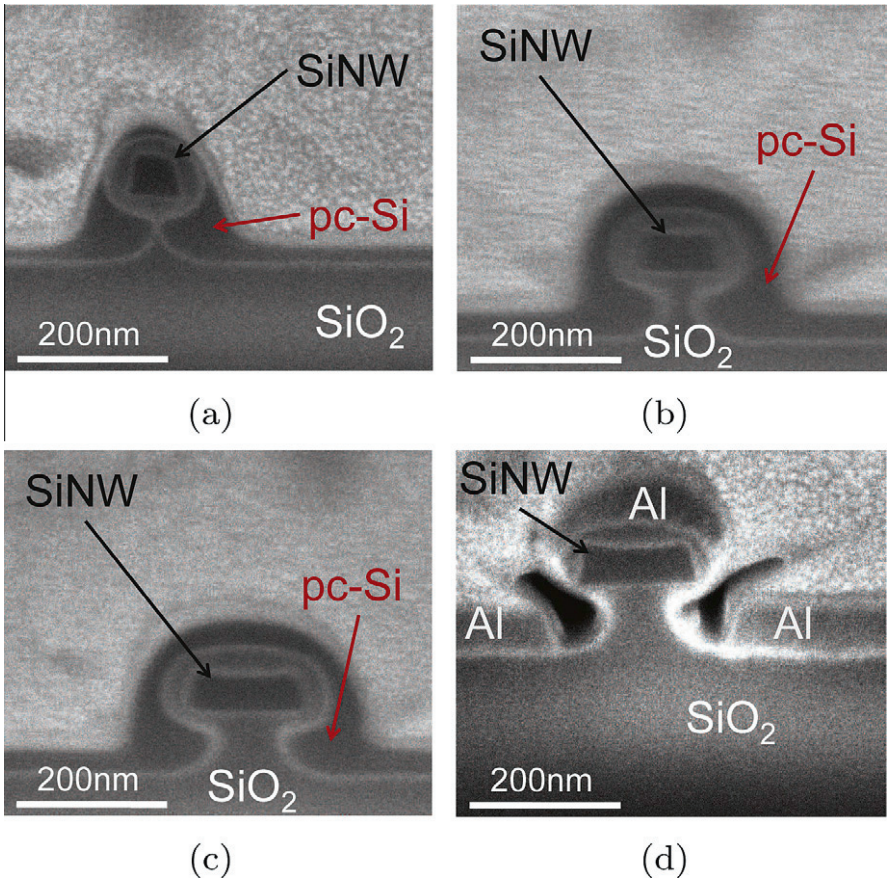


Fig. 2. FIB cross-sections showing the nanowire channels embedded in 40 nm oxide and gate materials: (a) pc-Si Ω-gate FinFET with 60 nm × 65 nm section. (b) pc-Si Ω-gate FinFET with 60 nm × 110 nm section. (c) pc-Si Ω-gate FinFET with 60 nm × 140 nm section. (d) Al stenciled-gate FinFET with 60 nm × 140 nm section.

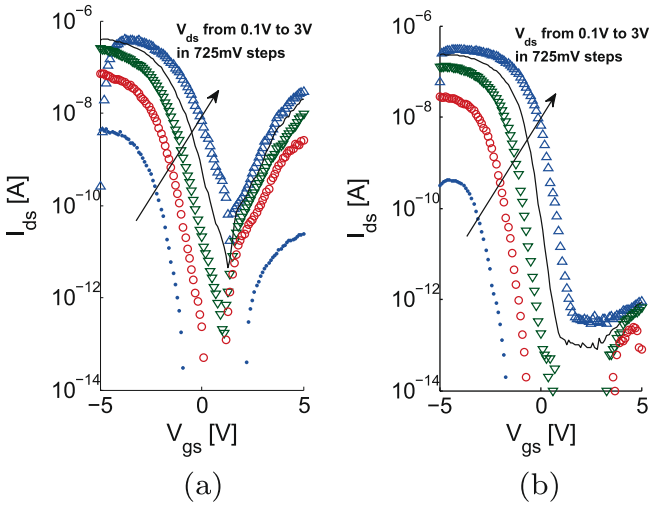


Fig. 3. (a) Ambipolar I_d–V_g curve of a pc-Si Ω-gated FinFET having 1 μm gate length and 60 nm × 110 nm nanowire section. (b) Ambipolar I_d–V_g curve of a stenciled Al-gate FinFET having 1 μm gate length and 60 nm × 110 nm nanowire section.

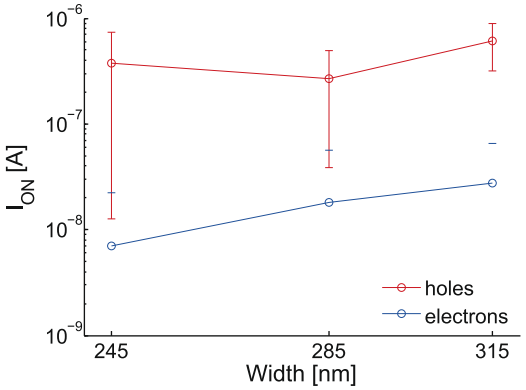


Fig. 4. Average I_{ON} for holes and electrons of pc-Si Ω-gated FinFETs of different widths. The error bar represents the standard deviation over a sample of eight devices.

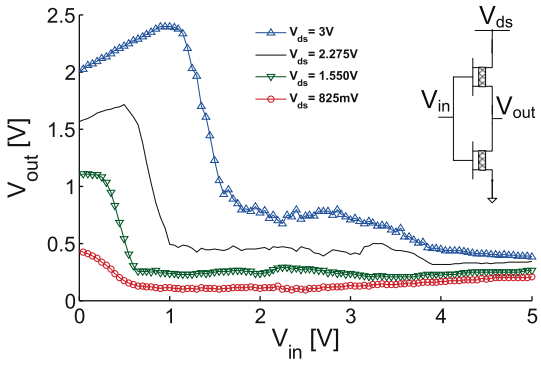


Fig. 5. Voltage transfer characteristic of a 2 in series connected pc-Si Ω-gate FinFETs on-a-wire and biased as for inverter operation. The insets represent the inverter bias scheme. Two ambipolar pc-Si FinFETs are connected in series.

resistance which in turn impacts the overall current conductance. Nevertheless, the main limiting factor for the current conductance is the injection of carriers over the Schottky barrier, and the series resistance is considered to play a minor role. This aspect is

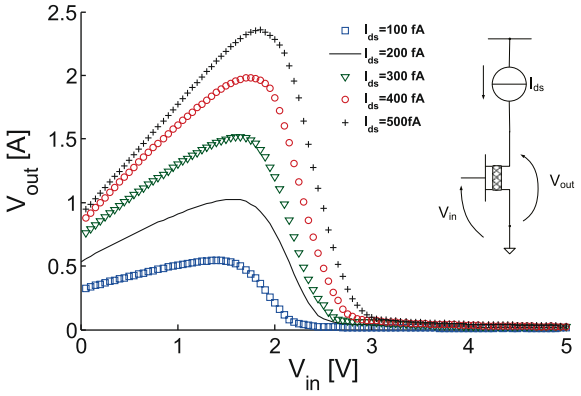


Fig. 6. pc-Si FinFET biased for pseudo-inverter operation having 2 μm gate lengths and 60 nm × 110 nm channel cross-section. The insets show the pseudo-inverter bias scheme using a single pc-Si FinFET and a current source.

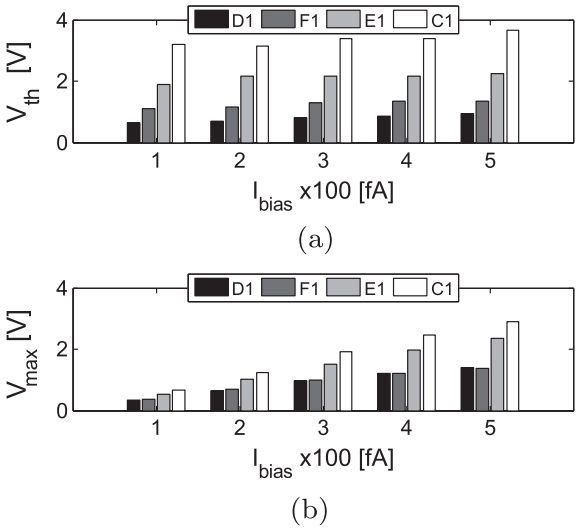


Fig. 7. (a) Threshold voltage (V_{th}) values for the pc-Si gated pseudo-inverters. The inversion voltages are stable under different current bias. (b) Maximum output voltages values for the pc-Si gated pseudo-inverters. The V_{max} values tend to increase linearly with I_{bias}.

confirmed by the observation of a lower I_{ON} for electrons than holes over a large number of samples. In Fig. 4, the average I_{ON} for holes and electrons is shown. The I_{ON} increase linearly with the channel width, which is calculated as the perimeter of the SiNW, since volume inversion effect are negligible for SiNW-channel diameters larger than 10 nm.

Conversely, Al-gated devices show a p-type conductance mainly (see Fig. 3(b)), which can be explained with Al contamination at pad regions due to the stencil process. This is also reflected in a SS ≈ 200 mV/dec, indicating that doping can effectively be used to improve SS by suppressing the ambipolar conductance. In both devices, I_{ON}/I_{OFF} ratios of more than six orders of magnitude are observed. The lower current for the *n*-branch in the Al gated devices might be due to metal gate-induced doping. The transfer characteristic of pc-Si Ω-gate inverters show (Fig. 5) an output voltage range V_{out} compatible with the input voltage range and a gain of $\Delta V_{out}/\Delta V_{in} \approx 4$. Thus, pc-Si gated inverters are suitable elements for cascading additional devices, enabling the construction of more complex circuits. Similarly, a current bias scheme for FinFETs can be used to obtain pseudo-inverter operation, which consist in using a current bias scheme as depicted in Fig. 6. For pseudo-inverter operation a triangular voltage transfer

characteristic is obtained, with very low power consumption ($\leqslant$1.2 pW). Data from different dies on the wafer show stability of the V_{in} value for which inversion occurs (V_{th}) under different current bias (see Fig. 7(a)). Moreover, as it is shown in Fig. 7(b), the maximum of V_{out} increases linearly with the current bias. Al gated inverters and pseudo-inverters are currently under investigation.

5. Conclusions

A fully CMOS compatible fabrication flow using low temperature a-Si LPCVD and stencil lithography has been developed and proved suitable for SiNW FinFETs having ambipolar conductance. Nanowires with up to 62 μm length with two separate gates have been successfully fabricated, giving space for complex circuit design. Moreover, the stencil lithography has been demonstrated for the first time as a suitable technique for metal gate patterning on 3D nanowire structures. The excellent performance of individual FinFETs and preliminary data of inverter functionality pave the way for the fabrication of more complex Si nanowire FinFET circuits. Further characterization of Al stenciled inverters and fabrication on high aspect ratio structures is envisaged as natural continuation of this work.

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Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography

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ABSTRACT

We report on the top-down fabrication of vertically-stacked polysilicon nanowire (NW) gate-all-around (GAA) field-effect-transistors (FET) by means of Inductively Coupled Plasma (ICP) etching and nanostencil lithography. The nanostencil is used to form sub-μm GAA gates over polysilicon NW array channels with high aspect ratio, considerably simplifying the lithographic steps above regions with deep 3D topography and non-planar surface features. This process lead to fabrication yields larger than 70% and authors envisage even larger yields of $\geqslant 85\%$ with optimized mask design. Electrical measurements confirm the results obtained from similar devices fabricated with a standard lithography method while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling.

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1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the planar transistor design [1,2]. Considering novel device structures, multiple-gated transistors have been proved of better electrostatic control and larger drive current with respect to the traditional planar transistor design [3]. These features are particularly attractive as enablers for further device scaling. In fact, double-gate and finFET structures are the first non-planar 3D gate constructions being successfully employed into commercial products. Nowadays, growing research efforts are spent with gate-all-around constructions with sub-10 nm diameter nanowire (NW) channels. Nevertheless, as the dimensions reduce and 3D structures are introduced, major difficulties arises due to the need of scaling while keeping large fabrication yields.

We report on a fully CMOS-compatible top-downfabrication flow of polysilicon channel finFETs and vertically-stacked polysilicon NW gate-all-around (GAA) FETs by means of an optimized Bosch process [4] and nanostencil lithography [5]. In a previous work, the authors envisaged stencil lithography [6] as a key enabler for gate patterning on 3D structures, such as vertically-stacked Si NW transistors [4]. In this work, nanostencil lithography is used to deposit the Al mask used to pattern sub-μm GAA polysilicon gates deposited with LPCVD as alternative solution for patterning nanoscaled features having high aspect ratio, which is a non trivial issue in photo-resist lithography. Moreover, a simple method to form vertically-stacked Si NWs on bulk-Si substrates [7] has been adapted to form vertically-stacked NWs onto polycristalline Si substrates. Preliminary electrical characterizations performed before the metal contact formation demonstrate functional memristive FET operation and confirming the behavior of previously reported devices fabricated with standard processing technology and μm-scale gate lengths [8]. The finFETs and the vertically-stacked polysilicon NW GAA devices are fabricated with yields larger than 70%, demonstrating a promising new method for 3D transistor fabrication with sub-μm nanostencil lithography.

In Section 2.1 we describe the structure of both finFETs and vertically-stacked GAA SiNW FETs. Then in Section 2.2 the fabrication flow for the devices is explained in detail, whereas the fabricated structures and discussion on the nano-fabrication results are provided in Section 3. Hence, the electrical measurement results are reported Section 4, with discussion among the difference in performance achieved by finFETs and vertically-stacked polysilicon NW GAA FETs. Finally, in Section 5 we draw the conclusions.

2. Device Fabrication

2.1. Device Description

The devices built can be grouped into two categories: finFETs and vertically-stacked SiNW FETs. In the first case, FETs or inverters having either 1 to 11 fins channels and tri-gate construction are built (in Fig. 1(a), a finFET with 3 fins is depicted). In the second

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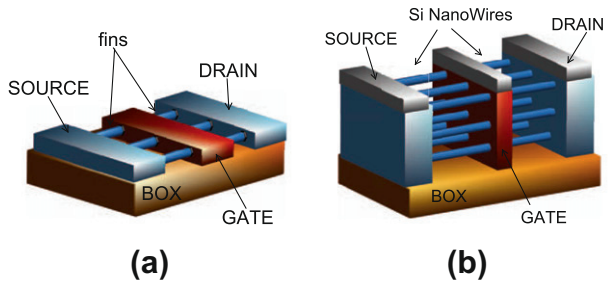


Fig. 1. Non-planar device topologies considered: (a) finFET with tri-gate construction.(b) Vertically-stacked SiNW FET with GAA construction.

case, FETs or inverters with 1 to 11 parallel strands consisting of 3 vertically-stacked SiNWs and GAA construction are built (in Fig. 1(b), a 3 times 3 SiNW matrix with GAA construction is shown). Apart from the fabrication of non-planar channels in such devices, the lithography definition of tri-gate or all-around gate structures above 3D channel regions is considered to be a significant challenge [1].

2.2. Process Flow

The fabrication starts with the substrate preparation for the two separate wafer batches. Bulk-Si wafers are oxidized in wet atmosphere to form 500 nm thermal oxide. Then either 50 nm or 350 nm thick LPCVD polysilicon is deposited as the device layer to build finFETs or vertically-stacked SiNW FETs, respectively. Individual or arrays of lines of widths of 50 nm and length of 8 μm are patterned with diluted *hydrogen silsesquioxane (HSQ)* using it e-beam lithography (EBL) (see Fig. 2(a)). The HSQ is then used as hard mask for the fins and the vertically-stacked SiNWs etching (Fig. 2(b)). For the fin formation, a Cl2 based plasma etching is used to obtain vertical sidewalls, whereas for the vertically-stacked SiNWs the etching consists of 3 cycles of passivation and etching steps, alternating low frequency pulses of C_4F_8 and SF_6 plasmas. The etching technique used for the stacked SiNW formation has been calibrated from the recipes previously described by the authors for the formation of vertically-stacked SiNWs in crystalline Si substrates [7]. Next, a 10 nm dry oxidation followed by a 100 nm LPCVD polysilicon deposition form the gate stack (see Fig. 2(c)). At the same time a low stress SiN nanostencil mask has been patterned with the gate design. The fabrication details of the nanostencil are described by the authors in a different publication [5]. In this work, the nanostencil is made of 100 nm thick LPCVD low stress Si_xN_y. The gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows. Then the nanostencil mask is aligned with a dedicated optical alignment tool and mechanically clamped with the device substrates. After loading the substrates with the nanostencil into a commercial e-beam evaporator, 40 nm Al are deposited, leaving an Al hard mask reproducing the gate design on top of the polysilicon layer (Fig. 2(d)). The Al mask gives better selectivity than SiO_2 hard maks for dry Si etching, thus enabling the patterning of higher aspect ratio structure. Hence, polysilicon gates are etched and Si_xN_y spacers are formed to provide good isolation barrier between the gate and the source/drain regions (Fig. 2(e)). This step is thus used to form pad areas for electrical characterization as well as polysilicon gates with lengths between 100 nm and 500 nm. Finally, a 30 nm thick Ni layer is deposited on the substrates, and a thermal annealing process at 400°C is utilized to form a stoichiometric 1:1 NiSi phase on top of the gates and to metallized source/drain regions. The unreacted Ni that was lying either on top of SiO_2 BOX layer or onto the spacers has been removed with a selective Piranha solution.

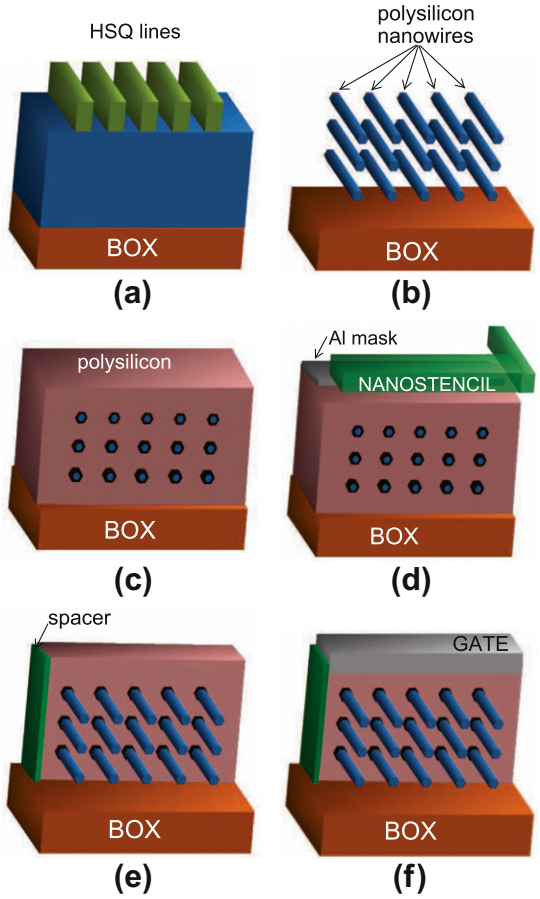


Fig. 2. Fabrication flow of the vertically-stacked GAA FETs. (a) HSQ lines are patterned with EBL. (b) A DRIE etching process is tuned to form 3 levels of stacked SiNWs. The nanowires are attached to polysilicon pillars at their extremes (not shown). (c) 10 nm dry oxide and 100 nm LPCVD polysilicon are deposited to form the gate stack. (d) A nanostencil mask is aligned and mechanically clamped with the substrate, serving as evaporation mask for Al deposition. The Al is then used as mask to pattern the gate.(e) After gate patterning a Si_xN_y spacer is formed on vertical sidewalls. (f) After Ni blanket deposition and a thermal annealing at 400°C, a Piranha wet etching is used to remove unreacted Ni from either BOX and spacer regions, thus forming self-aligned NiSi source/drain and gate areas.

Thanks to the self-alignment of the Si_xN_y spacers with the gates, self-aligned source/drain regions are formed and the devices are ready for electrical characterization.

3. Fabricated Devices

The fabricated devices included FETs or inverters designed with different number of channels, having either 1 to 11 parallel SiNWs for the finFETs. For the vertically-stacked SiNWs the same design is used, nevertheless, thanks to stacking 3 levels, the same devices have 3 to 33 parallel SiNW channels. Another difference among finFETs and vertically-stacked FETs is notably the gate structure, which are tri-gates and GAA, respectively. In Fig. 3, a finFET with 11 parallel SiNWs and tri-gate construction is shown. The SiNWs are interconnected every 500nm in order to improve the mechanical stiffness and so to avoid bending. In Fig. 4, a vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter and GAA construction is shown. In the inset, conformal coverage of 10nm thick SiO_2 dielectric and LPCVD polysilicon gate is shown.

In all substrates, the design included 150 FETs and 150 inverters, for which the fabrication yield has been checked. In Table 1 fabrication yields larger than 70% are reported, showing excellent reproducibility, considering the experimental nature of the

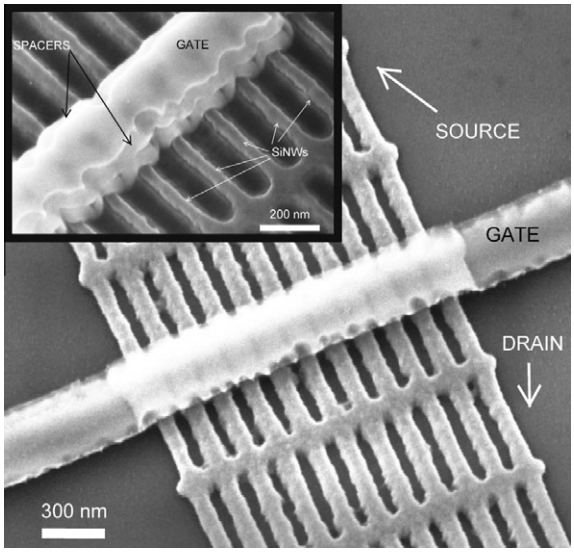


Fig. 3. Si nanowire FET with 11 channels with 50 nm times 50 nm channel cross-section, 350 nm long polysilicon gate. The nanowires are connected at regular intervals of 500nm in order to improve the stiffness of the structure. In the inset a magnified and tilted SEM view shows the nitride spacers and the SiNWs around the gate structure.

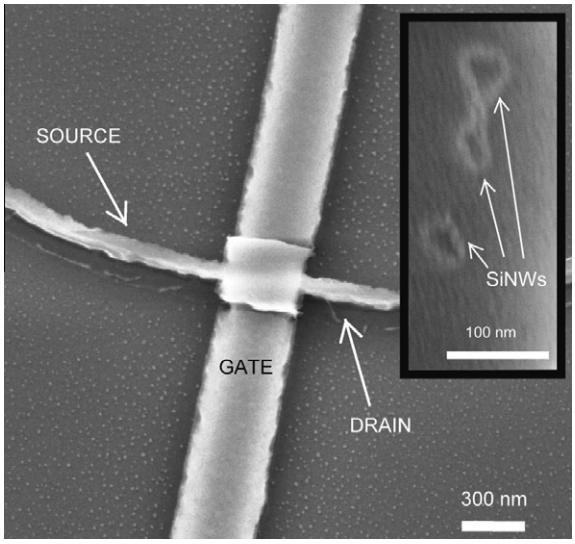


Fig. 4. Si nanowire FET with 3 vertically stacked single-stranded 30 nm diameter channels. In the inset, a Focused Ion Beam cross-section of the gate shows 3 SiNWs surrounded by 10 nm SiO_2 dielectric and 100 nm LPCVD polysilicon. Gate length is 350 nm.

process. Moreover, the failing sites have been observed the same for all the substrates, regardless of the process flow. This is the reason for the very similar yield reported for finFETs and vertically-stacked FETs. It is worth noticing that failing devices are mainly related with defects in the mask design, and that this aspect of the work has not been optimized. Thus, the main limitation on the fabrication yield is related with systematic errors in the design.

Table 1
Fabrication Yield measured for the 4 device types.

Yield	finFETs	vertically-stacked FETs
FETs	70%	70%
Inverters	85%	84%

For instance, one of the major fabrication issues is the mechanical stability of the nanostencil, whose robusteness is crucial for the correct patterning of the Al mask. If we consider the device subset of finFET inverters, the the larger yield of 85% is mainly attributed to the lower number of defective nanostencil patterns. Using a smaller size for the nanostencil, which would be a natural consequence when fabricating more scaled devices, improves stability and, at the same time, reduces the frequency of defective patterns. Hence, there is indication that fabrication yields larger than 85% with this process flow is possible with relatively little effort in the mask design.

4. Electrical Measurements

Electrical characterization is carried out with a manual probe station connected to a Agilent B1500 semiconductor parameter

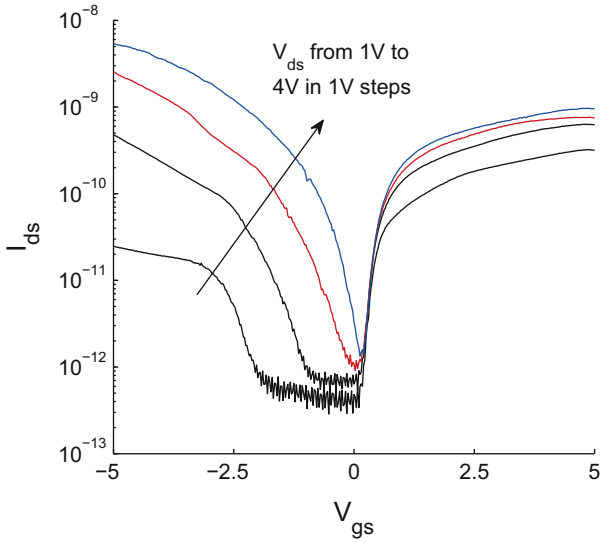


Fig. 5. $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 stacked channels. Measured minimum inverse subthreshold slopes for electrons (n-branch) and holes (p-branch) are $300mV/dec$ and $1300mV/dec$ at V_{ds}=4V.

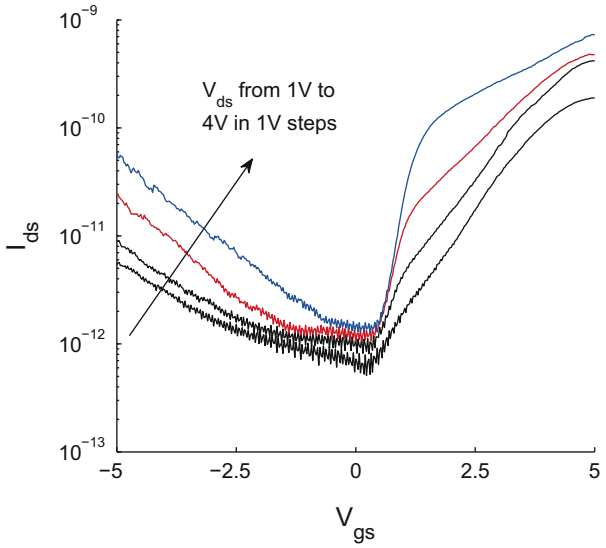


Fig. 6. $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 times 11 channels. Measured minimum inverse subthreshold slope for electrons is $350mV/dec$. Notice that the holes conduction is effectively suppressed due to the 3D nanowire mesh.

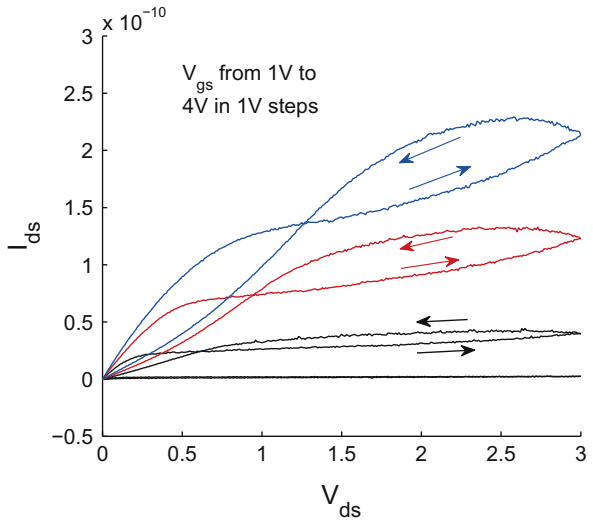


Fig. 7. $I_{ds} - V_{ds}$ memristive/hysteresis curve for vertically-stacked SiNW GAA FET with 3 stacked channels. The hysteresis lead to different saturation threshold due to the dynamics of charges with interface states at either the Shottky junctions or at the polysilicon grain boundaries.

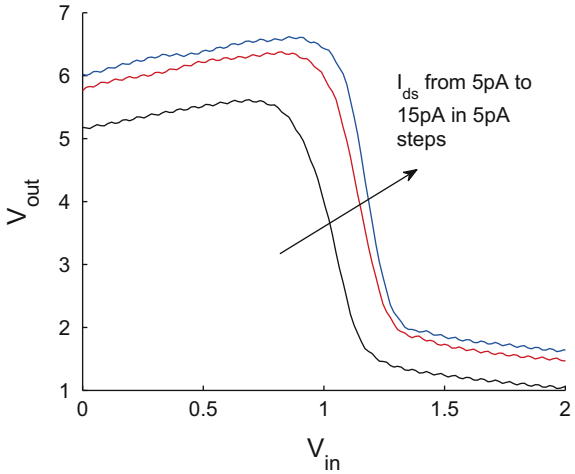


Fig. 8. Inverter operation obtained by biasing a FET with constant current. The $V_{out} - V_{in}$ characteristics switched from high to low V_{out} at $V_{in} \approx 1$ V.

analyzer. Tungsten tips are put in contact with the polysilicon source/drain pads and on the Al/polysilicon gate pad. Typical $I_{ds} - V_{gs}$ curves are first measured for finFETs which show large inverse subthreshold slopes of about $1500mV/dec$ and average $I_{ON} - I_{OFF}$ ratio of 3 orders of magnitude. These results are then compared with the electrical performance measured for the vertically-stacked GAA NW FETs. The $I_{ds} - V_{gs}$ curves (Fig. 5) for the vertically-stacked FETs with 3 stacked SiNWs show typical device ambipolarity with inverse subthreshold slopes for n- and p-branches up to $300mV/dec$ and up to $1300mV/dec$, respectively. Notice the strong dependence of the p-branch with applied V_{ds}. This undesired behavior is largely compensated for, in the devices with 3 times 11 parallel fingers, as shown in Fig. 6. The apparent robustness with respect to short channel effects is attributed to the different geometry of the 3D mesh with respect to the single stranded stacked SiNWs.

Another interesting result is the hysteresis observed for $I_{ds} - V_{ds}$ curves (see Fig. 7). The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward V_{ds} sweep is not identical to the same curve for backward V_{ds} sweep. This behavior can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [9]. More detailed explanation of the memristive electrical behavior can be found for similar, previously reported devices [8].

V_1 [V]	V_2 [V]	V_{out} [V]
0 (logic 0)	0 (logic 0)	$\approx$ 4 (logic 1)
0 (logic 0)	2 (logic 1)	$\approx$ 3 (logic 1)
2 (logic 1)	0 (logic 0)	$\approx$ 5 (logic 1)
2 (logic 1)	2 (logic 1)	$\approx$ 0.5 (logic 0)

Finally, inverter and logic NAND operation have been performed using a current biasing scheme. In Fig. 8, a current bias from 5 pA to 15 pA in 5 pA steps has been utilized. As shown in the graph, the inversion voltage saturates at $V_{in} \approx 1.2$V with a gain $\Delta V_{out} / \Delta V_{in} \approx 14$. Moreover, by using two vertically-stacked FETs in series connection, NAND functionality can be achieved by measuring the voltage drop across while sweeping the gate voltages of the two devices. With this method, typical NAND functionality is obtained, as shown in Table 1.

5. Conclusions

In conclusion, we demonstrated for the first time vertically-stacked Si nanowire FETs with polysilicon GAA having gate lengths down to 100 nm and yield larger than 70%. Moreover, the reported ambipolar behavior for vertically-stacked FETs achieves I_{ON}/I_{OFF} ratio up to 4 orders of magnitude and inverse subthreshold slopes (SS) up to $300mV/dec$, effectively improving the SS of $1500mV/dec$ obtained for finFETs. The method provide excellent step coverage on either finFETs and vertically-stacked SiNW FETs with strongly non-planar topography, thanks to the use of an Al etch mask deposited with nanostencil. The electrical behavior confirms the results obtained from similar devices fabricated with a standard lithography approach while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling. Finally, functional inverter and logic NAND operations are obtained, confirming the discussed fabrication flow as valuable tool to build logic circuits.

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Ambipolar Gate-Controllable SiNW FETs for Configurable Logic Circuits With Improved Expressive Capability

Davide Sacchetto, Yusuf Leblebici, and Giovanni De Micheli

***Abstract*—In this letter, we report on the fabrication and characterization of ambipolar silicon-nanowire (SiNW) field-effect transistors (FETs) with a double-independent-gate (DIG) structure for polarity control. Several structures are fabricated, showing the effectiveness of local back gate to enable switchable ambipolar functionality. Moreover, AND, NAND, NOR, XOR, and XNOR binary logic functions can be obtained with a single gate, depending on the encoding values used for the input signals. Repeatable behaviors of DIG SiNW FETs are considered as enablers for ambipolar-controlled logic, with all the benefits related to the maturity of the silicon technology.**

***Index Terms*—Ambipolar control, field-effect transistor (FET), nanowire, Schottky barrier.**

I. Introduction

THE CONTINUING pursuit for extending Moore's law to future device families also fuels the intensifying research on new device functionality for implementing next-generation circuits. New computational paradigms based on the control of alternative state variables [1] are being investigated along with novel structures, such as double-gate and gate-all-around nanowire devices [2], or new materials, such as higher κ dielectrics and metal gates, or different device concepts, such as modified Schottky-barrier field-effect transistors (FETs). Most of these paradigms require physics different from the physics of CMOS. For instance, computation has been demonstrated with devices based on the laws of photonics [3], spintronics [4], or nanoionics [5].

Nevertheless, alternative solutions that require a less dramatic impact on technological development would be preferable for practical applications. Regarding the different solutions, the ambipolar-controlled logic gates are among the most promising ones, owing to the higher expressive logic power due to the polarity control as state variable [6]. The polarity control can be achieved in ambipolar devices by using a double-independent-gate (DIG) structure. A few examples can be found for DIG FETs based on carbon nanotubes [7], [8], graphene [9], semiconducting polymers, and silicon nanowires (SiNWs) [10]. Nevertheless, very limited research has been done in terms of integrating ambipolar-controlled devices with CMOS-compatible top-down Si fabrication flow, which is crucial for large-scale system integration.

In this work, ambipolar SiNW FETs with a DIG structure enable the use of polarity control signals as a method toward Si circuits with increased logic expressive power. Moreover, the use of polarity control leads to improved performance in terms of $I_{\mathrm{ON}}-I_{\mathrm{OFF}}$ ratios and inverse subthreshold slopes with respect to the ambipolar behavior.

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Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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II. Device Description

The device consists of a 20-μm-long crystalline SiNW attached between two Si pillars on an SOI wafer [see Fig. 1(a)]. The SiNW is then covered by two independent n^{++} polysilicon gates with this scheme: a main central gate (gate 1) of 7.5-μm length and a second gate (gate 2) that is used to control the SiNW portions between the main gate and the source and drain regions, respectively.

A. Fabrication

First, a low-doping p-type ($N_A \approx 10^{15}$ atoms/cm^2) SOI wafer with a 1.5-μm device layer is spin coated. The photoresist is then patterned in 1.5-μm-wide lines [see Fig. 1(b)] and used as a mask for a next isotropic Si etching. A Si plasma etching recipe is tuned to form a triangular 75-nm-wide SiNW lying on top of the buried oxide layer [Fig. 1(c)]. Then, a 30-nm-thick gate oxide and a 150-nm polysilicon layer are deposited with low-pressure chemical vapor deposition (LPCVD) method to form a main gate with 7.5-μm length [gate 1 in Fig. 1(d)]. The main gate is then isolated by a 300-nm LPCVD low-temperature oxide (LTO). A second 500-nm polysilicon layer is then deposited. Then, a thick photoresist is spun over the wafer and planarized using a chemical mechanical polishing procedure similar to the one previously described by the authors in [11]. This method leaves a protective polymer layer that is used to etch a second polysilicon gate self-aligned within the cavity due to the topography [see gate 2 in Fig. 1(e)]. After standard cleaning steps, one additional patterning of gate 2

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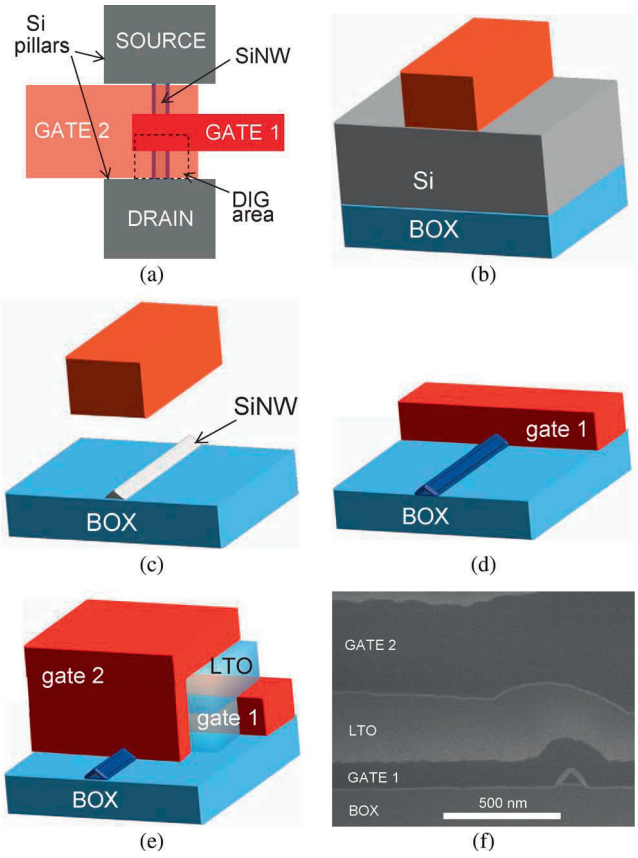


Fig. 1. Fabrication flow. (a) Top view of the dual-gate device. The next steps focus on the DIG area construction. (b) Photoresist mask is patterned. (c) After isotropic etching of Si, a triangular-shaped SiNW is formed. (d) Gate oxide and LPCVD polysilicon are deposited and patterned to form the main central gate stack. (e) LTO interpoly dielectric is deposited, and a second polysilicon gate is made self-aligned with the nanowire. (f) Focused ion beam cross section showing a triangular SiNW channel with two 75-nm sides and a 100-nm base. Gate 1, gate 2, and the LTO interpoly dielectric have 150-, 500-, and 300-nm thicknesses, respectively. The gate-1 dielectric is 30 nm thick.

is performed to remove the unnecessary polysilicon and to form areas for the contacts [see the top view of the device in Fig. 1(a)]. In Fig. 1(f), a focused ion beam cross section of the triangular SiNW channel with the DIG stack is shown. Then, source/drain contacts are formed by means of NiSi silicidation in a horizontal wall furnace in forming gas at 400 °C. Finally, Al metal lines and a pad area are defined for the electrical characterization.

B. Device Operation

The source/drain regions after NiSi silicidation have a midgap Schottky-barrier contact with the SiNW; thus, both electrons and holes can contribute to the current flow. The use of the two gates enables the selection of which carrier species shall prevail in the conduction. In the following discussions, the voltage applied to gate 1 is defined as $V_{\rm gs}$, while the voltage applied to gate 2 is defined as $V_{\rm bg}$. This scheme was proposed by Lin *et al.* [7] for the control of polarity of carbon-nanotube FETs. As shown in Fig. 2(a), a positive back-gate voltage $V_{\rm bg}$ enables electron flow, while the hole current is blocked. Similarly [Fig. 2(b)], a negative $V_{\rm bg}$ makes the opposite selection: The hole current is enabled while the electron flow is blocked.

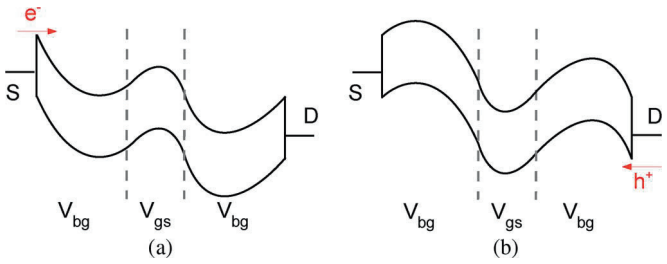


Fig. 2. (a) Conceptual band diagram for n-type operation. A positive $V_{\rm bg}$ is used to block the flow of holes from the drain. (b) Conceptual band diagram for p-type operation. A negative $V_{\rm bg}$ is used to block the flow of electrons from the source.

TABLE I
OBTAINED ELECTRICAL BEHAVIOR FOR DIFFERENT $V_{\rm bg}$ VOLTAGES

$V_{\rm bg}$[V]	$\frac{I^{h+}_{ON}}{I_{OFF}}$	$\frac{I^{e-}_{ON}}{I_{OFF}}$	SS^{h+}[mV/dec]	SS^{e-}[mv/dec]
+10	50	250	1000	600
+7.5	N/A	2000	N/A	250
+5	N/A	1000	N/A	250
+2.5	N/A	1000	N/A	325
0	1000	600	475	750
-2.5	1000	N/A	375	N/A
-5	5000	N/A	250	N/A
-7.5	10000	N/A	300	N/A
-10	30000	N/A	300	N/A

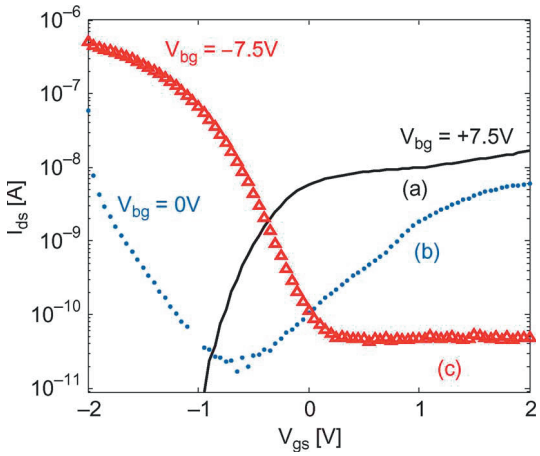


Fig. 3. Controlled ambipolar $I_{\rm ds}$–$V_{\rm gs}$ characteristics at different $V_{\rm bg}$ back-gate voltages. (a) Positive $V_{\rm bg} = +7.5$ V is used to obtain an n-type characteristic. (b) $V_{\rm bg} = 0$ V gives ambipolar $I_{\rm ds}$–$V_{\rm gs}$. (c) Negative $V_{\rm bg} = -7.5$ V is used to obtain a p-type characteristic.

III. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer in dark at room temperature. In Table I, the effect of $V_{\rm bg}$ on the inverse subthreshold slopes (SS^{h+} and SS^{e-}) for hole and electron conduction branches depicts a trend for improved SS^{h+} and SS^{e-} when increasing $V_{\rm bg}$ voltages of negative and positive polarities are applied, respectively. Similarly, improved $I_{\rm ON}-I_{\rm OFF}$ ratios ($I^{h+}_{\rm ON}/I_{\rm OFF}$ and $I^{e-}_{\rm ON}/I_{\rm OFF}$) are observed when larger $V_{\rm bg}$ voltages are applied. The improved performance is related to a reduced $I_{\rm OFF}$ current due to the screening of one of the two types of carriers for the conduction. As better shown in Fig. 3, positive or negative $V_{\rm bg}$ voltages can be used to obtain n-type or p-type

TABLE II
BINARY LOGIC VOLTAGE SIGNALS CODING FOR XOR, NAND, AND, AND NOR OPERATIONS

CODE	XOR		NAND		AND		NOR	
	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]
logic 0	+1	-7.5	-0.5	+7.5	0	0	0	+7.5
logic 1	-1	+7.5	+1	-7.5	-1	-7.5	-1	0

TABLE III
OUTPUT CURRENT LEVELS FOR THE FOUR LOGIC OPERATIONS: XOR, NAND, AND, AND NOR

logic values		XOR	NAND	AND	NOR
gate 1	gate 2	I_{OUT}[A]	I_{OUT}[A]	I_{OUT}[A]	I_{OUT}[A]
0	0	$4 \cdot 10^{-11}$	$2 \cdot 10^{-9}$	10^{-10}	$6 \cdot 10^{-9}$
0	1	10^{-8}	$2 \cdot 10^{-9}$	10^{-10}	10^{-10}
1	0	$7 \cdot 10^{-8}$	10^{-8}	10^{-11}	10^{-11}
1	1	10^{-11}	$4 \cdot 10^{-11}$	10^{-7}	$5 \cdot 10^{-11}$

I_{ds}–V_{gs}. Moreover, a symmetrical ambipolar I_{ds}–V_{gs} is obtained for $V_{bg} = 0$ V. This functionality allows for increased expressive logic power with a single FET. For instance, the two voltage signals V_{gs} and V_{bg} can be coded to make logic XOR operation with the device in Fig. 3, an operation that would require more transistors in standard CMOS technology. In Table II, V_{gs} and V_{bg} voltage values are encoded into logic levels 0 and 1 to map into four binary logic operations, namely, XOR, NAND, AND, and NOR, while using the data plot in Fig. 3. The results of the logic operations are summarized in Table III. Logic 0 and logic 1 outputs are represented by light and dark gray, respectively. Another solution that can be envisaged can use the same logic levels for both gates in order to save space for external encoding circuits. This solution will become the most desirable one by optimizing the thickness of the two gate dielectrics, which, in the current implementation, leads to a more effective electric field density for gate 1 than for gate 2. In future designs, this technological issue might be overcome by optimizing the dielectric thickness for the two gates and/or in combination with dopant segregation techniques to balance the Schottky-barrier heights for holes and electrons. Moreover, gate work-function engineering can be used to code the threshold voltage of the device, thus addressing the different logic 0/1 voltages needed for a specific logic function. Owing to these technological options, dense arrays of ambipolar DIG FETs can be envisaged as basic building blocks to map complex logic circuits. The ac characteristic of the proposed device concerning delay and power will depend, among other factors, on the capacitive coupling between the two gate electrodes. However, this parasitic coupling is estimated to be of the same order of magnitude of the source/drain-to-gate capacitance, and given the fact that the fabricated device performs a more expressive logic functionality, this additional coupling is not expected to be a limiting factor.

IV. CONCLUSION

In this study, a new device structure exploiting a DIG configuration with SiNW and top-down fabrication flow has been demonstrated as a useful building block for ambipolar-controlled logic operation. All the I_{ds}–V_{gs} characteristics, defining n-type, p-type, and ambipolar behavior, have been obtained with good $I_{ON}-I_{OFF}$ ratios of up to four orders of magnitude and with inverse subthreshold slopes close to those of state-of-the-art Schottky-barrier FETs. In addition, a single device can be used to perform any of the XOR, XNOR, NAND, AND, and NOR binary logic operations depending on the input signals encoding. The proposed integration scheme is envisaged for logic circuits exploiting the improved logic expressive power of ambipolar-controlled SiNW devices, which is enabled by the reliability of Si fabrication technology.

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New Insight on Bio-sensing by Nano-fabricated Memristors

Davide Sacchetto · Marie-Agnès Doucey · Giovanni De Micheli · Yusuf Leblebici · Sandro Carrara

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Abstract We report here on a new insight for bio-sensing based on the memristive effect of functionalized Schottky-barrier memristive silicon nanowire in dry environment. The device concept is discussed. Electrical measurements confirm the bio-detection by the narrowing of the memristive $I_{ds} - V_{ds}$ hysteresis upon interaction of antigen with antibody-functionalized nanowire.

Keywords Memristive · Ambipolar · Sensor · FET · Schottky barrier · Antibody · Antigen interaction

1 Introduction

Recently, there has been an increasing interest in nano-bio-sensing applications, due to possibility for minimal invasive, real-time monitoring for preventive treatments and therapy personalization [1]. In particular, one-dimensional silicon nanowires are good candidates for sensing devices due to their very large surface-to-volume ratio and quantum properties [2]. However, the sensing with nanowires is only exploited by the ion-sensitive field-effect-transistor paradigm [3]. Due to the nano-scale of the fabricated geometries [4], the recent discovery in solid-state devices of the memristive effect has been source of renewed research efforts in applications for high-density memory device [5]. The physical phenomena governing the memristive behavior are attributed to the change of an internal state variable, which modifies the conductance in a non-volatile manner [6]. As reported by Duan et al., memory devices are possible also with molecule-gated nanowire transistors by using redox active molecules [7]. In this short communication, we report the first evidence of unexpected new insights for a novel molecular sensing in dry conditions based on nanofabricated memristors functionalized with bio-molecular thin films. In Section 2, we describe the nano-fabrication of memristive Schottky-barrier silicon nanowires.

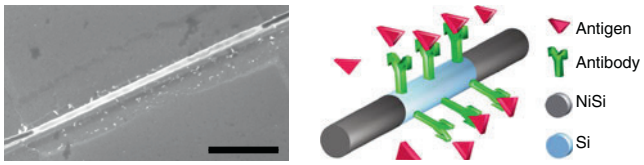
2 Device Nano-fabrication

The fabrication method utilizes some of the steps that were previously reported [8] for memristive Schottky-barrier silicon nanowire field-effect transistors. The process starts from low resistivity silicon-on-insulator substrates, with 1.5 μm device layer and 3 μm SiO_2 insulating layer. After standard lithography, the silicon nanowire is carved anchored at the top of two silicon pillars. Then, Ni is deposited on top of the pillars with overlap on the outer portions of the silicon nanowire. Hence, an annealing step at 450°C in a horizontal wall furnace forms NiSi contacts. Figure 1 shows a nano-fabricated memristive silicon nanowire with NiSi contacts.

3 Biomolecule Self-assembly

The silicon nanowire surface was derivatized with 3-glycidoxypropyltrimethoxysilane [9] and functionalized

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(a) (b)

Fig. 1 **a** Suspended functionalized silicon nanowire with NiSi extremities. *Scale bar* is 4 μm. **b** Concept model

by covalent attachment of anti-rabbit polyclonal antibodies (AB) [10]. Antigen (rabbit antibodies, AG) interact with the functionalized wire as depicted in Fig. 1b.

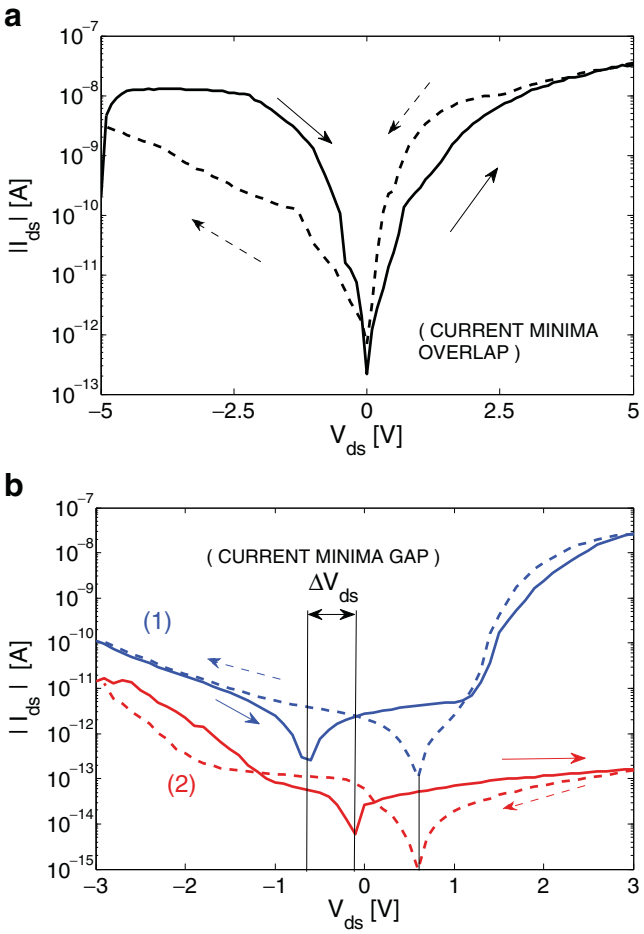


Fig. 2 $I_{ds} - V_{ds}$ curves: **a** before functionalization with AB biolayer. A typical memristive hysteresis is observed, with no ΔV_{ds} gap between I_{ds} minima in forward and backward regimes; **b** the *blue curve* (*1*) is measured after drying the sample from deionized water. The *red curve* (*2*) is measured after dipping in 5 pM AG solution and drying

4 Results and Discussion

Electrical measurements are carried out in a shielded probe station connected with HP4156C Semiconductor Parameter Analyzer and in dark, to avoid any photogenerated currents. Before functionalization with the AB layer, $I_{ds} - V_{ds}$ curves taken for forward and backward sweep do show a typical memristive behavior (see Fig. 2a), where the current minima always occur for $V_{ds} = 0\,V$, consistently with previously reported measurements [8] on non-functionalized devices. Conversely, functionalized silicon nanowires show different positions of the current minima for backward or forward regimes. This effect is observed after drying from (a) de-ionized H_2O solution and (b) 5 pM AG solution. The $I_{ds} - V_{ds}$ curve before AG up-take shows an hysteresis (curve 1 in Fig. 2b) due to charge trapping mechanisms at the Schottky junctions. The binding of an AG with the functionalized wire is responsible for a modification of the hysteresis (curve 2 in Fig. 2b), in particular to a reduction of the current minimum gap between forward and backward V_{ds} sweeps. Coherently, the up-take of increasing amounts of AG (in the pM range) results on a further diminishing of this gap.

5 Conclusions

We have demonstrated a new type of bio-sensing method, which is based on the memristive effect in Schottky-barrier silicon nanowires. This completely novel memristive detection principle is able to sense low concentrations of bio-molecules, due to interactions occurring at the nanoscale between the molecular charges trapped by the bio-layer at the surface of the wire and the ambipolar carriers supporting the memristive conductivity into the wire.

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Research Letters

Resistive Programmable Through-Silicon Vias for Reconfigurable 3-D Fabrics

Davide Sacchetto, Michael Zervas, Yuksel Temiz, Giovanni De Micheli, and Yusuf Leblebici

***Abstract*—In this letter, we report on the fabrication and characterization of titanium dioxide (TiO_2)-based resistive RAM (ReRAM) cointegration with 380 μm-height Cu through-silicon via (TSV) arrays for programmable 3-D interconnects. Nonvolatile resistive switching of $Pt/TiO_2/Pt$ thin films is first characterized with a resistance ratio up to five orders of magnitude. Then, cointegration of $Pt/TiO_2/Pt$ or Pt/TiO_2 memory cells on 140 and 60 μm diameter Cu TSVs is fabricated. Repeatable nonvolatile bipolar switching of the ReRAM cells is demonstrated for different structures.**

***Index Terms*—Memristive systems, memristor, resistive RAM (ReRAM), titanium dioxide (TiO_2), through-silicon via (TSV), 3-D integration.**

I. Introduction

THE KEY reason of the historical CMOS success lies with the exponential increase of device density that the silicon industry kept true for more than 40 years while reducing the unit cost of ICs. Recently, the pace of scaling has slowed down due to approaching fundamental limits at the device level. On one hand, researchers are striving to obtain more performant circuits by focusing on improvement of the Front-End-of-the-Line technology, for instance, innovating materials, device structures, and introducing novel state variables [1] for computation. On the other hand, the Back-End-of-the-Line technology is also addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in 3-D wafer/chip stacking solutions utilizing through-silicon vias (TSVs) [1], as well as in reconfigurable interconnect fabrics.

Considering new device technologies, the recent realization of Stanley Williams' memristor [2] [also classified as resistive RAM (ReRAM)] based on metal–insulator–metal structures, gave new push to solid-state research for logic and memory applications that can be implemented into the Back-End-of-the-Line technology. For instance, ultradense crossbar memristive memory arrays can be made thanks to the compactness of the two-terminal junction [3]. The physical realization of the memristor, whose behavior was postulated by Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6].

In this letter, the authors demonstrate the cointegration of TSVs with ReRAM stacks, offering a new path for reprogrammable 3-D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3-D chip interconnects.

II. Fabrication

A. Planar ReRAM Devices

First, high resistivity p-type ($N_A \approx 10^{15}$ atoms/cm^2) bulk-Si wafers are prepared by 500 nm thermal oxidation in H_2O atmosphere. Then, the deposition of the resistive switching materials is performed by sputtering of $Pt/TiO_2/Pt$ layers with $270/80/270$ nm thicknesses, respectively. A conceptual picture is shown in Fig. 1(a). The top electrode area of $100\,\mu m \times 100\,\mu m$ were patterned by standard lithography and etched by the ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

B. TSV Devices

The resistive switching materials were integrated with TSVs producing two different devices.

1) 140 μm TSV diameter in 380-μm thick wafer, using the $Pt/TiO_2/Pt$ memory stack.
2) 60 μm TSV diameter in 380-μm thick wafer, using the $Cu/TiO_2/Pt$ memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

The TSVs are fabricated using the same process in both the cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through-wafer etch, RCA wafer cleaning, and thermal oxidation in water atmosphere to grow a 3-μm thick oxide. A 750-nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step, the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

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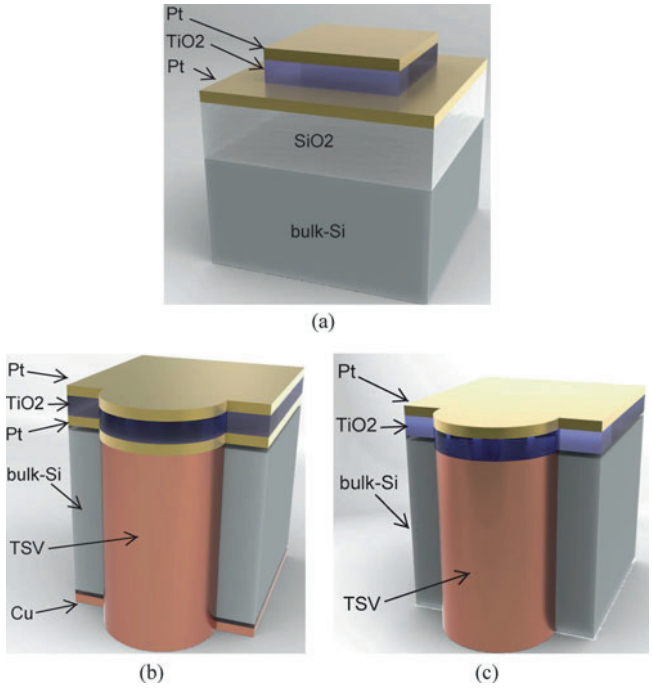


Fig. 1. (a) Concept image of planar ReRAM made of the $\mathrm{Pt/TiO_2/Pt}$ stack. (b) Concept image of the ReRAM–TSV using the $\mathrm{Pt/TiO_2/Pt}$ programmable fuse. (c) Concept image of the ReRAM–TSV using the $\mathrm{Cu/TiO_2/Pt}$ programmable fuse.

1) TSV With $\mathrm{Pt/TiO_2/Pt}$ *ReRAM:* For the first type of devices, once the TSVs are fabricated, the front side of the wafer is processed with the chemical mechanical polishing (CMP) technique to form a flat surface. The $\mathrm{Pt/TiO_2/Pt}$ stack is sputtered with layer thicknesses $270/80/270\,\mathrm{nm}$, accordingly. A concept picture of the fabricated structure can be seen in Fig. 1(b).

2) TSV With Cu/$\mathrm{TiO_2}$/Pt *ReRAM:* For the second type of devices, the wafer is polished using the CMP technique on both sides to remove the seed layer and to planarize the surfaces. Cu was, then, cleaned using an $\mathrm{NH_4 : H_2SO_4}$ etching solution at room temperature for 10 min. Then, the wafer was loaded into a vacuumed sputtering chamber and a $\mathrm{TiO_2/Pt}$ layer was deposited with thicknesses of 80 and $270\,\mathrm{nm}$, respectively. Cu of the TSV is acting as the bottom electrode of the ReRAM [see Fig. 1(c)]. Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Fig. 2(a) and (b), respectively.

III. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station under dark conditions. For electrical contacts, standard tungsten needles with $15\,\mu\mathrm{m}$ apex diameter were placed on the top electrode area very softly, since the dependence of the switching on needle pressure has been observed, similarly to the observation of local pressure-modulated conductance with atomic force microscopy tips [7]. Then, double *I–V* dc sweeps have been used to investigate the resistive switching behavior. In all the cases, the bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table I.

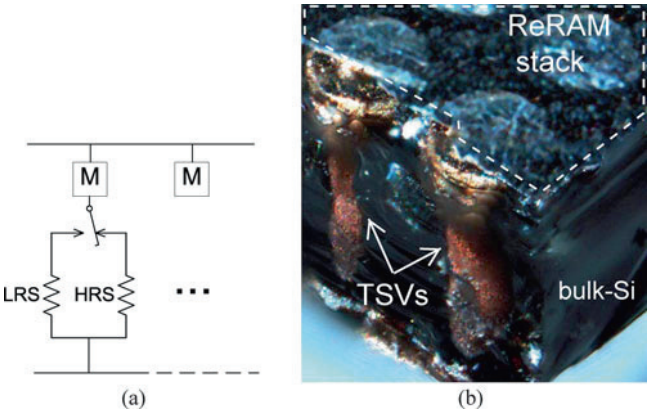


Fig. 2. (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element *M*). (b) Reconstructed 3-D photograph of the $\mathrm{TSV–Cu/TiO_2/Pt}$ device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

A. Planar ReRAM Devices

First, the planar $\mathrm{Pt/TiO_2/Pt}$ devices are characterized and it showed stable and repeatable bipolar switching behavior between $10\,\Omega$ and $1\,\mathrm{M}\Omega$ read or measured at $+1\,\mathrm{V}$ (see Fig. 3). Originally, the devices are in the high-resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low-resistance state (LRS) occurs at $+1.8\,\mathrm{V}$. After the SET event, the voltage sweep continues until $+2\,\mathrm{V}$ and, then, move back toward the negative-voltage region. When $-1.3\,\mathrm{V}$ is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about five orders of magnitude is read at $+0.5\,\mathrm{V}$.

B. TSV–$\mathrm{Pt/TiO_2/Pt}$ Devices

Next, $\mathrm{TSV–Pt/TiO_2/Pt}$ devices with the same layer thicknesses are measured, showing resistance switching below $\pm 1\,\mathrm{V}$ (see Fig. 4). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks, as well as to surface states acting as dopants for the $\mathrm{TiO_2}$ [8]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only $+0.6\,\mathrm{V}$, while the RESET voltage is measured at $-0.5\,\mathrm{V}$. Using a reading voltage of $+0.2\,\mathrm{V}$, an HRS of $2\,\mathrm{M}\Omega$ and LRS of $666\,\Omega$, with the resistance ratio of 3000 are measured.

C. TSV–$\mathrm{Cu/TiO_2/Pt}$ Devices

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the

TABLE I
OBTAINED RERAM ELECTRICAL PARAMETERS FOR DIFFERENT DEVICES

Device	SET	RESET	HRS	LRS	HRS/LRS	Reading
Planar $Pt/TiO_2/Pt$	$+1.8$ V	-1.3 V	10 MΩ	10 Ω	10^5	$+1$ V
TSV $-$ $Pt/TiO_2/Pt$	$+0.6$ V	-0.5 V	2 MΩ	666 Ω	3003	$+0.2$ V
TSV $-$ $Cu/TiO_2/Pt$	-4.2 V	$+5$ V	500 MΩ	5 Ω	10^5	$+1$ V

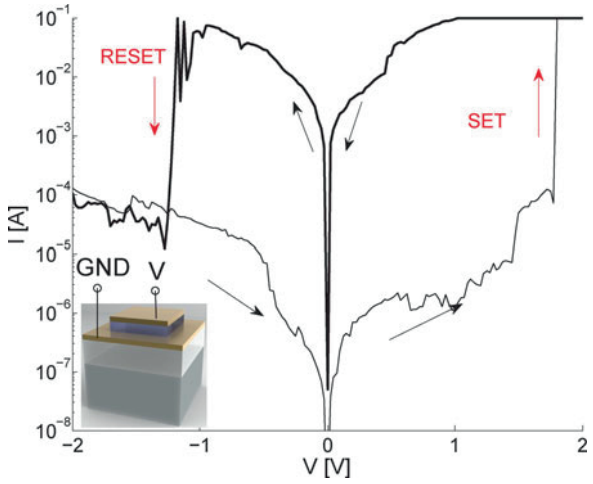


Fig. 3. Resistive switching through *I–V* sweeps for planar $Pt/TiO_2/Pt$ devices.

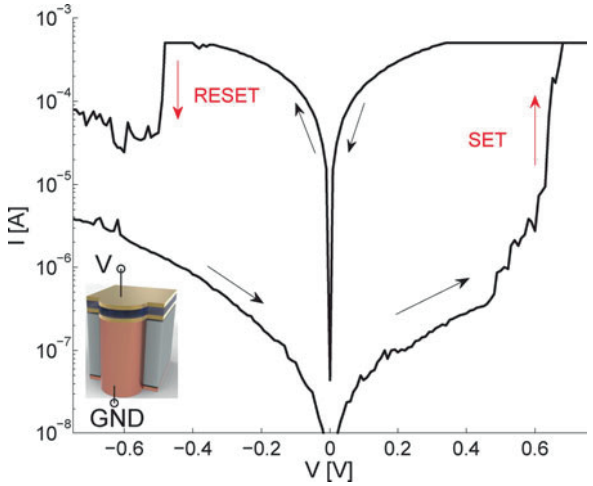


Fig. 4. Resistive switching through *I–V* sweeps using the TSV–$Pt/TiO_2/Pt$ programmable fuse.

TiO_2 layer [9], [10], which is an n-type semiconductor, an alternative device is obtained by depositing TiO_2 and Pt directly on top of the Cu–TSV. Thus, thanks to a larger Schottky barrier height at the Cu–TiO_2 interface, a larger programming window is obtained (see Fig. 5). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. An HRS of 500 MΩ and LRS of 5 kΩ are read at $+1$ V.

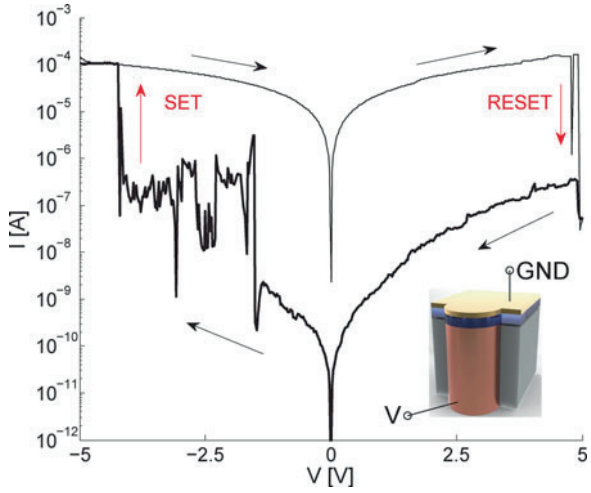


Fig. 5. Resistive switching through *I–V* sweeps using the TSV–$Cu/TiO_2/Pt$ programmable fuse.

IV. CONCLUSION

In this study, $Pt/TiO_2/Pt$ obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with the LRS to HRS resistance ratio up to five orders of magnitude. The device is successfully integrated on top of 140 and 60 μm TSV arrays either in the full $Pt/TiO_2/Pt$ stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The cointegration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3-D chip interconnects.

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INVITED PAPER

Multiterminal Memristive Nanowire Devices for Logic and Memory Applications: A Review

The authors of this paper introduce multiterminal memristive nanowire devices in memory applications.

By Davide Sacchetto, Giovanni De Micheli, *Fellow IEEE*, and Yusuf Leblebici, *Fellow IEEE*

ABSTRACT | Memristive devices have the potential for a complete renewal of the electron devices landscape, including memory, logic, and sensing applications. This is especially true when considering that the memristive functionality is not limited to two-terminal devices, whose practical realization has been demonstrated within a broad range of different technologies. For electron devices, the memristive functionality can be generally attributed to a material state modification, whose dynamics can be engineered to target a specific application. In this review paper, we show that trap charging dynamics can explain some of the memristive effects previously reported for Schottky-barrier field-effect Si nanowire transistors (SB SiNW FETs). Moreover, the SB SiNW FETs do show additional memristive functionality due to trap charging at the metal/semiconductor surface. The combination of these two memristive effects into multiterminal metal–oxide–semiconductor field-effect transistor (MOSFET) devices gives rise to new opportunities for both memory and logic applications as well as new sensors based on the physical mechanism that originate memristance. In the special case of four-terminal memristive Si nanowire devices, which are presented for the first time in this paper, enhanced functionality is demonstrated. Finally, the multiterminal memristive devices presented here have the potential of a very high integration density, and they are suitable for hybrid complementary metal–oxide–semiconductor (CMOS) cofabrication with a CMOS-compatible process.

KEYWORDS | Ambipolar; memristor; nanowire; Schottky barrier; transistor

I. INTRODUCTION

The main source of the complementary metal–oxide–semiconductor (CMOS) success lies in the exponential increase of device density that the silicon industry kept true for more than 40 years reducing the unit cost of integrated circuits. Recently, the pace of scaling has been slowed down due to approaching fundamental limits at the device level. While the paradigm of scaling is still alive, researchers are striving to follow Moore's law by focusing on new materials, new device structures, and new state variables. The basic building block for circuits has always been the four-terminal planar transistor but new versions of the metal–oxide–semiconductor field-effect transistor (MOSFET) structure such as the double-gate FET, the FinFET, the gate-all-around nanowire FET can be found in commercial products.

Due to the natural limitations of materials, future deeply scaled circuits will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages an end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. A long list of fundamental state variables other than charge includes the spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states [1]. Technologies using new state variables would have to be implemented within a completely new technological

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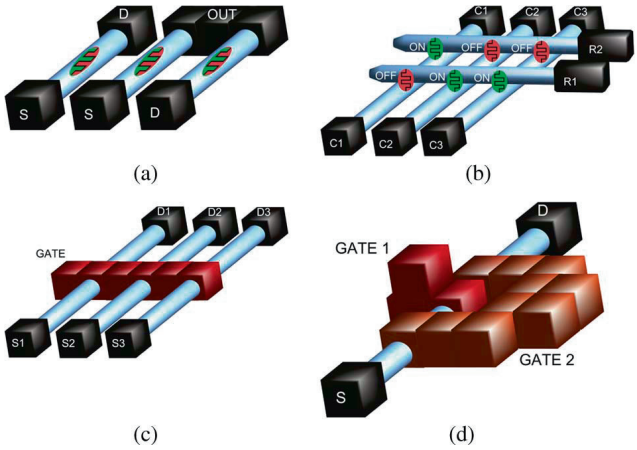


Fig. 1. ***(a) Parallel nanowire two-terminal memristive devices. (b) Crossbar array consisting of memristive cross points (two terminal). (c) Gate controlled three-terminal nanowire memristive device. (d) Double-gate four-terminal nanowire memristive devices.***

platform, and cannot be seen as CMOS-compatible alternatives.

The recent realization of devices by Strukov *et al.* [2] gave new push to solid state research for logic and memory applications. For instance, ultradense crossbar memristive memory arrays can be made thanks to the compactness of the two-terminal junction. Complementary logic based on two-terminal memristive devices [see Fig. 1(a)] or ultradense crossbar arrays with memristive cross points [see Fig. 1(b)] can dramatically improve device density up to 10^{11} b/cm^2 [3]. Moreover, the use of memristive effects as new state variables for computation can be exploited to build new types of functional devices with three or four terminals [see Fig. 1(c) and (d), respectively].

The physical realization of the memristor, whose behavior was postulated by Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6]. It is worth noting that a generalized model for memristive systems can be implemented under direct current (dc), small signal, and sinusoidal excitation [5]. The implications of such modeling are linked with the observation of memristive functionalities over a broad range of technologies based on nanoelectronics and nanoionics behaviors.

In this paper, a short review (see [7] and [8] for a more complete list) of two-terminal memristive devices is reported, while more space is given to multiterminal memristive devices that for their nature are readily implementable with front-end CMOS processes. Particular emphasis is given to devices based on the *gate-all-around (GAA) Schottky-barrier field-effect transistor (SB FET)* concept with *Si nanowire (SiNW)* channels on bulk-Si or silicon-on-insulator (SOI) wafers. The new concept of four-terminal memristive devices is presented in this paper for the first time and enhanced functionality is demonstrated. The coexistence of memristive functionality at both gate and drain electrodes with ambipolar conductance make these devices unique and capable of very high expressive power. The electrical characteristics can be attributed to the coexistence of different physical phenomena, such as device ambipolarity (both holes and electrons are responsible for conduction), Schottky barrier modulation induced by interface trap charging, and charge trapping at the gate oxide interface. It is highlighted that the unique properties of the emerging nanowire devices combine memristive functionality with ambipolar conductance, thus giving rise to novel conductance properties. We confirm some of these statements with previously reported *poly-crystalline Si nanowires (poly-SiNWs)* [9], which show a similar memristive behavior.

The memristive functionality is not a unique property of two-terminal passive devices but mainly a memory effect related to internal state variable changes. For instance, the memristive functionality can also arise from a delayed switching response of a Zener diode [10]. In the next sections, we review some of the two-terminal passive devices that can be modeled as memristive. The memristive functionality is seen as arising from different physical mechanism for different device classes. Thus, three- and four-terminal devices that show memristive functionality can be used for electrical control signals (either voltage or current). It is important to remember that a device showing a "pure" flux-charge relationship has not been found yet. Conversely, internal state variables can provide a stimulus response that can be modeled as memristive, thus adding more degrees of freedom for circuits designers.

This review paper is organized as follows. In Section II, two-terminal memristive devices are quickly surveyed. Then, in Section III, the electrical behavior of three-terminal memristive devices is discussed. Section IV will discuss on various fabrication methods for Si nanowire memristive devices. Hence, four-terminal memristive devices based on Si nanowires are discussed in Section V. Finally, possible applications for multiterminal memristive devices are discussed in Section VI.

II. TWO-TERMINAL MEMRISTIVE DEVICES

Two-terminal memristive devices can be based on metal/oxide switches, such as for SiO_2, HfO_2 [11], CuO [12], NiO [13], ZnO [14], Al_2O_3 [15], VO_2 [16], and $SrTiO_3$ [17]. These devices behave as solid-state electrochemical switches, whose resistance is defined by a metallic filament formation mechanism related to the solid-state redox reactions stimulated by the polarity of the applied electric field [18]. One example is the CuO-based ReRAM of Dong *et al.* [12] that shows repeatable resistive switching at very low voltages.

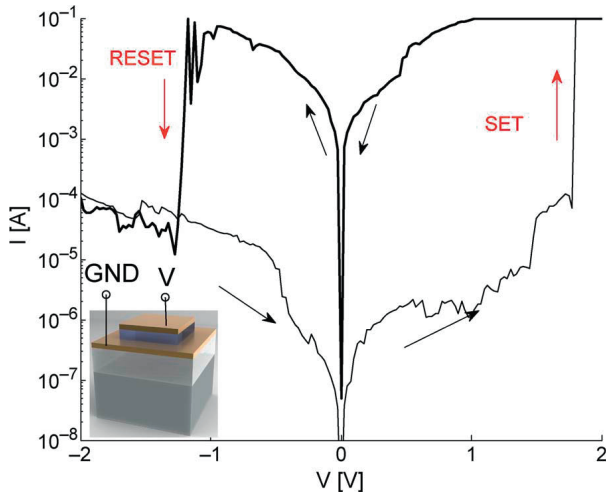


Fig. 2. *Resistive switching through I-V sweeps for planar Pt/TiO_2/Pt [21]. The inset shows the Pt/TiO_2/Pt ReRAM sandwich layer on top of an insulated substate with the two-terminal electrical contacts.*

The well-known TiO_2-based ReRAM [19], [20] seems to be based on a different mechanism, which is attributed to the vacancy/dopant diffusion in the oxide layer. The redistribution of oxygen vacancies into the TiO_2 depends on the polarity of the applied voltage, and it causes the switching between a semiconductor state into a metallic one. Typical ReRAM functionality of the TiO_2-based ReRAM is shown in Fig. 2 [21].

Another type of two-terminal memristive device is the phase change (PC) RAM [22]. The main switching mechanism is based on phase transition between an amorphous and a crystalline type due to Joule heating effects controlled by a voltage pulse. For instance, Si nanowires can be engineered such that melting and solidification processes can be iterated, thus giving rise to alternate restates [23].

Another class is based on polymers [24]. Several memristive switches can be built by interposing a biomolecule layer with properties ranging from molecule-dependent switching, such as rotaxanes [3], or more in general on interlocked molecules [25] but also on molecule-independent switching, where a filament formation mechanism through the molecular layer is involved [26].

A fifth class belongs to spintronics [27]. The spin-transfer-induced domain wall motion in a spin valve structure is by nature a memristive effect and is confirmed by some recently published results [28]. Moreover, Pershin *et al.* demonstrated that electron-spin polarization controlled by the external voltage applied to a spintronic device acts as a state variable that can be modeled as memristance [29].

In all these devices the amplitude and frequency of the input signal contribute in the formation of a so-called pinched hysteresis loop, whose salient feature is its zero crossing property [5], which is critical for ultralow power operation.

III. THREE-TERMINAL MEMRISTIVE DEVICES

The new concept of three-terminal memristive device is presented in terms of memristive functionality for logic and memory applications.

Examples of three-terminal memristive devices are the electrochemical organic memristor [31], the solid-electrolyte nanometer switch [32], the ferroelectric FET [33], and the ambipolar Si nanowire Schottky barrier FET [9], [34].

A classification of three-terminal memristive devices can be based from the general concept of the FET structure [see Fig. 3(a)] in which memristive functionality can be inserted either by engineering the gate dielectric or by gating a memristive channel. For instance, trap charging dielectric layers inserted between the channel and the gate fall into the category of FET with capacitive memory storage [Fig. 3(b)]. Examples of devices falling into this category can be the flash memory for which the trap charging into the gate dielectric influences the transconductance state of the channel. Thus, a first category that exploits the operation of writing/erasing cycles into the gate dielectric will be a generalization of the flash memory concept, for which volatility of the charges that are injected into the trap charging layer can be tuned accordingly to a desired frequency response.

A second category is the one of the gated memristor [Fig. 3(c)]. A few examples are the electrochemical organic memristor [31], the biomemristive nanowire [30], and the solid-electrolyte nanometer switch [32]. In the electrochemical organic memristor, the gate potential is represented by the potential of the bath, which is used to transfer positively charged Rb^+ ions into a polyaniline

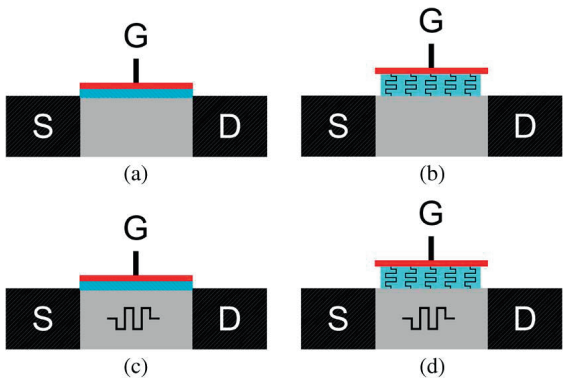


Fig. 3. *Categorization of FETs with memristive functionalities: (a) Conventional FET. (b) FET with memristive gate dielectric. (c) Gated memristor (memristive channel). (d) Gated memristor with memristive dielectric.*

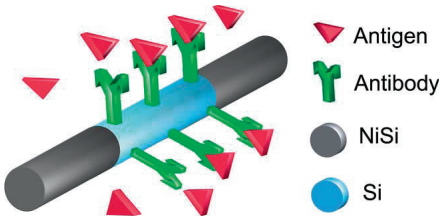


Fig. 4. *Suspended functionalized Si nanowire with NiSi extremities. The functionalized layer is capable of trapping antigen molecules which in turn affects the memristive hysteresis behavior, giving a new method for biosensing [30].*

(PANI) layer. The conductivity change can be iterated by switching the polarity of the bath potential, thus giving rise to a unipolar I_{ds}–V_{ds} curve that can be modeled as a memristor. In this case, the device can be set into either memristive or diode functionality. Similarly, a novel method for biosensing that has been recently proposed exploits the memristive effect to detect low concentration of biomolecules [30]. The device consisting of a NiSi/Si/NiSi nanowire structure coated with antibody layer (see Fig. 4) shows memristive behavior. The hysteresis loop of this device has been demonstrated for detection of low concentrations of biomolecules (antigen) in a dry environment (see Fig. 5). Conversely, the three-terminal solid-state electrolyte nanometer switch shows a typical bistable resistance state but using 100 times less current than standard two terminal operation [35]. This device is based on controlling the filament formation mechanism using the voltage of a gate terminal.

The ambipolar SB FET with SiNW channel reported in [36] [see Fig. 3(d)] falls in both categories of gated memristor and trap charging dielectric, as it shows dynamic trap charging mechanisms at the Schottky junctions and in the gate dielectric insulator. The result depicted in Fig. 6 shows a hysteretic behavior that is reminiscent of a two-terminal monolithic memristive device [37]. The hysteresis reflects the fact that the I_{ds}–V_{ds} curve for forward V_{ds} sweep is not identical to the same curve for backwards V_{ds} sweep. It can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [38]. First, two-terminal measurements are performed. The drain/source current I_{ds} is measured versus the drain/source voltage V_{ds} at constant $V_{gs} = 5$ V. The device is equivalent to two back-to-back Schottky diodes. The two diodes operate in opposite regimes: for negative V_{ds}, the source-to-channel diode is reversely biased while the drain-to-channel diode is forward biased. For positive V_{ds} both diodes invert their respective bias conditions. In either case, I_{ds} is limited by the current flowing in the reverse-biased diode. The reverse current of a metal/insulator/semiconductor diode has been observed to be very sensitive to charge trapping at the metal/semiconductor interface [15]. The large current value in the range of mA is most likely due to the large parallel parasitic structure in the bulk. In an ideal Schottky diode, the current is given by

$$I = I_S \cdot e^{-\phi_B q/kT}\left(e^{Vq/kT} - 1\right) \tag{1}$$

with I and V the diode current and voltage, respectively, ϕ_B the Schottky barrier, k the Boltzmann constant, q the

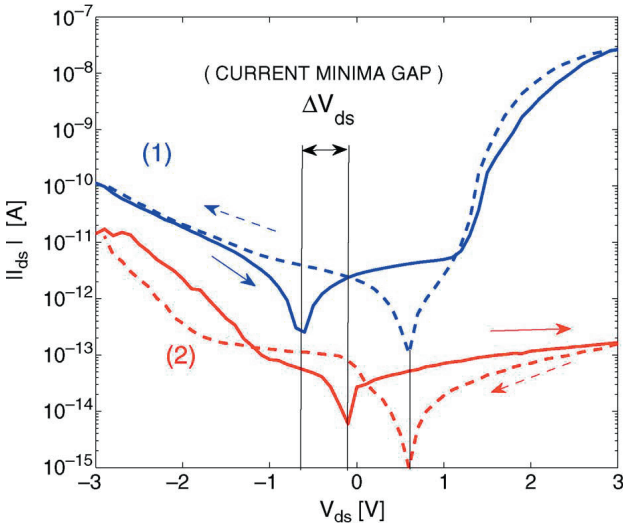


Fig. 5. *A typical memristive hysteresis is observed; the blue curve (1) is measured after drying the sample from deionized water. The red curve (2) is measured after dipping in 5-pM antigen solution and drying. The measured V_{ds} is proportional to the concentration of antigen [30].*

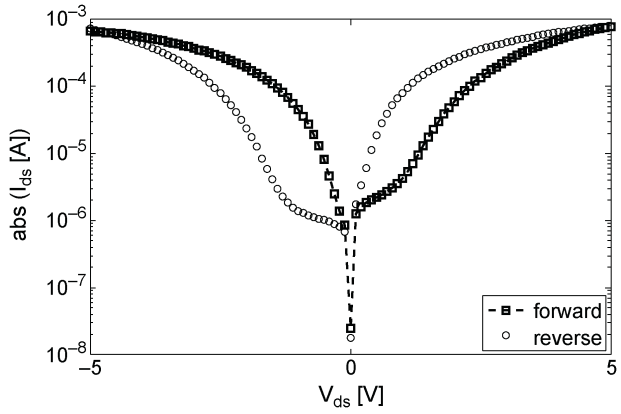


Fig. 6. *I_{ds}–V_{ds} characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 SiNW in parallel. The forward sweep curve has a symmetrical correspondence with the reverse sweep curve, showing the respective Schottky barrier modulation. A current ratio of about 50 is found at either $V_{ds} = \pm 1$ V. This behavior is typical of two-terminal memristive devices for ReRAM applications.*

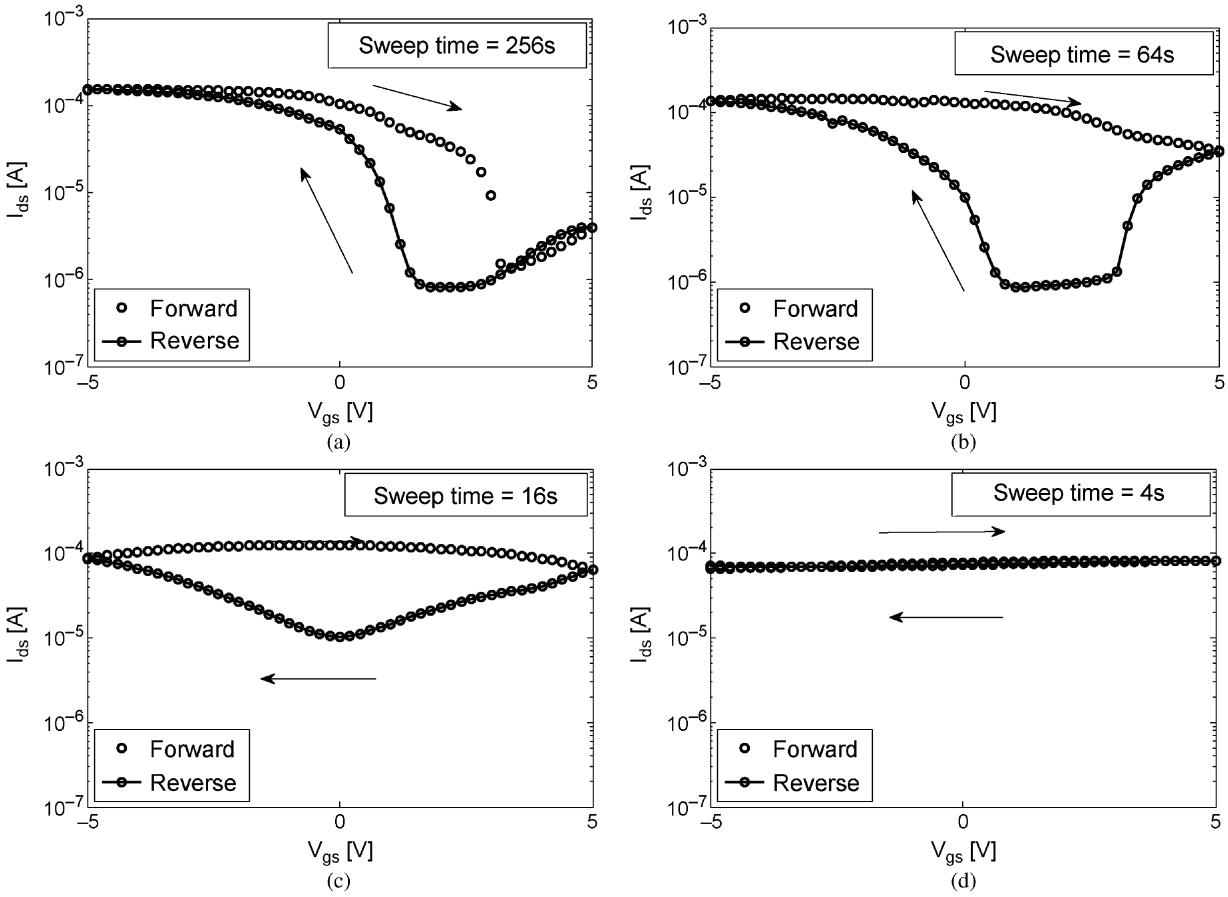


Fig. 7. ***Hysteretic dependence with the measurement (sweep time) duration; the hysteresis window closes by reducing the measurement time: (a) 256 s; (b) 64 s; (c) 16 s; and (d) 4 s.***

elementary charge, and T the absolute temperature. From the measured hysteretic behavior, it seems that the diode curve is modified as follows:

$$I = I_S \cdot e^{-\phi_B q/kT}\left(e^{(V-V_0(V))q/kT} - 1\right) \qquad (2)$$

with V_0 a built-in voltage at the Schottky contact that is positive for a positive V sweep and negative for a negative V sweep.

Another memristive functionality is linked with charging/decharging mechanisms into the gate dielectric. We measure I_{ds} for constant $V_{ds} = 1$ V while sweeping V_{gs} back and forth between -5 and $+5$ V [see Fig. 7(d)]. The devices are not annealed, and the source is connected to the substrate. This measurement is repeated for different integration times, which is a parameter of the measurement setup that can be set by the operator; and it represents the time over which the measurement is repeated and averaged. The I_{ds}–V_{gs} curves show an ambipolar behavior, meaning a large current conductance under either high or low gate bias. This is mainly due to the utilization of a silicide (NiSi) having a work function value that falls within the silicon bandgap, and to the utilization of a lightly doped silicon. On the other hand, the I_{ds}–V_{gs} curves have a hysteretic behavior that suggests the hypothesis of charge trapping at the semiconductor/oxide interface of the MOS capacitor, as well as the existence of interface states at the metal/semiconductor junction. Both ambipolarity and hysteresis depend on the integration time (see Fig. 7). When V_{gs} reaches $+5$ V in forward mode, the electrons experience a maximum probability of charges being trapped in the gate oxide, which is enhanced when the integration time is longer. Due to the electron trapping at the gate oxide, the channel operates in accumulation mode, with a lower conductance state for positive V_{gs}, than in the inversion mode for negative V_{gs}. Sweeping V_{gs} back to negative values reduces the amount of electrons trapped and the device operates in inversion mode, which restores the higher conductance state.

The threshold at which this high conductance state is reached depends on the integration time. The hysteresis window is larger when the integration time is shorter, because the charges have less time to be trapped and

detrapped. In the case of a very short integration time, the charges cannot be completely trapped and the lower conductance state is not reached (see Fig. 7).

IV. Si NANOWIRE MEMRISTIVE DEVICE FABRICATION METHODS

This section summarizes the main fabrication steps for multiterminal memristive devices based on CMOS-compatible Si nanowire technology. More details about the process flow can be found in [9], [36], and [39] for crystalline-Si (c-Si), polycrystalline-Si (poly-Si), and amorphous-Si (α-Si) nanowire channels. All the techniques yield nanowires with a subphotolithographic thickness. The general scheme is the one of the SB SiNW FET with midgap source/drain junctions. The use of a NiSi/poly-Si or NiSi/Si with undoped or lightly doped channel gives rise to a midgap Schottky barrier responsible for ambipolar conductance (see Fig. 8). The ambipolar nature of the midgap Schottky barrier field effect transistor (SBFET) can be qualitatively understood by the equal probability of either electron or hole injection, which is related to the midgap Schottky barriers. Both devices confirm the existence of an ambipolar conduction with a hysteretic behavior due to either charge trapping or modulation of the Schottky barrier through current flow. The following section surveys the fabrication details for three types of device.

A. Gate-All-Around Si Nanowire FETs

Bulk-Si wafers with low boron concentration ($N_A \sim 10^{15}$ atoms/cm^3) have been used as a substrate for the fabricated devices. Vertical stacks of Si nanowires are defined on the substrate by optical lithography [see Fig. 9(a)] without any constraint on the resolution limit (1 μm). The photoresist is then used as a mask for a deep reactive ion etching (DRIE) [Fig. 9(b)]. The optimized DRIE technique, which alternates plasma etching with passivation steps, defines scalloped trenches attached to Si pillars with high reproducibility. The enhanced scalloping effect produces vertical modulation of the trench width. A

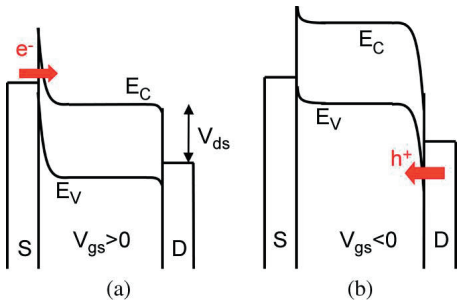


Fig. 8. *Band diagram explaining ambipolarity: (a) positive V_{gs} reduces the width of the Schottky barriers for electrons; (b) negative V_{gs} reduces the width of Schottky barrier for holes.*

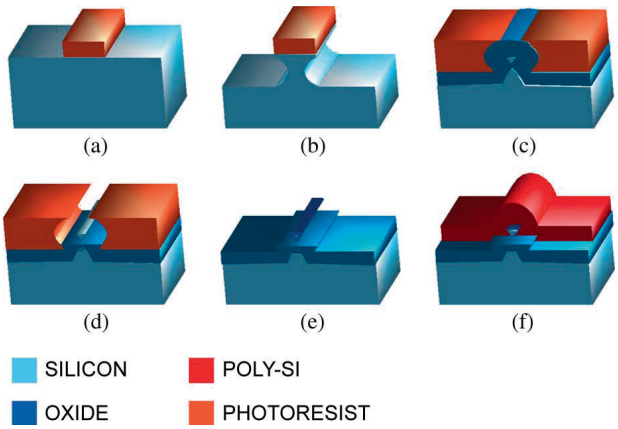


Fig. 9. *GAA SiNW SBFET process flow. (a) A photoresist line determines the nanowire position. (b) DRIE etching forms a scalloped trench. (c) After wet oxidation, the Si trench reduces to a suspended nanowire. The caves are filled with photoresist and planarized with CMP. (d) Buffered HF oxide etch releases the SiNWs. (e) Gate oxidation. (f) Polysilicon is deposited and patterned to form the gate.*

sacrificial oxidation is then carried out with the double purpose of eliminating the Si where the trench is thin, and also to reduce the surface roughness induced by the etching [Fig. 9(c)]. A combination of chemical mechanical polishing (CMP) and buffered HF (BHF) dip leaves vertically stacked nanowires suspended on a thick layer of insulating oxide [Fig. 9(d)]. The gate oxide is grown in a horizontal furnace with a dry atmosphere [Fig. 9(e)]. The gate polysilicon is conformally deposited and doped with phosphorous by means of a diffusion process and then patterned with a combination of isotropic and anisotropic plasma etching steps [Fig. 9(f)]. The fabrication of SBFETs requires the use of metallic source and drain contacts, meaning source-to-body and drain-to-body Schottky junctions. We pattern a Cr/Ni bilayers (10 nm/50 nm) on top of the Si pillars, partially covering the SiNW at the anchor points (see Fig. 10). This leads to the silicidation of the nanowire channel from the Cr/Ni bilayer toward the gated region of the nanowire. The process presented here is compatible with the one presented in [34] for dense SiNW FET arrays. An example of 3-D crossbar construction with 1 GAA poly-Si gate and 4 $\times$ 4 SiNW channels is shown in Fig. 11.

B. Poly-Si Nanowire FETs

The spacer technique is a promising approach to define subphotolithographic dimensions by using standard photolithography and CMOS steps [9]. The process flow is illustrated in Fig. 12. First, a sacrificial layer of SiO_2 is defined on a Si substrate followed by the deposition of a thin conformal layer of poly-Si [Fig. 12(a)]. Next, the poly-Si is etched by a reactive ion etching (RIE) technique, in order to remove the lateral layer and keep the sidewalls as a spacer [Fig. 12(b)]. Then a second low temperature

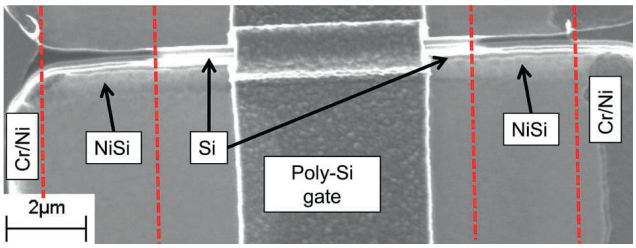


Fig. 10. *GAA SiNW SBFET with Cr/Ni source/drain after the liftoff process. The change in contrast on the NW channel is attributed to a difference between Si and silicided regions.*

oxide (LTO) spacer is defined next to the poly-Si in order to isolate the first poly-Si spacer [Fig. 12(c)]. The spacers form the nanowires with thicknesses ranging between 20 and 60 nm. The contact regions of the undoped poly-Si nanowire are defined by the electron-beam evaporation of 10-nm Cr and 50-nm nichrome ($Ni_{0.8}Cr_{0.2}$) and liftoff [Fig. 12(d)]. The Cr enhances the adhesion and thermal stability of Ni to oxidation during the following two-step annealing process. The substrate is used as a back-gate with a thick dry oxide as insulator (up to 400 nm thick). A scanning electron microscope (SEM) image of the obtained structure with an additional top gate defined on the poly-SiNW is shown in Fig. 13. This process has been reported for the construction of dense poly-SiNW crossbar arrays [40]. A small crossbar with one upper poly-SiNW and four lower poly-SiNW is shown in Fig. 14.

C. Low-Temperature Fabrication of α-Si Nanowires FETs

The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500-nm-thick wet oxide and a 100-nm LTO layer. Then, a 100-nm α-Si film is deposited as the active layer. A 70-nm-thick dilution of hydrogen-silsesquioxane (HSQ) is spin coated and patterned with e-beam lithography. Lines having widths ranging from

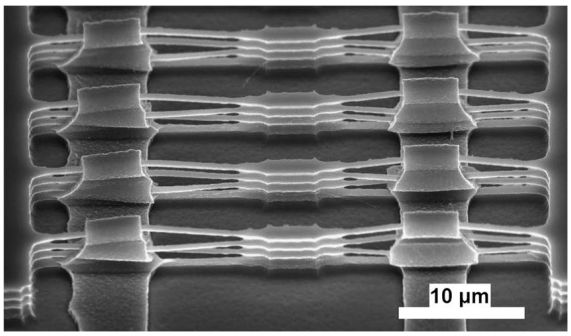


Fig. 11. *A 4 × 4 SiNW array with 2 poly-Si gate-all-around construction. The image is taken from [34].*

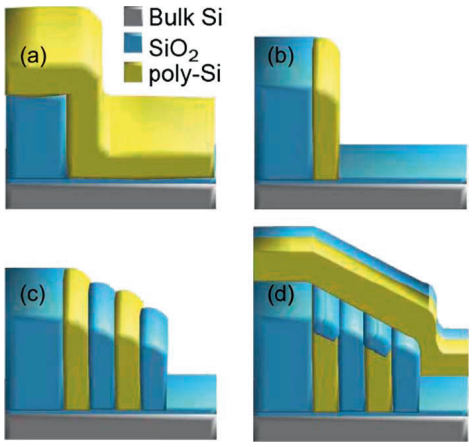


Fig. 12. *Nanowire arrays constructed using multi-spacer patterning technique [36]. (a) Conformal deposition of poly-Si. (b) RIE etch. (c) Definition of a SiO_2 spacer and iteration of previous steps. (d) Contacts formation.*

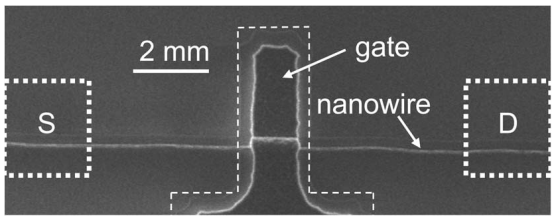


Fig. 13. *SEM image of a poly-SiNW with a top gate and Cr/$Ni_{0.8}Cr_{0.2}$*

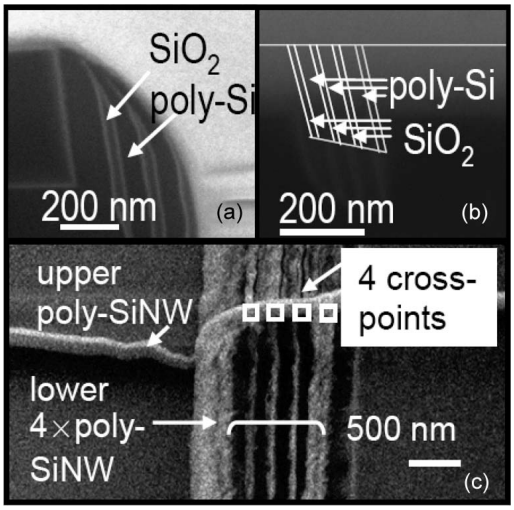


Fig. 14. *(a) Poly-Si NWs cross-section. (b) Poly-Si and SiO_2 spacers. (c) SEM image of a small crossbar with 1 upper and 4 lower poly-Si spacers [40].*

70 to 250 nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip BHF step. The obtained α-Si nanowires are then covered by a 40-nm dry oxide and a 50-nm LPCVD poly-Si

layers. Large 100 μm $\times$ 100 μm poly-Si pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, poly-Si Ω-gated FinFETs with gate lengths between 1 and 10 μm are obtained.

Then, a bilayer of 20-nm Ti/55-nm Ni is patterned with liftoff to form electrical contacts between the Si nanowires and the pads. A 400 °C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been chosen for its midgap work function and for its use in α-Si metal induced recrystallization process [41]. The fabrication flow is completed by the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100-nm-thick SiN membranes with apertures having widths between 100 nm and 1 μm [42]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2-μm [42] accuracy using a customized SUSS MA/BA6 mask aligner [43]. The clamped substrate-stencil setup is placed in an evaporator where 100-nm-thick Al gates are deposited. FinFETs and inverters with up to 62-μm nanowire length were fabricated. An example of a 2-μm-long poly-Si gate FinFET having 100 nm $\times$ 65 nm Si nanowire channel is shown in the SEM tilted view of Fig. 15(a). In Fig. 15(b), a Si nanowire transistor with 130 nm $\times$ 65 nm channel [see Fig. 16(d)] cross section and 700-nm large stenciled Al gate is shown. Focused ion beam (FIB) cross sections [see Fig. 16(a)–(c)] demonstrate nanowire channels sections having widths between 65 and 130 nm. The total Si thickness is reduced from the initial value of 100 to 65 nm due to processing. Narrower nanowires (the expected nanowire size was around 35 nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

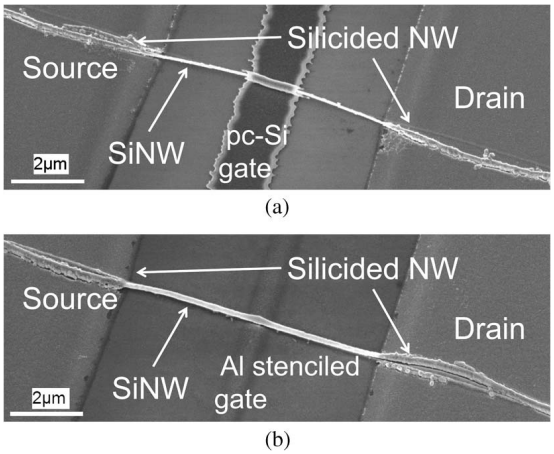


Fig. 15. *FinFETs with silicided nanowire portions at source/drain contacts: (a) poly-Si FinFET having 2-μm-long gate and 60 nm $\times$ 65 nm channel cross section. (b) Al stenciled FinFET having 700-nm gate length and 60 nm $\times$ 140 nm channel cross section.*

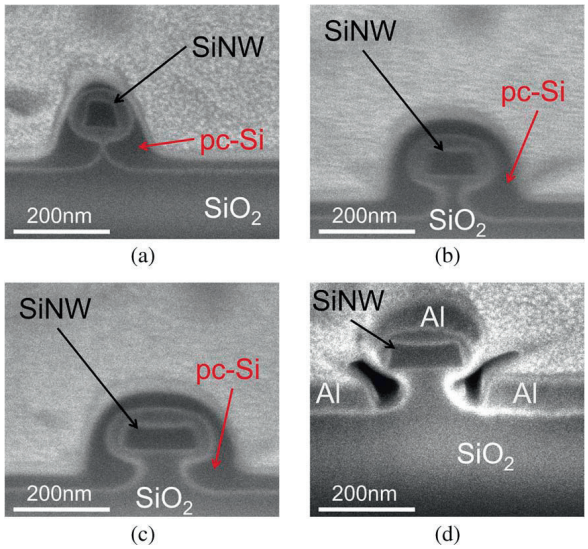


Fig. 16. *FIB cross sections showing the nanowire channels embedded in 40-nm oxide and gate materials: (a) poly-Si -gate FinFET with 60 nm $\times$ 65 nm section; (b) poly-Si -gate FinFET with 60 nm $\times$ 110 nm section; (c) poly-Si -gate FinFET with 60 nm $\times$ 140 nm section; (d) Al stenciled-gate FinFET with 60 nm $\times$ 140 nm section.*

V. FOUR-TERMINAL MEMRISTIVE DEVICES

Memristive functionality can be seen as state variable that can be used for more expressive logic gates [6]. The memristive behavior reported in Section III for the SB SiNW FETs can be tuned by operating on the polarity of the gate voltage. This type of behavior is linked with the

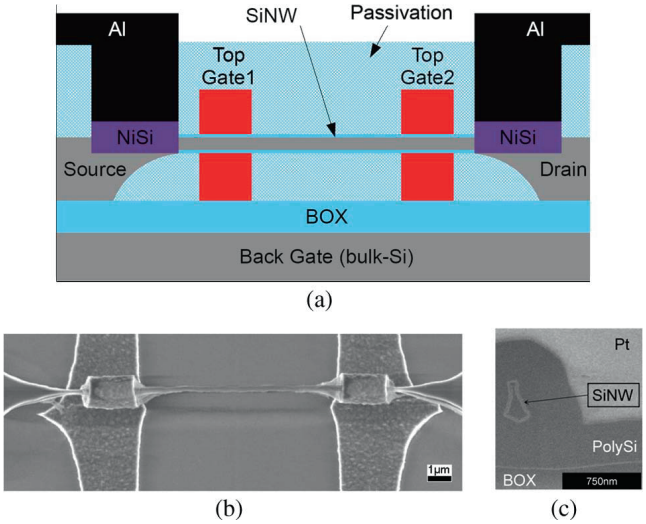


Fig. 17. *(a) Schematic cross section of a dual-gate device with NiSi source and drain regions on SOI substrate. (b) A 20-μm-long SiNW with two parallel GAA polysilicon gates having 4-μm gate lengths. (c) A FIB cut cross-section image showing the SiNW channel surrounded by a 500-nm polysilicon top gate.*

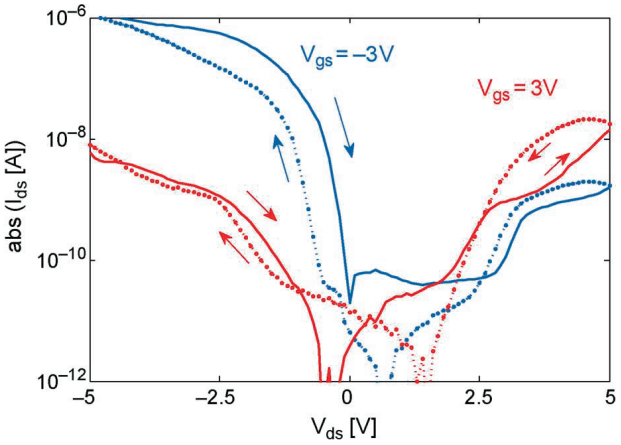


Fig. 18. ***Controlled memristance for fixed top and back gate voltages $V_{bf} = -5$ V.***

double conductance, for holes and electrons. As described in [44] for SB carbon-nanotube (CNT) FETS, the ambipolarity can be controlled by using an additional control gate, such that it blocks one type of carrier conductance. Following this principle, four-terminal memristive SB SiNW FETs can be built (see Fig. 17). In the following, two modes of operation are reported, depending on the nature of the controlling signal applied at the Si nanowire channel.

A. Voltage-Controlled Four-Terminal Memristive Device

A voltage-controlled four-terminal memristive Schottky barrier SiNW FET is obtained by using a dual-gate configuration such that one of the two gates is controlling a portion of the channel that is between the source/drain contacts and the main gate. This configuration is exploited to control the ambipolarity imbalance, such as for CNT FETs [44]. Since the back-gate voltage

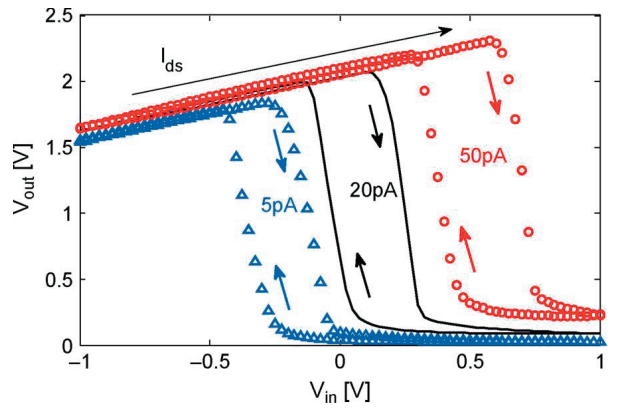


Fig. 19. ***Current-controlled memristive Schottky barrier SiNW FET hysteresis loop.***

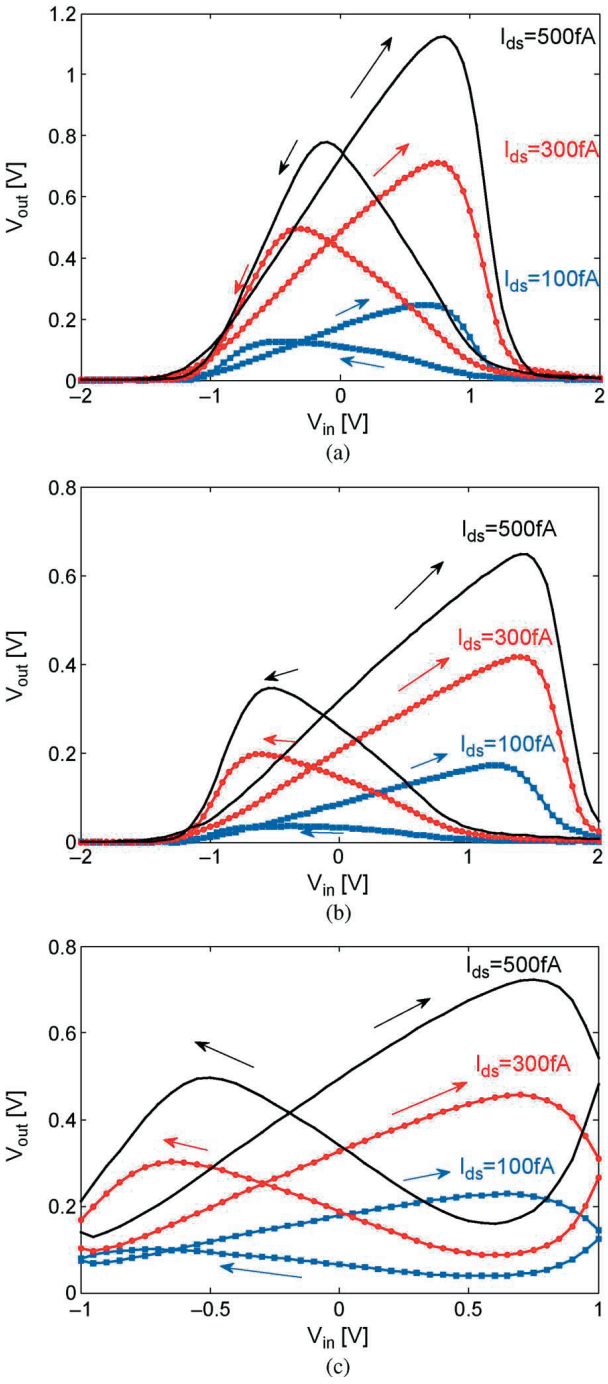


Fig. 20. ***V_{out} voltages for increasing with I_{ds} current bias. In all the figures I_{ds} bias values are 100, 300, and 500 fA. Notice the output voltage hysteresis narrows for increasing frequency sweep: (a) 24 s; (b) 6 s; and (c) 0.5 s.***

modifies the ambipolar conductance, this fact can be used in ambipolar memristive devices to limit the current levels for one of the carriers. A fixed back-gate voltage $V_{bg} = 0$ V leads to imbalanced bistable hysteresis loops under different V_{gs} voltages. By applying a negative $V_{bg} = -5$ V this imbalance is toggled for the negative side of the characteristics, giving a complementary effect (Fig. 18).

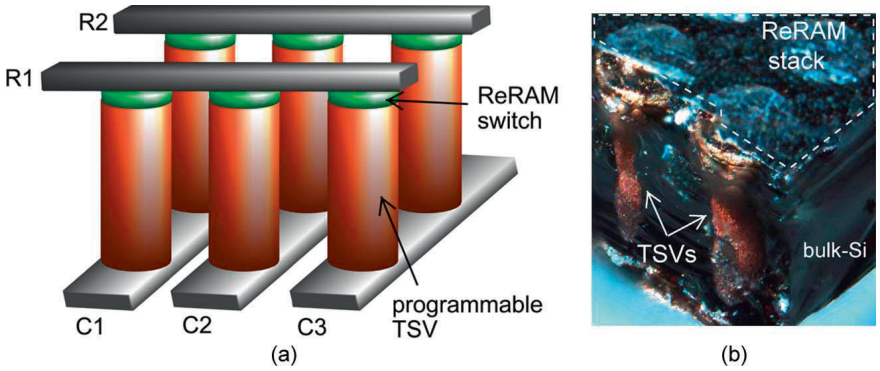


Fig. 21. *(a) A crossbar architecture with programmable TSVs made of ReRAM stacks [21]. (b) Reconstructed 3-D photograph of the TSV-ReRAM stack. The die is cleaved in order to reveal the TSV and the ReRAM layer deposited on top.*

Finally, a $V_{\rm bg} = +5$ V levels off the conductances of electrons and holes, giving a pretty symmetric hysteresis.

B. Current-Controlled Four-Terminal Memristive Devices

A current-controlled version of the four-terminal memristive Schottky barrier SiNW FET is obtained by using a current I_{ds} bias instead of a V_{ds}. The output voltage is then compared with V_{gs} (Fig. 19). The obtained hysteresis can be used as a latch device, whose position in the $V_{\rm out} - V_{\rm in}$ plane can be adjusted by using a different value of the current bias. A similar behavior has been exploited with three-terminal Schottky-barrier polysilicon nanowire FETs circuits to build a new logic family based on precharge and evaluation scheme [45]. Moreover, a similar scheme has been demonstrated for DRAM type of memory [46] and for pA current and temperature detection [47]. Similarly, SB Si nanowire transistors fabricated with a low thermal budget process and biased in current-controlled mode shows a similar hysteresis. Moreover, polycrystalline SiNWs SB FETs can give a hysteretic transfer characteristic (Fig. 20) very similar to the one reported for crystilline SiNW SB FETs fabricated with a low thermal budget process [39]. As is shown in Fig. 20, the maximum output voltage in the transfer characteristics increases with the $I_{\rm ds}$ bias current. From Fig. 20(a)–(c), the sweep time is reduced. Similarly to what was discussed for the three-terminal SB SiNW FET memristive device, the sweeping time impacts on the amount of charge that traps at the gate oxide/channel interface, thus influencing the conductance state of the nanowire channel. A faster sweeping time outbalances the charge trapping/detrapping mechanism, resulting in lower output voltages [see Fig. 20(a) and (b) compared with Fig. 20(c)].

VI. APPLICATIONS

Very different applications belonging to signal processing, memory, and sensing are envisaged for multiterminal memristive devices. The possibility to build very dense crossbar arrays of two-terminal memristive devices is often seen as a disruptive technology for ultradense ReRAM or write at once (WORM) nonvolatile memory storage [48]. In this concern, all the nonvolatile two-terminal memristive technologies are suitable candidates to replace flash memory in the future, given their higher density storage per cost. This feature is especially interesting because it can be utilized to stack nonvolatile memory elements in the back-end-of-the-line, increasing both density and access speed among logic and memory layers. Good examples are the recently proposed hybrid semiconductor/nanowire/molecular (CMOL) integrated circuits [49], as well as 3-D field-programmable gate array (FPGA) architectures with programmable through silicon vias (TSVs) [21] (see Fig. 21). The two-terminal memristive crossbars can also be integrated into programmable logic array architectures to compute Boolean logic functions. The memristive crossbar architecture can be exploited to reprogram itself. For instance, in [50], a very dense nanowire crossbar with TiO_2 memristive junctions was used to perform logic functions and to store the result into another portion of the same crossbar. Moreover, memristive switches can be used to perform material implication function[1] and exploited to build latches that use resistance in place of voltage or charges as physical state variable [6]. Another application that can exploit the memristive functionality is related to the design of cellular neural networks [8]. The Hodgkin–Huxley model for the synapse was one of the earlier examples reported by Chua and Kang [5] of systems that can be modeled with the memristor. Recently, the use of two-terminal memristive devices in combination with digital-to-analog converters demonstrated a way of reproducing the associative memory of animals [51]. The modification of the memristive characteristic to environmental condition can also be utilized for different types of

[1]Here for material implication it is meant a fundamental Boolean logic operation on two variables "p" and "q" such that pIMPq is equivalent to (NOTp)ORq.

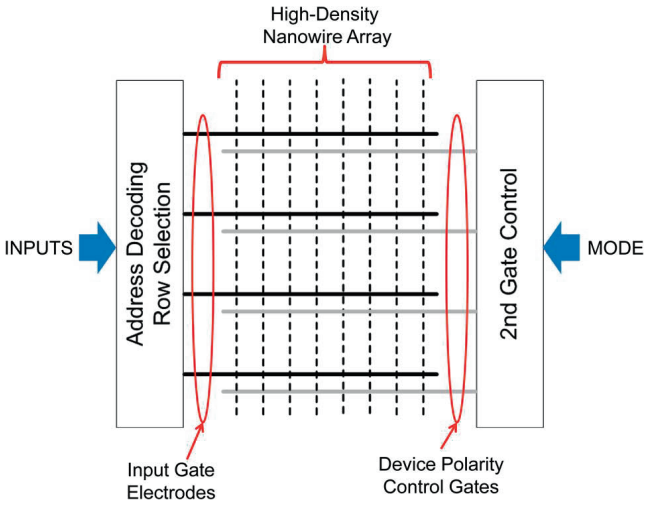


Fig. 22. ***A crossbar architecture with polarity control and address decoding made with high-density four-terminal memristive SiNW arrays.***

sensing. For instance, functionalization of nanowires with redox active molecules give rise to the typical memristive pinched hysteresis loop [52]. Another example can be the sensing of temperature with spintronic memristor [53]. The temperature change can cause a variation of the domain-wall mobility that in turn is sensed thanks to a positive feedback loop electronics. This type of sensor has been reported to be very compact ($\leq 1\ \mu m^2$ cell size) and to operate with very low power.

Multiterminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [32] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for biomolecule detection in dry environment [30]. More specifically, in [30], the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authors [47]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [45]. For instance, in [45], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR, and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing a hysteretical negative differential resistance [46]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel. In Section IV, it is shown that a similar hysteresis can also be obtained independently on the phase state of the Si nanowire channel. Similarly, the same structure can exploit the functionality of an additional gate to tune the polarity of an SB SiNW FET, thus giving even more functionality (Section IV). A very high expressive power architecture can be made of four-terminal memristive devices arranged in a crossbar implementation that exploits the high density of the SiNW arrays (Fig. 22).

VII. CONCLUSION

A general overview on multiterminal memristive devices is reported. The functionality of the devices can be used for logic, memory and sensing applications. Ultradense memristive ReRAMs crossbar arrays can be used for ultradense nonvolatile memory storage. It was shown that three- and four-terminal memristive devices can be used for both logic and memory applications. In particular, Schottky-barrier silicon nanowire FETs are very interesting devices due to their CMOS compatibility and ease of fabrication. Disruptive applications exploiting the high expressive power of four-terminal memristive devices arranged in crossbar arrays are foreseen as a significant advance in the electronic computation. ■

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Pro-Active R&D engineer with strong motivation in seeking novel nanotechnology solutions for cutting-edge products. Profound knowledge in clean room technologies and device prototyping in a team or independent work. Expertise in lithography, dry etching and thin-films deposition. Design of experiments for the development of semiconductor device technology and process optimization. Very good presentation skills sharpened through experience at international conferences.

Process optimization, design of experiment, lithography, etching, thin-films, teamwork, communication

WORK EXPERIENCE

Research Assistant (2008-2013)
EPFL, Switzerland

- Involved in at least 4 successful project definition and proposals writing for research funding
- Experience with micro- and nano- fabrication tools within a class 100 clean room environment
- Research project planning and team management
- Design, Fabrication and Characterization of ambipolar Vertically-stacked Si nanowire platform
- Demonstration of novel bio-sensing method exploiting memory effects in ambipolar Si nanowires
- Fabrication and characterization of novel resistive RAM concepts for standalone memories and for FPGA applications
- Lecturer and assistant in technical projects for classes of 60+ M.Sc. students
- Advisor of 3 M.Sc. projects involving successful fabrication of Si nanowire resonators and bio-sensors.
- Author of more than 25 scientific publications in international conferences and journals

Exceptional Performance Award of the faculty of engineering at EPFL, 2010
Best Paper Award at Nanoarch 2012

EDUCATION

Doctor of philosophy (PhD) of sciences in Micro-Systems and Micro-Technologies
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Thesis title: Multi-Terminal Am-Bipolar Memristive Devices for Emerging Logic and Memory Architectures
Advisors: Prof. Yusuf Leblebici and Prof. Giovanni De Micheli

Master in Micro and Nanotechnologies for the ITCs (2006-2008)
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Dissertation: Fabrication and Characterization of Vertically-Stacked Si nanowire transistors

Master Project (2008, 6months)
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- Definition of a top-down fabrication flow for vertically-stacked Si nanowire N-FETs
- Design of photolithographic masks with Cadence Virtuoso
- Fabrication and Characterization of vertically-stacked Si nanowire N-FETs

Summer Internship (2007, 3months)
X-Lab, Chivasso, Italy

- Development of a polymeric Lab-On-a-Chip
- Hot Embossing of PC, PMMA, COC and realization of microfluidics with PDMS bonding and interconnects

Bachelor in Physics Engineering (2003-2007)
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Dissertation: Nuclear physics in fission reactors and technological considerations

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[1] D. Sacchetto, P.-E. Gaillardon, M. Zervas, S. Carrara, G. De Micheli, and Y. Leblebici, "Applications of Multiterminal Memristive Nanowire Devices for Logic and Memory: A Review," accepted for publication in *Circuits and Systems Magazine*, 2013

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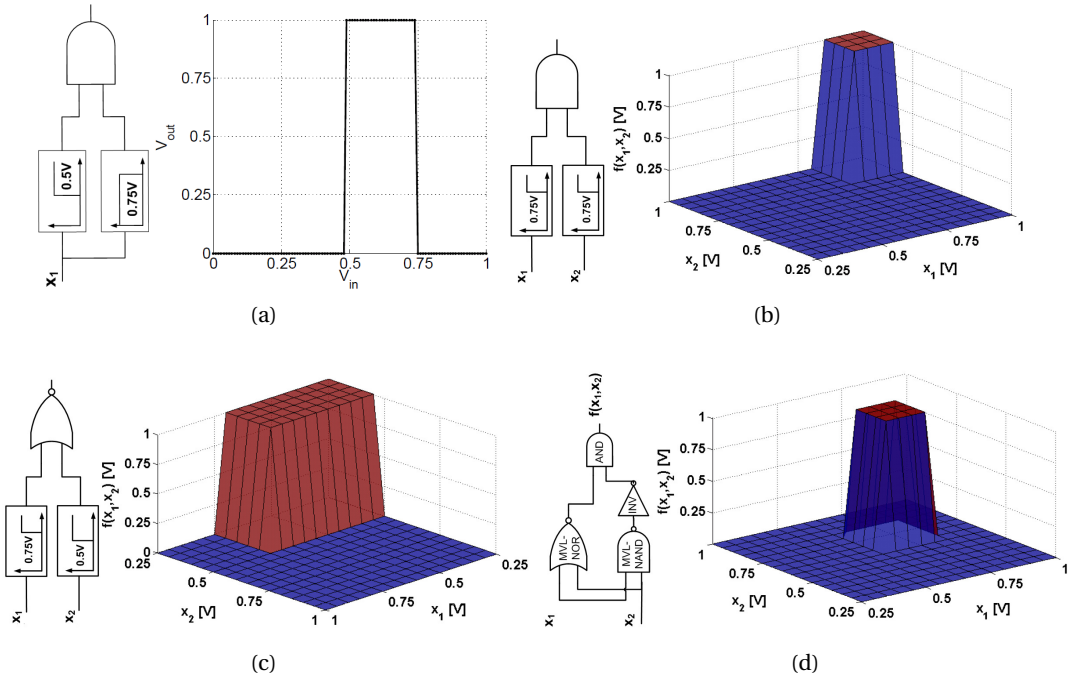


Figure 4.11: (a)Opposite polarities TL nanowire gates having two different threshold voltages are used to construct a literal function of MVL input. (b) MVL-AND function obtained from two TL nanowire gates and a AND logic gate. (c) MVL-AND function obtained from two TL nanowire gates and a AND logic gate. (d) Product of terms function obtained using a MVL-NOR gate and MVL-NAND in combination with a inverter and a Boolean logic AND gate.

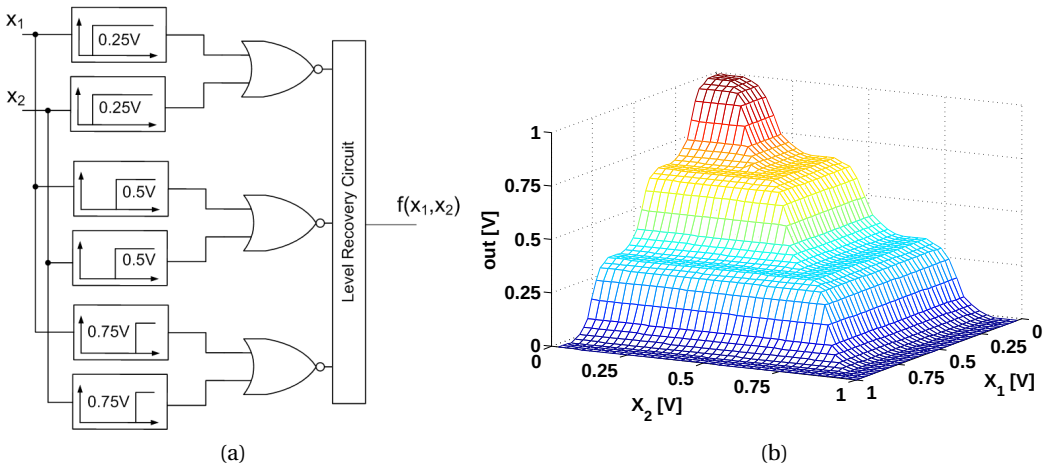


Figure 4.12: (a)Circuit schematic of a NMAX logic function. Three MVL-NOR gates driving a level recovery circuit are used for mapping a two-variable input space into a one-variable output space. Note that the NMIN function can be implemented by changing the Boolean layer into a NAND one. (b) Output representation of the MVL-NMAX function implemented with nanowire based threshold gates.

4.4 Logic functions with polarity controllable devices

An ambipolar SiNW FETs with *Double Independent Gate (DIG)* structure enable the use of polarity control signals as a method toward Si circuits with increased logic expressive power. Moreover, the use of polarity control leads to improved performance in terms of $I_{ON} - I_{OFF}$ ratio and inverse subthreshold slopes with respect to the ambipolar behavior.

4.4.1 Device Description

The device consists of a 20μm-long crystalline SiNW attached between two Si pillars on a SOI wafer (see Fig. 5.19a). The SiNW is then covered by two independent n++ polysilicon gates with this scheme: a main central gate (gate 1) of 7.5μm length and a second gate (gate 2) that is used to control the SiNW portions between the main gate and source and drain regions, respectively.

4.4.2 Fabrication

First, a low doping p-type ($N_A \approx 10^{15}$atoms/cm^2) SOI wafer with 1.5μm device layer is spin coated. The photoresist is then patterned in 1.5μm wide lines (see Fig. 5.19b) and used as mask for a next isotropic Si etching. A Si plasma etching recipe is tuned to form a triangular 75nm wide SiNW lying on top of the BOX layer (Fig. 5.19c. Then a 30nm thick gate oxidation and a 150nm polysilicon layer are deposited with LPCVD method to form a main gate with 7.5μm length (gate 1, Fig. 4.13d). The main gate is then isolated by a 300nm LPCVD LTO. A second 500nm polysilicon layer is then deposited. Then a thick photoresist is spun over the wafer and planarized using a chemical mechanical polishing procedure similar to the one previously described by the authors in [9]. This method leaves a protective polymer layer that is used to etch a second polysilicon gate self-aligned within the cavity thanks to the topography (see gate 2 in Fig. 4.13e). After standard cleaning steps, one additional patterning of gate 2 is performed to remove the unnecessary polysilicon and to form areas for the contacts (see the top view of the device in Fig. 5.19a). In Fig. 4.13f, a focused ion beam cross-section of the triangular SiNW channel with the DIG stack is shown. Then source/drain contacts are formed by means of NiSi silicidation in a horizontal wall furnace in forming gas at 400°C. Finally Al metal lines and pad area are defined for the electrical characterization.

4.4.3 Device Operation

The source/drain regions after NiSi silicidation have a mid-gap Schottky barrier contact with the SiNW, thus both electrons and holes can contribute to the current flow. The use of the two gates enables the selection of which carrier species shall prevail in the conduction. In the following discussions, the voltage applied to gate 1 is defined as V_{gs}, while the voltage applied to gate 2 V_{bg}. This scheme was proposed by Lin et al. [15] for the control of polarity of CNT FETs. As depicted in Fig. 5.5a, positive back gate voltage V_{bg} enable electron flow, while holes current is blocked. Similarly, (Fig. 5.5b) negative V_{bg} makes the opposite selection: holes current is enabled while the electron flow is blocked.

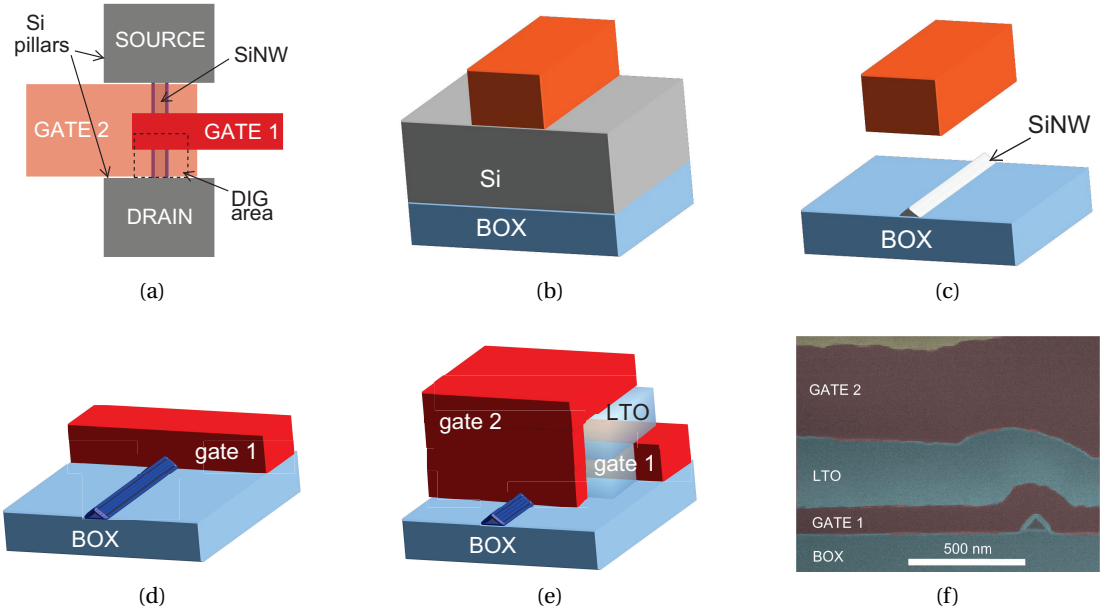


Figure 4.13: Fabrication flow. (a) Top view of the dual-gate device. The next steps focuses on the DIG area construction. (b) Photoresist mask is patterned. (c) After isotropic etching of Si a triangular-shaped SiNW is formed. (d) Gate oxidation and LPCVD polysilicon are deposited and patterned to form the main, central gate stack. (e) A LTO inter-poly dielectric is deposited and a second polysilicon gate is made self-aligned with the nanowire. (f) Focused ion beam cross-section showing a triangular SiNW channel with two 75nm sides and 100nm base. The gate 1, gate 2 and the LTO inter-poly dielectric have 150nm, 500nm and 300nm thicknesses, respectively. Gate 1 dielectic is 30nm thick.

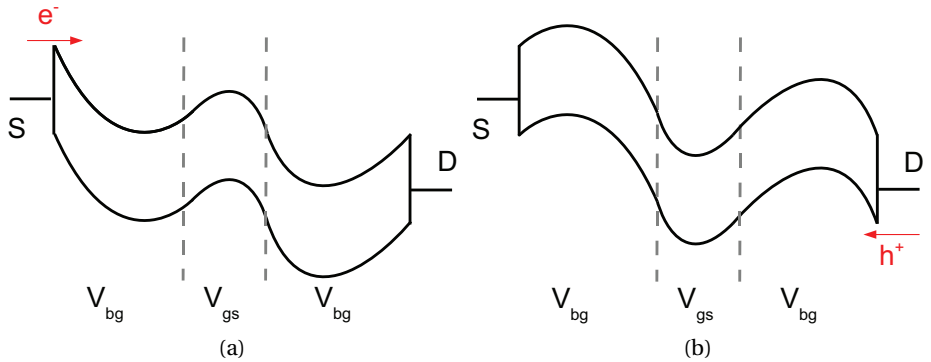


Figure 4.14: (a) Conceptual band diagram for n-type operation. A positive V_{bg} is used to block the flow of holes from the drain. (b) Conceptual band diagram for p-type operation. A negative V_{bg} is used to block the flow of electrons from the source.

V_{bg}[V]	$\frac{I^{h+}_{ON}}{I_{OFF}}$	$\frac{I^{e-}_{ON}}{I_{OFF}}$	SS^{h+}[mV/dec]	SS^{e-}[mv/dec]
+10	50	250	1000	600
+7.5	N/A	2000	N/A	250
+5	N/A	1000	N/A	250
+2.5	N/A	1000	N/A	325
0	1000	600	475	750
-2.5	1000	N/A	375	N/A
-5	5000	N/A	250	N/A
-7.5	10000	N/A	300	N/A
-10	30000	N/A	300	N/A

Table 4.2: Obtained electrical behavior for different V_{bg} voltages.

4.4.4 Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer in dark at room temperature. In Table 5.1 the effect of V_{bg} on the inverse subthreshold slopes (SS^{h+}, SS^{e-}) for hole and electron conduction branches depicts a trend for improved SS^{h+} and SS^{e-} when increasing V_{bg} voltages of negative and positive polarities are applied, respectively. Similarly, improved $I_{ON} - I_{OFF}$ ratio ($\frac{I^{h+}_{ON}}{I_{OFF}}$, $\frac{I^{e-}_{ON}}{I_{OFF}}$) is observed when larger V_{bg} voltages are applied. The improved performance is related with a reduced I_{OFF} current due to the screening of one of the two types of carriers for the conduction. As better shown in Fig. 5.26b, positive or negative V_{bg} voltages can be used to obtain n-type or p-type $I_{ds} - V_{gs}$. Moreover, a symmetrical ambipolar $I_{ds} - V_{gs}$ is obtained for $V_{bg} = 0$V. This functionality allows for increased expressive logic power with a single FET. For instance, the two voltage signals, V_{gs} and V_{bg} can be coded to make logic XOR operation with the device of Fig. 5.26b; an operation that would require more transistors in standard CMOS technology. In Table 4.3, V_{gs} and V_{bg} voltage values are encoded into logic levels 0 and 1 to map into four binary logic operations: XOR, NAND, AND and NOR, while using the data plot in Fig. 5.26b. The result of the logic operation are summarized in Table 4.4. Logic 0 and logic 1 outputs are represented by light and dark gray, respectively. Another solution that can be envisaged can use the same logic levels for both gates in order to save space for external encoding circuits. This solution will become a most desirable one by optimizing the thickness of the two gate dielectrics, which in the current implementation lead to a more effective electric field density for gate 1 than for gate 2. In future designs, this technological issue might be overcome by optimizing the dielectric thickness for the two gates and/or in combination with dopant segregation techniques to balance the Schottky barrier heights for holes and electrons. Moreover, gate workfunction engineering can be used to code the threshold voltage of the device, thus addressing the different logic 0/1 voltages needed for a specific logic function. Thanks to these technological options, dense arrays of ambipolar DIG FETs can be envisaged as basic building blocks to map complex logic circuits. The AC characteristic of the proposed device concerning delay and power will depend, among other factors, on the capacitive coupling between the two gate electrodes. However, this parasitic coupling is estimated to be of the same order of magnitude of the source/drain to gate capacitance, and giving the fact that the fabricated device performs a more expressive logic functionality, this additional coupling is not expected to be a limiting factor.

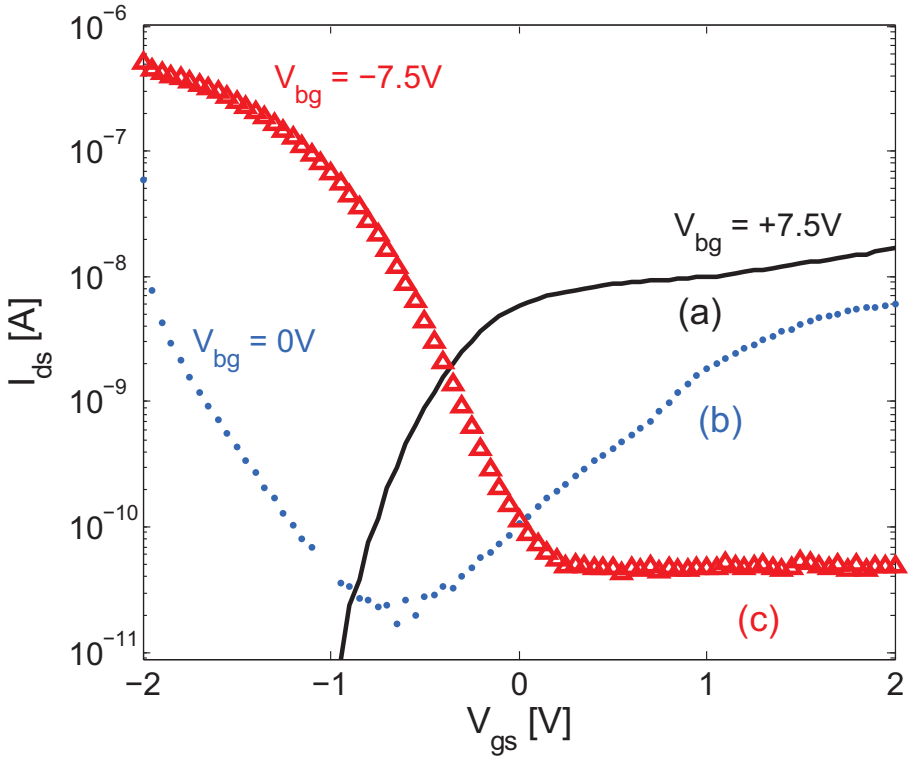


Figure 4.15: Controlled ambipolar $I_{ds} - V_{gs}$ characteristics at different V_{bg} back gate voltages. (a) A positive $V_{bg} = +7.5V$ is used to obtain a n-type characteristic. (b) A $V_{bg} = 0V$ gives ambipolar $I_{ds} - V_{gs}$. (c) A negative $V_{bg} = -7.5V$ is used to obtain a p-type characteristic.

CODE	XOR		NAND		AND		NOR	
	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]
logic 0	+1	-7.5	-0.5	+7.5	0	0	0	+7.5
logic 1	-1	+7.5	+1	-7.5	-1	-7.5	-1	0

Table 4.3: Binary logic - voltage signals coding for XOR, NAND, AND and NOR operation.

logic values		XOR	NAND	AND	NOR
gate 1	gate 2	I_{OUT} [A]	I_{OUT} [A]	I_{OUT} [A]	I_{OUT} [A]
0	0	$4 \cdot 10^{-11}$	$2 \cdot 10^{-9}$	10^{-10}	$6 \cdot 10^{-9}$
0	1	10^{-8}	$2 \cdot 10^{-9}$	10^{-10}	10^{-10}
1	0	$7 \cdot 10^{-8}$	10^{-8}	10^{-11}	10^{-11}
1	1	10^{-11}	$4 \cdot 10^{-11}$	10^{-7}	$5 \cdot 10^{-11}$

Table 4.4: Output current levels for the 4 logic operations: XOR, NAND, AND, NOR.

4.4.5 Summary

In this study a new device structure exploiting a double independent gate configuration with SiNW and top-down fabrication flow has been demonstrated as useful building block for ambipolar-controlled logic operation. All the $I_{ds} - V_{gs}$ characteristics, defining n-type, p-type and ambipolar behavior have been obtained with good $I_{ON} - I_{OFF}$ ratio of up to 4 orders of magnitude and inverse subthreshold slopes close to state-of-the art Schottky barrier FETs. In addition, a single device can be used to perform any of the XOR, XNOR, NAND, AND and NOR binary logic operations depending on the input signals encoding. The proposed integration scheme is envisaged for logic circuits exploiting the improved logic expressive power of ambipolar-controlled SiNW devices, which is enabled by the reliability of Si fabrication technology.

4.5 Chapter Summary and Conclusions

In this chapter applications of ambipolar devices have been discussed. In particular, asymmetric ambipolar devices can be exploited for ternary logic, as they provide two ON state conductance (one for electrons and one for holes) and one OFF state. This feature can be exploited to build ternary logic gates. Another interesting feature of ambipolar SiNW transistor is the possibility of building precise threshold gates by using a current biasing scheme. Then, the threshold gates can be utilized to build generic multi-value logic gates, as the base for more complex multi-value functions such as NMAX. Finally, the use of double independent gate construction enables the control of the electric field at the Schottky junctions, independently from the gate built around the central portion of the channel. This feature can be exploited to compute boolean logic functions with a single device and paves the way for more complex logic circuits exploiting the ambipolarity as a computational state variable.

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5 Applications of Memristance

5.1 Introduction

Very different applications belonging to signal processing, memory and sensing are envisaged for multi-terminal memristive devices. The possibility to build very dense crossbar arrays of two-terminal memristive devices is often seen as a disruptive technology for ultra-dense ReRAM or *Write-at-Once Memory (WORM)* storage [1]. In this concern, all the non-volatile two-terminal memristive technologies are suitable candidates to replace flash memory in the future, given their higher density storage per cost. This feature is especially interesting because it can be utilized to stack non-volatile memory elements in the BEoL, increasing both density and access speed among logic and memory layers. Good examples are the recently proposed hybrid semiconductor/nanowire/molecular (CMOL) integrated circuits [2], as well as 3D *Field Programmable Gate Arrays (FPGA)* architectures with programmable *Through Silicon Vias (TSVs)* [3] (see Fig. 5.1). The two-terminal memristive crossbars can also be integrated into programmable logic array architectures to compute Boolean logic functions. The memristive crossbar architecture can be exploited to re-program itself. For instance in [4], a very dense nanowire crossbar with TiO_2 memristive junctions was used to perform logic functions and to store the result into another portion of the same crossbar. Moreover, memristive switches can be used to perform material implication function [1] and exploited to build latches that use resistance in place of voltage or charges as physical state variable [5]. Another application that can exploit the memristive functionality is related to the design of Cellular Neural Networks [6]. The Hodgkin-Huxley model for the synapse was one of the earlier examples reported by Chua and Kang [7] of systems that can be modeled with the memristor. Recently, the use of two-terminal memristive devices in combination with digital to analog converters demonstrated a way of reproducing the associative memory of animals [8]. The modification of the memristive characteristic to environmental conditions can also be utilized for different types of sensing. For instance, functionalization of nanowires with redox active molecules give rise to the typical memristive pinched hysteresis loop [9]. Another example can be the sensing of temperature with spintronic memristor [10]. The temperature change can cause a variation of the domain-wall mobility that in turns is sensed thanks to a positive feedback loop electronics. This type of sensor has been reported to be

[1] Here, the material implication is used for a fundamental Boolean logic operation on two variables p and q such that pIMPq is equivalent to (NOTp)ORq

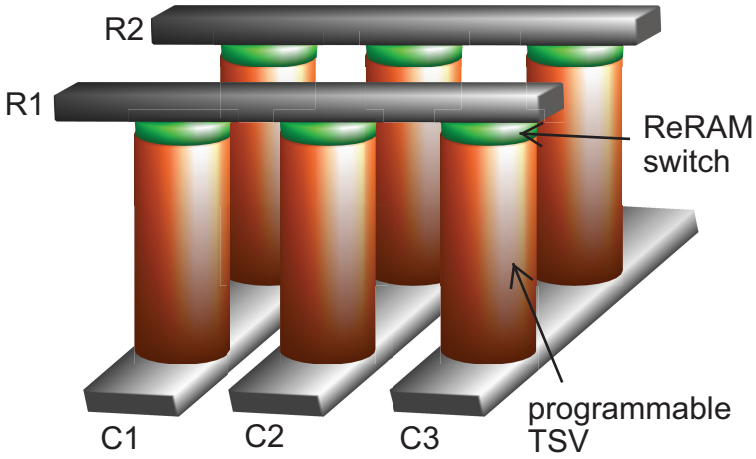


Figure 5.1: A crossbar architecture with programmable TSVs made of ReRAM stacks [3].

very compact ($\leq$1 μm^2 cell size) and to operate with very low power.

Multi-terminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [11] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for bio-molecule detection in dry environment [12]. More specifically, in [12] the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all-around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authours [13]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [14]. For instance in [14], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing an hysteretical negative differential resistance [15]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel. In chapter 3, it has been shown that a similar hysteresis can also be obtained independently on the phase state of the Si nanowire channel. Similarly, the same structure can exploit the functionality of an additional gate to tune the polarity of a SB SiNW FET, thus giving even more functionality, as described in the previous chapter. A very high expressive power architecture can be made of four-terminal memristive devices arranged in a crossbar implementation that exploits the high-density of the SiNW arrays (Fig. 5.2).

In this chapter applications for two-terminal memristive devices, and specifically bipolar resistive RAM are discussed. In Section 5.2 an example of fabrication and characterization of bipolar resistive RAM based on Al_2O_3 and Ta_2O_5 is discussed. Then a *Generic Memory Structure (GMS)* made of two resistive RAM devices is presented and discussed for FPGA applications (Section 5.3). Another example of resistive RAM application is given in Section 5.4. Then in Section 5.5 applications for multi-terminal memristive SiNW devices are showcased. Finally,

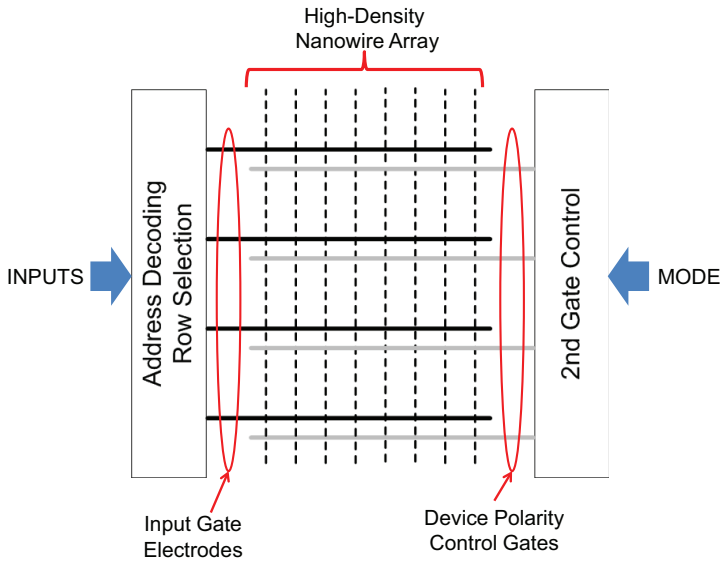


Figure 5.2: A crossbar architecture with polarity control and address decoding made with high-density 4-T memristive SiNW arrays.

in Section 5.6 the original contributions of this chapter are summarized.

5.2 Standalone Memories

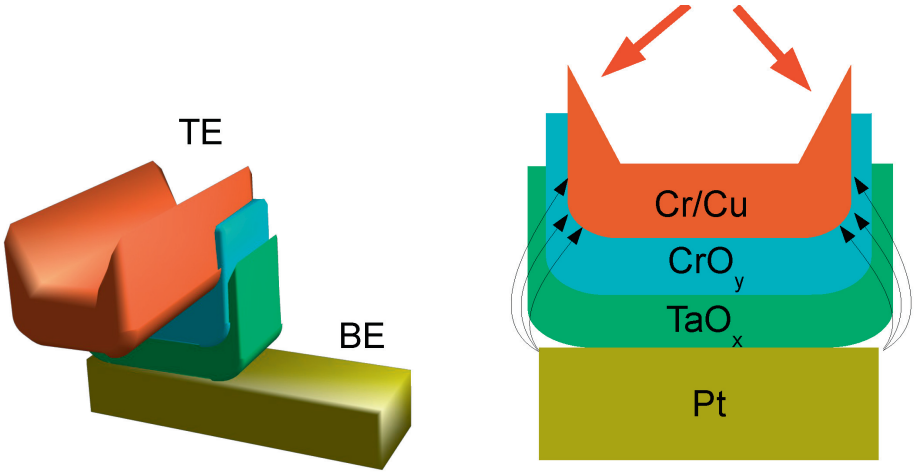
5.2.1 Introduction

Future deeply scaled circuits will see their performances limited by the physical limitations of the materials. To keep pushing the performance of computation and the density of storage, the microelectronics industry envisages using more efficient state variable than the electronic charge. In this sense, the memristor is an attractive candidate for both computation and memory, thanks to its programmable resistive state. When considering the Resistive RAM (ReRAM) memories, which can be classified as memristors, excellent scalability and programming time can be obtained if compared to traditional Flash, which make ReRAMs suitable candidates for standalone memory applications.

In this section, a ReRAM technology demonstrating a *Multi-Level (ML)* forming-free $Pt/TaO_x/CrO_y/Cr/Cu$ crossbars built with low thermal budget ≤200°C is discussed. The devices show excellent scalability down to $2.5x10^9 bit/cm^2$ with device half-pitch of 100nm with projections of practical storage density of up to $10^{12} bit/cm^2$ at the 10nm technology node [16].

5.2.2 Fabrication

The basic device concept is a ReRAM composed of 2 metal lines crossing orthogonally and a transition metal oxide stack in between (see Fig.5.19a). Moreover, the shape of the *Top Electrode (TE)* has been fabricated such that corners are smoothed (Fig.5.19b). This feature



(a) (b)

Figure 5.3: (a) 3D cross-point ReRAM concept with fence-like Top Electrode (TE) shape. (b) Lateral cross-section view of Pt/TaO_x/CrO_y/Cr/Cu cross-point ReRAM device. The fence-like TE enables better scalability of the cross-point device thanks to a reduction of the intense electric field distribution at the corners.

reduces the fringing field intensity at the wire ends, thus improving both reliability and scalability of the devices. Two different ReRAM (Pt/TaO_x/CrO_y/Cr/Cu and Al/TiO_2/Al with the Bottom Electrode/Transition Oxide/Top Electrode order) stacks have been built and compared in terms of performance. Both stacks have forming-free property and as such they do not require special forming steps to form the devices. This is a considerable advantage for actual implementation on chip. Several devices have been built in a passive crossbar array fashion as explained in the following text. Si bulk wafers are first isolated by depositing 100nm thick Al_2O_3 with *Atomic Layer Deposition (ALD)* (Fig. 5.20a). Then, PMMA bi-layers are patterned with e-beam lithography as lift-off masks for 10nm/80nm Pt *Bottom Electrodes (BE)* deposition (Fig.5.20b). In the next step, a second lift-off mask is defined and 15nm TaO_x oxide layer (Fig.5.4c) is deposited by sputtering from a Ta_2O_5 target with increasing RF power in Ar/O_2 atmosphere (Fig.5.4e). Finally, 50nm/100nm thick Cr/Cu bi-layers TE are deposited by e-beam evaporation (Fig.5.4d). For Al/TiO_2/Al devices, the Al electrodes are deposited with e-beam evaporation while 10nm thick TiO_2 is deposited by ALD. In Fig.5.5a and 5.5b SEM images of 100nm wide BE lines and 64bit passive crossbar are shown, respectively. In Fig.5.5c, a 3D reconstructed AFM profile is shown. About 250 individual Pt/TaO_x/CrO_y/Cr cross-points for area sizes varying from 100nm x 100nm to 1μm x 1μm, and 64bit crossbars with half-pitch varying from 100nm x 100nm to 500nm x 500nm are built on the same sample following the proposed fabrication steps. In Fig.5.6a and Fig.5.6b, a tilted SEM view, and a 3D reconstructed AFM profile of a cross-point device with fence-like TE are shown, respectively.

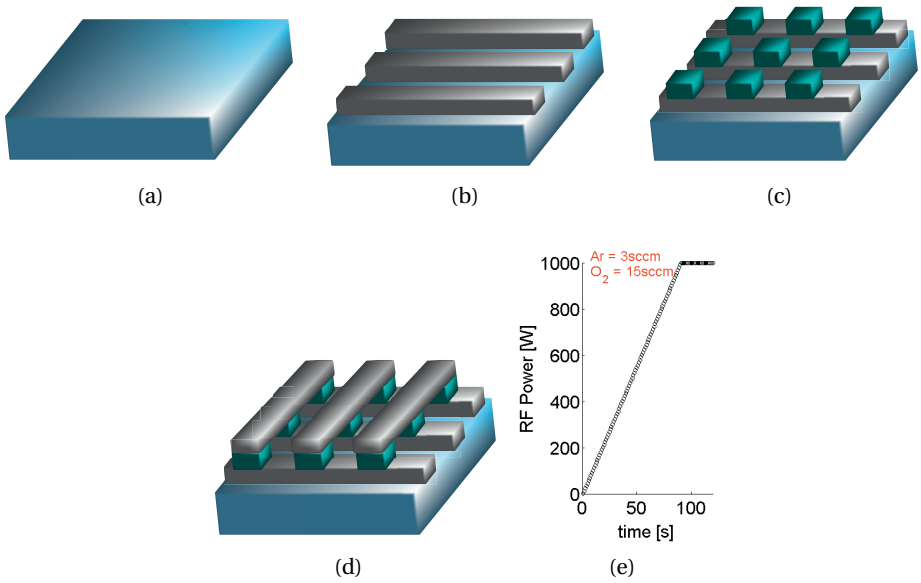


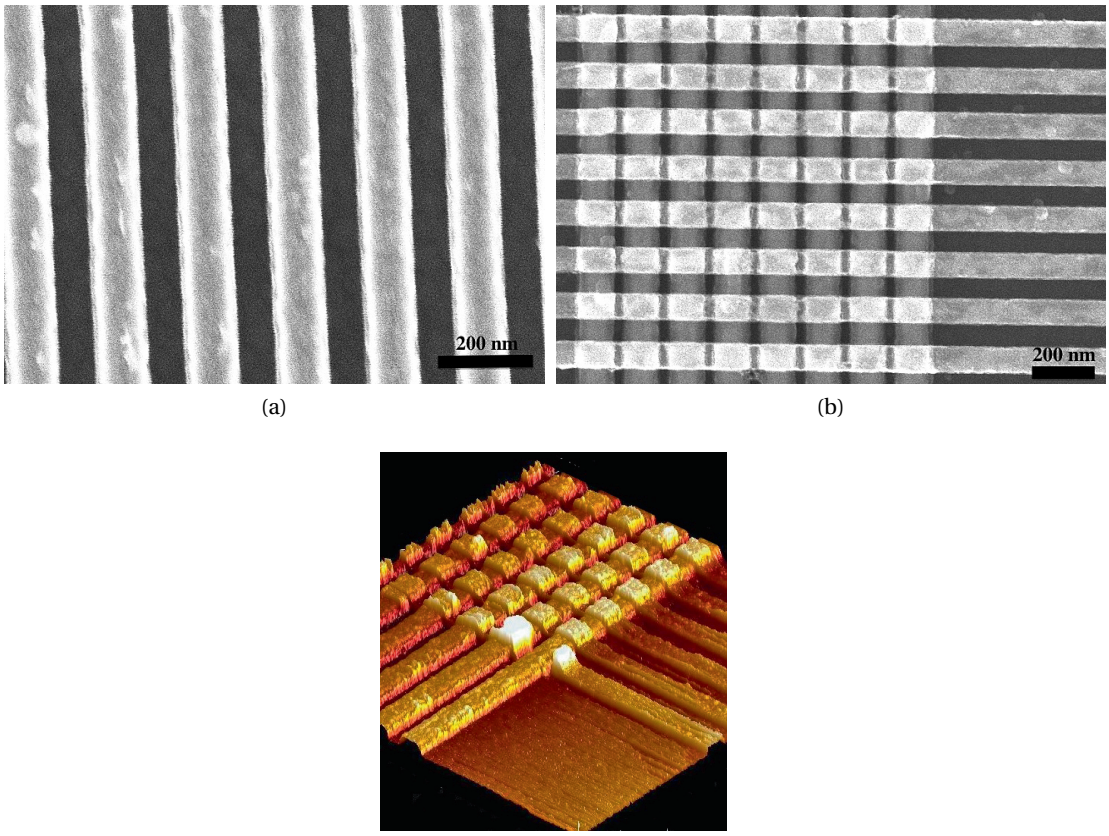
Figure 5.4: Process Flow. (a) Insulated Si substrate; (b) Pt bottom electrode lift-off; (c) TaO_x sputtering deposition; (d) TE lift-off (e) Sputtering parameters of TaO_x, with increasing RF power and constant 3sccm/15sccm Ar/O_2 flows.

5.2.3 Electrical Characterization

Electrical measurements are carried out with an Agilent B1500 semiconductor device analyzer. Pulse mode sweeps with pulses of 500μs demonstrate forming-free *Bipolar Resistive Switching (BRS)* for $Pt/TaO_x/CrO_y/Cr/Cu$ (Fig.5.21c). The BRS is obtained for a voltage range of less than 1V with pristine ON state in the same range of the *Low Resistance State (LRS)*. This is an important advantage compared with non forming-free ReRAM devices, because the forming operation requires higher voltages. A forming voltage of -3.4V has indeed been necessary for the $Al/TiO_2/Al$ (Fig.5.7b), that then show similar performance as the $Pt/TaO_x/CrO_y/Cr/Cu$ devices. In Table I structural and electrical parameters of the different cells are reported.

5.2.4 Discussion

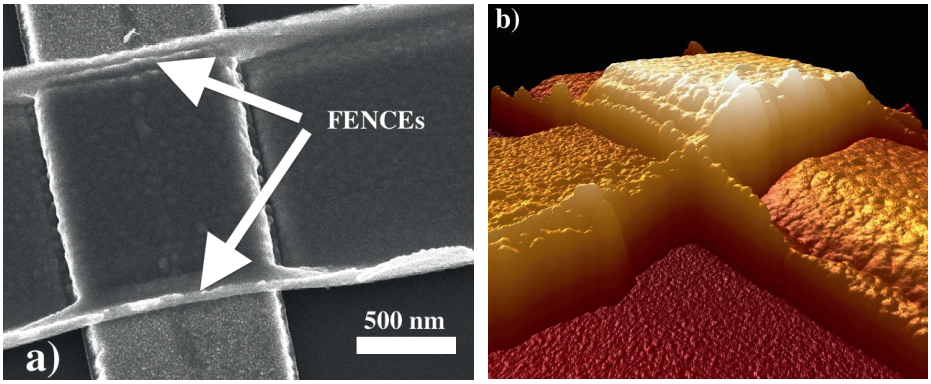
Material characterization has been carried out to understand the pristine ON state of the $Pt/TaO_x/CrO_y/Cr/Cu$ device. The X-ray diffraction pattern of Fig.5.8a shows peaks from the TE and the Si substrate. The absence of any Ta_2O_5 or TaO_2 peaks indicates that the material is in amorphous state, due to the low deposition temperature. The visible peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. The pristine ON state excludes the conductive filament mechanism and observing the double logarithmic plot of the *I-V* curve (Fig.5.9a), quasi-Ohmic regimes with slopes $\approx$1 are obtained for regions far from the SET condition. Typical trap-assisted *Space-Charge-Limited-Conduction (SCLC)* is observed close to the SET condition. The SCLC conduction is also observed for $Al/TiO_2/Al$ devices (Fig.5.9b) whose slopes indicate a more abrupt distribution of trap density, which can be



(a) (b)

(c)

Figure 5.5: Top SEM view of: (a) bottom electrode lines; (b) complete 64bit crossbar array of devices with 100nm half-pitch; (c) reconstructed 3D image from AFM profile.



(a) (b)

Figure 5.6: Pt/TaO_x/CrO_y/Cr/Cu cross-point device with 900nm x 900nm cross-point area. (a) Tilted SEM image view. Notice the fence-like structures at the edges of the TE line. (b) Reconstructed 3D AFM image of the pristine cross-point device. Average roughness on TE is $\sigma \approx$42.6nm.

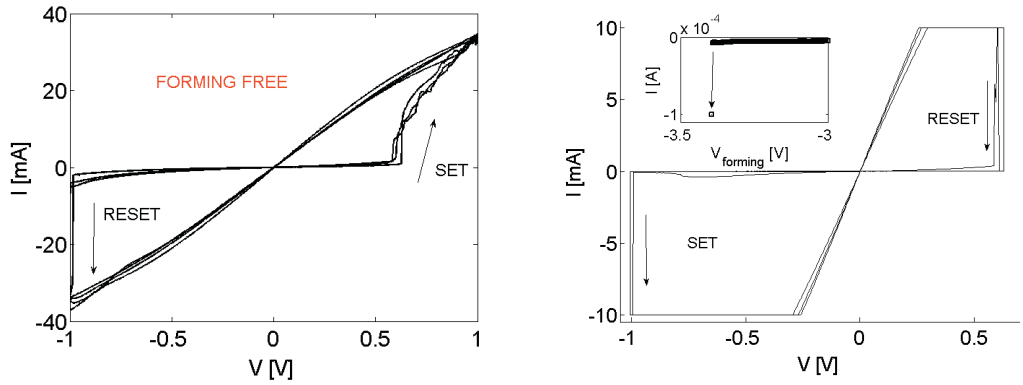
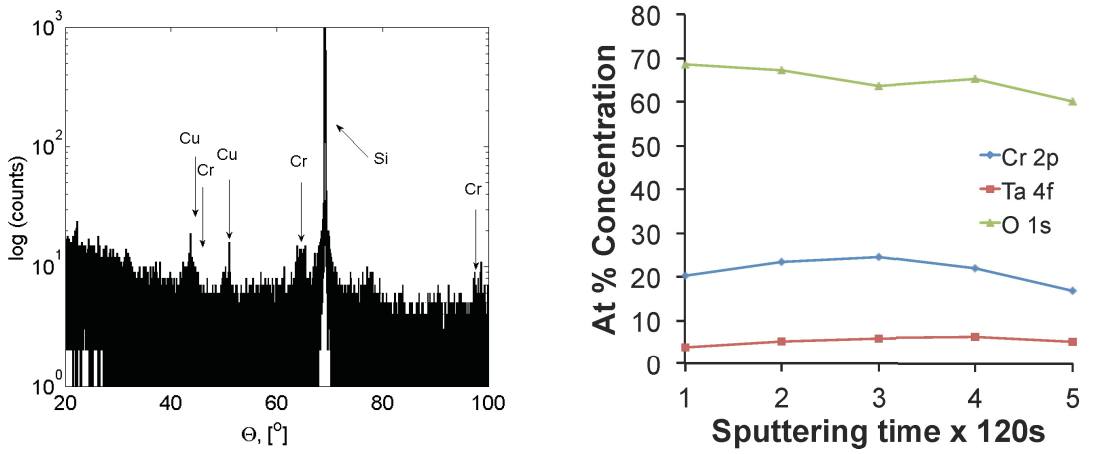


Figure 5.7: (a) Typical I-V characteristic of the Pt/TaO_x/CrO_y/Cr/Cu ReRAM cell showing resistance ratio of 10^4. Notice very low V_{SET} = +0.8V and VRESET=-1V. After fabrication the devices are forming-free and in the ON state. (b) Typical *I-V* characteristic of the Al/TiO_2/Al ReRAM cell after forming with $V_{SET} = -1V$ and $V_{RESET} = +0.8V$. Inset shows $V_{FORMING} = -3.4V$.

related to the different deposition methods. In both devices, the resistive switching mechanism can be attributed to Redox reaction linked with the motion of oxygen-vacancies [17, 18]. Moreover, structural modification is observed from the roughness profile of Pt/TaO_x/CrO_y/Cr/Cu cross-point after 100cycles. As shown in Fig.5.10a and Fig.5.10b, the Pt/TaO_x/CrO_y/Cr/Cu average roughness (Ra) measured above the TE broadens. The Ra changes from a pristine 100nm variation into a 200nm broad window, indicating structural modification by the motion of oxygen vacancies upon switching. In addition, XPS-depth analysis (Fig.5.8b) confirms that $Ta_2O_{5-\delta}$ and $TaO_{2-\gamma}$ phases are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE that is consistent with the Redox switching mechanism.

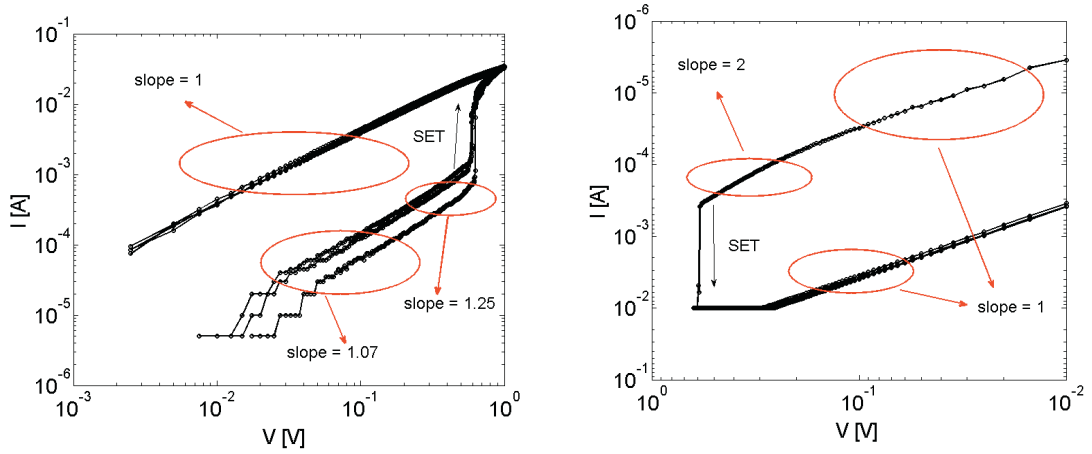
High Density Multi-Valued Crossbars

Several resistance levels of Pt/TaO_x/CrO_y/Cr/Cu devices can be programmed. As shown in Fig.5.11a, four levels of resistance (encoding 2bits) are found within a 4 orders of magnitude range. A larger resistance window of 1bit is found for Al/TiO_2/Al devices, which show a LRS around 30Ω and an HRS at 1M Ω within 2 orders of magnitude variation (see Fig.5.11b). The Al/TiO_2/Al show stable LRS and HRS in a large V_{READ} voltage range (Fig.5.12a). The Pt/TaO_x/CrO_y/Cr/Cu devices demonstrate excellent scalability, as the HRS/LRS ratio improves for smaller device sizes (Fig.5.12b). For instance, 2bit can be written in a Pt/TaO_x/CrO_y/Cr/Cu by using shorter SET pulses in order to program the cell in one of the stable *Intermediate Resistance (IR)* states. An example of 2bit storage using LRS, HRS and 2 IRs is demonstrated in Fig. 5.13, each level is separated of about one order of magnitude from each other for various V_{READ}. The devices could be easily assembled into dense 2.5x10^9bit/cm^2 passive crossbar arrays whose storage density improves to 10^{10}bit/cm^2 thanks to ML capability of Pt/TaO_x/CrO_y/Cr ReRAMs.



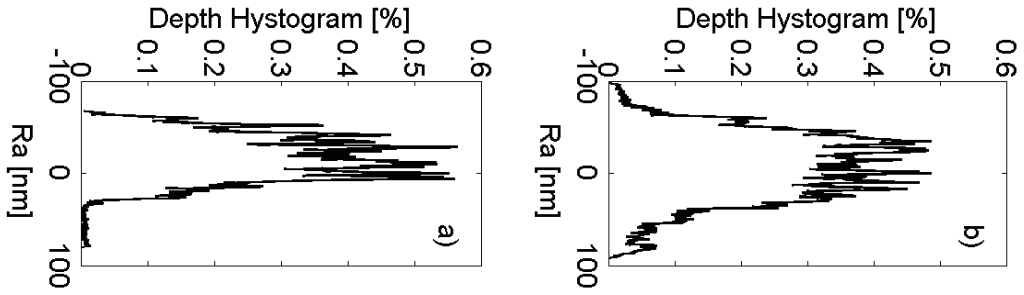
(a) (b)

Figure 5.8: (a) X-ray diffraction pattern on a Si wafer demonstrating amorphous TaO_x/CrO_y. The peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. (b) XPS depth profile analysis showing the presence of both Cr and Ta in oxidized states. Both $Ta_2O_{5-\delta}$ and$TaO_{2-\gamma}$ are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE.



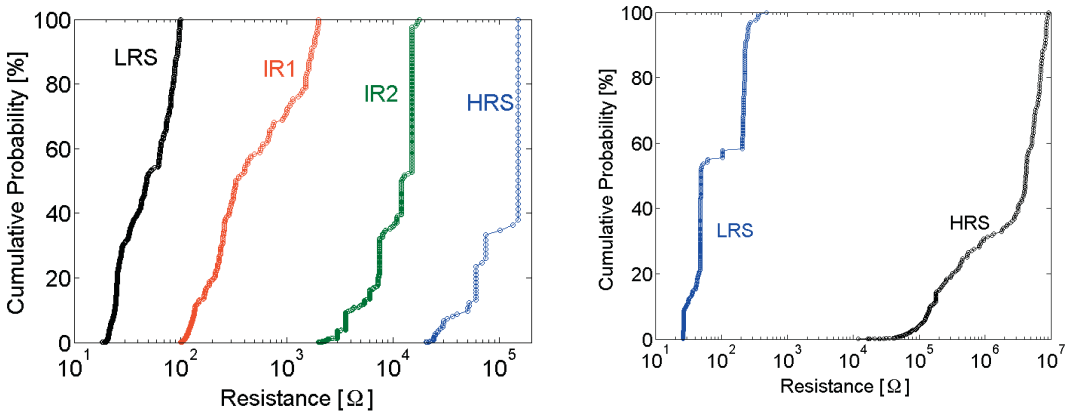
(a)

Figure 5.9: (a) The log(I)-log(V) plot of $Pt/TaO_x/CrO_y/Cr/Cu$ shows typical trap-controlled conduction of *Space-Charge-Limited-Conduction (SCLC)* before SET. In the SET region, the slope is about 25 and it is indication of gradual distribution of defects. (b) The log(I)-log(V) plot of the $Al/TiO_2/Al$ shows typical trap-controlled conduction of SCLC with quadratic V dependence before SET condition, thus following Child's law dependence. In the SET region, the slope is about 50, and it is indication of an abrupt distribution of defects.



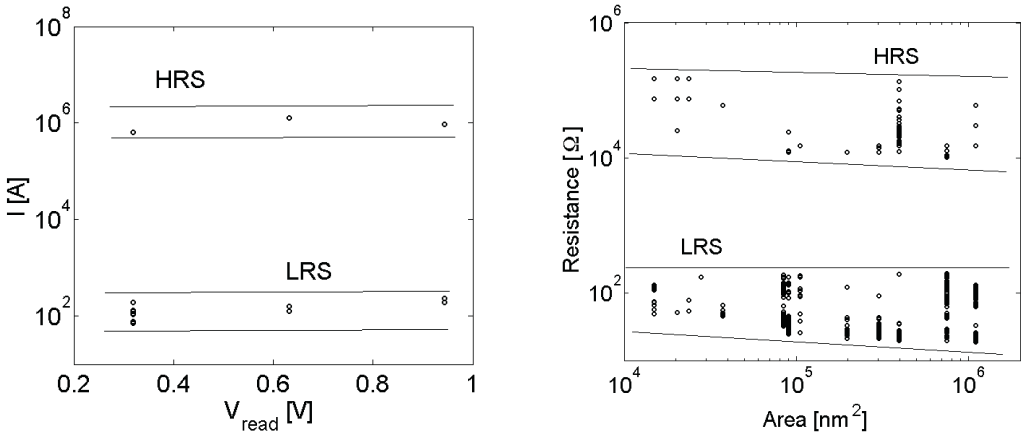
(a) (b)

Figure 5.10: Average roughness profiles for TaO_x cross-points: (a) $\sigma \approx 42.6$nm after fabrication; (b) $\sigma \approx 56.3$nm after 100 cycles. The broadening is attributed to the structural change induced by the motion of oxygen-vacancies upon cycling.



(a) (b)

Figure 5.11: (a) Cumulative probability of *Low Resistance State (LRS), Intermediate Resistance states 1 (IR1) and 2 (IR2)* and *High Resistance State (HRS)* for $Pt/TaO_x/CrO_y/Cr$ devices are shown. The LRS, IR1 and IR2 are obtained by using SET pulses of 2ms, 1ms and 500μs at 1V, respectively. The HRS is obtained with a 500μs RESET pulse at -1V. (b) Cumulative probability of LRS and HRS for $Al/TiO_2/Al$ devices are shown. The LRS and the HRS are obtained by using SET and RESET pulses of 500μs at -1V and +1V, respectively.



(a) (b)

Figure 5.12: (a) LRS and HRS resistance distributions for increasing V_{READ} of the Al/TiO_2/Al cell. The 10^4 resistance ratio is constant over a large range of reading voltage. (b) Measured HRS and LRS values for the Pt/TaO_x/CrO_y/Cr cell devices with different cross-point area demonstrating excellent scalability, indicating local switching at the nanoscale.

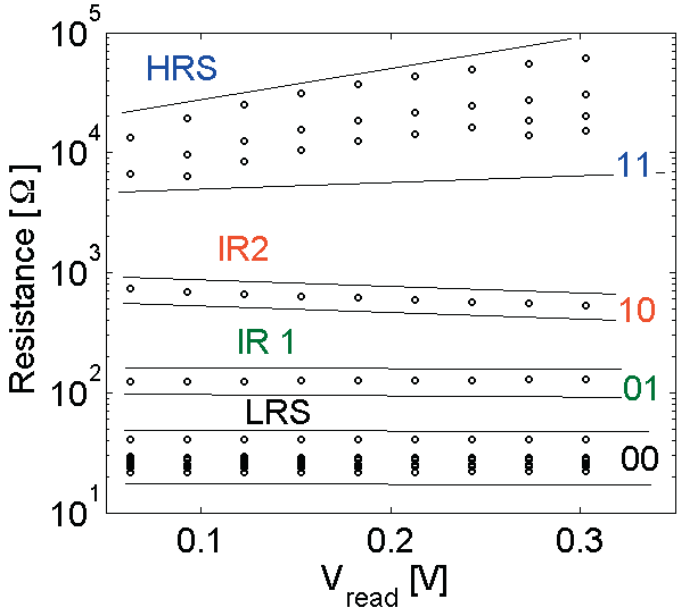


Figure 5.13: Resistance distributions for multi-value storages vs. increasing V_{READ} of the Pt/TaO_x/CrO_y/Cr cell. The HRS, IR2, IR1, LRS are encoded in 2bit.

5.2.5 Summary

Bipolar Resistive Switching Pt/TaO_x/CrO_y/Cr/Cu and Al/TiO_2/Al devices built with thermal budget ≤200°C have been fabricated and characterized. Very large storage density of TaO_x/CrO_y based ReRAMs is demonstrated up to 10^{10}bit/cm^2 thanks to the excellent scalability of the fence-like top electrode lines.

5.3 Generic Memory Structure (GMS) for non-volatile FPGAs

5.3.1 Introduction

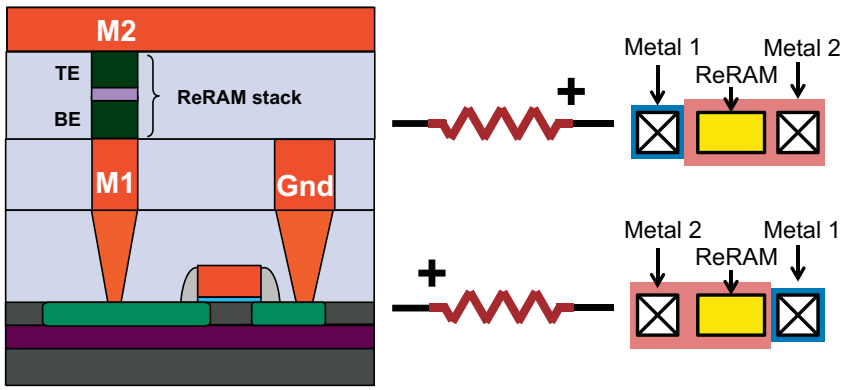
While a lot of research effort targets high density ReRAM-based standalone memories [19], the focus of this work is the usage of ReRAMs for FPGAs. The reason behind this choice is that in reconfigurable logic, up to 40% of the area is dedicated to the storage of configuration signals [20]. Traditionally, the configuration data is serially loaded in SRAM cells, distributed throughout the circuit [21]. As a consequence, power up of the circuit is limited by the slow serial configuration. To overpass SRAM volatility and loading time issue, Flash NVM have been proposed [22]. Nevertheless, the use of an hybrid CMOS-Flash technology results in high fabrication costs. Conversely, ReRAMs are fabricated within the Back-End-of-the-Line (BEoL) metal lines, moving the configuration memory to the top of the chip and reducing the area utilization [23]. Similarly, the ReRAM cells can be utilized in combination with TSVs, enabling 3-D stacked FPGA architectures [3]. In this paper, we propose a complete proof of concept of an ReRAM-based *Generic Memristive Structure (GMS)* circuit for FPGAs from technology development to architectural evaluation. The main idea is to replace the pass-transistors in SRAM-based FPGAs by ReRAMs. Hence, the ReRAMs store the information in their resistive states and can be either used to route signals through lowresistive paths, or to isolate them by means of high-resistive paths. Such a functionality is envisaged either to build routing Multiplexers (MUXs) or configuration nodes. In order to keep the programming complexity in the same range of SRAM-based FPGAs, we propose an efficient methodology based on the inherent GMS complementary programming. The proposed methodology, with GMS-based complementary programming has been validated by electrical measurements on a fabricated device.

5.3.2 BEoL integration of ReRAMs

As per the previous section, ReRAMs can be fabricated within the BEoL processing. Hence, it is possible to fabricate them between two metal layers (e.g. in between Metal 1 and Metal 2). Because of the BRS of the ReRAMs of this study, depending on the forming polarity, either the Metal 1 or the Metal 2 terminal can be utilized as the positive electrode of the memory, giving two possible configurations (see Fig.5.14a).

5.3.3 Device Description

In the GMS, two ReRAMs are interconnected as shown in Fig.5.15a. The positive terminal of the top memory is connected to the negative terminal of the bottom memory. This arrangement



(a) (b)

Figure 5.14: Cross sectional schematic showing the integration of a ReRAM integrated between the M1 and M2 interconnection levels in the back-end-of-line. (a) The bottom electrode is thus directly connected to a MOSFET selector (bottom) forming a 1-Transistor 1-Resistor (1T1R) memory node. (b) ReRAM polarity selection by physical design.

enables complementary programming of the two ReRAMs composing a GMS. We call the concurrent programming of the GMS a complementary programming operation. A similar programming scheme was previously used for low power crossbars [24]. Fig.5.15b illustrates the programming of the top path (i.e. left to right arrow in the programming graph shown in Fig. 5.15d). R_1 and R_2 are switched simultaneously to R_{OFF} and to R_{ON} respectively. This operation is achieved by grounding the common right terminal and biasing the left terminal to $-V$th (which corresponds to the SET voltage $-V$th for R_1 and to the RESET voltage $+V$th for R_2). The programming of the bottom path (see Fig.5.15c) is obtained by inverting the $-V$th and the GND (which corresponds to the RESET voltage for R_1 and to the SET voltage for R_2). In addition to speed up the programming operation, due to the complementary scheme, only two voltages are needed (GND and Vth).

The complementary programming operation has been validated by electrical measurements, while the MUX performances have been extracted by electrical simulations. Fig.5.16 depicts the resistance values of R_1 and R_2 of an GMS-based MUX21. Resistances are read at V_{READ}= +0.1V.

After a preliminary forming step, R_1 and R_2 are set to R_{ON}. The devices are then read for 10 cycles, showing a stable non-volatile resistance. Hence R_1 and R_2 are switched using the complementary programming operation presented in the previous section. During the first writing operation SET and RESET events are induced on R_2 and R_1, respectively (see Fig.5.15c) by applying a voltage pulse for 500μs. After reading the resistance values for another 10 cycles, again validating the non-volatility of the resistance states, a second complementary switching operation is performed. Now the resistance states of R_1 and R_2 are complementary switching, as seen in the reading sequence of Fig.5.16. As can be noticed the resistance values of R_1 and R_2 do not exactly match. This is due to the different ReRAM geometries and to the large variability of the cells utilized for the demonstrator. Nevertheless, improved variability of one order of magnitude has been demonstrated for ReRAM prototypes fabricated with industrial

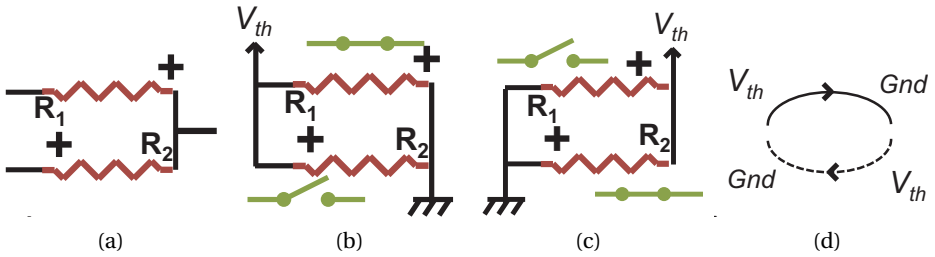


Figure 5.15: GMS complementary programming. (a) Two BRS resistive RAMs are in series connected after forming. (b) When V_{th} is applied, R_1 switches ON, while R_2 switches OFF. (c) When $-V_{\text{th}}$ is applied, R_1 switches OFF, while R_2 switches ON. (d) Graph representation of the complementary switching operation.

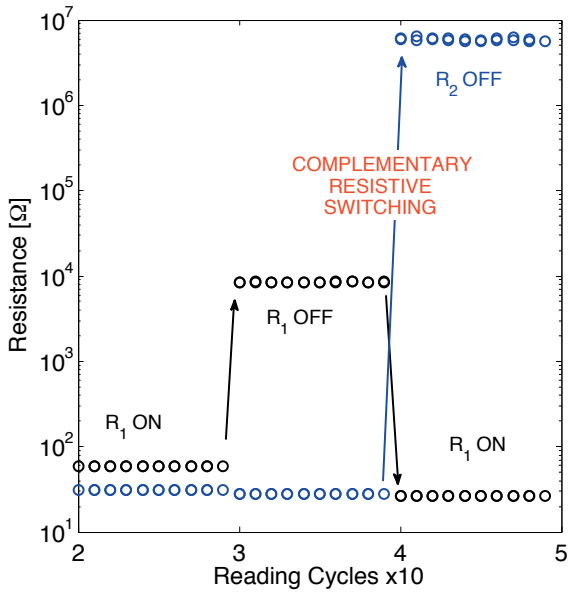


Figure 5.16: Complementary switching operation for the ReRAM-based GMS.

methods [25].

5.3.4 GMS memory node

In this section, we present an elementary circuit used to move most of the configuration part of reprogrammable circuits to the back-end, reducing their impact on front-end occupancy. Such a memory node is dedicated to drive LUT inputs. The memory node is based on a unique GMS node and provides intrinsically the retained information as a voltage level. Furthermore, it shall allow a layout efficient line sharing.

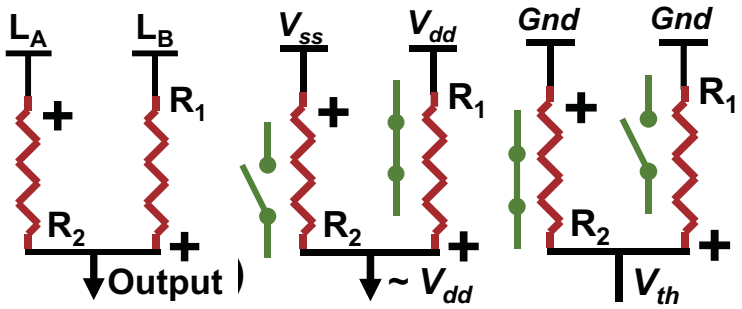


Figure 5.17: GMS complementary programming: (a) Two in-series connected BRS RAMs forming a voltage divider between 2 metal lines, LA, LB. (b) Voltage distribution to program a logic 1 into the GMS cell. (c) Voltage distribution to program a logic 0 into the GMS cell.

Overall Structure

The basic memory node is presented in Fig. 5.17c . The circuit consists of 2 ReRAMs connected in a voltage divider configuration between 2 fixed voltage lines (LA and LB). The memories are used in a complementary manner, in order to improve reliability. Reliability is required as far as the output is not restored by an inverter for compactness purpose. The output is designed to place a fixed voltage on a conventional standard cell input. Read operations are intrinsic with the structure, while programming is an external operation to perform on the cell.

Read operation

A voltage divider is used in this topology to intrinsically realize the conversion from a bit of data stored in the variable resistance to voltage level. Fig. 5.17b presents a configuration example where the node stores a '1'. Voltage lines LA and LB are respectively connected to VSS and VDD. For the sake of example, consider that the resistive memory R_1, connected to the VDD line, is configured to the low resistivity state. The other memory R_2, connected to VSS, is in the high resistivity state. As a consequence, a voltage divider is configured and the output node is charged close to the voltage of the branch with a high conductivity.

Write Operation

Fig. 5.17c presents the programming phase of the node. First, the lines LA and LB are disconnected from the power lines and connected to the programming signals. The programming signals are chosen according to the GMS programming scheme. Fig. 5.18 presents the programming circuits required to program an array of GMS-based configuration memories. To provide individual access, each GMS has its own selection transistor. Thus, the different lines can be shared in a standalone-memory-type architecture, yielding an efficient layout strategy. The different modes and programming signals are selected by line-driving multiplexers.

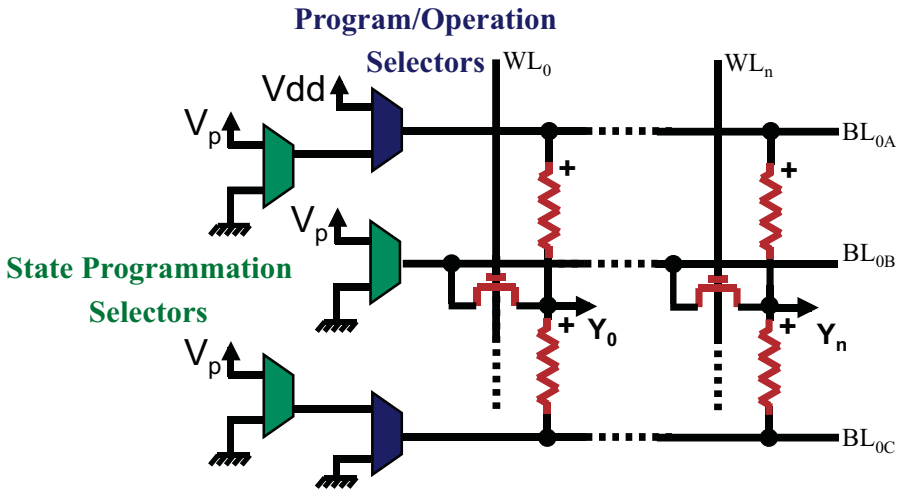


Figure 5.18: Complementary switching operation for the ReRAM-based GMS.

5.3.5 Summary

This paper introduced a novel design, called GMS, based on resistive memories, designed to replace traditional routing resources in reconfigurable logic circuits. Resistive RAM memories combined into a complementary switching GMS cells were used to reduce the footprint and to improve the electrical performances of the data path. The GMS cell can also be used to replace standalone memories, leading to more compact LUTs and steering logic, due to the BEoL integration of ReRAMs.

Thanks to ReRAMs, the area and the delay are reduced by 7% and 58% respectively due to the compactness and the low on-resistance of ReRAMs.

5.4 Resistive Programmable TSVs

In this section, BEoL technology for 3D interconnects is addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in *three-dimensional (3D)* wafer/chip stacking solutions utilizing *Through Silicon Vias (TSVs)* [26] as well as in reconfigurable interconnect fabrics. The discussed BEoL demonstrate the co-integration of TSVs with ReRAM stacks, offering a new path for re-programmable 3D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3D chip interconnects. the fabrication and characterization of titanium dioxide (TiO_2)-based *resistive RAM (ReRAM)* co-integration with 380 μm-height Cu *Through Silicon Via (TSV)* arrays for programmable 3D interconnects is discussed. Non-volatile resistive switching of Pt/TiO_2/Pt thin films are first characterized with resistance ratio up to 5 orders of magnitude. Then co-integration of Pt/TiO_2/Pt or Pt/TiO_2 memory cells on 140 μm and 60 μm diameter Cu TSV are fabricated. Repeatable non-volatile bipolar switching of the ReRAM cells are demonstrated for different structures.

5.4.1 Fabrication

Planar ReRAM devices

First, high resistivity p-type ($N_A \approx 10^{15}$atoms/cm^2) bulk-Si wafers are prepared by 500nm thermal oxidation in H_2O atmosphere. Then the deposition of the resistive switching materials is performed by sputtering of Pt/TiO_2/Pt layers with 270nm/80nm/270nm thicknesses. A conceptual picture is shown in Fig. 5.19a. The top electrode area of 100μm by 100μm squares were patterned by standard lithography and etched by ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

TSV devices

The resistive switching materials were integrated with TSVs producing two different devices:

- 140μm TSV diameter in 380μm thick wafer, using Pt/TiO_2/Pt memory stack
- 60μm TSV diameter in 380μm thick wafer, using Cu/TiO_2/Pt memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

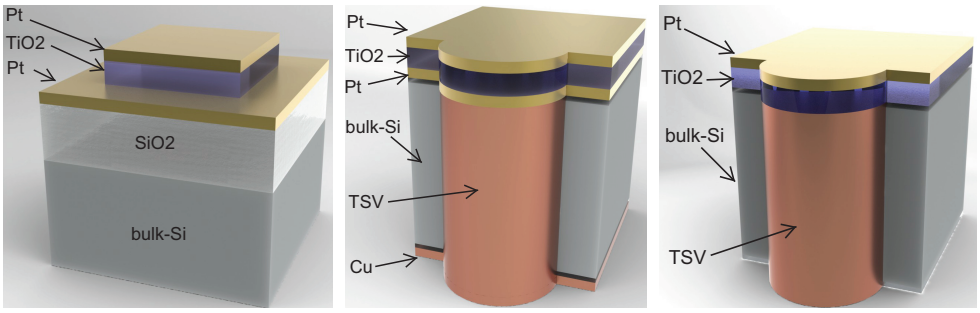
The TSVs are fabricated using the same process in both cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through wafer etch, RCA wafer cleaning and thermal oxidation in water atmosphere to grow a 3μm thick oxide. A 750 nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

TSV with Pt/TiO_2/Pt ReRAM

For the first type of devices, once the TSVs are fabricated the front side of the wafer is processed with *Chemical Mechanical Polishing (CMP)* technique to form a flat surface. The Pt/TiO_2/Pt stack is sputtered with layer thicknesses 270nm/80nm/270nm accordingly. A concept picture of the fabricated structure can be seen in Fig. 5.19b.

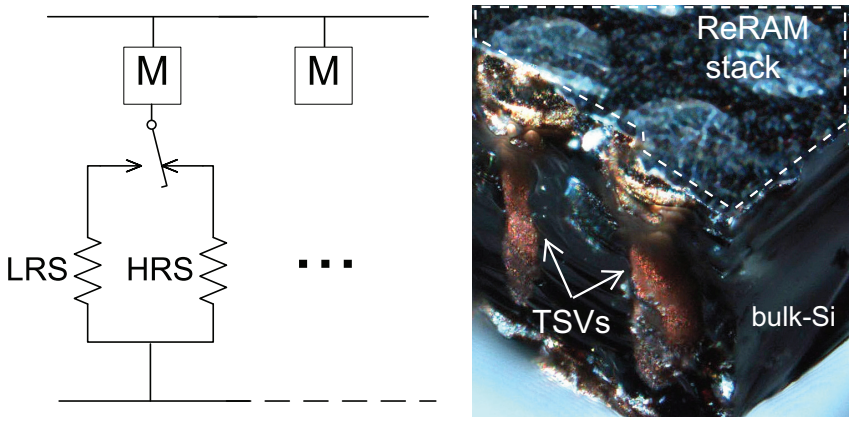
TSV with Cu/TiO_2/Pt ReRAM

For the second type of devices the wafer is polished using CMP on both sides to remove the seed layer and to planarize the surfaces. The Cu was then cleaned using a $NH_4 : H_2SO_4$ etching solution at room temperature for 10 minutes. Then the wafer was loaded into a vacuumed sputtering chamber and a TiO_2/Pt layer was deposited with thicknesses of 80nm and 270nm respectively. The Cu of the TSV is acting as the bottom electrode of the ReRAM (see Fig. 5.19c). Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Fig. 5.20a and 5.20b, respectively.



(a) (b) (c)

Figure 5.19: (a) Concept image of planar ReRAM made of $Pt/TiO_2/Pt$ stack. (b) Concept image of the ReRAM-TSV using $Pt/TiO_2/Pt$ programmable fuse. (c) Concept image of the ReRAM-TSV using $Cu/TiO_2/Pt$ programmable fuse.



(a) (b)

Figure 5.20: (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element M). (b) Reconstructed 3D photograph of the TSV – $Cu/TiO_2/Pt$ device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

5.4.2 Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station in dark conditions. For electrical contacts, standard tungsten needles with 15μm apex diameter were placed on the top electrode area very softly, since a dependence of the switching with needle pressure has been observed, similarly to the observation of local pressure modulated conductance with AFM tips [27]. Then double $I-V$ DC sweeps have been used to investigate the resistive switching behavior. In all the cases, bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table 5.1.

5.4.3 Planar ReRAM devices

First the planar Pt/TiO_2/Pt are characterized and it showed stable and repeatable bipolar switching behavior between 10 Ω and 1MΩ read or measured at +1V (see Fig. 5.26a). Originally the devices are in the high resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low resistance state (LRS) occurs at +1.8V. After the SET event, the voltage sweep continues until +2V and then move backward toward negative voltage region. When −1.3V is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about 5 orders of magnitude is read at +0.5V.

5.4.4 TSV − Pt/TiO_2/Pt devices

Next, TSV − Pt/TiO_2/Pt with the same layer thicknesses are measured, showing resistance switching below ± 1V (see Fig. 5.26b). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks as well as to surface states acting as dopants for the TiO_2 [28]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only +0.6V, while the RESET voltage is measured at −0.5V. Using a reading voltage of +0.2V, an HRS of 2MΩ and a LRS of 665Ω, with resistance ratio of 3000 are measured.

5.4.5 TSV − Cu/TiO_2/Pt devices

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the TiO_2 layer [29, 30], that is a n-type semiconductor, an alternative device is obtained by depositing TiO_2 and Pt directly on top of the Cu − TSV. Thus, thanks to a larger Schottky barrier height at the Cu − TiO_2 interface, a larger programming window is obtained (Fig. 5.21c). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. A HRS of 500MΩ and LRS of 5kΩ are read at +1V.

Device	SET	RESET	HRS	LRS	HRS/LRS	Reading
Planar $Pt/TiO_2/Pt$	+1.8V	−1.3V	10MΩ	10Ω	10^5	+1V
$TSV-Pt/TiO_2/Pt$	+0.6 V	−0.5V	2MΩ	665Ω	3003	+0.2V
$TSV-Cu/TiO_2/Pt$	−4.2V	+5V	500MΩ	5Ω	10^5	+1V

Table 5.1: Obtained ReRAM electrical parameters for the different devices

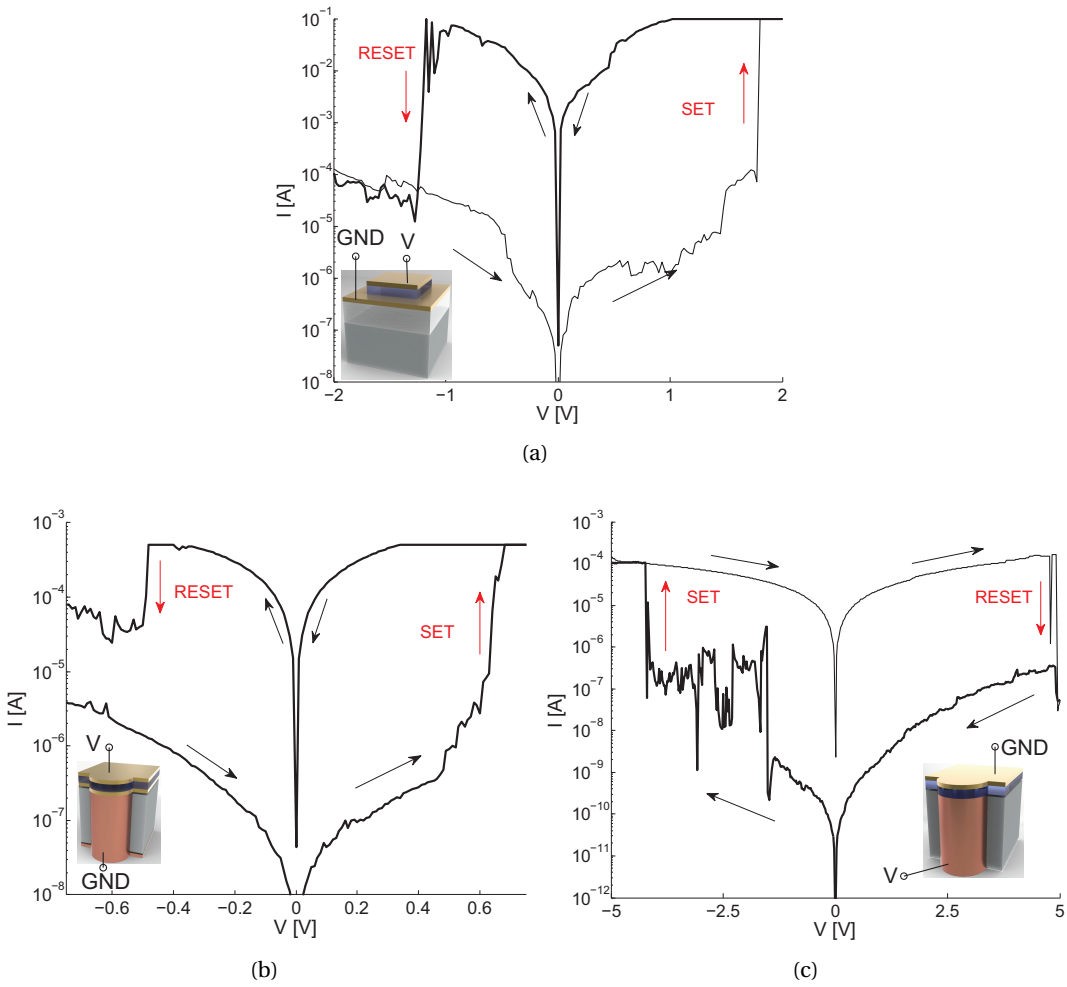


Figure 5.21: (a) Resistive switching through $I-V$ sweeps for planar $Pt/TiO_2/Pt$. (b) Resistive switching through $I-V$ sweeps using $TSV-Pt/TiO_2/Pt$ programmable fuse. (c) Resistive switching through $I-V$ sweeps using $TSV-Cu/TiO_2/Pt$ programmable fuse.

5.4.6 Summary

In this study, Pt/TiO_2/Pt obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with LRS to HRS resistance ratio up to 5 orders of magnitude. The device is successfully integrated on top of 140μm and 60μm TSV arrays either in the full Pt/TiO_2/Pt stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The co-integration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3D chip interconnects.

5.5 Sensing

5.5.1 Temperature sensing with Ambipolar Si nanowire transistors

This section reports on the fabrication and characterization of a pA current and temperature sensing device with ultra-low power consumption based on a Schottky barrier silicon nanowire transistor. Thermionic and trap-assisted tunneling current conduction mechanisms are identified and discussed on the base of the device sensitivity upon current and temperature biasing. In particular, very low current sensing properties are confirmed also with previously reported polysilicon-channel nanowire Schottky barrier transistors. demonstrating that these devices are suitable for temperature and current sensing applications. Moreover, the process flow compatibility for both sensing and logic applications makes these devices suitable for heterogeneous integration. In this work we extend the application of Si nanowires to temperature sensing. A range of device operation conditions are investigated, showing how an ambipolar device can be used for different applications, the only requirement being the biasing condition.

Device Description

The device scheme consists of a suspended Si nanowire having NiSi silicide source/drain junctions with 2 parallel polysilicon gates having gate-all-around (GAA) configuration on a SOI substrate. Typical Si nanowire with drop-like cross-section shape has an average diameter of 100nm.

Device Fabrication

The process flow is based on a previously reported technique utilized for the fabrication of vertically-stacked Si nanowire FET arrays [31]. Here a deep reactive ion etching technique is adapted to form a single suspended Si ribbon over the buried oxide. A sacrificial oxidation is performed to reduce the cross-section down to a 100nm. Then a 20nm dry oxidation is performed followed by a 500nm polysilicon layer deposited by low pressure chemical vapor deposition. Contact regions are etched in a low temperature oxide passivation layer. Then a 50nm Ni + 10nm Al bi-layer is evaporated and annealed to form a silicide/Si mid-gap Schottky junction. The Al is used as a cap layer to prevent Ni oxidation during the silicidation step and to provide a good interface with final metallization. Finally, 1μm thick Al is patterned for

electrical characterizations.

I-V dependence

For Schottky barrier FETs, Ids can be described by the sum of a tunneling I_{tunnel} and a thermionic-emission I_{th} component [32]:

$$I_{\text{ds}} = I_{\text{th}} + I_{\text{tunnel}} \tag{5.1}$$

$$I_{\text{th}} = A_C A^* T^2 e^{\left(-\frac{\phi_{\text{Beff}}}{kT}\right)} \left\{ e^{\left(-\frac{\phi_{V\text{a}}}{kT}\right)} - 1 \right\} \tag{5.2}$$

$$I_{\text{tunnel}} = A_C \frac{q^2 F^2}{8\pi h \phi_{\text{Beff}}} e^{\left(-\frac{8\pi}{3hqF}\sqrt{2m(q\phi_{\text{Beff}})^3}\right)} \tag{5.3}$$

Where A_C is the contact area of the source to channel junction, F the electric field across the Schottky barrier, A^* the Richardson's constant, h the Plank's constant, m the electron rest mass, q the elementary electron charge, ϕ_{Beff} the effective Schottky barrier height, T the temperature, V_{a} the applied voltage across the Schottky junction, k the Boltzmann's constant.

Temperature dependence

The $I_{\text{ds}} - V_{\text{gs}}$ dependence with T is mainly attributed to the I_{th}, however T also influences the I_{tunnel} since hotter carriers pass through a narrower Schottky barrier, leading to an increasing current level [32]. The I_{OFF} current is increasing exponentially with temperature and, as suggested by Eq. 5.2, its main contribution is a thermionic emission component. A different behavior has been observed for the I_{ON} current. Increasing the temperature makes the I_{ON} current to decrease until the temperature reaches 55°C and then it rise exponentially with linear increase of T. At lower temperatures tunneling and trap-assisted tunneling are more important than thermionic emission. Rising T up to 70°C makes the charges trapped into the gate oxide to un-trap, reducing the I_{tunnel} component. A different behavior is observed for the I_{ON} currents for 70°C≤T≤115°C. In this range, the I_{ON} exponentially increases with T. This effect is evidence of two main current components, for which the I_{ON} changes from a tunneling to a thermionic emission dominated regime. A set of $I_{\text{ds}} - V_{\text{ds}}$ curves (Fig. 5.22a) taken at different temperatures at constant V_{ds} = 100mV and V_{bg} = 5V are used to extrapolate the Arrhenius plot shown in Fig. 5.23a. The constant V_{bg} = 5V is used to set the device operation more favorable for electron conductance at low V_{gs}. Constant subthreshold swings ≈ 110mV/dec are observed independently from the temperature (see Fig. 5.22b). Low negative V_{gs} voltages ranging from −1V to 0V show an almost linear slope with inverse of temperature and can be correlated to a thermionic-emission regime. However, for this V_{gs} range the current level is on the order of fAs, which is comparable to the background noise, and it cannot be used to extrapolate the Schottky barrier height. Another distinct regime is observed for $-0.3\text{V} \leq V_{\text{gs}} \leq -0.5\text{V}$, for which the slopes are greatly affected by tunneling. This regime shows a dominant tunneling component for the two lowest temperatures. Finally, an exponential

dependence with T is observed again for $V_{gs}\geq$0V with the exception of the lower temperature. All these regimes demonstrate that the current in our device is mainly thermionic for $T\geq$ 70°C and that the tunneling contribution is trap assisted. The slopes from the Arrhenius plot are then used to extract the effective Schottky barrier height ϕ_{Beff} with the activation energy E_a method. As shown in inset A of Fig. 5.23b, an average effective barrier height $E_a\approx 450\pm 5$meV is found over a large range of $V_{gs\geq 0.2V}$. However, these values cannot be taken as Schottky barrier height since in this regime the device has both tunneling and thermionic components. As suggested by Svensson et al. [33], a better evaluation of the Schottky barrier height can be taken at the maximum of E_a for low current levels. As shown in the inset B of Fig. 5.23b, this maximum corresponds to $V_{gs}=-0.45$V and gives a $\phi_{Beff}=$ 525meV, confirming the mid-gap Schottky barrier height.

Current sensing

Current biasing the devices with a constant Ids current makes the device to behave as a pseudo-inverter configuration with hysteretic transfer function. Thanks to the ambipolarity, the $V_{out}-V_{in}$ curves shift linearly with the applied current bias. For instance in Fig. 5.24a, low pA current levels can be either read from the high-to-low or the low-to-high transition voltage with sensitivities of 17mV/pA. A similar biasing scheme for polysilicon nanowires has been previously characterized by the authors show a similar trend. In Fig. 5.24b, forward and reverse threshold voltages for currents between 100fA and 500fA show a linear increase with current.

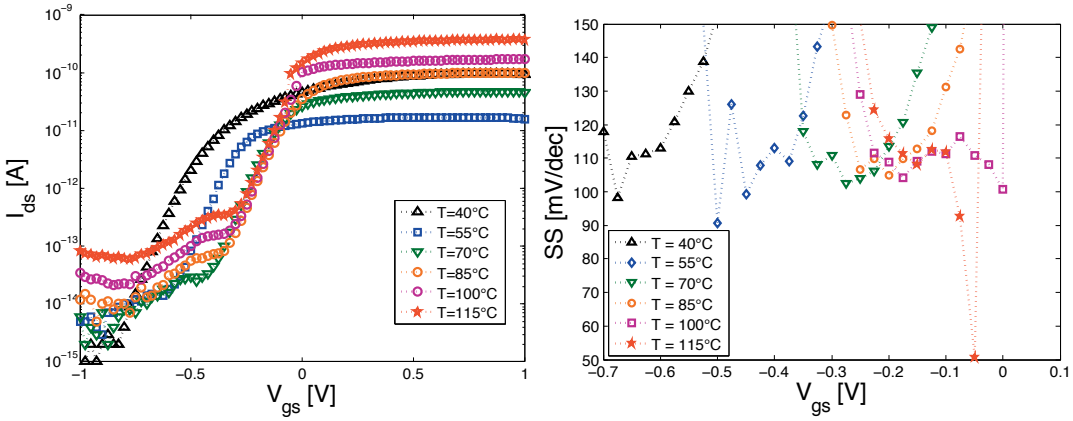
Temperature sensing

Upon application of increasing temperature of operation, the hysteresis window observed in pseudo-inverter biasing scheme shrinks. The crystalline Si nanowire Schottky barrier FET shows different sensitivities at different temperature regimes, depending on which mechanism dominates the conductance. Since the hysteresis is attributed to the storage of charges in either gate oxide and/or at the Schottky barrier junctions [34], an increased hysteresis window is expected for the lowest temperatures. The highest sensitivity of 40mV/°C is found in the T range around 40°C at which the trap tunneling mechanisms dominates. For temperatures higher than 55°C the sensitivity tends to saturate according to the dominance of thermionic current contribution, leading to lower sensitivity of 10mV/°C. In Fig. 5.24c the hysteresis window shrink for increasing T when 70°C≤T≤100°C is shown.

5.5.2 Bio-sensing with memristive ambipolar Si nanowires

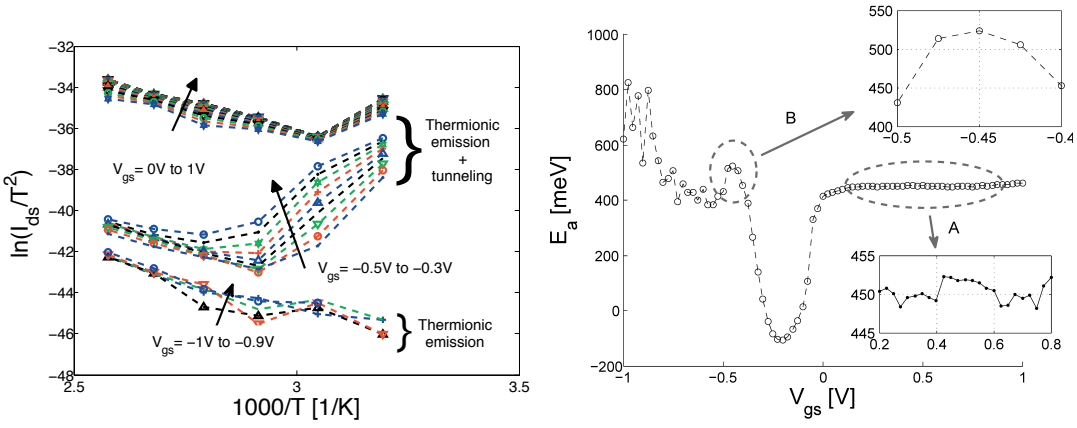
Introduction

Recently, there has been an increasing interest in nano-bio-sensing applications, due to possibility for minimal invasive, real-time monitoring for preventive treatments and therapy personalization [36]. In particular, one-dimensional silicon nanowires are good candidates for sensing devices due to their very large surface-to-volume ratio and quantum properties [37]. However, the sensing with nanowires is only exploited by the ion-sensitive field-



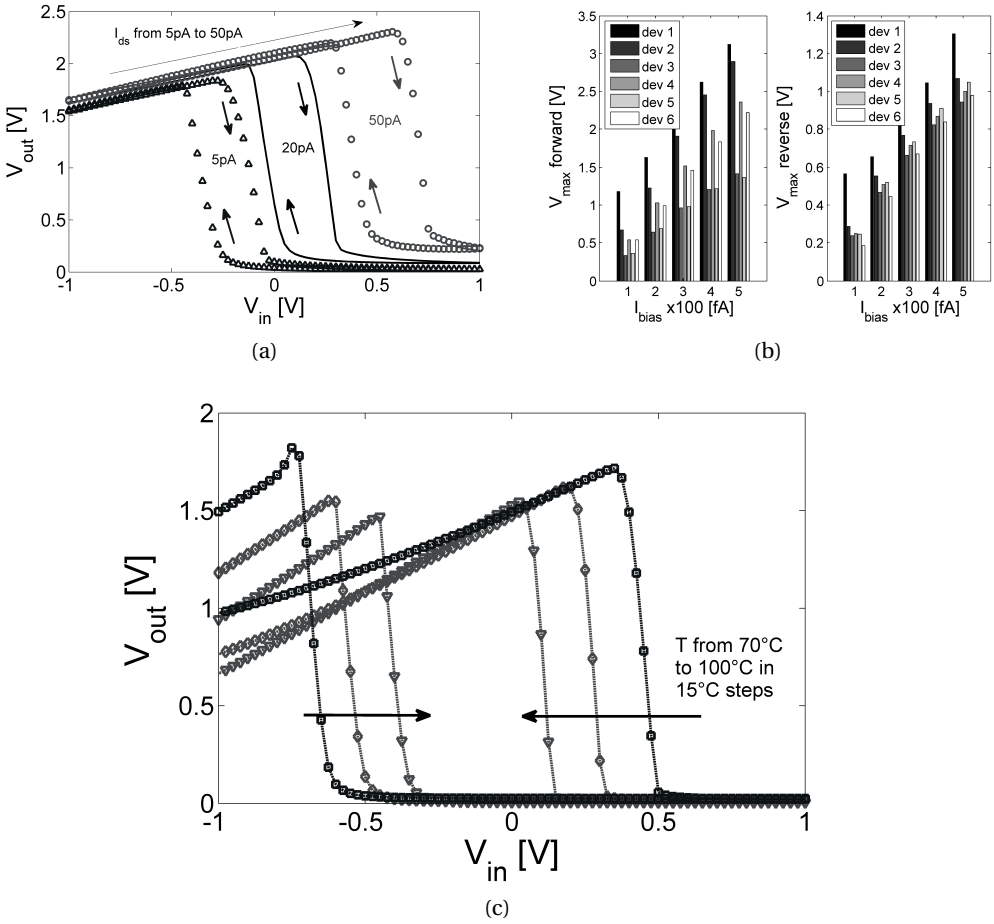
(a) (b)

Figure 5.22: (a) Effect of the temperature on the ambipolar I_{ds}–V_{gs} at V_{ds} = 100mV. (b) Subthreshold swings associated with the I_{ds}–V_{gs} plots. Very low swing minima are measured at 100°C and 115°C close to threshold voltages. Notice the voltage shift with temperature increase and the extremely low minima of 50mV/dec for the highest temperature.



(a) (b)

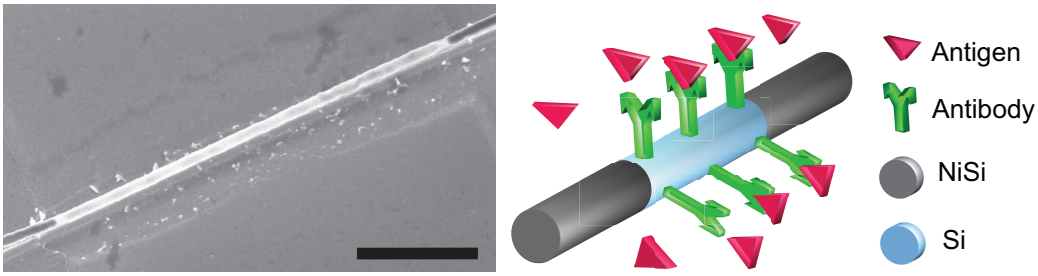
Figure 5.23: (a) Arrhenius plot for different V_{gs} extracted from the plots of Fig. 5.22b showing both thermionic emission and tunneling mechanisms. The linear decreasing slopes are associated with thermionic emission regimes. (b) Extracted E_a over a large range of V_{gs} . The inset A shows a constant $E_a = 450 \pm 5$meV over $-0.2\text{V} \leq V_{gs} \leq -0.8\text{V}$. Inset B shows the maximum of E_a = 525meV which is associated to the ϕ_{Beff}.



(a) (b)

(c)

Figure 5.24: (a) Measured input-output transfer characteristics of a hysteretic inverter based on a single Si nanowire FET with low current bias, showing current-dependent thresholds. (b) Forward and reverse threshold voltages for polysilicon Schottky barrier FETs under constant current biasing from 100fA up to 500fA (adapted from ref. [35]). (c) The hysteresis window shrinks with increasing temperature. Within this T range, the temperature sensitivity of 10mV/°C is related with the thermionic current regime.



(a) (b)

Figure 5.25: (a) Suspended functionalized silicon nanowire with NiSi extremities. Scale bar is 4 μm. (b) Concept model.

effect-transistor paradigm [38]. Due to the nano-scale of the fabricated geometries [39], the recent discovery in solid-state devices of the memristive effect has been source of renewed research efforts in applications for high-density memory device [1]. The physical phenomena governing the memristive behavior are attributed to the change of an internal state variable, which modifies the conductance in a non-volatile manner [7]. As reported by Duan et al., memory devices are possible also with molecule-gated nanowire transistors by using redox active molecules [9]. In here, we report on the first evidence of unexpected new insights for a novel molecular sensing in dry conditions based on nanofabricated memristors functionalized with bio-molecular thin films.

Device Nano-Fabrication

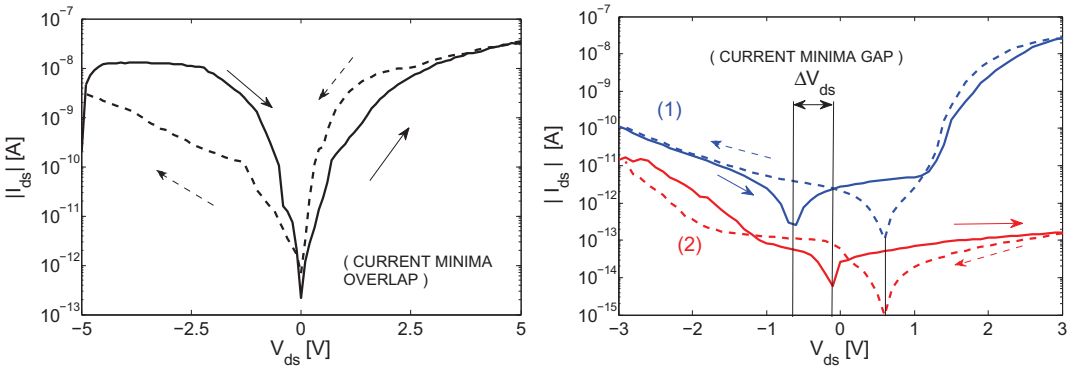
The fabrication method utilizes some of the steps that were previously reported [34] for memristive Schottky-barrier silicon nanowire field-effect-transistors. The process starts from low resistivity Silicon-On-Insulator substrates, with 1.5 μm device layer and 3 μm SiO_2 insulating layer. After standard lithography, the silicon nanowire is carved anchored at the top of two silicon pillars. Then, Ni is deposited on top of the pillars with overlap on the outer portions of the silicon nanowire. Hence, an annealing step at 450°C in a horizontal wall furnace forms NiSi contacts. Fig. 5.25a shows a nano-fabricated memristive silicon nanowire with NiSi contacts.

Biomolecule self-assembly

The silicon nanowire surface was derivatised with 3-glycidoxypropyltrimethoxysilane GPTS [40] and functionalized by covalent attachment of anti-rabbit polyclonal antibodies (AB) [41]. Antigen (rabbit antibodies, AG) interact with the functionalized wire as depicted in Fig. 5.25b.

Results and Discussion

Electrical measurements are carried out in a shielded probe station connected with HP4615C Semiconductor Parameter Analyzer and in dark, to avoid any photo-generated currents. Before functionalization with the AB layer, $I_{ds} - V_{ds}$ curves taken for forward and backward sweep do



(a) (b)

Figure 5.26: $I_{ds} - V_{ds}$ curves: (a) before functionalization with AB bio-layer. A typical memristive hysteresis is observed, with no ΔV_{ds} gap between I_{ds} minima in forward and backward regimes; (b) the blue curve (1) is measured after drying the sample from de-ionized water. The red curve (2) is measured after dipping in 5 pM AG solution and drying.

show a typical memristive behavior (see Fig. 5.26a), where the current minima always occur for $V_{ds=\ 0\ V}$; consistently with previously reported measurements [34] on non-functionalized devices. Conversely, functionalized silicon nanowires show different positions of the current minima for backward or forward regimes. This effect is observed after drying from: (a) de-ionized H_2O solution and (b) 5 pM AG solution. The $I_{ds} - V_{ds}$ curve before AG up-take shows an hysteresis (curve (1) in Fig. 5.26b) due to charge trapping mechanisms at the Schottky junctions. The binding of an AG with the functionalized wire is responsible for a modification of the hysteresis (curve (2) in Fig. 5.26b), in particular to a reduction of the current minimum gap between forward and backward V_{ds} sweeps. Coherently, the up-take of increasing amounts of AG (in the pM range) results on a further diminishing of this gap.

5.6 Chapter Summary and Conclusions

In this chapter several applications of two-terminals and multi-terminal memristive devices are discussed. Specifically, fabrication of resistive RAM memories have been presented for their potential for standalone memories. The resistive RAM can also be exploited for increased FPGA functionality, such as lookup tables, datapath routing. In here we propose the use of a generic memory structure to replace the pass-transistor in SRAM-based FPGAs. Another application envisages the use of ReRAM on top of Through Silicon Via for fully-3D programmable interconnects. A low thermal budget fabrication scheme of resistive programmable TSV has been developed and discussed. In the last section of the chapter, three-terminal memristive SiNW devices are exploited for sensing physical and biological quantities. Moreover, an innovative device exploting the hysteresis of functionalized Si nanowires is a first-time approach for bio-sensing in a controlled dry environment.

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6 Conclusions and Outlook

In this thesis several devices were developed and discussed. The main goals focused on enabling new functionalities for logic, memory and sensing applications. Such goals have been achieved by exploiting two phenomena that are typically disregarded in conventional nanoscale devices: ambipolar conductance and memory effects. Starting from the evidence that both phenomena are likely to increase as the scaling progresses, this these focused instead on making use of these rather than suppressing them. By relaxing these constraints on nanoscaled devices, additional functionality can be brought about several applications which are developed through the chapters.

In Chapter 1, fabrication methodologies for ambipolar Si nanowire devices are discussed. The methods enable the *top-down fabrication of vertically-stacked Si nanowires* of sub-lithographic dimensions, with sub-10nm nanowire sizes reachable out of a single sequence of optimized DRIE dry etching, without the need of additional oxidation steps. Such achievements are interesting for several applications, for instance advanced logic design, nanowire resonating structures, ultra-dense FLASH, new PLA architectures. Indeed logic design of *Carry Lookahead Adders* with vertically-stacked CMOS Si nanowire technology demonstrate additional benefits due to higher density and performance than planar CMOS gates.

The ambipolar conductance of the Schottky-barrier SiNW FETs has been exploited in several logic applications as a feature to perform more powerful computation. *Ternary logic gates* have been built from Schottky barrier Si nanowire FETs, by exploiting the ambipolar conductance. At the same time, ambipoalr Si nanowire FETs can also be utilized to obtain compact *threshold logic gates*, by means of a current-biasing scheme. The threshold can be precisely controlled by the amount of current and, combined with standard boolean logic circuits, enables multi-valued logic functions. Nevertheless, there are difficulties related to the compatibility between the input and output voltages and the usefuleness of such approach yet has to be demonstrated. Moreover, *ambipolar Double Independent SB SiNW FET* can be utilized as polarity-control device to build several Boolean logic functions with a single device. In addition, an optimized implementation demonstrated its potential for large logic circuits exploiting the ambipolarity as a computational state variable [1]. In this respect, *Sea-of-Tiles* architectures have been envisaged to fully exploit the potential of polarity-controlled devices [2].

As memory effects arise naturally from nanoscale systems, many applications ranging from

standalone memories, non-volatile FPGA, programmable interconnects, as well as sensing have been envisaged. In this thesis, *multi-value ReRAM* devices arranged in dense-crossbar are demonstrated with a top-down process flow compatibile with BEoL post-processing due to the low thermal budget (T < 200°C). Preliminary results on a CMOS chip demonstrate the feasibility of BEoL post-processing, opening new possibilities for FPGAs, standalone memories, ultra-low power analog design, neuromorphic architectures. In particular, ReRAMs with bipolar resistive switching mechanism can be arranged to form an equivalent of the pass-gate devices with the advantage high-density and very-low energy consumption. This feature can be exploited in the proposed *Generic Memory Structures (GMS)* that can be beneficial for either routing Multiplexers or configuration nodes in FPGAs.

In addition, memory effects in ambipolar SiNW SBFETs can be exploited for additional functionality. One possibility will be to exploit the retention of the memristive SBFETs to build a new type of DRAM. As the same structure can be utilized for both memory and logic, architectures based on distributed elements of memory and logic can be envisaged. Moreover, the hysteresis dependence over the current-bias and over the temperature have been exploited to sense these physical quantities. Moreover, as the hysteresis depends on the trap charging into the dielectric and the body of the nanowires, such dynamic can be effected by the presence of bio-functionalization layers. This is exploited in a novel device based on ambipolar Si nanowires for *bio-sensing* applications.

In future work, a platform hosting both logic and memory elements developed througout this thesis would enable new architectures either as a standalone platform or in the framework of CMOS post-processing, eventually generating novel research ideas. For instance, neuromorphic architectures can benefit from the *threshold function* of the ambipolar Si nanowire FETs with the current-biasing scheme as it is one of the elements in the *Perceptron model of the neuron* as well as from the non-volatility and density of the resistive RAM crossbars, whose electrical behavior can emulate the *synaptic interconnections* or, in other words, the weighted links in some of the *Artificial Neural Networks* architectures.

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A Process Flow Steps

A.1 ebeam lithography

The e-beam lithography is carried out with a VISTEC EBPG5000 providing a 100keV electron acceleration voltage. Negative tone Hydrogen SilsessQuioxane (HSQ) XR-1514 2% dilution from Dow Corning™ has been used as hard mask for the patterning of Si nanowires, while positive tone resist ZEP based on Styrene Methil Acrylate polymer is utilized for the patterning of the gates.

A.2 Si dry etching

The etching steps are carried out in an Alcatel Adixen AMS200 and it is operated with pulsed Low Frequency (LF) wafer biasing with alternative SF_6 and C_4F_8 gas flows for controlled Si etching. On SOI substrates an End Point Detection mechanism is utilized to verify that the Si device layer is correctly etched. This process has also been utilized to produce vertically-stacked SiNWs after the NiSi regions were formed on an SOI device layer (an example is shown in false colors in Fig. A.1).

A.3 Sacrifical wet oxydation

In the early examples, Si nanowires have been obtained by means of sacrificial oxydation steps. This method has also the purpose of forming a thick isolation layer at the bottom of the Si trenches.

A.4 Gate Stack

A.4.1 Polysilicon Gate Stack

After the nanowire formation process a Si oxydation in O_2 atmosphere is carried out. Different recipes were utilized and for thin nananowires a self-limiting oxydation at 850°C is carried out. Since the oxydation is carried out below the viscosity transition temperature of Si/SiO_2

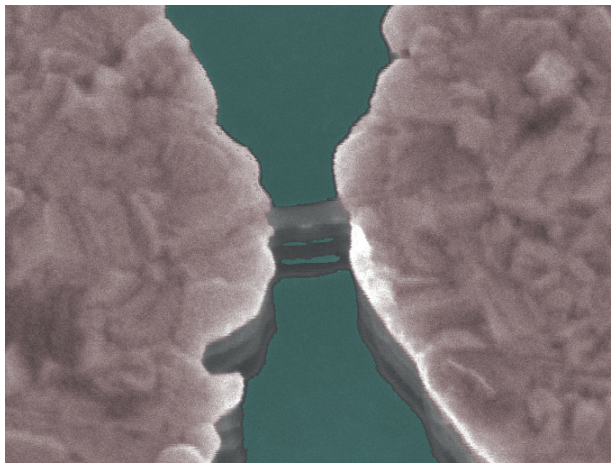


Figure A.1: 100nm long vertically-stacked SiNWs formed after the NiSi regions by DRIE. The etching has been performed after Ni lift-off and annealing. The NiSi source/drain regions then served as etching layer.

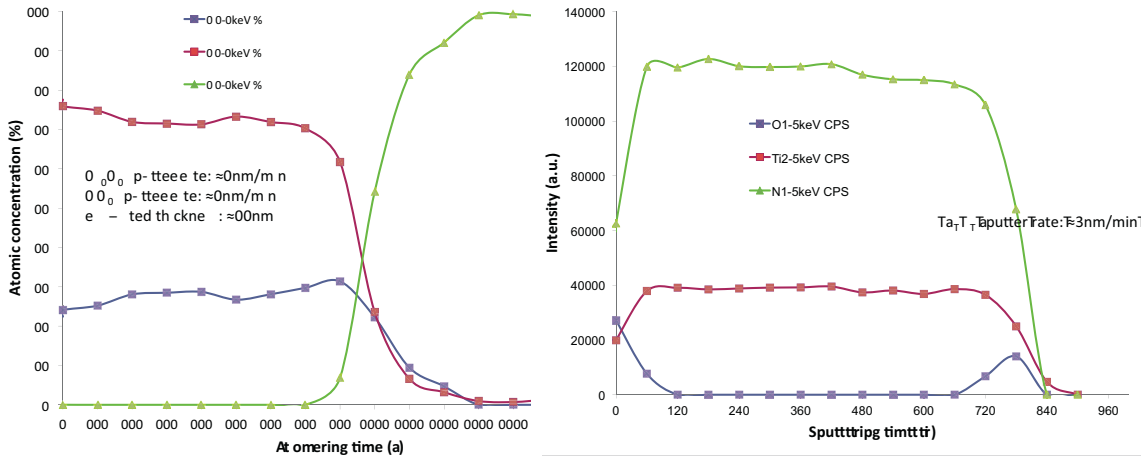
(960°C), compressive stress builds up and slows the oxydation rate. This phenomena can be exploited to achieve a good control of nanowire diameters. Typical SiO_2 thicknesses for Si nanowire transistors are between 5nm and 20nm. Then polysilicon layers of thickness between 50nm and 500nm were deposited by LPCVD, giving excellent conformality.

A.4.2 High-κ/Metal Gate

The High-κ/metal gate stack has been deposited by ALD. In particular, HfO_2 and TiN have been choosed for their thermal stability with Si. Concerning the resistive RAM development, TiO_2 stochiometry and the quality of the TiN are also important, and as such, the ALD deposition quality of TiO_2 and TiN at CMi has been checked with AES (see Fig. A.2a) and XPS (see Fig. A.2b) profiles, respectively.

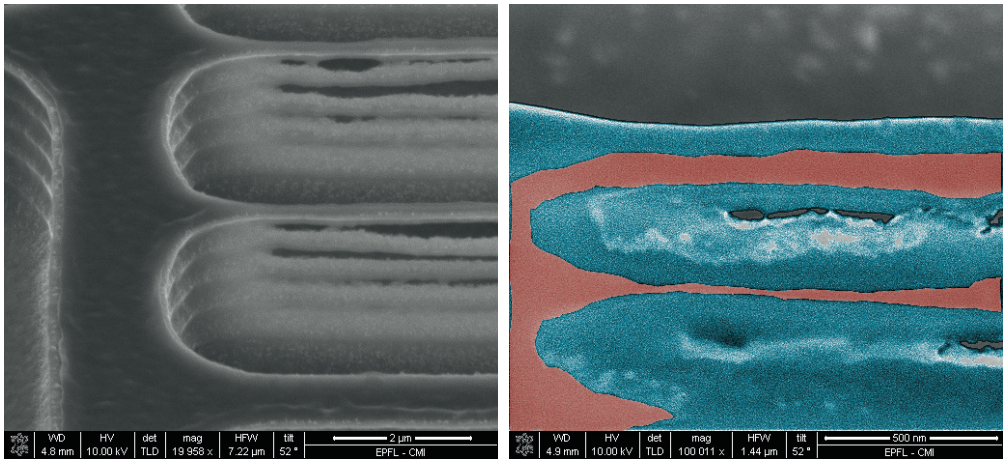
A.5 NiSi silicidation

A 30nm thick Ni layer is deposited by e-beam evaporation in Alcatel EVA600 evaporation system in vacuum level of $5 \cdot 10^{-7}$mbar. The substrate is quickly loaded into EVA600 just after a short BHF step to remove native oxide from the Si surface. In this way the formation of a fresh SiO_x layer that can prevent NiSi formation is limited. The EVA600 has been chosed because it can provide a uniform coverage of Ni all-around the nanowires. This feature has been tested on arrays of vertically-stacked Si nanowires and characterized by FIB cross-section after Ni silicidation (see Fig. A.3. After the Ni deposition, the substrate are loaded into a furnace for NiSi formation. The NiSi recipe has been carried out by a triple-step thermal annealing of a Ni layer in forming gas in a horizontal wall furnace. The three-step annealing refers to three plateau temperatures, each corresponding to a specific NixSiy phase (see Fig.A.4. At 200°C Ni-rich phases are formed. Then a second plateau at 300°C is exploited so that a Ni_2Si phase is obtained. Finally a 400°C plateau is kept for 20min to produce the Ni_1Si_1 phase required



(a) (b)

Figure A.2: Characterization of the ALD-deposited TiO_2 and TiN: (a) XPS profile of TiO_2, showing a 1:2 Ti:O stochiometric ratio. (b) AES profile of TiN showing a little oxide layer at the surface and at the bottom of the layer, which should be minimized to reduce resistivity.



(a) (b)

Figure A.3: NiSi nanowires after annealing in forming gas: (a) SEM tilted view. (b) FIB cross-section. The central Si section has been colored in red, while NiSi is colored in blue.

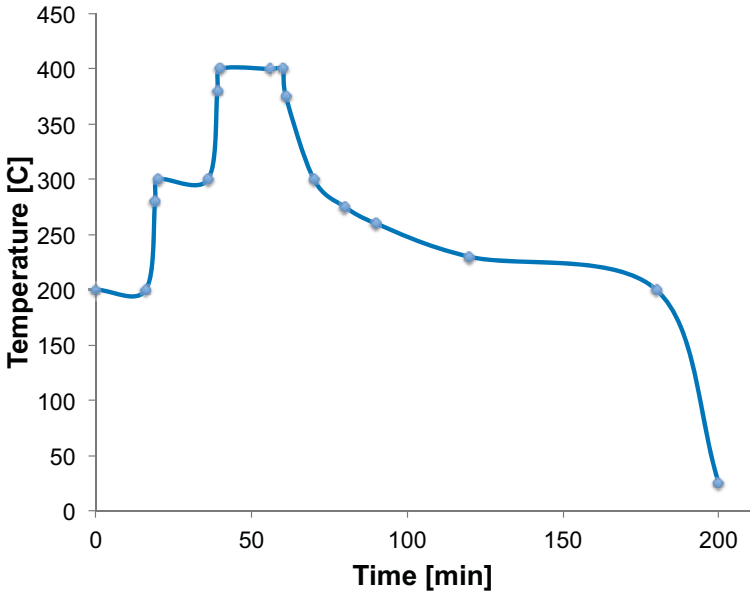


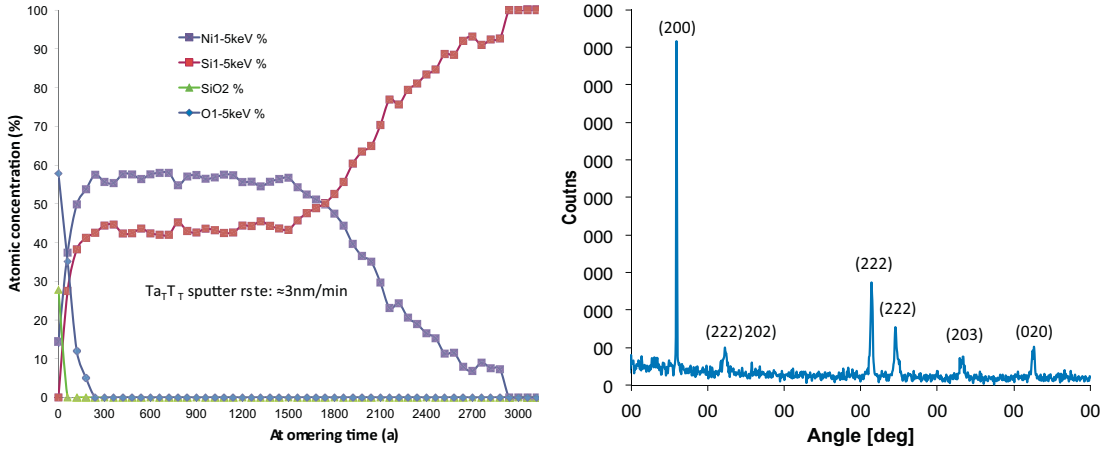
Figure A.4: Temperature-Time chart of the NiSi triple-step annealing. The substrates are loaded at 200°C (the furnace has been pre-heated) and after a 5min purge phase with 20slm N_2, $N_2 : H_2$ forming gas is injected while temperature is kept constant for 20min at 200°C. Then a second temperature plateau is reached at 200°C and kept for another 20min. Finally, the NiSi phase is obtained by increasing the temperature up to 400°C for 20min. Then the substrates are slowly cooled down, to avoid any thermal stress that might generate defects and unwanted interfacial states at the NiSi/Si junction. At 200°C the H_2 flux is stopped and the substrates are removed from the furnace.

for a mid-gap Schottky barrier contact. The Ni_1Si_1 phase is also chosen because it has been proven to be among several silicides to be the one with lowest resistivity. All thermal steps above 200°C are carried out in forming gas consisting of 9:1 N_2:H_2 mixture with a total flow rate of 100sccm/min.

The correct formation of NiSi has been checked with Auger Electron Spectroscopy (AES) and X-ray diffraction. The XPS/AES analysis has been carried out in a XPS/ESCA KRATOS AXIS ULTRA and in-depth profiling of NiSi layer has been carried out by Argon sputtering. The XRD tests were carried out in a Θ-2Θ X-ray diffractometer, and the instrument has been calibrated exploiting the position of the 400 Si peak.

A.6 BEoL post-processing

The development of a process flow compatible with CMOS Back-End-of-Line is fundamental for providing large access to this novel technology with a limited development costs. The main objective is to develop some integration techniques that allow to efficiently process ReRAM stacks on top of dies, processed by conventional CMOS foundries. One of the big advantages of ReRAM technology is its CMOS-compatibility. Indeed, the materials involved in ReRAMs are deposited at low temperature, compatible with metal line process. Different integration



(a) (b)

Figure A.5: Characterization of the NiSi thin-films after annealing: (a) Auger Electron Spectroscopy profile. Notice the Oxygen content at 0sec of sputtering, which is probably due to a thin native oxyde at the surface of NiSi. (b) X-ray Diffraction.

options might then be envisaged. First, it is possible to deposit the ReRAMs on the last metal layer of conventional process flow and add a final top cap layer that provides access to the top terminal of the ReRAMs. As an illustration, a schematic cross section and a temptative process flow of a co-integrated ReRAM-CMOS BEoL are shown in Fig. A.6.

The proposed solution illustrates a very conventional integration, that requires three lithographic steps. Additional lithographic steps increase the cost of the whole integration process, and decrease the reliability of the fabricated dies. To reduce the number of lithography steps, a second solution, using only a unique step, will be developed. As shown in Fig. A.7, the CMOS die is fabricated such that the last CMOS BEoL includes patterns that can be used as a mask for the definition of top electrodes. At the same time, the lower metal layers in the BEOL are exploited as bottom electrode lines, in this way the post-processing scheme is dramatically simplified as it requires only one lithography for the passivation opening. Finally, a third solution (Fig. A.8) envisages additional one or two lithographic steps in order to obtain a ReRAM stack in between the last metal layer and the last via layer. This solution is the most compact one and it also offer the flexibility for the implementation of top and bottom electrodes of different materials.

A.6.1 On going post-processing

A first CMOS chip with cross-bar arrangement of 32x32 rows and columns has been designed with pass-gates and decoder for the addressing. The design of the basic cell of the arrays is exploiting the presence of an MMC layer, which will be utilized as the upper electrode. Since the distance between the MMC electrode and the bottom metal (metal 5) is only 35nm, the current post-processing involves the etching of the ILD and the deposition of a *Resistive Switching Material*. In Fig. A.9a a tilted SEM view shows the basic cell with metal 6, MMC and

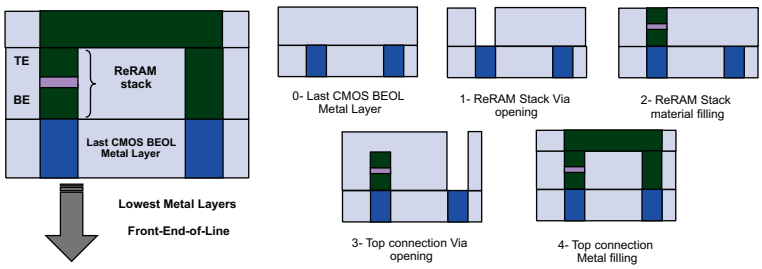


Figure A.6: Cross-sectional schematic and associated process flow showing the integration of a ReRAM device (on the top of a pro-processed CMOS die. The device is including a oxide layer between bottom (BE) and top (TE) electrode contacts and is integrated between the last metal layer and an additional one patterned on top of the existing die.

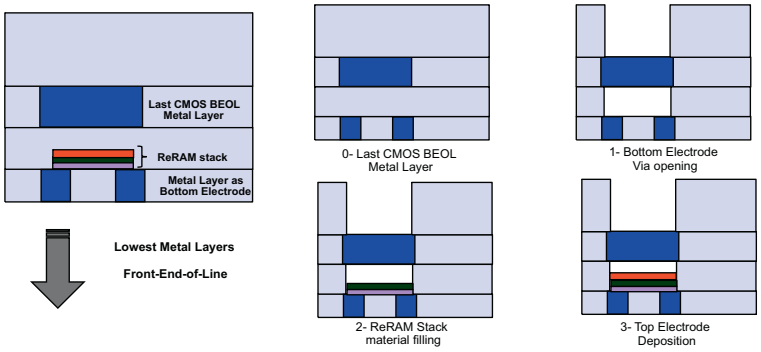


Figure A.7: Cross-sectional schematic and associated process flow showing the integration of a ReRAM device with an alternative process. Since the last CMOS BEOL metal is utilized as shadow mask for top electrode patterning, this scheme of ReRAM co-integration only use 1lithographic step for patterning, allowing for a more precise alignment of the different parts.

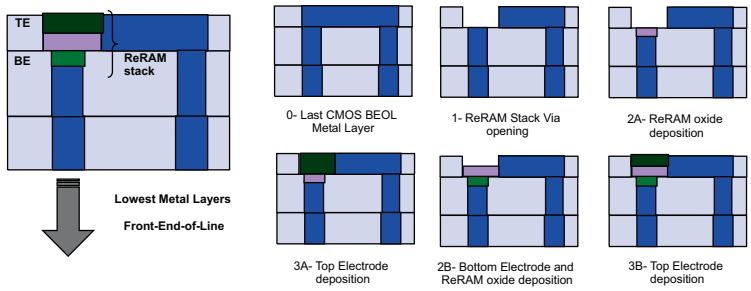


Figure A.8: Cross-sectional schematic and associated process flow showing the integration of a ReRAM device with an alternative process. In here, two (three) lithographyc steps are needed, allowing for the integration of top (top and bottom) electrodes of different materials.



(a) (b)

Figure A.9: (a) Tilted SEM view of a MMC cross-point. The MMC layer is colored in blue. Metal 5 is colored pink while metal 6 is colored brown. The bright parts of the image are due to charging of the dielectric layers. (b) FIB cross-section of the MMC electrode (in blue) with a bottom metal 5 electrode (brown color). A 35nm dielectric layer electrically separates the MMC and the metal 5.

metal 5 after the ILD etching.

Fabrication and Characterization of Vertically Stacked Gate-All-Around Si Nanowire FET Arrays

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***Abstract*— We describe the fabrication of vertically stacked Silicon Nanowire Field Effect Transistors (SiNW FETs) in Gate-All Around (GAA) configuration. Stacks with the number of channels ranging from 1 to 12 have been successfully produced by means of a micrometer scale lithography and conventional fabrication techniques. It is shown that demonstrator Schottky Barrier (SB) devices fabricated with Cr/NiCr contacts present good subthreshold slope (70mV/dec), I_{ON}/I_{OFF} ratio $\geq 10^4$ and reproducible ambipolar behavior.**

***Index Terms*— nanowire, FET, multichannel, ambipolar, vertical integration**

I. Introduction

Continuing efforts in Complementary-Metal-Oxide-Semiconductor (CMOS) research have lead to the exponential increase of device integration density during the last 40 years. More recently increasing fabrication costs and increasing overall variability have become an obstacle for the scaling trend. In order to overcome such limitations, considerable research is dedicated for instance to the use of new materials (such as high-κ dielectrics with metal gates), dual-gate devices, novel isolation techniques that make use of Silicon-On-Nothing (SON) or Silicon-On-Insulator (SOI) substrates [1]. In particular, dual-gate technology in conjunction with the geometry of the device can enhance the control over the transistor channel. In this sense, further improvements can be achieved with tri-gate, omega-gate or Gate All-Around technologies (GAA) [2].

Recent works explored the vertical stacking of SiNWs as channels for FET devices [3], [4]. The vertically stacked SiNWs represent channels of the same SiNW FET, whose electrostactic control can be enhanched by using a GAA configuration [5]. In addition, SiNW FETs can also be used to build new logic architectures [6], [7] or as ultimate memory architectures for Ultra-Large-Silicon-Integration (ULSI) [8], [9].

In this work we discuss novel and promising fabrication method for vertically-stacked SiNW FETs with different number of channels on bulk Si wafers. The reported method has also been applied to fabricate single channel devices that demonstrate excellent reproducible performance.

II. Related Work

Recently, a multichannel structure with GAA configuration has been proposed as a candidate for high-performance devices. Its implementation has the advantage of enhanced on-current (I_{ON}) along with low leakage as well as a small footprint for multi-finger (multi-channel) devices [10], [4]. The fabrication process described in [10], [4] is based on creating epitaxial layers to alternate Si and SiGe layers one on top of each other. A vertical trench is etched in the grown structure. A successive SiGe selective etching leaves vertically-stacked Si nanowires. Hydrogen annealing is then used to change the SiNW shapes from rectangular to circular, thus yielding channels with less surface roughness and improved controllability.

An alternative approach for the fabrication of vertically-stacked SiNWs [11] is based on producing a scalloped trench in bulk silicon by means of Deep Reactive Ion Etching (DRIE). Sacrificial oxidation steps are performed to reduce the dimensions of the trench. Thanks to scalloping, the Si trench is totally consumed in its thinner parts, leaving a vertical stack of suspended SiNWs. Although the DRIE process defines trenches of micrometer dimensions, the iteration of oxidation steps is capable for reducing the structures to suspended nanowires with of 20 nm in diameter [11]. This approach has also been demonstrated to be suitable for producing vertically stacked SiNW with small dimensions and different section shapes [12], yet it has not been used so far for GAA FET fabrication.

III. Device fabrication

In our work we produce vertical SiNW arrays by means of optical lithography with 1 μm resolution limit. Sub-micrometer features are obtained through sacrificial oxidation steps. Although the integration density would have been further increased by means of advanced lithography, the developed process already allows us to produce very high channel densities without making use of non standard fabrication steps.
We start by defining a photoresist line on a p-type ($N \sim 10^{15}$) silicon bulk wafer (see Fig. 1.a). Then a DRIE technique (also called Bosch process) is performed. This technique, that alternates a plasma etching with a passivation step, has been optimized to produce a scalloped trench in silicon with high reproducibility. Etching time, passivation time and plasma platen power have been optimized in order to enhance the scalloping effect. The application of the DRIE technique gives a trench like the one depicted in Fig. 1.b. The flexibility of the process allows us to change the number of scallops easily. After a wet oxidation step (see Fig. 1.c) vertically stacked SiNWs are formed. Then the cavities produced by the Bosch process are filled with photoresist. After a combination of chemical mechanical polishing (CMP) and BHF dip, the wet oxide is removed around the NWs (see Fig. 1.f). The oxide at the bottom of the cavity is left to isolate the substrate from the successive processes. The vertical structure obtained is then oxidized to produce a high quality dry oxide (20 nm thick, see Fig. 1.g) as gate dielectric. Then between 200 nm and 500 nm of Low Pressure Chemical Vapour Deposition (LPCVD) polysilicon is deposited (Fig. 1.h). The polysilicon gate is patterned by means of a combination of isotropic and anisotropic recipes (see Fig. 1.i). A final field oxide isolation and Al or Cr/NiCr patterning make the external electrical connections.

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A SOI wafer has been used to fabricate demonstrator devices with single channel layer. In this case we patterned Cr/NiCr through a lift-off technique to form source and drain. An advantage for using Ni is that it can easily form silicides with mid-gap workfunctions at low temperature, thus allowing the fabrication of FETs in few process steps and with a low thermal budget [13]. However, the main difference with FETs defined by implantation is the formation of Schottky Barrier (SB) source/drain thus leading to a device with ambipolar characteristic. The ambipolarity refers to the $I_{ds} - V_{gs}$ electrical characteristic of a transistor having both p- and n-type behaviour [13]. A double step annealing (at 200°C and 400°C, respectively) has been choosen to form silicided regions. This annealing process has been seen as good choice in terms of I_{ON}/I_{OFF} ratio improvement [14]. After the annealing steps, the unreacted Cr/NiCr parts were removed in wet etchant. Finally a 1 μm thick layer of Al has been patterned after via opening on the field oxide.

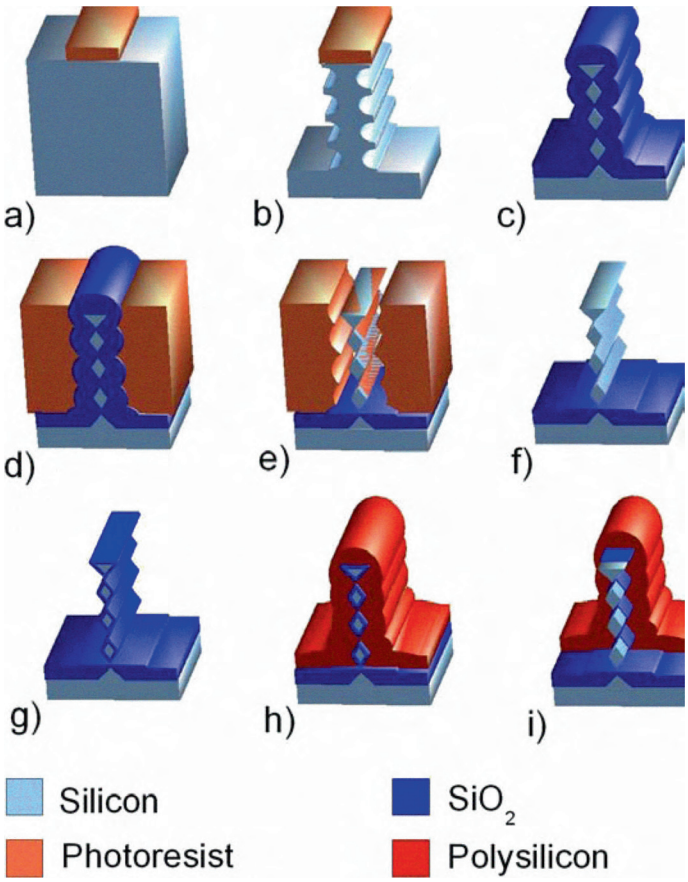


Fig. 1. Process flow of vertically stacked Si-NW FET. a) A photoresist line is defined on the Si wafer. b) A Bosch process is performed to produce a scalloped trench. c) Wet oxidation. d) A 5 μm thick photoresist is spin-coated in order to fill the cavities formed around the trench. e) The oxide removal step free the SiNWs withouth removing the oxide at the bottom of the cave. f) SiNWs are vertically stacked and electrically isolated from the substrate. g) A high quality dry oxide is formed. h) LPCVD polysilicon deposition. i) Gate patterning

IV. Discussion on the fabricated structures

Three dimensional SiNW FET arrays have been fabricated in vertical stacks with the number of channels varying between 1 and 12 (see Fig. 2). Initially, the formed SiNWs have diameters ranging from 70 nm to 200 nm, several techniques can be applied in order to refine the dimensions in a controlled manner. For instance, it has been demonstrated that the use of self-limiting oxidation is capable of producing channels with nanometer dimensions and good controllability [4], [15]. Surface irregularities of the suspended NWs can be improved either by means of a self-limiting oxidation or by hydrogen annealing step [10]. It was found that the proposed fabrication method consistently produces repeatable and very controllable dimensions of clearly separated NW stacks, by optimizing the etch/oxidation conditions. A uniform and thin gate oxide is formed around the suspended NWs by dry oxidation in a horizontal furnace under 10 slm O_2 flux. By combining isotropic and anisotropic etch techniques, polysilicon gate lengths down to 200 nm (see Fig. 3.a) were produced using 1 μm lithography. It can be seen that the polysilicon gate completely surrounds the suspended NW segment without any gaps, and that the silicon NW is covered by a 20nm thick gate oxide (Fig. 3.b). The proposed GAA device fabrication technique has also been succesfully applied for NW stacks with 3 suspended channels (Fig. 4). Fig. 4.a shows a structure with two parallel polysilicon gates, and Fig. 4.b shows the cross-section of the structure where individual wires and the surrounding polysilicon gate are clearly visible. Note that the cross-section of each suspended NW (with the exception of the top wire) has a well-defined rhombic shape that is dictated by the successive etching/oxidation steps used to produce the wire stacks. The top wire has a triangular profile that is also defined by the process. Schottky-barrier (SB) SiNW FETs demonstrator devices in GAA configuration have also been fabricated successfully on SOI, and shown in Fig. 5. In this particular example, the suspended NW segment has a trapezoidal cross-section.

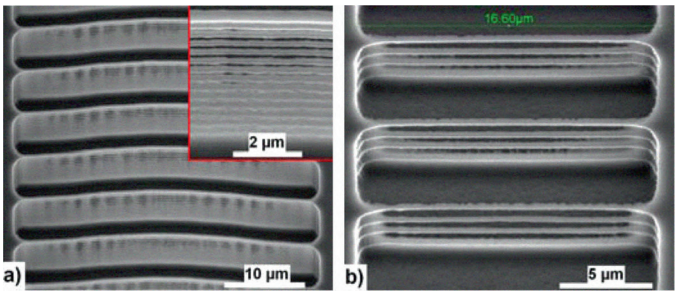


Fig. 2. a) Vertically stacked SiNWs in array configuration after oxide removal. The nanowires are free and sligthly bent due to residual stress. In this sample the number of vertically stacked nanowires amounts to 12. b) Another array with 3 vertically stacked SiNW channels.

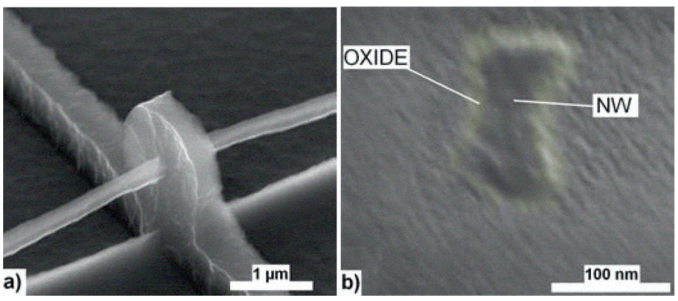


Fig. 3. a) Single nanowire surrounded by 500 nm thick polysilicon gate; $L_g \sim 200$ nm. b) Gate stack cross-section showing the Si core surrounded by 20 nm gate oxide and polysilicon.

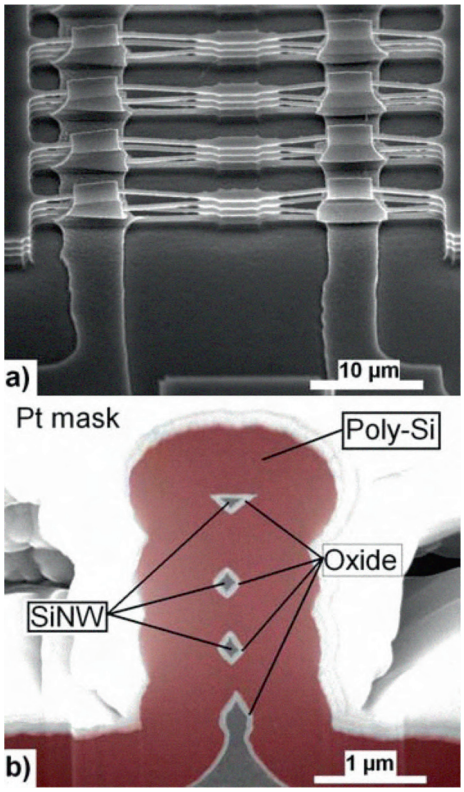


Fig. 4. a) Long nanowire channels with two parallel gate construction. b) Gate stack crossection showing three SiNW channels.

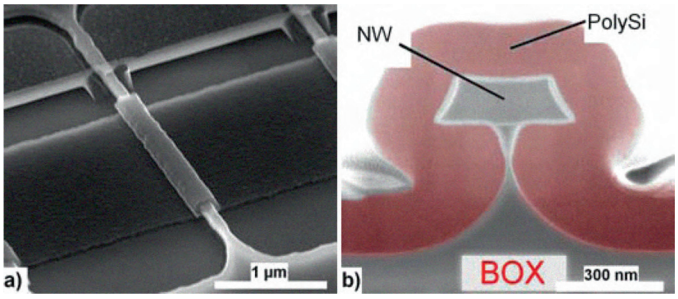


Fig. 5. a) Single GAA-NW device with polysilicon gate. b) Gate stack cross-section and highlight on different stack materials.

V. Electrical Measurements

The measured electrical performance of two SB SiNW FET devices with single SiNW channel in the stack are reported in the following. Each NW channel have $5\,\mu m$ gate length and an effective width of $930\,nm$. Since the NW cross-section is trapezoidal, the effective channel width is the perimeter of the NW. The devices (see Fig. 6) show an ambipolar behaviour with good performance of both p- and n- branches. Table I reports the device (device A) parameters demonstrating device ambipolarity, I_{ON}/I_{OFF} ratio $\geq 10^4$ and a subthreshold slope (SS) lower than 70 mV/dec for the p-type portion of the curves ($V_{gs} > V_{th}^{h^+}$ for h^+), and around 250 mV/dec for the n-type part ($V_{gs} < V_{th}^{e^-}$ for e^-). The $I_{ds} - V_{ds}$ curves have been measured for positive V_{gs} (Fig. 7.a) and negative V_{gs} (Fig. 7.b). The device behavior in the "triode" region indicates very distinct gate control over the drain current. The plots also show a Negative Differential Resistance (NDR) region when the channel is in inversion mode.

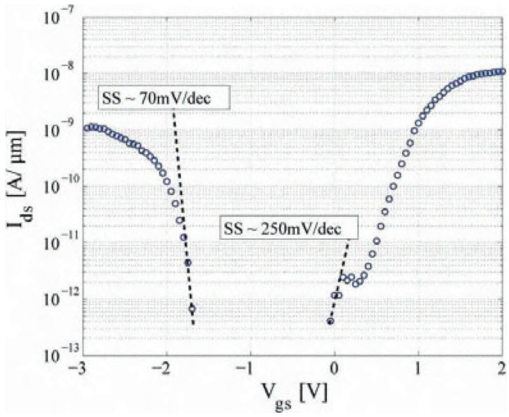


Fig. 6. Device A: $I_{ds} - V_{gs}$ curve for $V_{ds} = 1\,V$. The observed ambipolarity is typical for the metallic source and drain MOSFETs. Note the very high subthreshold slopes in both modes.

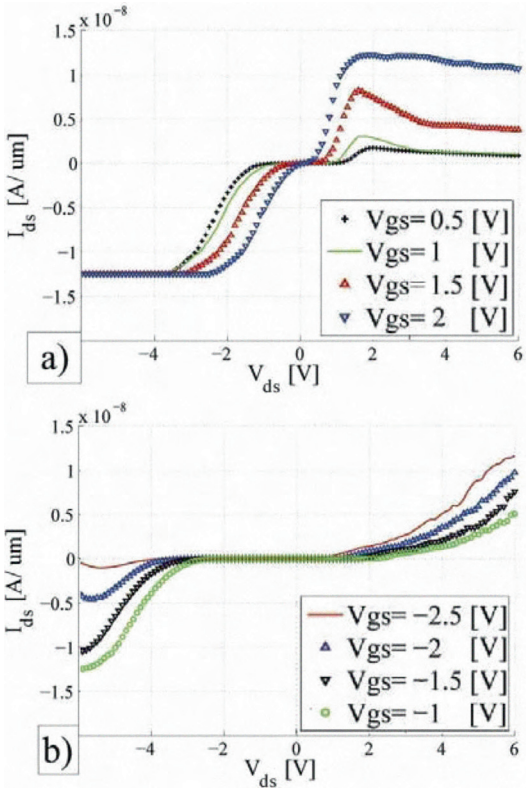


Fig. 7. Device A: $I_{ds} - V_{ds}$ curves showing negative differential resistance when the channel is at the inversion: a) for $V_{gs} \geq 0\,V$ channel in inversion mode for positive V_{ds} and in accumulation mode for negative V_{ds}. b) For $V_{gs} \leq 0\,V$ the channel is in inversion mode for negative V_{ds} and in accumulation mode when V_{ds} is positive.

TABLE I
Device A: SB SiNW FET parameters.

	$\frac{I_{ON}}{I_{OFF}}$	V_{th}^{+} or $V_{th}^{e^-}$ [V]	SS $[\frac{mV}{dec}]$	$I_{ON}^{h^+}$ $[\frac{nA}{\mu m}]$	$I_{ON}^{e^-}$ $[\frac{nA}{\mu m}]$
h^+	2900	−2	< 70	12.5	-
e^-	31000	1	250	-	2

A partially gated device (source and drain have been designed 1 μm far away from the gated channel) shows ambipolar behaviour (see Fig. 8). The extracted parameters for this device (device B) are reported in Table II. The high V_{gs} required for the onset of conduction is believed to be due to the non controlled portion of the channel. This behaviour is confirmed in [16]. Moreover, in [16] the possibility of making the device unipolar by using a dual gates was discussed as well. A dependency of the I_{OFF} on the applied V_{ds} is found (see Fig. 9).

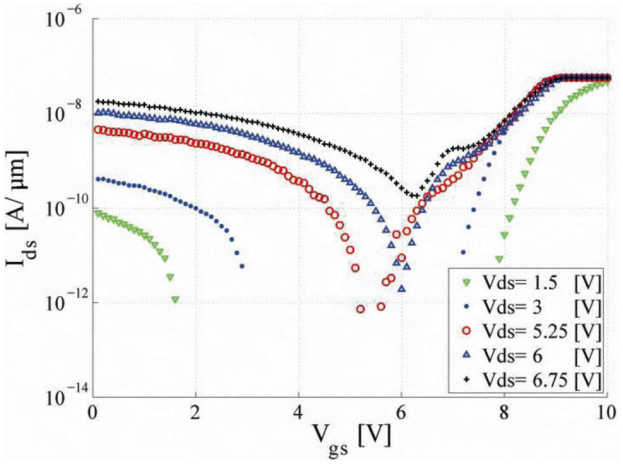


Fig. 8. Device B: $I_{ds}-V_{gs}$ curves for a partially gated device showing ambipolar behaviour and dependence to the applied V_{ds} .

TABLE II

DEVICE B: AMBIPOLAR BEHAVIOUR PARAMETERS FOR POSITIVE GATE VOLTAGES AFTER TWO STEP SILICIDATION ANNEALING.

V_{ds} [V]	$I_{OFF}^{h^+}$ [$\frac{pA}{\mu m}$]	$I_{OFF}^{e^-}$ [$\frac{pA}{\mu m}$]	$\frac{I_{ON}}{I_{OFF}}^{h^+}$	$\frac{I_{ON}}{I_{OFF}}^{e^-}$	SS^{h^+} [$\frac{mV}{dec}$]	SS^{e^-} [$\frac{mV}{dec}$]
1.5	1	8	300	7500	400	250
3	6	10	333	6000	700	350
5.25	0.7	0.7	10000	85700	200	300
6	2	2	10000	30000	200	200
6.75	200	200	150	300	N/A	N/A

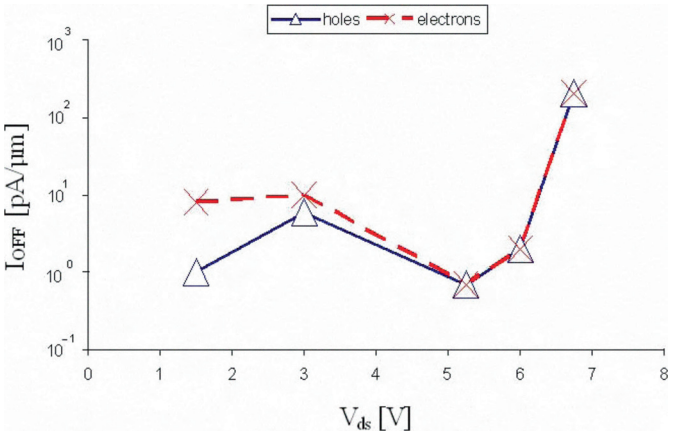


Fig. 9. Device B: I_{OFF} for holes (p-type portion of the $I_{ds} - V_{gs}$ curve) and electrons (n-type portion of the $I_{ds} - V_{gs}$ curve) conduction at different V_{ds}.

VI. CONCLUSIONS

High channel density SiNW GAA FETs have been fabricated by means of a DRIE technique for the first time. The same low cost top-down approach has been succesfully deployed to fabricate vertical SiNW stacks with different number of SiNW channels; i.e. the number of channels composing the vertical stack could be easily tuned from 1 to 12. Moreover, the process can be easily adopted for different substrates (bulk or SOI wafers) without any additional complexity. Finally, SB SiNW devices fabricated with good repeatability show excellent performance (the measured $SS < 70\,mV/dec$ is close to the optimal value for SiNW devices for room temperature operation) making the approach suitable for further investigations.

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Ambipolar silicon nanowire FETs with stenciled-deposited metal gate

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ABSTRACT

We report on a fully CMOS compatible fabrication method for ambipolar silicon nanowire FinFETs. The low thermal budget processing, compatible with monolithic 3D device integration, makes use of low pressure chemical vapor deposition (LPCVD) of amorphous Si (a-Si) and SiO_2 layers as well as metal gate patterning using stencil lithography, demonstrated for the first time. FinFETs with stenciled Al gates are successfully co-fabricated with polycrystalline silicon Ω-gated devices. Stencil lithography is envisaged as a key enabler for gate patterning on 3D structures, such as vertically stacked nanowire transistors.

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1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures or different state variables other than charge [1]. All these approaches will lead to significant modifications of the traditional planar transistor design. Considering novel device structures, the nanowire (NW) channel transistor with FinFET construction has been demonstrated to be one of the best in terms of electrostatic control, thus enabling further device scaling [2]. Another example can be the monolithic 3D integration, a process integration scheme that achieves higher device density by stacking p-type FETs on top of n-type FETs [3]. In terms of state variables, one example is given by device ambipolarity. The ambipolar property can be described by the presence of two high conductance states for the same FET, each of these related to carriers of opposite charge values [4]. Preliminary works on device ambipolarity show how it can be used to compute more complex logic functions per chip [5]. However, in terms of process integration, a few technologies have the flexibility to be implemented within 3D integration schemes and, at the same time, offer the ambipolar property with good CMOS compatibility and electrical performance.

We report on a fully CMOS compatible fabrication of ambipolar SiNW FinFETs by means of amorphous Si (a-Si) and low temperature oxide (LTO) deposited with low pressure chemical vapor deposition (LPCVD) technique. FinFETs with stenciled Al gates are successfully co-fabricated with polycrystalline Si (pc-Si) gated devices achieving excellent performance. The difficulty of achieving high resolution gate patterning on non-planar devices is addressed for the first time by means of stencil metal deposition [6]. We envisage the use of this technique also for metal patterning on high aspect ratio FETs, such as vertically stacked nanowire transistors [7]. It is worth noting that this process can be repeated several times, eventually being used for monolithic 3D integration.

In Section 2 we present the fabrication steps to build the devices. Then in Section 3 the fabricated structures are shown and described. In Section 4 we describe the electrical behavior of the two types of FinFETs fabricated and on the pseudo-inverter operation of pc-Si FinFETs. Finally, in Section 5 we draw the conclusions.

2. Process flow

The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500 nm thick wet oxide and a 100 nm LTO layer. Then a 100 nm a-Si film is deposited as the active layer. A 70 nm thick dilution of hydrogen silsesquioxane (HSQ) is spin coated and patterned with e-beam lithography. Lines having widths ranging from 70 nm to 250 nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip buffered hydrofluoridric acid (BHF) step. The obtained a-Si nanowires are then covered by a 40 nm dry oxide and a 50 nm LPCVD pc-Si layers. Large 100 μm × 100 μm pc-Si pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, pc-Si Ω-gated FinFETs with gate lengths between 1 μm and 10 μm are obtained.

Then a bi-layer of 20 nm Ti/55 nm Ni is patterned with lift-off to form electrical contacts between the Si nanowires and the pads. A 400 °C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been

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chosen for its mid-gap work function and for its use in a-Si metal induced recrystallization process [8]. The fabrication flow is completed by the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100 nm thick SiN membranes with apertures having widths between 100 nm and 1 μm [9]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2 μm [9] accuracy using a customized SUSS MA/BA 6 mask aligner [10]. The clamped substrate–stencil setup is placed in an evaporator where 100 nm thick Al gates are deposited.

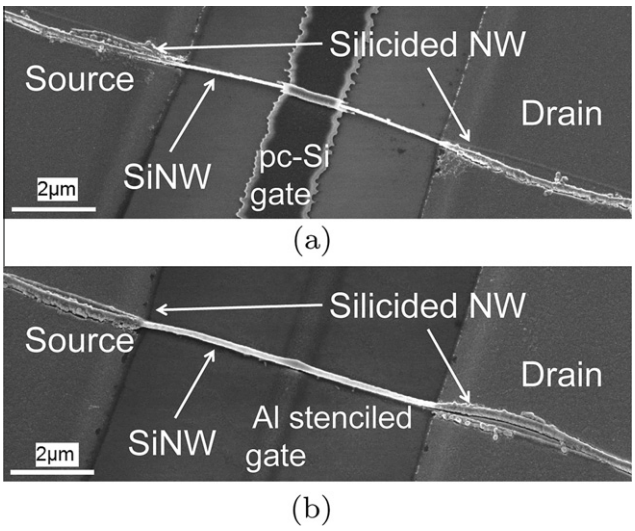


Fig. 1. FinFETs with silicide nanowire portions at source/drain contacts: (a) pc-Si FinFET having 2 μm long gate and 60 nm × 65 nm channel cross-section. (b) Al stenciled FinFET having 700 nm gate length and 60 nm × 140 nm channel cross-section.

3. Fabricated structures

FinFETs and inverters with up to 62 μm nanowire length were fabricated. An example of a 2 μm long pc-Si gate FinFET having 100 nm × 65 nm Si nanowire channel is shown in the SEM tilted view of Fig. 1(a). In Fig. 1(b), a Si nanowire transistor with 130 nm × 65 nm channel (see Fig. 2(d)) cross-section and 700 nm large stenciled Al gate is shown. Focused ion beam (FIB) cross-sections (see Fig. 2(a)–(c)) demonstrate nanowire channels sections having widths between 65 nm and 130 nm. The total Si thickness is reduced from the initial value of 100 nm to 65 nm due to processing. Narrower nanowires (the expected nanowire size was around 35 nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

4. Electrical measurements and discussion

The I_{ds}–V_{gs} curve of a pc-Si Ω-gate FinFET has a typical ambipolar behavior, with a higher conductance for holes (at negative V_{gs} voltages) than for electrons (Fig. 3(a)). In the holes-conductance regime, a subthreshold slope SS ≈ 420 mV/dec is observed, while a larger SS is observed for the electron-dominated current. The gate misalignment error is source of variation for the channel series

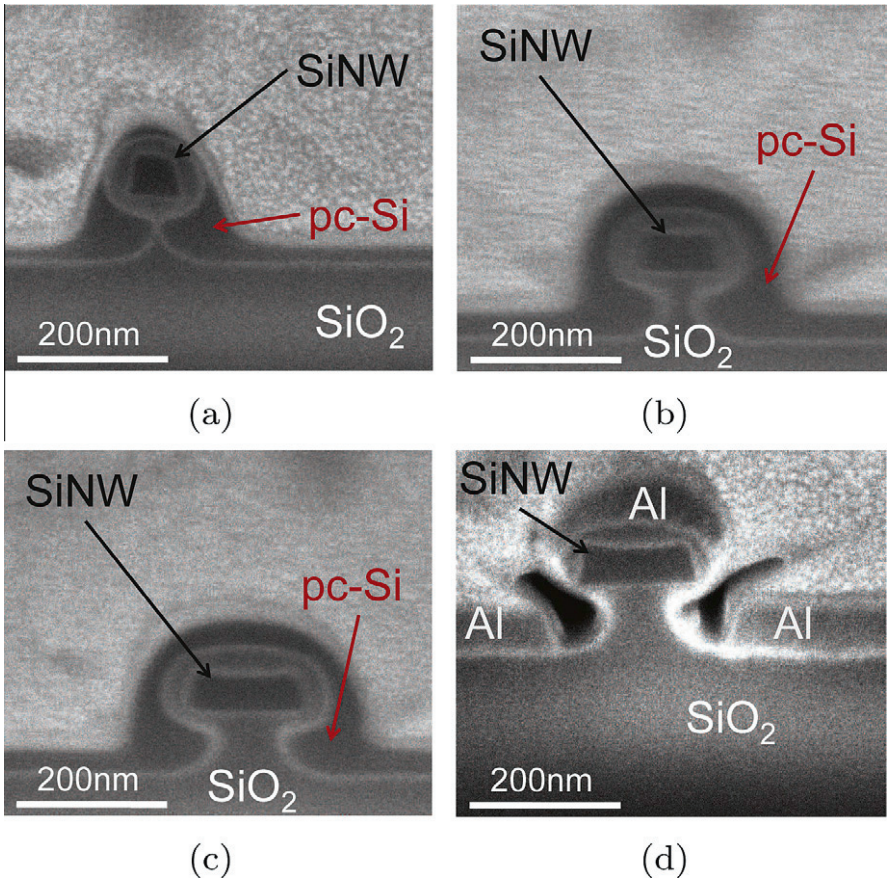


Fig. 2. FIB cross-sections showing the nanowire channels embedded in 40 nm oxide and gate materials: (a) pc-Si Ω-gate FinFET with 60 nm × 65 nm section. (b) pc-Si Ω-gate FinFET with 60 nm × 110 nm section. (c) pc-Si Ω-gate FinFET with 60 nm × 140 nm section. (d) Al stenciled-gate FinFET with 60 nm × 140 nm section.

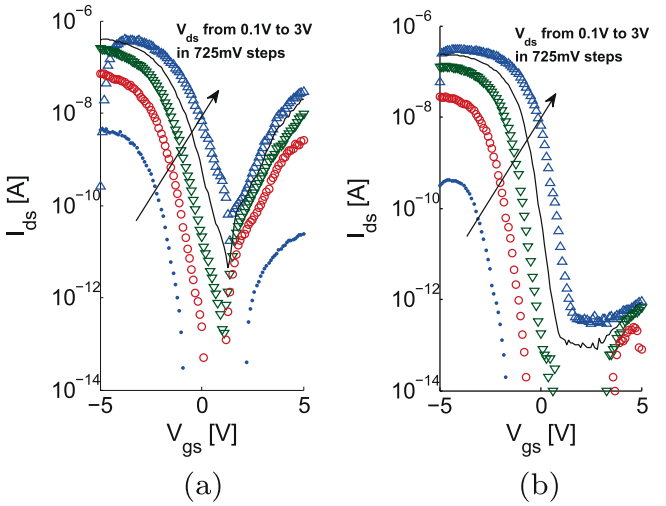


Fig. 3. (a) Ambipolar I_d–V_g curve of a pc-Si Ω-gated FinFET having 1 μm gate length and 60 nm × 110 nm nanowire section. (b) Ambipolar I_d–V_g curve of a stenciled Al-gate FinFET having 1 μm gate length and 60 nm × 110 nm nanowire section.

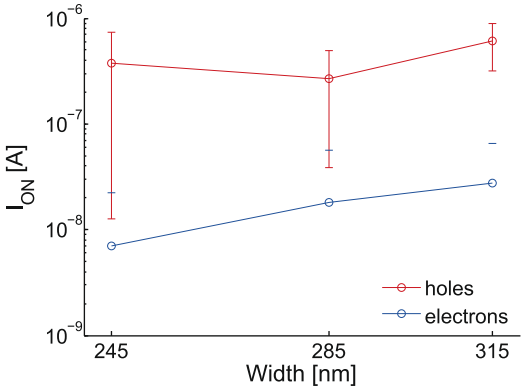


Fig. 4. Average I_{ON} for holes and electrons of pc-Si Ω-gated FinFETs of different widths. The error bar represents the standard deviation over a sample of eight devices.

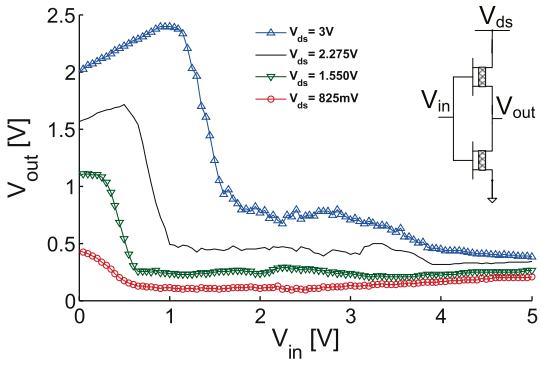


Fig. 5. Voltage transfer characteristic of a 2 in series connected pc-Si Ω-gate FinFETs on-a-wire and biased as for inverter operation. The insets represent the inverter bias scheme. Two ambipolar pc-Si FinFETs are connected in series.

resistance which in turn impacts the overall current conductance. Nevertheless, the main limiting factor for the current conductance is the injection of carriers over the Schottky barrier, and the series resistance is considered to play a minor role. This aspect is

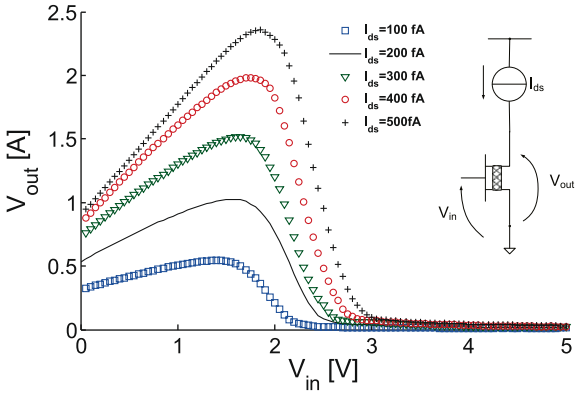


Fig. 6. pc-Si FinFET biased for pseudo-inverter operation having 2 μm gate lengths and 60 nm × 110 nm channel cross-section. The insets show the pseudo-inverter bias scheme using a single pc-Si FinFET and a current source.

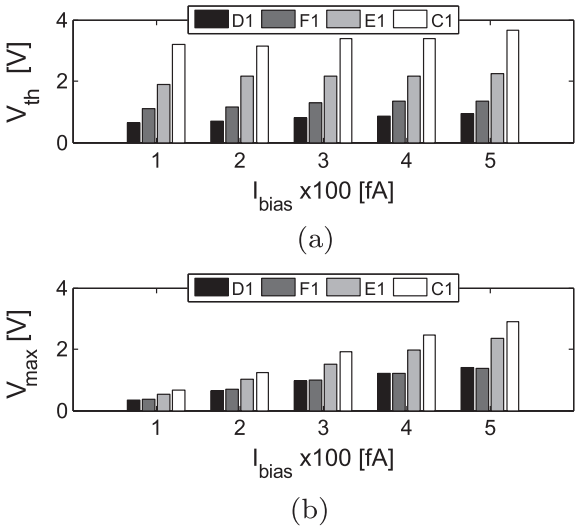


Fig. 7. (a) Threshold voltage (V_{th}) values for the pc-Si gated pseudo-inverters. The inversion voltages are stable under different current bias. (b) Maximum output voltages values for the pc-Si gated pseudo-inverters. The V_{max} values tend to increase linearly with I_{bias}.

confirmed by the observation of a lower I_{ON} for electrons than holes over a large number of samples. In Fig. 4, the average I_{ON} for holes and electrons is shown. The I_{ON} increase linearly with the channel width, which is calculated as the perimeter of the SiNW, since volume inversion effect are negligible for SiNW-channel diameters larger than 10 nm.

Conversely, Al-gated devices show a p-type conductance mainly (see Fig. 3(b)), which can be explained with Al contamination at pad regions due to the stencil process. This is also reflected in a SS ≈ 200 mV/dec, indicating that doping can effectively be used to improve SS by suppressing the ambipolar conductance. In both devices, I_{ON}/I_{OFF} ratios of more than six orders of magnitude are observed. The lower current for the *n*-branch in the Al gated devices might be due to metal gate-induced doping. The transfer characteristic of pc-Si Ω-gate inverters show (Fig. 5) an output voltage range V_{out} compatible with the input voltage range and a gain of $\Delta V_{out}/\Delta V_{in} \approx 4$. Thus, pc-Si gated inverters are suitable elements for cascading additional devices, enabling the construction of more complex circuits. Similarly, a current bias scheme for FinFETs can be used to obtain pseudo-inverter operation, which consist in using a current bias scheme as depicted in Fig. 6. For pseudo-inverter operation a triangular voltage transfer

characteristic is obtained, with very low power consumption ($\leqslant$1.2 pW). Data from different dies on the wafer show stability of the V_{in} value for which inversion occurs (V_{th}) under different current bias (see Fig. 7(a)). Moreover, as it is shown in Fig. 7(b), the maximum of V_{out} increases linearly with the current bias. Al gated inverters and pseudo-inverters are currently under investigation.

5. Conclusions

A fully CMOS compatible fabrication flow using low temperature a-Si LPCVD and stencil lithography has been developed and proved suitable for SiNW FinFETs having ambipolar conductance. Nanowires with up to 62 μm length with two separate gates have been successfully fabricated, giving space for complex circuit design. Moreover, the stencil lithography has been demonstrated for the first time as a suitable technique for metal gate patterning on 3D nanowire structures. The excellent performance of individual FinFETs and preliminary data of inverter functionality pave the way for the fabrication of more complex Si nanowire FinFET circuits. Further characterization of Al stenciled inverters and fabrication on high aspect ratio structures is envisaged as natural continuation of this work.

Acknowledgments

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Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography

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ABSTRACT

We report on the top-down fabrication of vertically-stacked polysilicon nanowire (NW) gate-all-around (GAA) field-effect-transistors (FET) by means of Inductively Coupled Plasma (ICP) etching and nanostencil lithography. The nanostencil is used to form sub-μm GAA gates over polysilicon NW array channels with high aspect ratio, considerably simplifying the lithographic steps above regions with deep 3D topography and non-planar surface features. This process lead to fabrication yields larger than 70% and authors envisage even larger yields of $\geqslant 85\%$ with optimized mask design. Electrical measurements confirm the results obtained from similar devices fabricated with a standard lithography method while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling.

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1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the planar transistor design [1,2]. Considering novel device structures, multiple-gated transistors have been proved of better electrostatic control and larger drive current with respect to the traditional planar transistor design [3]. These features are particularly attractive as enablers for further device scaling. In fact, double-gate and finFET structures are the first non-planar 3D gate constructions being successfully employed into commercial products. Nowadays, growing research efforts are spent with gate-all-around constructions with sub-10 nm diameter nanowire (NW) channels. Nevertheless, as the dimensions reduce and 3D structures are introduced, major difficulties arises due to the need of scaling while keeping large fabrication yields.

We report on a fully CMOS-compatible top-downfabrication flow of polysilicon channel finFETs and vertically-stacked polysilicon NW gate-all-around (GAA) FETs by means of an optimized Bosch process [4] and nanostencil lithography [5]. In a previous work, the authors envisaged stencil lithography [6] as a key enabler for gate patterning on 3D structures, such as vertically-stacked Si NW transistors [4]. In this work, nanostencil lithography is used to deposit the Al mask used to pattern sub-μm GAA polysilicon gates deposited with LPCVD as alternative solution for patterning nanoscaled features having high aspect ratio, which is a non trivial issue in photo-resist lithography. Moreover, a simple method to form vertically-stacked Si NWs on bulk-Si substrates [7] has been adapted to form vertically-stacked NWs onto polycristalline Si substrates. Preliminary electrical characterizations performed before the metal contact formation demonstrate functional memristive FET operation and confirming the behavior of previously reported devices fabricated with standard processing technology and μm-scale gate lengths [8]. The finFETs and the vertically-stacked polysilicon NW GAA devices are fabricated with yields larger than 70%, demonstrating a promising new method for 3D transistor fabrication with sub-μm nanostencil lithography.

In Section 2.1 we describe the structure of both finFETs and vertically-stacked GAA SiNW FETs. Then in Section 2.2 the fabrication flow for the devices is explained in detail, whereas the fabricated structures and discussion on the nano-fabrication results are provided in Section 3. Hence, the electrical measurement results are reported Section 4, with discussion among the difference in performance achieved by finFETs and vertically-stacked polysilicon NW GAA FETs. Finally, in Section 5 we draw the conclusions.

2. Device Fabrication

2.1. Device Description

The devices built can be grouped into two categories: finFETs and vertically-stacked SiNW FETs. In the first case, FETs or inverters having either 1 to 11 fins channels and tri-gate construction are built (in Fig. 1(a), a finFET with 3 fins is depicted). In the second

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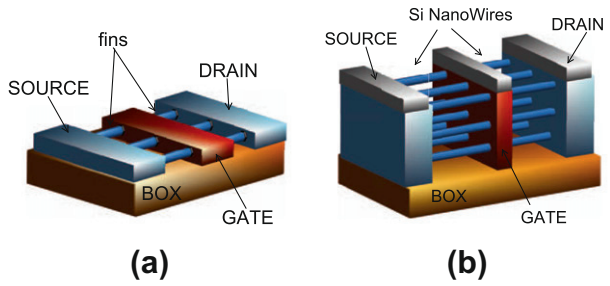


Fig. 1. Non-planar device topologies considered: (a) finFET with tri-gate construction.(b) Vertically-stacked SiNW FET with GAA construction.

case, FETs or inverters with 1 to 11 parallel strands consisting of 3 vertically-stacked SiNWs and GAA construction are built (in Fig. 1(b), a 3 times 3 SiNW matrix with GAA construction is shown). Apart from the fabrication of non-planar channels in such devices, the lithography definition of tri-gate or all-around gate structures above 3D channel regions is considered to be a significant challenge [1].

2.2. Process Flow

The fabrication starts with the substrate preparation for the two separate wafer batches. Bulk-Si wafers are oxidized in wet atmosphere to form 500 nm thermal oxide. Then either 50 nm or 350 nm thick LPCVD polysilicon is deposited as the device layer to build finFETs or vertically-stacked SiNW FETs, respectively. Individual or arrays of lines of widths of 50 nm and length of 8 μm are patterned with diluted *hydrogen silsesquioxane (HSQ)* using it e-beam lithography (EBL) (see Fig. 2(a)). The HSQ is then used as hard mask for the fins and the vertically-stacked SiNWs etching (Fig. 2(b)). For the fin formation, a Cl2 based plasma etching is used to obtain vertical sidewalls, whereas for the vertically-stacked SiNWs the etching consists of 3 cycles of passivation and etching steps, alternating low frequency pulses of C_4F_8 and SF_6 plasmas. The etching technique used for the stacked SiNW formation has been calibrated from the recipes previously described by the authors for the formation of vertically-stacked SiNWs in crystalline Si substrates [7]. Next, a 10 nm dry oxidation followed by a 100 nm LPCVD polysilicon deposition form the gate stack (see Fig. 2(c)). At the same time a low stress SiN nanostencil mask has been patterned with the gate design. The fabrication details of the nanostencil are described by the authors in a different publication [5]. In this work, the nanostencil is made of 100 nm thick LPCVD low stress Si_xN_y. The gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows. Then the nanostencil mask is aligned with a dedicated optical alignment tool and mechanically clamped with the device substrates. After loading the substrates with the nanostencil into a commercial e-beam evaporator, 40 nm Al are deposited, leaving an Al hard mask reproducing the gate design on top of the polysilicon layer (Fig. 2(d)). The Al mask gives better selectivity than SiO_2 hard maks for dry Si etching, thus enabling the patterning of higher aspect ratio structure. Hence, polysilicon gates are etched and Si_xN_y spacers are formed to provide good isolation barrier between the gate and the source/drain regions (Fig. 2(e)). This step is thus used to form pad areas for electrical characterization as well as polysilicon gates with lengths between 100 nm and 500 nm. Finally, a 30 nm thick Ni layer is deposited on the substrates, and a thermal annealing process at 400°C is utilized to form a stoichiometric 1:1 NiSi phase on top of the gates and to metallized source/drain regions. The unreacted Ni that was lying either on top of SiO_2 BOX layer or onto the spacers has been removed with a selective Piranha solution.

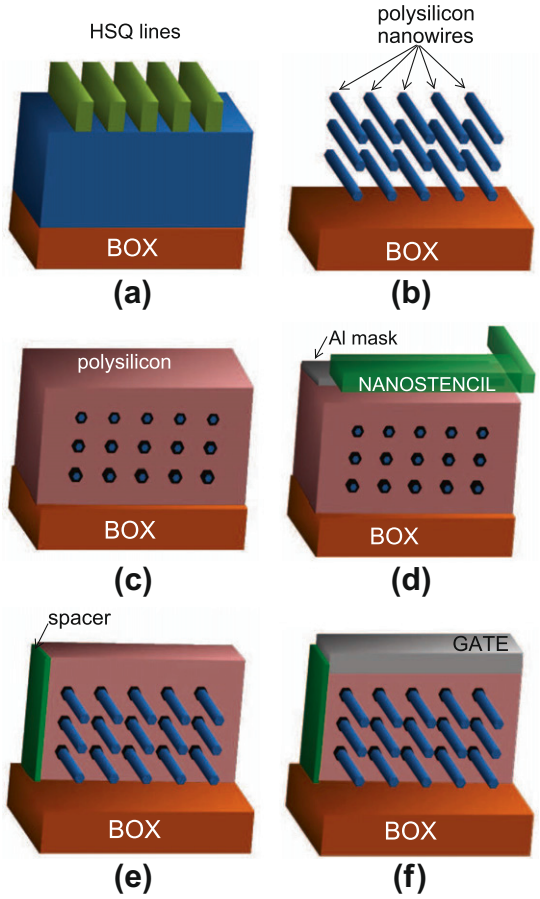


Fig. 2. Fabrication flow of the vertically-stacked GAA FETs. (a) HSQ lines are patterned with EBL. (b) A DRIE etching process is tuned to form 3 levels of stacked SiNWs. The nanowires are attached to polysilicon pillars at their extremes (not shown). (c) 10 nm dry oxide and 100 nm LPCVD polysilicon are deposited to form the gate stack. (d) A nanostencil mask is aligned and mechanically clamped with the substrate, serving as evaporation mask for Al deposition. The Al is then used as mask to pattern the gate.(e) After gate patterning a Si_xN_y spacer is formed on vertical sidewalls. (f) After Ni blanket deposition and a thermal annealing at 400°C, a Piranha wet etching is used to remove unreacted Ni from either BOX and spacer regions, thus forming self-aligned NiSi source/drain and gate areas.

Thanks to the self-alignment of the Si_xN_y spacers with the gates, self-aligned source/drain regions are formed and the devices are ready for electrical characterization.

3. Fabricated Devices

The fabricated devices included FETs or inverters designed with different number of channels, having either 1 to 11 parallel SiNWs for the finFETs. For the vertically-stacked SiNWs the same design is used, nevertheless, thanks to stacking 3 levels, the same devices have 3 to 33 parallel SiNW channels. Another difference among finFETs and vertically-stacked FETs is notably the gate structure, which are tri-gates and GAA, respectively. In Fig. 3, a finFET with 11 parallel SiNWs and tri-gate construction is shown. The SiNWs are interconnected every 500nm in order to improve the mechanical stiffness and so to avoid bending. In Fig. 4, a vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter and GAA construction is shown. In the inset, conformal coverage of 10nm thick SiO_2 dielectric and LPCVD polysilicon gate is shown.

In all substrates, the design included 150 FETs and 150 inverters, for which the fabrication yield has been checked. In Table 1 fabrication yields larger than 70% are reported, showing excellent reproducibility, considering the experimental nature of the

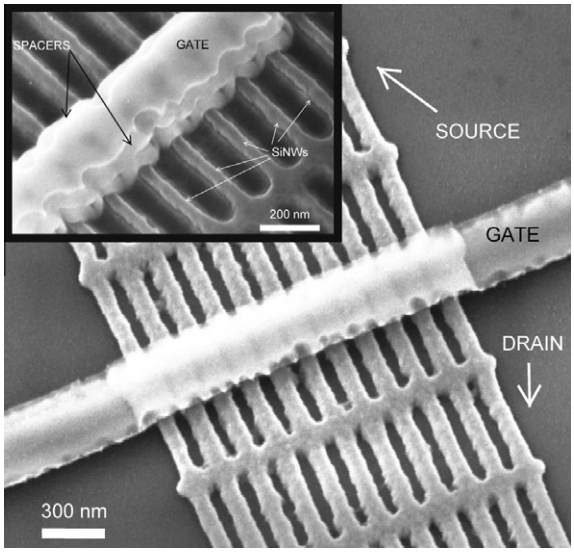


Fig. 3. Si nanowire FET with 11 channels with 50 nm times 50 nm channel cross-section, 350 nm long polysilicon gate. The nanowires are connected at regular intervals of 500nm in order to improve the stiffness of the structure. In the inset a magnified and tilted SEM view shows the nitride spacers and the SiNWs around the gate structure.

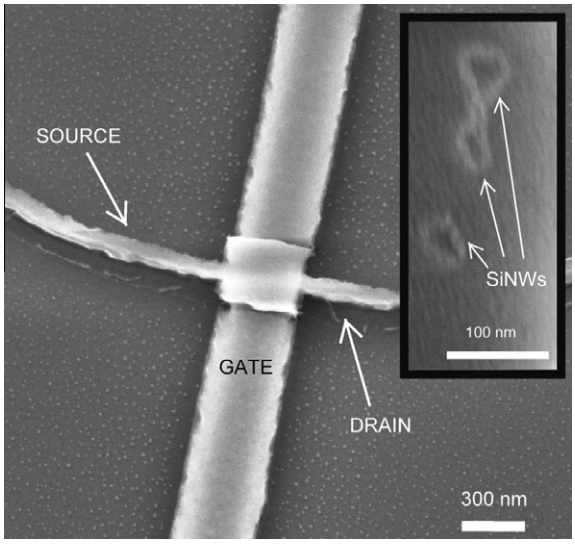


Fig. 4. Si nanowire FET with 3 vertically stacked single-stranded 30 nm diameter channels. In the inset, a Focused Ion Beam cross-section of the gate shows 3 SiNWs surrounded by 10 nm SiO_2 dielectric and 100 nm LPCVD polysilicon. Gate length is 350 nm.

process. Moreover, the failing sites have been observed the same for all the substrates, regardless of the process flow. This is the reason for the very similar yield reported for finFETs and vertically-stacked FETs. It is worth noticing that failing devices are mainly related with defects in the mask design, and that this aspect of the work has not been optimized. Thus, the main limitation on the fabrication yield is related with systematic errors in the design.

Table 1
Fabrication Yield measured for the 4 device types.

Yield	finFETs	vertically-stacked FETs
FETs	70%	70%
Inverters	85%	84%

For instance, one of the major fabrication issues is the mechanical stability of the nanostencil, whose robusteness is crucial for the correct patterning of the Al mask. If we consider the device subset of finFET inverters, the the larger yield of 85% is mainly attributed to the lower number of defective nanostencil patterns. Using a smaller size for the nanostencil, which would be a natural consequence when fabricating more scaled devices, improves stability and, at the same time, reduces the frequency of defective patterns. Hence, there is indication that fabrication yields larger than 85% with this process flow is possible with relatively little effort in the mask design.

4. Electrical Measurements

Electrical characterization is carried out with a manual probe station connected to a Agilent B1500 semiconductor parameter

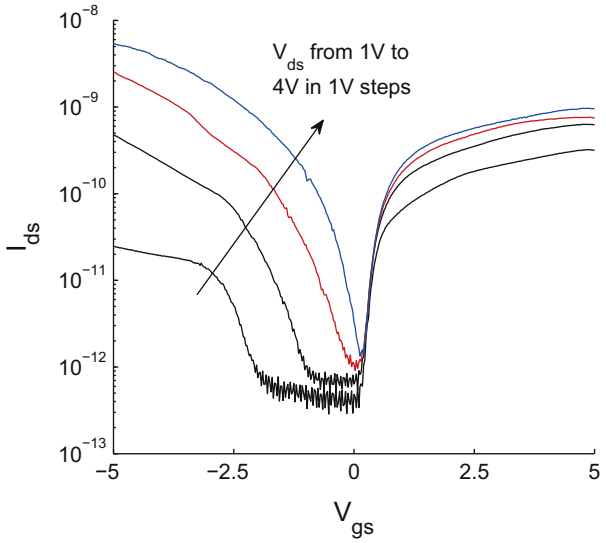


Fig. 5. $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 stacked channels. Measured minimum inverse subthreshold slopes for electrons (n-branch) and holes (p-branch) are $300mV/dec$ and $1300mV/dec$ at V_{ds}=4V.

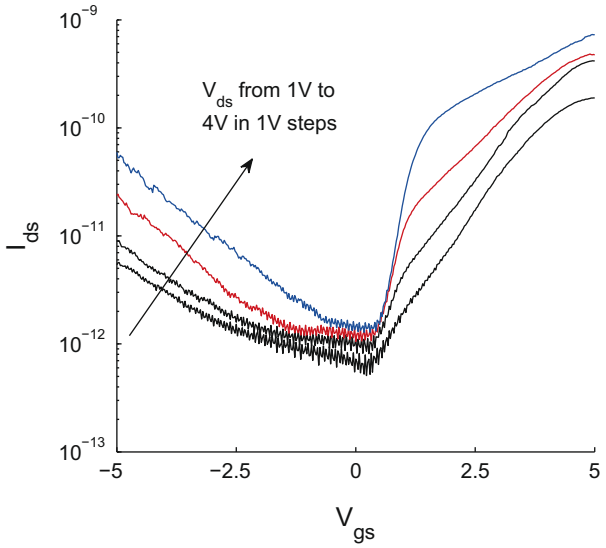


Fig. 6. $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 times 11 channels. Measured minimum inverse subthreshold slope for electrons is $350mV/dec$. Notice that the holes conduction is effectively suppressed due to the 3D nanowire mesh.

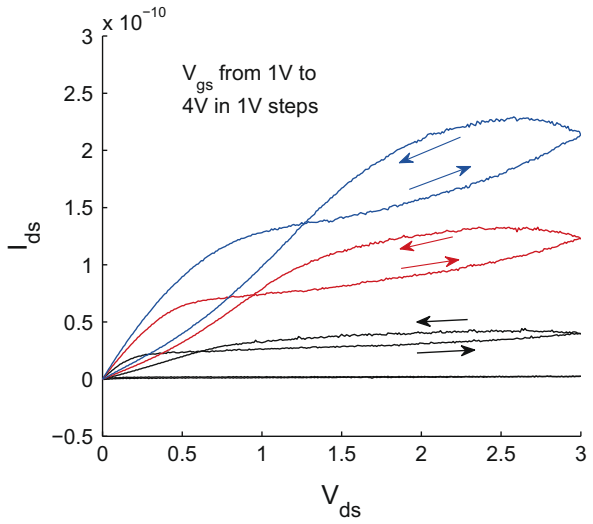


Fig. 7. $I_{ds} - V_{ds}$ memristive/hysteresis curve for vertically-stacked SiNW GAA FET with 3 stacked channels. The hysteresis lead to different saturation threshold due to the dynamics of charges with interface states at either the Shottky junctions or at the polysilicon grain boundaries.

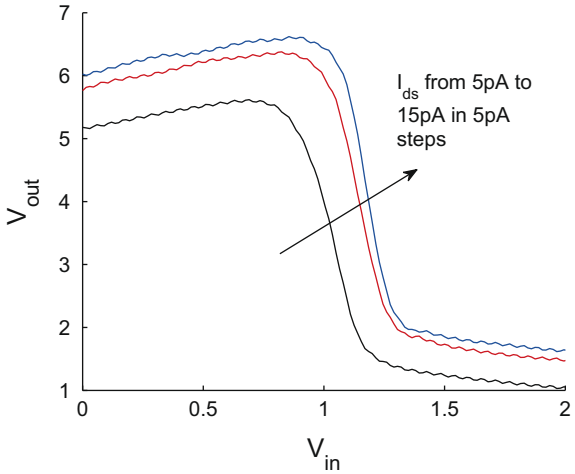


Fig. 8. Inverter operation obtained by biasing a FET with constant current. The $V_{out} - V_{in}$ characteristics switched from high to low V_{out} at $V_{in} \approx 1$ V.

analyzer. Tungsten tips are put in contact with the polysilicon source/drain pads and on the Al/polysilicon gate pad. Typical $I_{ds} - V_{gs}$ curves are first measured for finFETs which show large inverse subthreshold slopes of about $1500mV/dec$ and average $I_{ON} - I_{OFF}$ ratio of 3 orders of magnitude. These results are then compared with the electrical performance measured for the vertically-stacked GAA NW FETs. The $I_{ds} - V_{gs}$ curves (Fig. 5) for the vertically-stacked FETs with 3 stacked SiNWs show typical device ambipolarity with inverse subthreshold slopes for n- and p-branches up to $300mV/dec$ and up to $1300mV/dec$, respectively. Notice the strong dependence of the p-branch with applied V_{ds}. This undesired behavior is largely compensated for, in the devices with 3 times 11 parallel fingers, as shown in Fig. 6. The apparent robustness with respect to short channel effects is attributed to the different geometry of the 3D mesh with respect to the single stranded stacked SiNWs.

Another interesting result is the hysteresis observed for $I_{ds} - V_{ds}$ curves (see Fig. 7). The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward V_{ds} sweep is not identical to the same curve for backward V_{ds} sweep. This behavior can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [9]. More detailed explanation of the memristive electrical behavior can be found for similar, previously reported devices [8].

V_1 [V]	V_2 [V]	V_{out} [V]
0 (logic 0)	0 (logic 0)	$\approx$ 4 (logic 1)
0 (logic 0)	2 (logic 1)	$\approx$ 3 (logic 1)
2 (logic 1)	0 (logic 0)	$\approx$ 5 (logic 1)
2 (logic 1)	2 (logic 1)	$\approx$ 0.5 (logic 0)

Finally, inverter and logic NAND operation have been performed using a current biasing scheme. In Fig. 8, a current bias from 5 pA to 15 pA in 5 pA steps has been utilized. As shown in the graph, the inversion voltage saturates at $V_{in} \approx 1.2$V with a gain $\Delta V_{out} / \Delta V_{in} \approx 14$. Moreover, by using two vertically-stacked FETs in series connection, NAND functionality can be achieved by measuring the voltage drop across while sweeping the gate voltages of the two devices. With this method, typical NAND functionality is obtained, as shown in Table 1.

5. Conclusions

In conclusion, we demonstrated for the first time vertically-stacked Si nanowire FETs with polysilicon GAA having gate lengths down to 100 nm and yield larger than 70%. Moreover, the reported ambipolar behavior for vertically-stacked FETs achieves I_{ON}/I_{OFF} ratio up to 4 orders of magnitude and inverse subthreshold slopes (SS) up to $300mV/dec$, effectively improving the SS of $1500mV/dec$ obtained for finFETs. The method provide excellent step coverage on either finFETs and vertically-stacked SiNW FETs with strongly non-planar topography, thanks to the use of an Al etch mask deposited with nanostencil. The electrical behavior confirms the results obtained from similar devices fabricated with a standard lithography approach while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling. Finally, functional inverter and logic NAND operations are obtained, confirming the discussed fabrication flow as valuable tool to build logic circuits.

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Ambipolar Gate-Controllable SiNW FETs for Configurable Logic Circuits With Improved Expressive Capability

Davide Sacchetto, Yusuf Leblebici, and Giovanni De Micheli

***Abstract*—In this letter, we report on the fabrication and characterization of ambipolar silicon-nanowire (SiNW) field-effect transistors (FETs) with a double-independent-gate (DIG) structure for polarity control. Several structures are fabricated, showing the effectiveness of local back gate to enable switchable ambipolar functionality. Moreover, AND, NAND, NOR, XOR, and XNOR binary logic functions can be obtained with a single gate, depending on the encoding values used for the input signals. Repeatable behaviors of DIG SiNW FETs are considered as enablers for ambipolar-controlled logic, with all the benefits related to the maturity of the silicon technology.**

***Index Terms*—Ambipolar control, field-effect transistor (FET), nanowire, Schottky barrier.**

I. Introduction

THE CONTINUING pursuit for extending Moore's law to future device families also fuels the intensifying research on new device functionality for implementing next-generation circuits. New computational paradigms based on the control of alternative state variables [1] are being investigated along with novel structures, such as double-gate and gate-all-around nanowire devices [2], or new materials, such as higher κ dielectrics and metal gates, or different device concepts, such as modified Schottky-barrier field-effect transistors (FETs). Most of these paradigms require physics different from the physics of CMOS. For instance, computation has been demonstrated with devices based on the laws of photonics [3], spintronics [4], or nanoionics [5].

Nevertheless, alternative solutions that require a less dramatic impact on technological development would be preferable for practical applications. Regarding the different solutions, the ambipolar-controlled logic gates are among the most promising ones, owing to the higher expressive logic power due to the polarity control as state variable [6]. The polarity control can be achieved in ambipolar devices by using a double-independent-gate (DIG) structure. A few examples can be found for DIG FETs based on carbon nanotubes [7], [8], graphene [9], semiconducting polymers, and silicon nanowires (SiNWs) [10]. Nevertheless, very limited research has been done in terms of integrating ambipolar-controlled devices with CMOS-compatible top-down Si fabrication flow, which is crucial for large-scale system integration.

In this work, ambipolar SiNW FETs with a DIG structure enable the use of polarity control signals as a method toward Si circuits with increased logic expressive power. Moreover, the use of polarity control leads to improved performance in terms of $I_{\mathrm{ON}}-I_{\mathrm{OFF}}$ ratios and inverse subthreshold slopes with respect to the ambipolar behavior.

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II. Device Description

The device consists of a 20-μm-long crystalline SiNW attached between two Si pillars on an SOI wafer [see Fig. 1(a)]. The SiNW is then covered by two independent n^{++} polysilicon gates with this scheme: a main central gate (gate 1) of 7.5-μm length and a second gate (gate 2) that is used to control the SiNW portions between the main gate and the source and drain regions, respectively.

A. Fabrication

First, a low-doping p-type ($N_A \approx 10^{15}$ atoms/cm^2) SOI wafer with a 1.5-μm device layer is spin coated. The photoresist is then patterned in 1.5-μm-wide lines [see Fig. 1(b)] and used as a mask for a next isotropic Si etching. A Si plasma etching recipe is tuned to form a triangular 75-nm-wide SiNW lying on top of the buried oxide layer [Fig. 1(c)]. Then, a 30-nm-thick gate oxide and a 150-nm polysilicon layer are deposited with low-pressure chemical vapor deposition (LPCVD) method to form a main gate with 7.5-μm length [gate 1 in Fig. 1(d)]. The main gate is then isolated by a 300-nm LPCVD low-temperature oxide (LTO). A second 500-nm polysilicon layer is then deposited. Then, a thick photoresist is spun over the wafer and planarized using a chemical mechanical polishing procedure similar to the one previously described by the authors in [11]. This method leaves a protective polymer layer that is used to etch a second polysilicon gate self-aligned within the cavity due to the topography [see gate 2 in Fig. 1(e)]. After standard cleaning steps, one additional patterning of gate 2

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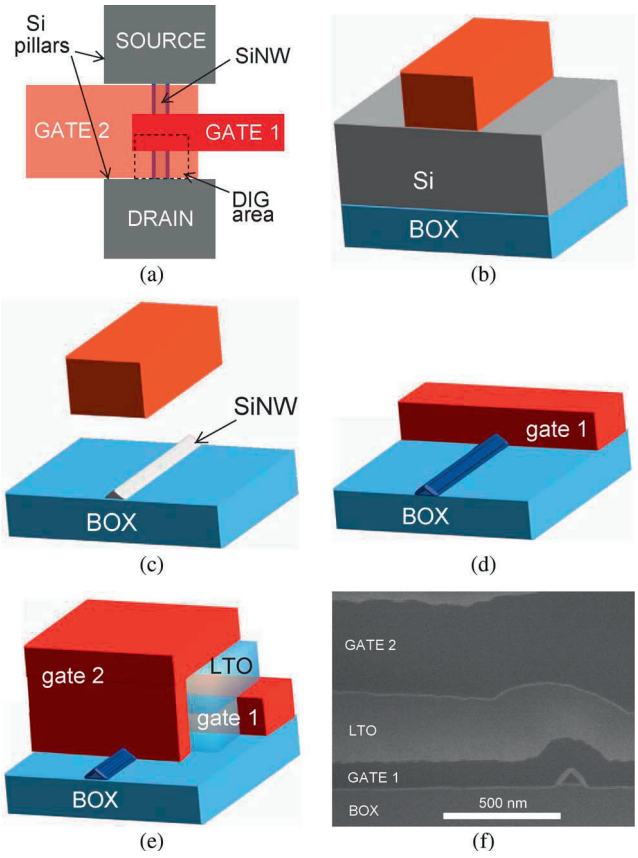


Fig. 1. Fabrication flow. (a) Top view of the dual-gate device. The next steps focus on the DIG area construction. (b) Photoresist mask is patterned. (c) After isotropic etching of Si, a triangular-shaped SiNW is formed. (d) Gate oxide and LPCVD polysilicon are deposited and patterned to form the main central gate stack. (e) LTO interpoly dielectric is deposited, and a second polysilicon gate is made self-aligned with the nanowire. (f) Focused ion beam cross section showing a triangular SiNW channel with two 75-nm sides and a 100-nm base. Gate 1, gate 2, and the LTO interpoly dielectric have 150-, 500-, and 300-nm thicknesses, respectively. The gate-1 dielectric is 30 nm thick.

is performed to remove the unnecessary polysilicon and to form areas for the contacts [see the top view of the device in Fig. 1(a)]. In Fig. 1(f), a focused ion beam cross section of the triangular SiNW channel with the DIG stack is shown. Then, source/drain contacts are formed by means of NiSi silicidation in a horizontal wall furnace in forming gas at 400 °C. Finally, Al metal lines and a pad area are defined for the electrical characterization.

B. Device Operation

The source/drain regions after NiSi silicidation have a midgap Schottky-barrier contact with the SiNW; thus, both electrons and holes can contribute to the current flow. The use of the two gates enables the selection of which carrier species shall prevail in the conduction. In the following discussions, the voltage applied to gate 1 is defined as $V_{\rm gs}$, while the voltage applied to gate 2 is defined as $V_{\rm bg}$. This scheme was proposed by Lin *et al.* [7] for the control of polarity of carbon-nanotube FETs. As shown in Fig. 2(a), a positive back-gate voltage $V_{\rm bg}$ enables electron flow, while the hole current is blocked. Similarly [Fig. 2(b)], a negative $V_{\rm bg}$ makes the opposite selection: The hole current is enabled while the electron flow is blocked.

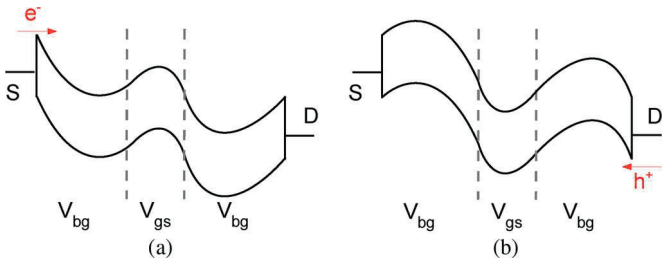


Fig. 2. (a) Conceptual band diagram for n-type operation. A positive $V_{\rm bg}$ is used to block the flow of holes from the drain. (b) Conceptual band diagram for p-type operation. A negative $V_{\rm bg}$ is used to block the flow of electrons from the source.

TABLE I
OBTAINED ELECTRICAL BEHAVIOR FOR DIFFERENT $V_{\rm bg}$ VOLTAGES

$V_{\rm bg}$[V]	$\frac{I^{h+}_{ON}}{I_{OFF}}$	$\frac{I^{e-}_{ON}}{I_{OFF}}$	SS^{h+}[mV/dec]	SS^{e-}[mv/dec]
+10	50	250	1000	600
+7.5	N/A	2000	N/A	250
+5	N/A	1000	N/A	250
+2.5	N/A	1000	N/A	325
0	1000	600	475	750
-2.5	1000	N/A	375	N/A
-5	5000	N/A	250	N/A
-7.5	10000	N/A	300	N/A
-10	30000	N/A	300	N/A

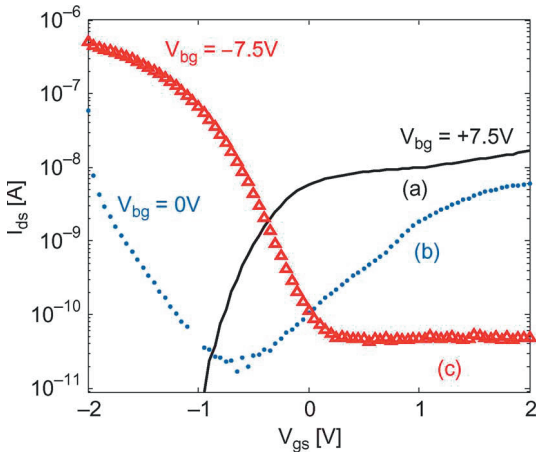


Fig. 3. Controlled ambipolar $I_{\rm ds}$–$V_{\rm gs}$ characteristics at different $V_{\rm bg}$ back-gate voltages. (a) Positive $V_{\rm bg} = +7.5$ V is used to obtain an n-type characteristic. (b) $V_{\rm bg} = 0$ V gives ambipolar $I_{\rm ds}$–$V_{\rm gs}$. (c) Negative $V_{\rm bg} = -7.5$ V is used to obtain a p-type characteristic.

III. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer in dark at room temperature. In Table I, the effect of $V_{\rm bg}$ on the inverse subthreshold slopes (SS^{h+} and SS^{e-}) for hole and electron conduction branches depicts a trend for improved SS^{h+} and SS^{e-} when increasing $V_{\rm bg}$ voltages of negative and positive polarities are applied, respectively. Similarly, improved $I_{\rm ON}-I_{\rm OFF}$ ratios ($I^{h+}_{\rm ON}/I_{\rm OFF}$ and $I^{e-}_{\rm ON}/I_{\rm OFF}$) are observed when larger $V_{\rm bg}$ voltages are applied. The improved performance is related to a reduced $I_{\rm OFF}$ current due to the screening of one of the two types of carriers for the conduction. As better shown in Fig. 3, positive or negative $V_{\rm bg}$ voltages can be used to obtain n-type or p-type

TABLE II
BINARY LOGIC VOLTAGE SIGNALS CODING FOR XOR, NAND, AND, AND NOR OPERATIONS

CODE	XOR		NAND		AND		NOR	
	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]
logic 0	+1	-7.5	-0.5	+7.5	0	0	0	+7.5
logic 1	-1	+7.5	+1	-7.5	-1	-7.5	-1	0

TABLE III
OUTPUT CURRENT LEVELS FOR THE FOUR LOGIC OPERATIONS: XOR, NAND, AND, AND NOR

logic values		XOR	NAND	AND	NOR
gate 1	gate 2	I_{OUT}[A]	I_{OUT}[A]	I_{OUT}[A]	I_{OUT}[A]
0	0	$4 \cdot 10^{-11}$	$2 \cdot 10^{-9}$	10^{-10}	$6 \cdot 10^{-9}$
0	1	10^{-8}	$2 \cdot 10^{-9}$	10^{-10}	10^{-10}
1	0	$7 \cdot 10^{-8}$	10^{-8}	10^{-11}	10^{-11}
1	1	10^{-11}	$4 \cdot 10^{-11}$	10^{-7}	$5 \cdot 10^{-11}$

I_{ds}–V_{gs}. Moreover, a symmetrical ambipolar I_{ds}–V_{gs} is obtained for $V_{bg} = 0$ V. This functionality allows for increased expressive logic power with a single FET. For instance, the two voltage signals V_{gs} and V_{bg} can be coded to make logic XOR operation with the device in Fig. 3, an operation that would require more transistors in standard CMOS technology. In Table II, V_{gs} and V_{bg} voltage values are encoded into logic levels 0 and 1 to map into four binary logic operations, namely, XOR, NAND, AND, and NOR, while using the data plot in Fig. 3. The results of the logic operations are summarized in Table III. Logic 0 and logic 1 outputs are represented by light and dark gray, respectively. Another solution that can be envisaged can use the same logic levels for both gates in order to save space for external encoding circuits. This solution will become the most desirable one by optimizing the thickness of the two gate dielectrics, which, in the current implementation, leads to a more effective electric field density for gate 1 than for gate 2. In future designs, this technological issue might be overcome by optimizing the dielectric thickness for the two gates and/or in combination with dopant segregation techniques to balance the Schottky-barrier heights for holes and electrons. Moreover, gate work-function engineering can be used to code the threshold voltage of the device, thus addressing the different logic 0/1 voltages needed for a specific logic function. Owing to these technological options, dense arrays of ambipolar DIG FETs can be envisaged as basic building blocks to map complex logic circuits. The ac characteristic of the proposed device concerning delay and power will depend, among other factors, on the capacitive coupling between the two gate electrodes. However, this parasitic coupling is estimated to be of the same order of magnitude of the source/drain-to-gate capacitance, and given the fact that the fabricated device performs a more expressive logic functionality, this additional coupling is not expected to be a limiting factor.

IV. CONCLUSION

In this study, a new device structure exploiting a DIG configuration with SiNW and top-down fabrication flow has been demonstrated as a useful building block for ambipolar-controlled logic operation. All the I_{ds}–V_{gs} characteristics, defining n-type, p-type, and ambipolar behavior, have been obtained with good $I_{ON}-I_{OFF}$ ratios of up to four orders of magnitude and with inverse subthreshold slopes close to those of state-of-the-art Schottky-barrier FETs. In addition, a single device can be used to perform any of the XOR, XNOR, NAND, AND, and NOR binary logic operations depending on the input signals encoding. The proposed integration scheme is envisaged for logic circuits exploiting the improved logic expressive power of ambipolar-controlled SiNW devices, which is enabled by the reliability of Si fabrication technology.

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New Insight on Bio-sensing by Nano-fabricated Memristors

Davide Sacchetto · Marie-Agnès Doucey · Giovanni De Micheli · Yusuf Leblebici · Sandro Carrara

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Abstract We report here on a new insight for bio-sensing based on the memristive effect of functionalized Schottky-barrier memristive silicon nanowire in dry environment. The device concept is discussed. Electrical measurements confirm the bio-detection by the narrowing of the memristive $I_{ds} - V_{ds}$ hysteresis upon interaction of antigen with antibody-functionalized nanowire.

Keywords Memristive · Ambipolar · Sensor · FET · Schottky barrier · Antibody · Antigen interaction

1 Introduction

Recently, there has been an increasing interest in nano-bio-sensing applications, due to possibility for minimal invasive, real-time monitoring for preventive treatments and therapy personalization [1]. In particular, one-dimensional silicon nanowires are good candidates for sensing devices due to their very large surface-to-volume ratio and quantum properties [2]. However, the sensing with nanowires is only exploited by the ion-sensitive field-effect-transistor paradigm [3]. Due to the nano-scale of the fabricated geometries [4], the recent discovery in solid-state devices of the memristive effect has been source of renewed research efforts in applications for high-density memory device [5]. The physical phenomena governing the memristive behavior are attributed to the change of an internal state variable, which modifies the conductance in a non-volatile manner [6]. As reported by Duan et al., memory devices are possible also with molecule-gated nanowire transistors by using redox active molecules [7]. In this short communication, we report the first evidence of unexpected new insights for a novel molecular sensing in dry conditions based on nanofabricated memristors functionalized with bio-molecular thin films. In Section 2, we describe the nano-fabrication of memristive Schottky-barrier silicon nanowires.

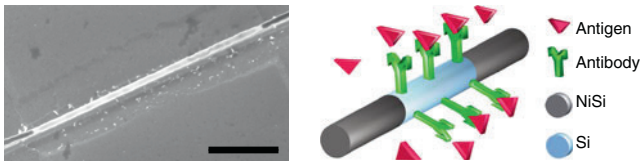
2 Device Nano-fabrication

The fabrication method utilizes some of the steps that were previously reported [8] for memristive Schottky-barrier silicon nanowire field-effect transistors. The process starts from low resistivity silicon-on-insulator substrates, with 1.5 μm device layer and 3 μm SiO_2 insulating layer. After standard lithography, the silicon nanowire is carved anchored at the top of two silicon pillars. Then, Ni is deposited on top of the pillars with overlap on the outer portions of the silicon nanowire. Hence, an annealing step at 450°C in a horizontal wall furnace forms NiSi contacts. Figure 1 shows a nano-fabricated memristive silicon nanowire with NiSi contacts.

3 Biomolecule Self-assembly

The silicon nanowire surface was derivatized with 3-glycidoxypropyltrimethoxysilane [9] and functionalized

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(a) (b)

Fig. 1 **a** Suspended functionalized silicon nanowire with NiSi extremities. *Scale bar* is 4 μm. **b** Concept model

by covalent attachment of anti-rabbit polyclonal antibodies (AB) [10]. Antigen (rabbit antibodies, AG) interact with the functionalized wire as depicted in Fig. 1b.

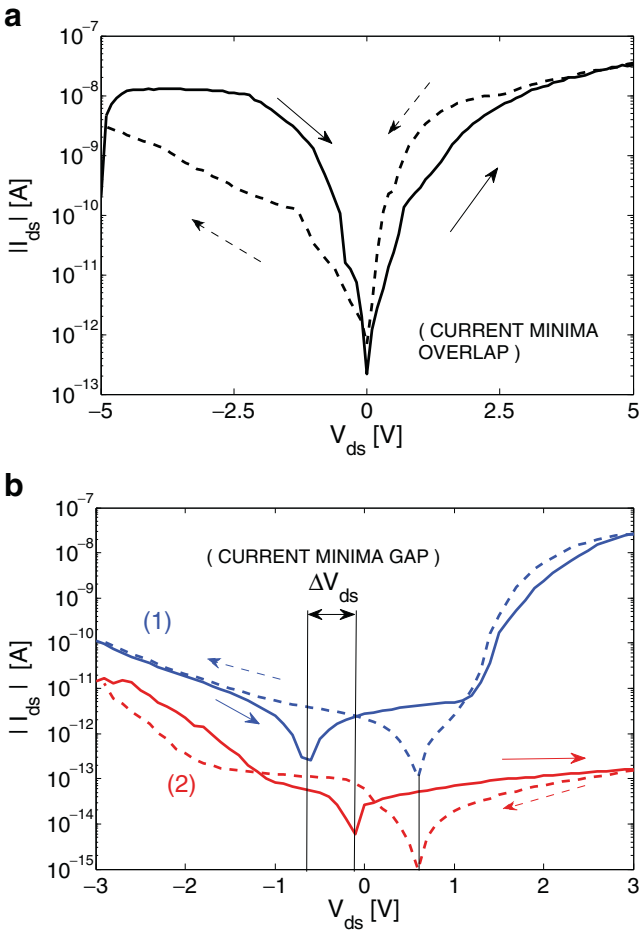


Fig. 2 $I_{ds} - V_{ds}$ curves: **a** before functionalization with AB biolayer. A typical memristive hysteresis is observed, with no ΔV_{ds} gap between I_{ds} minima in forward and backward regimes; **b** the *blue curve* (*1*) is measured after drying the sample from deionized water. The *red curve* (*2*) is measured after dipping in 5 pM AG solution and drying

4 Results and Discussion

Electrical measurements are carried out in a shielded probe station connected with HP4156C Semiconductor Parameter Analyzer and in dark, to avoid any photogenerated currents. Before functionalization with the AB layer, $I_{ds} - V_{ds}$ curves taken for forward and backward sweep do show a typical memristive behavior (see Fig. 2a), where the current minima always occur for $V_{ds} = 0\,V$, consistently with previously reported measurements [8] on non-functionalized devices. Conversely, functionalized silicon nanowires show different positions of the current minima for backward or forward regimes. This effect is observed after drying from (a) de-ionized H_2O solution and (b) 5 pM AG solution. The $I_{ds} - V_{ds}$ curve before AG up-take shows an hysteresis (curve 1 in Fig. 2b) due to charge trapping mechanisms at the Schottky junctions. The binding of an AG with the functionalized wire is responsible for a modification of the hysteresis (curve 2 in Fig. 2b), in particular to a reduction of the current minimum gap between forward and backward V_{ds} sweeps. Coherently, the up-take of increasing amounts of AG (in the pM range) results on a further diminishing of this gap.

5 Conclusions

We have demonstrated a new type of bio-sensing method, which is based on the memristive effect in Schottky-barrier silicon nanowires. This completely novel memristive detection principle is able to sense low concentrations of bio-molecules, due to interactions occurring at the nanoscale between the molecular charges trapped by the bio-layer at the surface of the wire and the ambipolar carriers supporting the memristive conductivity into the wire.

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Research Letters

Resistive Programmable Through-Silicon Vias for Reconfigurable 3-D Fabrics

Davide Sacchetto, Michael Zervas, Yuksel Temiz, Giovanni De Micheli, and Yusuf Leblebici

***Abstract*—In this letter, we report on the fabrication and characterization of titanium dioxide (TiO_2)-based resistive RAM (ReRAM) cointegration with 380 μm-height Cu through-silicon via (TSV) arrays for programmable 3-D interconnects. Nonvolatile resistive switching of $Pt/TiO_2/Pt$ thin films is first characterized with a resistance ratio up to five orders of magnitude. Then, cointegration of $Pt/TiO_2/Pt$ or Pt/TiO_2 memory cells on 140 and 60 μm diameter Cu TSVs is fabricated. Repeatable nonvolatile bipolar switching of the ReRAM cells is demonstrated for different structures.**

***Index Terms*—Memristive systems, memristor, resistive RAM (ReRAM), titanium dioxide (TiO_2), through-silicon via (TSV), 3-D integration.**

I. Introduction

THE KEY reason of the historical CMOS success lies with the exponential increase of device density that the silicon industry kept true for more than 40 years while reducing the unit cost of ICs. Recently, the pace of scaling has slowed down due to approaching fundamental limits at the device level. On one hand, researchers are striving to obtain more performant circuits by focusing on improvement of the Front-End-of-the-Line technology, for instance, innovating materials, device structures, and introducing novel state variables [1] for computation. On the other hand, the Back-End-of-the-Line technology is also addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in 3-D wafer/chip stacking solutions utilizing through-silicon vias (TSVs) [1], as well as in reconfigurable interconnect fabrics.

Considering new device technologies, the recent realization of Stanley Williams' memristor [2] [also classified as resistive RAM (ReRAM)] based on metal–insulator–metal structures, gave new push to solid-state research for logic and memory applications that can be implemented into the Back-End-of-the-Line technology. For instance, ultradense crossbar memristive memory arrays can be made thanks to the compactness of the two-terminal junction [3]. The physical realization of the memristor, whose behavior was postulated by Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6].

In this letter, the authors demonstrate the cointegration of TSVs with ReRAM stacks, offering a new path for reprogrammable 3-D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3-D chip interconnects.

II. Fabrication

A. Planar ReRAM Devices

First, high resistivity p-type ($N_A \approx 10^{15}$ atoms/cm^2) bulk-Si wafers are prepared by 500 nm thermal oxidation in H_2O atmosphere. Then, the deposition of the resistive switching materials is performed by sputtering of $Pt/TiO_2/Pt$ layers with $270/80/270$ nm thicknesses, respectively. A conceptual picture is shown in Fig. 1(a). The top electrode area of $100\,\mu m \times 100\,\mu m$ were patterned by standard lithography and etched by the ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

B. TSV Devices

The resistive switching materials were integrated with TSVs producing two different devices.

1) 140 μm TSV diameter in 380-μm thick wafer, using the $Pt/TiO_2/Pt$ memory stack.
2) 60 μm TSV diameter in 380-μm thick wafer, using the $Cu/TiO_2/Pt$ memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

The TSVs are fabricated using the same process in both the cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through-wafer etch, RCA wafer cleaning, and thermal oxidation in water atmosphere to grow a 3-μm thick oxide. A 750-nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step, the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

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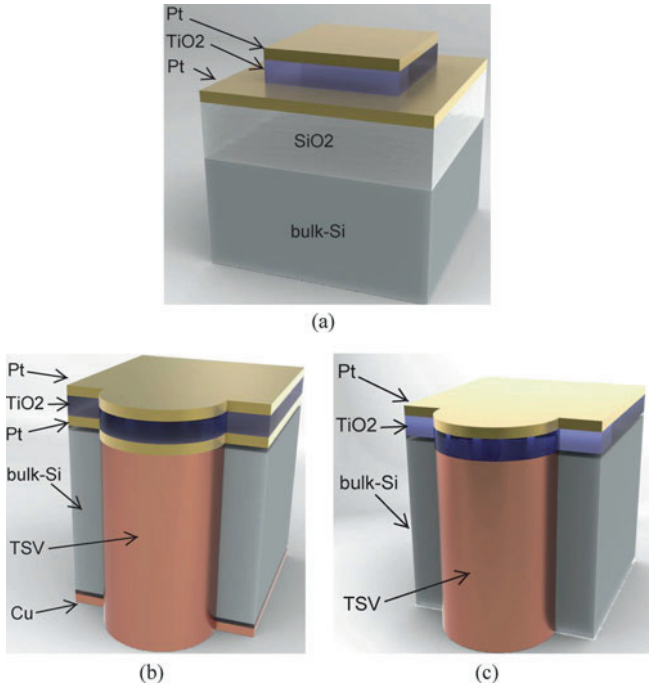


Fig. 1. (a) Concept image of planar ReRAM made of the $\mathrm{Pt/TiO_2/Pt}$ stack. (b) Concept image of the ReRAM–TSV using the $\mathrm{Pt/TiO_2/Pt}$ programmable fuse. (c) Concept image of the ReRAM–TSV using the $\mathrm{Cu/TiO_2/Pt}$ programmable fuse.

1) TSV With $\mathrm{Pt/TiO_2/Pt}$ *ReRAM:* For the first type of devices, once the TSVs are fabricated, the front side of the wafer is processed with the chemical mechanical polishing (CMP) technique to form a flat surface. The $\mathrm{Pt/TiO_2/Pt}$ stack is sputtered with layer thicknesses $270/80/270\,\mathrm{nm}$, accordingly. A concept picture of the fabricated structure can be seen in Fig. 1(b).

2) TSV With Cu/$\mathrm{TiO_2}$/Pt *ReRAM:* For the second type of devices, the wafer is polished using the CMP technique on both sides to remove the seed layer and to planarize the surfaces. Cu was, then, cleaned using an $\mathrm{NH_4 : H_2SO_4}$ etching solution at room temperature for 10 min. Then, the wafer was loaded into a vacuumed sputtering chamber and a $\mathrm{TiO_2/Pt}$ layer was deposited with thicknesses of 80 and $270\,\mathrm{nm}$, respectively. Cu of the TSV is acting as the bottom electrode of the ReRAM [see Fig. 1(c)]. Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Fig. 2(a) and (b), respectively.

III. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station under dark conditions. For electrical contacts, standard tungsten needles with $15\,\mu\mathrm{m}$ apex diameter were placed on the top electrode area very softly, since the dependence of the switching on needle pressure has been observed, similarly to the observation of local pressure-modulated conductance with atomic force microscopy tips [7]. Then, double *I–V* dc sweeps have been used to investigate the resistive switching behavior. In all the cases, the bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table I.

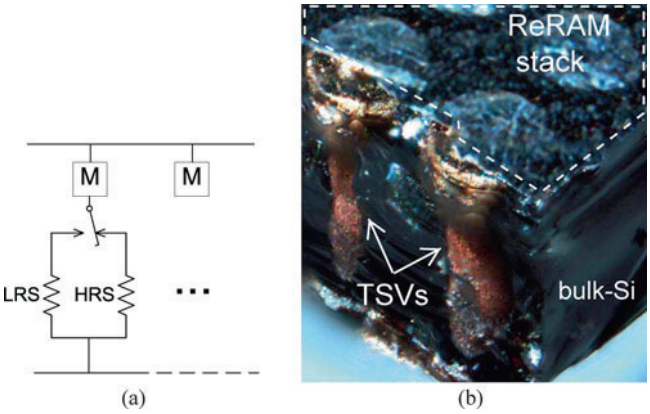


Fig. 2. (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element *M*). (b) Reconstructed 3-D photograph of the $\mathrm{TSV–Cu/TiO_2/Pt}$ device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

A. Planar ReRAM Devices

First, the planar $\mathrm{Pt/TiO_2/Pt}$ devices are characterized and it showed stable and repeatable bipolar switching behavior between $10\,\Omega$ and $1\,\mathrm{M}\Omega$ read or measured at $+1\,\mathrm{V}$ (see Fig. 3). Originally, the devices are in the high-resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low-resistance state (LRS) occurs at $+1.8\,\mathrm{V}$. After the SET event, the voltage sweep continues until $+2\,\mathrm{V}$ and, then, move back toward the negative-voltage region. When $-1.3\,\mathrm{V}$ is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about five orders of magnitude is read at $+0.5\,\mathrm{V}$.

B. TSV–$\mathrm{Pt/TiO_2/Pt}$ Devices

Next, $\mathrm{TSV–Pt/TiO_2/Pt}$ devices with the same layer thicknesses are measured, showing resistance switching below $\pm 1\,\mathrm{V}$ (see Fig. 4). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks, as well as to surface states acting as dopants for the $\mathrm{TiO_2}$ [8]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only $+0.6\,\mathrm{V}$, while the RESET voltage is measured at $-0.5\,\mathrm{V}$. Using a reading voltage of $+0.2\,\mathrm{V}$, an HRS of $2\,\mathrm{M}\Omega$ and LRS of $666\,\Omega$, with the resistance ratio of 3000 are measured.

C. TSV–$\mathrm{Cu/TiO_2/Pt}$ Devices

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the

TABLE I
OBTAINED RERAM ELECTRICAL PARAMETERS FOR DIFFERENT DEVICES

Device	SET	RESET	HRS	LRS	HRS/LRS	Reading
Planar $Pt/TiO_2/Pt$	$+1.8$ V	-1.3 V	10 MΩ	10 Ω	10^5	$+1$ V
TSV $-$ $Pt/TiO_2/Pt$	$+0.6$ V	-0.5 V	2 MΩ	666 Ω	3003	$+0.2$ V
TSV $-$ $Cu/TiO_2/Pt$	-4.2 V	$+5$ V	500 MΩ	5 Ω	10^5	$+1$ V

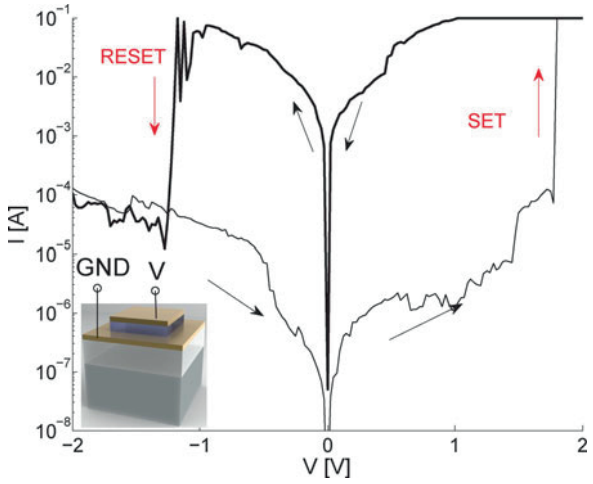


Fig. 3. Resistive switching through *I–V* sweeps for planar $Pt/TiO_2/Pt$ devices.

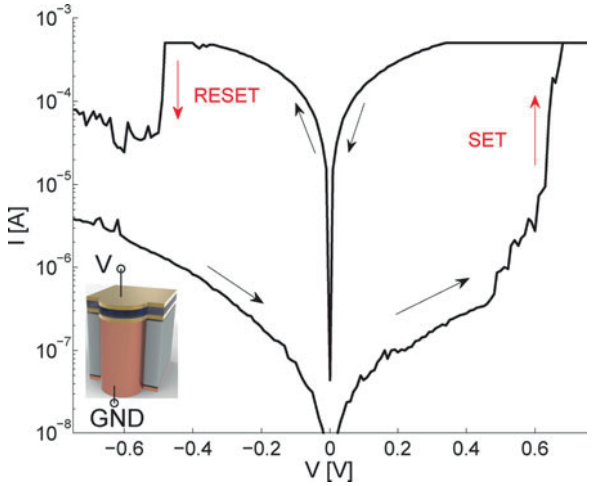


Fig. 4. Resistive switching through *I–V* sweeps using the TSV–$Pt/TiO_2/Pt$ programmable fuse.

TiO_2 layer [9], [10], which is an n-type semiconductor, an alternative device is obtained by depositing TiO_2 and Pt directly on top of the Cu–TSV. Thus, thanks to a larger Schottky barrier height at the Cu–TiO_2 interface, a larger programming window is obtained (see Fig. 5). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. An HRS of 500 MΩ and LRS of 5 kΩ are read at $+1$ V.

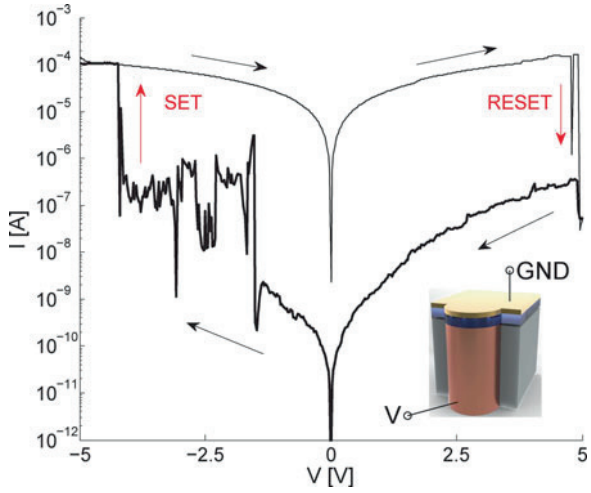


Fig. 5. Resistive switching through *I–V* sweeps using the TSV–$Cu/TiO_2/Pt$ programmable fuse.

IV. CONCLUSION

In this study, $Pt/TiO_2/Pt$ obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with the LRS to HRS resistance ratio up to five orders of magnitude. The device is successfully integrated on top of 140 and 60 μm TSV arrays either in the full $Pt/TiO_2/Pt$ stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The cointegration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3-D chip interconnects.

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INVITED PAPER

Multiterminal Memristive Nanowire Devices for Logic and Memory Applications: A Review

The authors of this paper introduce multiterminal memristive nanowire devices in memory applications.

By Davide Sacchetto, Giovanni De Micheli, *Fellow IEEE*, and Yusuf Leblebici, *Fellow IEEE*

ABSTRACT | Memristive devices have the potential for a complete renewal of the electron devices landscape, including memory, logic, and sensing applications. This is especially true when considering that the memristive functionality is not limited to two-terminal devices, whose practical realization has been demonstrated within a broad range of different technologies. For electron devices, the memristive functionality can be generally attributed to a material state modification, whose dynamics can be engineered to target a specific application. In this review paper, we show that trap charging dynamics can explain some of the memristive effects previously reported for Schottky-barrier field-effect Si nanowire transistors (SB SiNW FETs). Moreover, the SB SiNW FETs do show additional memristive functionality due to trap charging at the metal/semiconductor surface. The combination of these two memristive effects into multiterminal metal–oxide–semiconductor field-effect transistor (MOSFET) devices gives rise to new opportunities for both memory and logic applications as well as new sensors based on the physical mechanism that originate memristance. In the special case of four-terminal memristive Si nanowire devices, which are presented for the first time in this paper, enhanced functionality is demonstrated. Finally, the multiterminal memristive devices presented here have the potential of a very high integration density, and they are suitable for hybrid complementary metal–oxide–semiconductor (CMOS) cofabrication with a CMOS-compatible process.

KEYWORDS | Ambipolar; memristor; nanowire; Schottky barrier; transistor

I. INTRODUCTION

The main source of the complementary metal–oxide–semiconductor (CMOS) success lies in the exponential increase of device density that the silicon industry kept true for more than 40 years reducing the unit cost of integrated circuits. Recently, the pace of scaling has been slowed down due to approaching fundamental limits at the device level. While the paradigm of scaling is still alive, researchers are striving to follow Moore's law by focusing on new materials, new device structures, and new state variables. The basic building block for circuits has always been the four-terminal planar transistor but new versions of the metal–oxide–semiconductor field-effect transistor (MOSFET) structure such as the double-gate FET, the FinFET, the gate-all-around nanowire FET can be found in commercial products.

Due to the natural limitations of materials, future deeply scaled circuits will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages an end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. A long list of fundamental state variables other than charge includes the spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states [1]. Technologies using new state variables would have to be implemented within a completely new technological

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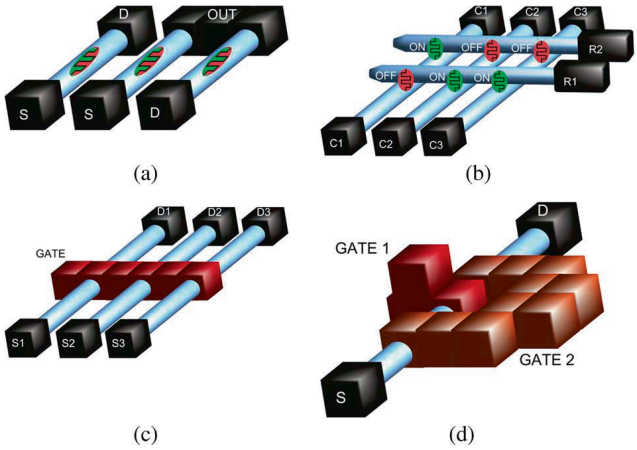


Fig. 1. ***(a) Parallel nanowire two-terminal memristive devices. (b) Crossbar array consisting of memristive cross points (two terminal). (c) Gate controlled three-terminal nanowire memristive device. (d) Double-gate four-terminal nanowire memristive devices.***

platform, and cannot be seen as CMOS-compatible alternatives.

The recent realization of devices by Strukov *et al.* [2] gave new push to solid state research for logic and memory applications. For instance, ultradense crossbar memristive memory arrays can be made thanks to the compactness of the two-terminal junction. Complementary logic based on two-terminal memristive devices [see Fig. 1(a)] or ultradense crossbar arrays with memristive cross points [see Fig. 1(b)] can dramatically improve device density up to 10^{11} b/cm^2 [3]. Moreover, the use of memristive effects as new state variables for computation can be exploited to build new types of functional devices with three or four terminals [see Fig. 1(c) and (d), respectively].

The physical realization of the memristor, whose behavior was postulated by Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6]. It is worth noting that a generalized model for memristive systems can be implemented under direct current (dc), small signal, and sinusoidal excitation [5]. The implications of such modeling are linked with the observation of memristive functionalities over a broad range of technologies based on nanoelectronics and nanoionics behaviors.

In this paper, a short review (see [7] and [8] for a more complete list) of two-terminal memristive devices is reported, while more space is given to multiterminal memristive devices that for their nature are readily implementable with front-end CMOS processes. Particular emphasis is given to devices based on the *gate-all-around (GAA) Schottky-barrier field-effect transistor (SB FET)* concept with *Si nanowire (SiNW)* channels on bulk-Si or silicon-on-insulator (SOI) wafers. The new concept of four-terminal memristive devices is presented in this paper for the first time and enhanced functionality is demonstrated. The coexistence of memristive functionality at both gate and drain electrodes with ambipolar conductance make these devices unique and capable of very high expressive power. The electrical characteristics can be attributed to the coexistence of different physical phenomena, such as device ambipolarity (both holes and electrons are responsible for conduction), Schottky barrier modulation induced by interface trap charging, and charge trapping at the gate oxide interface. It is highlighted that the unique properties of the emerging nanowire devices combine memristive functionality with ambipolar conductance, thus giving rise to novel conductance properties. We confirm some of these statements with previously reported *poly-crystalline Si nanowires (poly-SiNWs)* [9], which show a similar memristive behavior.

The memristive functionality is not a unique property of two-terminal passive devices but mainly a memory effect related to internal state variable changes. For instance, the memristive functionality can also arise from a delayed switching response of a Zener diode [10]. In the next sections, we review some of the two-terminal passive devices that can be modeled as memristive. The memristive functionality is seen as arising from different physical mechanism for different device classes. Thus, three- and four-terminal devices that show memristive functionality can be used for electrical control signals (either voltage or current). It is important to remember that a device showing a "pure" flux-charge relationship has not been found yet. Conversely, internal state variables can provide a stimulus response that can be modeled as memristive, thus adding more degrees of freedom for circuits designers.

This review paper is organized as follows. In Section II, two-terminal memristive devices are quickly surveyed. Then, in Section III, the electrical behavior of three-terminal memristive devices is discussed. Section IV will discuss on various fabrication methods for Si nanowire memristive devices. Hence, four-terminal memristive devices based on Si nanowires are discussed in Section V. Finally, possible applications for multiterminal memristive devices are discussed in Section VI.

II. TWO-TERMINAL MEMRISTIVE DEVICES

Two-terminal memristive devices can be based on metal/oxide switches, such as for SiO_2, HfO_2 [11], CuO [12], NiO [13], ZnO [14], Al_2O_3 [15], VO_2 [16], and $SrTiO_3$ [17]. These devices behave as solid-state electrochemical switches, whose resistance is defined by a metallic filament formation mechanism related to the solid-state redox reactions stimulated by the polarity of the applied electric field [18]. One example is the CuO-based ReRAM of Dong *et al.* [12] that shows repeatable resistive switching at very low voltages.

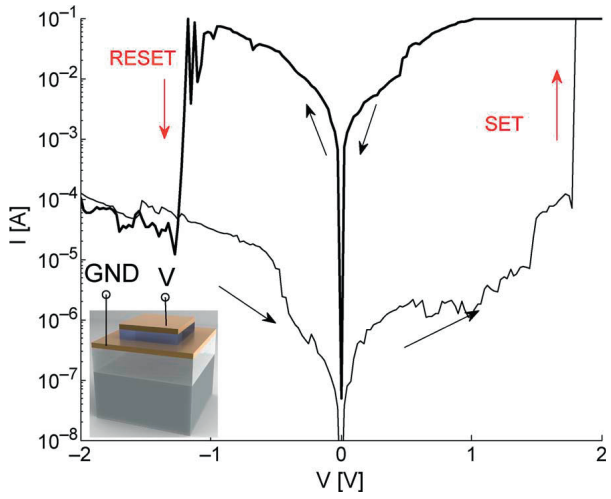


Fig. 2. *Resistive switching through I-V sweeps for planar Pt/TiO_2/Pt [21]. The inset shows the Pt/TiO_2/Pt ReRAM sandwich layer on top of an insulated substate with the two-terminal electrical contacts.*

The well-known TiO_2-based ReRAM [19], [20] seems to be based on a different mechanism, which is attributed to the vacancy/dopant diffusion in the oxide layer. The redistribution of oxygen vacancies into the TiO_2 depends on the polarity of the applied voltage, and it causes the switching between a semiconductor state into a metallic one. Typical ReRAM functionality of the TiO_2-based ReRAM is shown in Fig. 2 [21].

Another type of two-terminal memristive device is the phase change (PC) RAM [22]. The main switching mechanism is based on phase transition between an amorphous and a crystalline type due to Joule heating effects controlled by a voltage pulse. For instance, Si nanowires can be engineered such that melting and solidification processes can be iterated, thus giving rise to alternate restates [23].

Another class is based on polymers [24]. Several memristive switches can be built by interposing a biomolecule layer with properties ranging from molecule-dependent switching, such as rotaxanes [3], or more in general on interlocked molecules [25] but also on molecule-independent switching, where a filament formation mechanism through the molecular layer is involved [26].

A fifth class belongs to spintronics [27]. The spin-transfer-induced domain wall motion in a spin valve structure is by nature a memristive effect and is confirmed by some recently published results [28]. Moreover, Pershin *et al.* demonstrated that electron-spin polarization controlled by the external voltage applied to a spintronic device acts as a state variable that can be modeled as memristance [29].

In all these devices the amplitude and frequency of the input signal contribute in the formation of a so-called pinched hysteresis loop, whose salient feature is its zero crossing property [5], which is critical for ultralow power operation.

III. THREE-TERMINAL MEMRISTIVE DEVICES

The new concept of three-terminal memristive device is presented in terms of memristive functionality for logic and memory applications.

Examples of three-terminal memristive devices are the electrochemical organic memristor [31], the solid-electrolyte nanometer switch [32], the ferroelectric FET [33], and the ambipolar Si nanowire Schottky barrier FET [9], [34].

A classification of three-terminal memristive devices can be based from the general concept of the FET structure [see Fig. 3(a)] in which memristive functionality can be inserted either by engineering the gate dielectric or by gating a memristive channel. For instance, trap charging dielectric layers inserted between the channel and the gate fall into the category of FET with capacitive memory storage [Fig. 3(b)]. Examples of devices falling into this category can be the flash memory for which the trap charging into the gate dielectric influences the transconductance state of the channel. Thus, a first category that exploits the operation of writing/erasing cycles into the gate dielectric will be a generalization of the flash memory concept, for which volatility of the charges that are injected into the trap charging layer can be tuned accordingly to a desired frequency response.

A second category is the one of the gated memristor [Fig. 3(c)]. A few examples are the electrochemical organic memristor [31], the biomemristive nanowire [30], and the solid-electrolyte nanometer switch [32]. In the electrochemical organic memristor, the gate potential is represented by the potential of the bath, which is used to transfer positively charged Rb^+ ions into a polyaniline

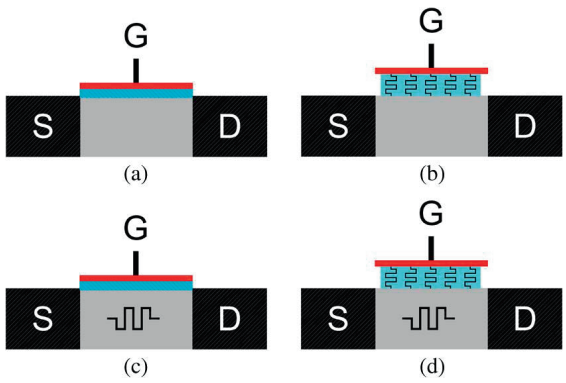


Fig. 3. *Categorization of FETs with memristive functionalities: (a) Conventional FET. (b) FET with memristive gate dielectric. (c) Gated memristor (memristive channel). (d) Gated memristor with memristive dielectric.*

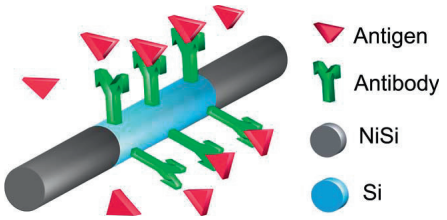


Fig. 4. *Suspended functionalized Si nanowire with NiSi extremities. The functionalized layer is capable of trapping antigen molecules which in turn affects the memristive hysteresis behavior, giving a new method for biosensing [30].*

(PANI) layer. The conductivity change can be iterated by switching the polarity of the bath potential, thus giving rise to a unipolar I_{ds}–V_{ds} curve that can be modeled as a memristor. In this case, the device can be set into either memristive or diode functionality. Similarly, a novel method for biosensing that has been recently proposed exploits the memristive effect to detect low concentration of biomolecules [30]. The device consisting of a NiSi/Si/NiSi nanowire structure coated with antibody layer (see Fig. 4) shows memristive behavior. The hysteresis loop of this device has been demonstrated for detection of low concentrations of biomolecules (antigen) in a dry environment (see Fig. 5). Conversely, the three-terminal solid-state electrolyte nanometer switch shows a typical bistable resistance state but using 100 times less current than standard two terminal operation [35]. This device is based on controlling the filament formation mechanism using the voltage of a gate terminal.

The ambipolar SB FET with SiNW channel reported in [36] [see Fig. 3(d)] falls in both categories of gated memristor and trap charging dielectric, as it shows dynamic trap charging mechanisms at the Schottky junctions and in the gate dielectric insulator. The result depicted in Fig. 6 shows a hysteretic behavior that is reminiscent of a two-terminal monolithic memristive device [37]. The hysteresis reflects the fact that the I_{ds}–V_{ds} curve for forward V_{ds} sweep is not identical to the same curve for backwards V_{ds} sweep. It can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [38]. First, two-terminal measurements are performed. The drain/source current I_{ds} is measured versus the drain/source voltage V_{ds} at constant $V_{gs} = 5$ V. The device is equivalent to two back-to-back Schottky diodes. The two diodes operate in opposite regimes: for negative V_{ds}, the source-to-channel diode is reversely biased while the drain-to-channel diode is forward biased. For positive V_{ds} both diodes invert their respective bias conditions. In either case, I_{ds} is limited by the current flowing in the reverse-biased diode. The reverse current of a metal/insulator/semiconductor diode has been observed to be very sensitive to charge trapping at the metal/semiconductor interface [15]. The large current value in the range of mA is most likely due to the large parallel parasitic structure in the bulk. In an ideal Schottky diode, the current is given by

$$I = I_S \cdot e^{-\phi_B q/kT}\left(e^{Vq/kT} - 1\right) \tag{1}$$

with I and V the diode current and voltage, respectively, ϕ_B the Schottky barrier, k the Boltzmann constant, q the

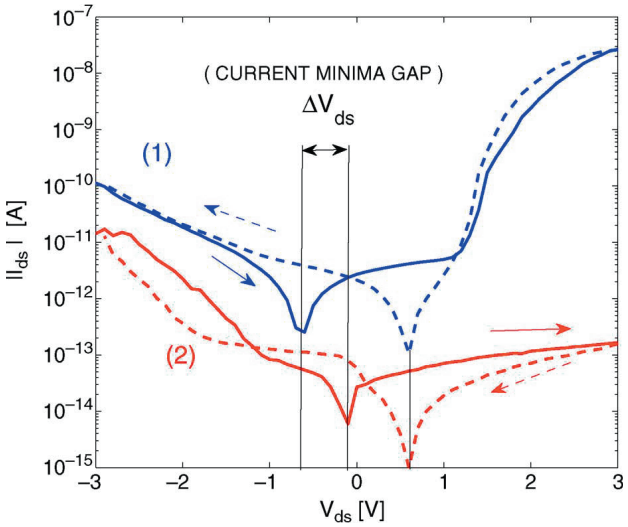


Fig. 5. *A typical memristive hysteresis is observed; the blue curve (1) is measured after drying the sample from deionized water. The red curve (2) is measured after dipping in 5-pM antigen solution and drying. The measured V_{ds} is proportional to the concentration of antigen [30].*

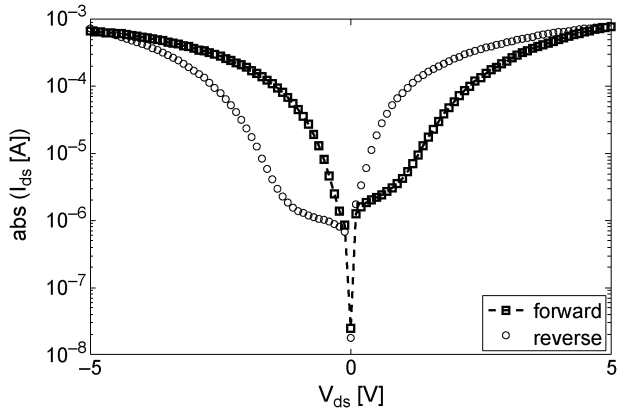


Fig. 6. *I_{ds}–V_{ds} characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 SiNW in parallel. The forward sweep curve has a symmetrical correspondence with the reverse sweep curve, showing the respective Schottky barrier modulation. A current ratio of about 50 is found at either $V_{ds} = \pm 1$ V. This behavior is typical of two-terminal memristive devices for ReRAM applications.*

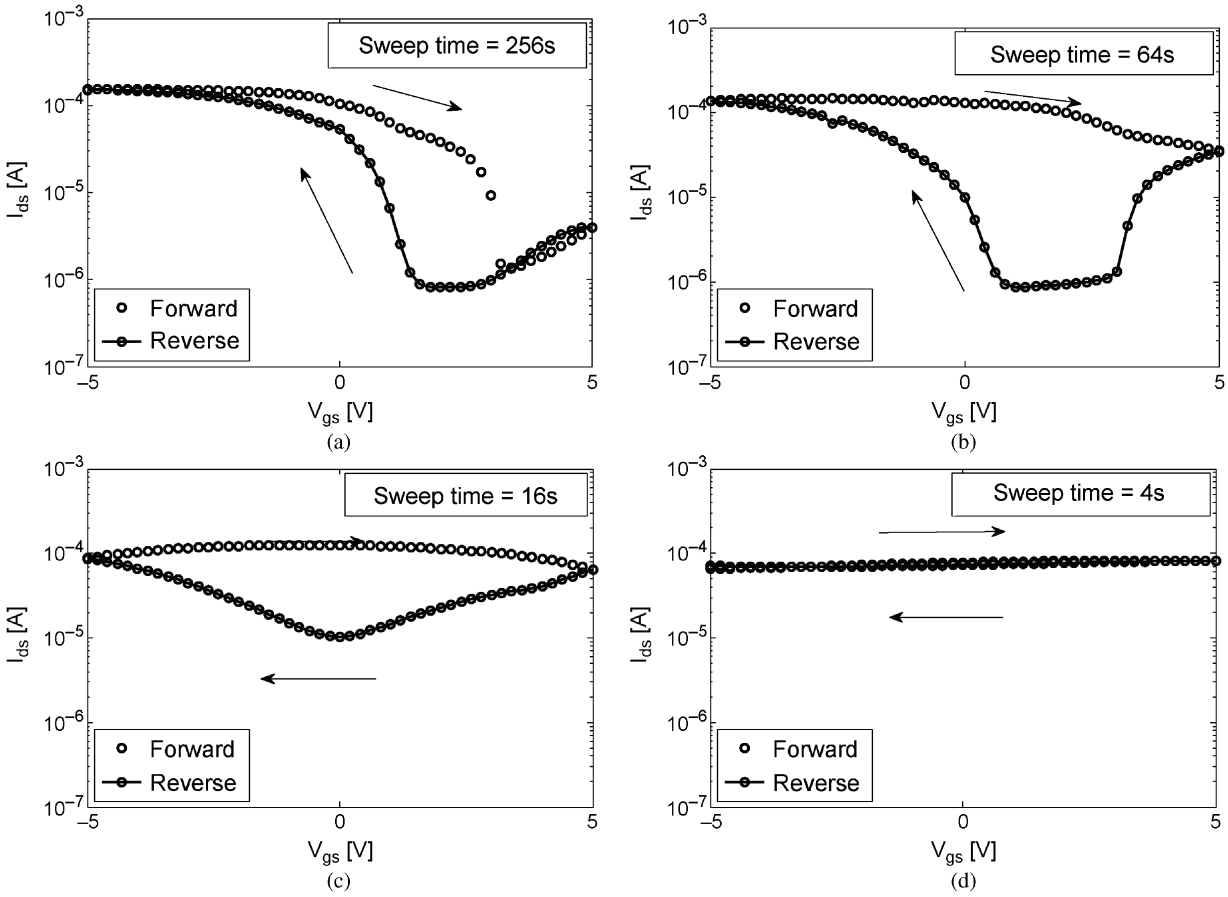


Fig. 7. ***Hysteretic dependence with the measurement (sweep time) duration; the hysteresis window closes by reducing the measurement time: (a) 256 s; (b) 64 s; (c) 16 s; and (d) 4 s.***

elementary charge, and T the absolute temperature. From the measured hysteretic behavior, it seems that the diode curve is modified as follows:

$$I = I_S \cdot e^{-\phi_B q/kT}\left(e^{(V-V_0(V))q/kT} - 1\right) \qquad (2)$$

with V_0 a built-in voltage at the Schottky contact that is positive for a positive V sweep and negative for a negative V sweep.

Another memristive functionality is linked with charging/decharging mechanisms into the gate dielectric. We measure I_{ds} for constant $V_{ds} = 1$ V while sweeping V_{gs} back and forth between -5 and $+5$ V [see Fig. 7(d)]. The devices are not annealed, and the source is connected to the substrate. This measurement is repeated for different integration times, which is a parameter of the measurement setup that can be set by the operator; and it represents the time over which the measurement is repeated and averaged. The I_{ds}–V_{gs} curves show an ambipolar behavior, meaning a large current conductance under either high or low gate bias. This is mainly due to the utilization of a silicide (NiSi) having a work function value that falls within the silicon bandgap, and to the utilization of a lightly doped silicon. On the other hand, the I_{ds}–V_{gs} curves have a hysteretic behavior that suggests the hypothesis of charge trapping at the semiconductor/oxide interface of the MOS capacitor, as well as the existence of interface states at the metal/semiconductor junction. Both ambipolarity and hysteresis depend on the integration time (see Fig. 7). When V_{gs} reaches $+5$ V in forward mode, the electrons experience a maximum probability of charges being trapped in the gate oxide, which is enhanced when the integration time is longer. Due to the electron trapping at the gate oxide, the channel operates in accumulation mode, with a lower conductance state for positive V_{gs}, than in the inversion mode for negative V_{gs}. Sweeping V_{gs} back to negative values reduces the amount of electrons trapped and the device operates in inversion mode, which restores the higher conductance state.

The threshold at which this high conductance state is reached depends on the integration time. The hysteresis window is larger when the integration time is shorter, because the charges have less time to be trapped and

detrapped. In the case of a very short integration time, the charges cannot be completely trapped and the lower conductance state is not reached (see Fig. 7).

IV. Si NANOWIRE MEMRISTIVE DEVICE FABRICATION METHODS

This section summarizes the main fabrication steps for multiterminal memristive devices based on CMOS-compatible Si nanowire technology. More details about the process flow can be found in [9], [36], and [39] for crystalline-Si (c-Si), polycrystalline-Si (poly-Si), and amorphous-Si (α-Si) nanowire channels. All the techniques yield nanowires with a subphotolithographic thickness. The general scheme is the one of the SB SiNW FET with midgap source/drain junctions. The use of a NiSi/poly-Si or NiSi/Si with undoped or lightly doped channel gives rise to a midgap Schottky barrier responsible for ambipolar conductance (see Fig. 8). The ambipolar nature of the midgap Schottky barrier field effect transistor (SBFET) can be qualitatively understood by the equal probability of either electron or hole injection, which is related to the midgap Schottky barriers. Both devices confirm the existence of an ambipolar conduction with a hysteretic behavior due to either charge trapping or modulation of the Schottky barrier through current flow. The following section surveys the fabrication details for three types of device.

A. Gate-All-Around Si Nanowire FETs

Bulk-Si wafers with low boron concentration ($N_A \sim 10^{15}$ atoms/cm^3) have been used as a substrate for the fabricated devices. Vertical stacks of Si nanowires are defined on the substrate by optical lithography [see Fig. 9(a)] without any constraint on the resolution limit (1 μm). The photoresist is then used as a mask for a deep reactive ion etching (DRIE) [Fig. 9(b)]. The optimized DRIE technique, which alternates plasma etching with passivation steps, defines scalloped trenches attached to Si pillars with high reproducibility. The enhanced scalloping effect produces vertical modulation of the trench width. A

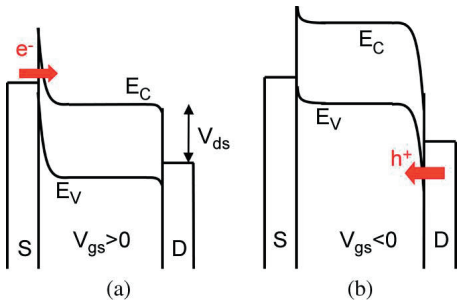


Fig. 8. *Band diagram explaining ambipolarity: (a) positive V_{gs} reduces the width of the Schottky barriers for electrons; (b) negative V_{gs} reduces the width of Schottky barrier for holes.*

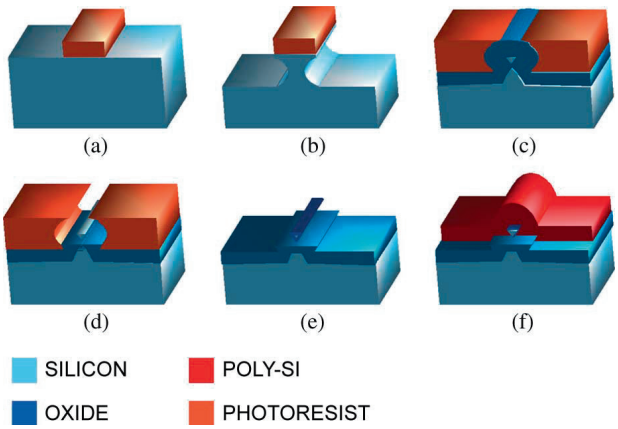


Fig. 9. *GAA SiNW SBFET process flow. (a) A photoresist line determines the nanowire position. (b) DRIE etching forms a scalloped trench. (c) After wet oxidation, the Si trench reduces to a suspended nanowire. The caves are filled with photoresist and planarized with CMP. (d) Buffered HF oxide etch releases the SiNWs. (e) Gate oxidation. (f) Polysilicon is deposited and patterned to form the gate.*

sacrificial oxidation is then carried out with the double purpose of eliminating the Si where the trench is thin, and also to reduce the surface roughness induced by the etching [Fig. 9(c)]. A combination of chemical mechanical polishing (CMP) and buffered HF (BHF) dip leaves vertically stacked nanowires suspended on a thick layer of insulating oxide [Fig. 9(d)]. The gate oxide is grown in a horizontal furnace with a dry atmosphere [Fig. 9(e)]. The gate polysilicon is conformally deposited and doped with phosphorous by means of a diffusion process and then patterned with a combination of isotropic and anisotropic plasma etching steps [Fig. 9(f)]. The fabrication of SBFETs requires the use of metallic source and drain contacts, meaning source-to-body and drain-to-body Schottky junctions. We pattern a Cr/Ni bilayers (10 nm/50 nm) on top of the Si pillars, partially covering the SiNW at the anchor points (see Fig. 10). This leads to the silicidation of the nanowire channel from the Cr/Ni bilayer toward the gated region of the nanowire. The process presented here is compatible with the one presented in [34] for dense SiNW FET arrays. An example of 3-D crossbar construction with 1 GAA poly-Si gate and 4 $\times$ 4 SiNW channels is shown in Fig. 11.

B. Poly-Si Nanowire FETs

The spacer technique is a promising approach to define subphotolithographic dimensions by using standard photolithography and CMOS steps [9]. The process flow is illustrated in Fig. 12. First, a sacrificial layer of SiO_2 is defined on a Si substrate followed by the deposition of a thin conformal layer of poly-Si [Fig. 12(a)]. Next, the poly-Si is etched by a reactive ion etching (RIE) technique, in order to remove the lateral layer and keep the sidewalls as a spacer [Fig. 12(b)]. Then a second low temperature

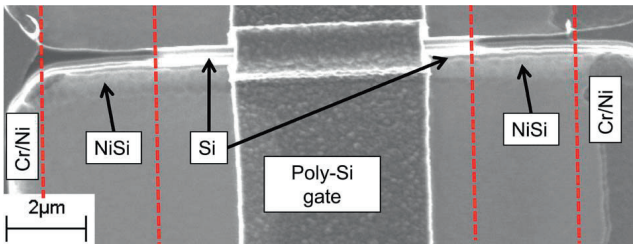


Fig. 10. *GAA SiNW SBFET with Cr/Ni source/drain after the liftoff process. The change in contrast on the NW channel is attributed to a difference between Si and silicided regions.*

oxide (LTO) spacer is defined next to the poly-Si in order to isolate the first poly-Si spacer [Fig. 12(c)]. The spacers form the nanowires with thicknesses ranging between 20 and 60 nm. The contact regions of the undoped poly-Si nanowire are defined by the electron-beam evaporation of 10-nm Cr and 50-nm nichrome ($Ni_{0.8}Cr_{0.2}$) and liftoff [Fig. 12(d)]. The Cr enhances the adhesion and thermal stability of Ni to oxidation during the following two-step annealing process. The substrate is used as a back-gate with a thick dry oxide as insulator (up to 400 nm thick). A scanning electron microscope (SEM) image of the obtained structure with an additional top gate defined on the poly-SiNW is shown in Fig. 13. This process has been reported for the construction of dense poly-SiNW crossbar arrays [40]. A small crossbar with one upper poly-SiNW and four lower poly-SiNW is shown in Fig. 14.

C. Low-Temperature Fabrication of α-Si Nanowires FETs

The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500-nm-thick wet oxide and a 100-nm LTO layer. Then, a 100-nm α-Si film is deposited as the active layer. A 70-nm-thick dilution of hydrogen-silsesquioxane (HSQ) is spin coated and patterned with e-beam lithography. Lines having widths ranging from

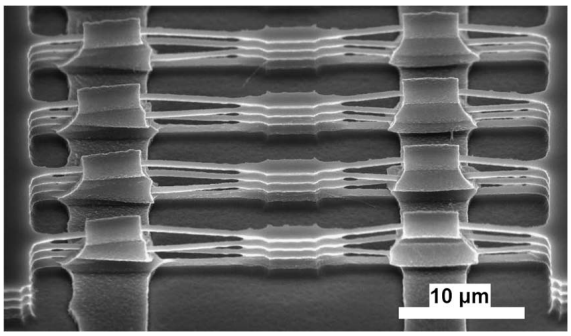


Fig. 11. *A 4 × 4 SiNW array with 2 poly-Si gate-all-around construction. The image is taken from [34].*

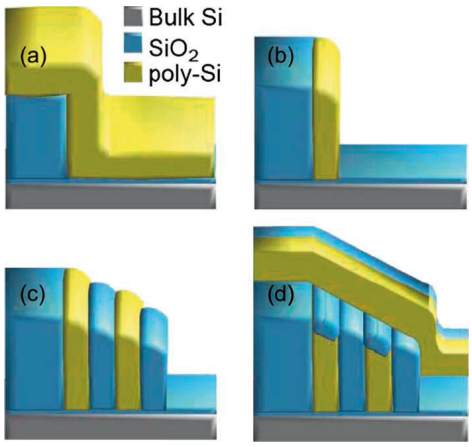


Fig. 12. *Nanowire arrays constructed using multi-spacer patterning technique [36]. (a) Conformal deposition of poly-Si. (b) RIE etch. (c) Definition of a SiO_2 spacer and iteration of previous steps. (d) Contacts formation.*

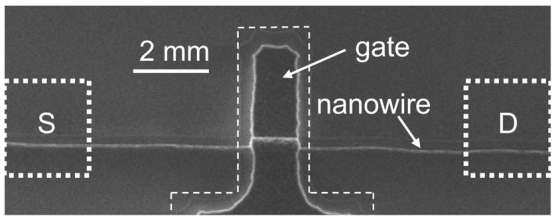


Fig. 13. *SEM image of a poly-SiNW with a top gate and Cr/$Ni_{0.8}Cr_{0.2}$*

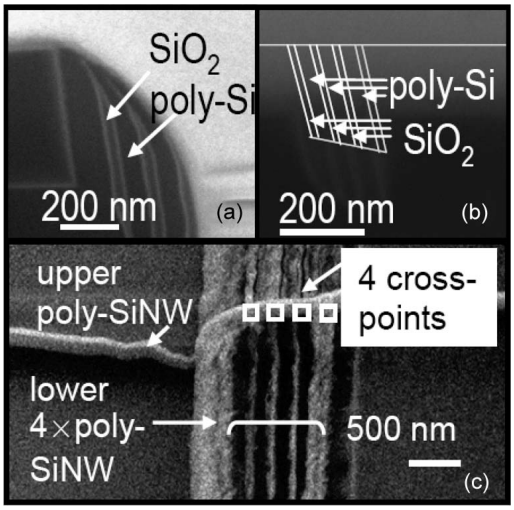


Fig. 14. *(a) Poly-Si NWs cross-section. (b) Poly-Si and SiO_2 spacers. (c) SEM image of a small crossbar with 1 upper and 4 lower poly-Si spacers [40].*

70 to 250 nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip BHF step. The obtained α-Si nanowires are then covered by a 40-nm dry oxide and a 50-nm LPCVD poly-Si

layers. Large 100 μm $\times$ 100 μm poly-Si pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, poly-Si Ω-gated FinFETs with gate lengths between 1 and 10 μm are obtained.

Then, a bilayer of 20-nm Ti/55-nm Ni is patterned with liftoff to form electrical contacts between the Si nanowires and the pads. A 400 °C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been chosen for its midgap work function and for its use in α-Si metal induced recrystallization process [41]. The fabrication flow is completed by the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100-nm-thick SiN membranes with apertures having widths between 100 nm and 1 μm [42]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2-μm [42] accuracy using a customized SUSS MA/BA6 mask aligner [43]. The clamped substrate-stencil setup is placed in an evaporator where 100-nm-thick Al gates are deposited. FinFETs and inverters with up to 62-μm nanowire length were fabricated. An example of a 2-μm-long poly-Si gate FinFET having 100 nm $\times$ 65 nm Si nanowire channel is shown in the SEM tilted view of Fig. 15(a). In Fig. 15(b), a Si nanowire transistor with 130 nm $\times$ 65 nm channel [see Fig. 16(d)] cross section and 700-nm large stenciled Al gate is shown. Focused ion beam (FIB) cross sections [see Fig. 16(a)–(c)] demonstrate nanowire channels sections having widths between 65 and 130 nm. The total Si thickness is reduced from the initial value of 100 to 65 nm due to processing. Narrower nanowires (the expected nanowire size was around 35 nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

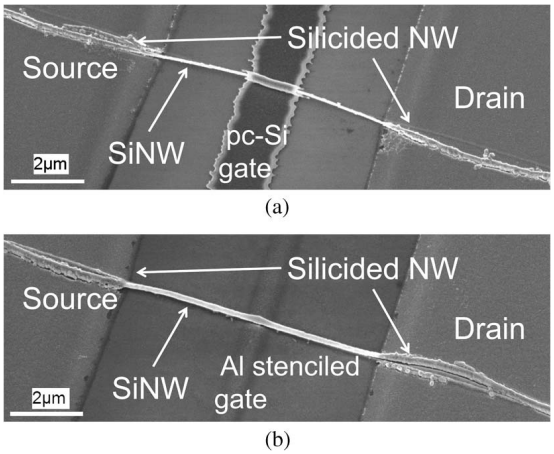


Fig. 15. *FinFETs with silicided nanowire portions at source/drain contacts: (a) poly-Si FinFET having 2-μm-long gate and 60 nm $\times$ 65 nm channel cross section. (b) Al stenciled FinFET having 700-nm gate length and 60 nm $\times$ 140 nm channel cross section.*

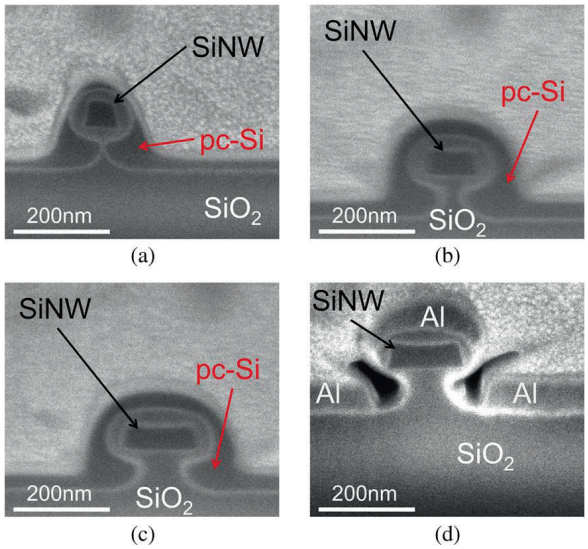


Fig. 16. *FIB cross sections showing the nanowire channels embedded in 40-nm oxide and gate materials: (a) poly-Si -gate FinFET with 60 nm $\times$ 65 nm section; (b) poly-Si -gate FinFET with 60 nm $\times$ 110 nm section; (c) poly-Si -gate FinFET with 60 nm $\times$ 140 nm section; (d) Al stenciled-gate FinFET with 60 nm $\times$ 140 nm section.*

V. FOUR-TERMINAL MEMRISTIVE DEVICES

Memristive functionality can be seen as state variable that can be used for more expressive logic gates [6]. The memristive behavior reported in Section III for the SB SiNW FETs can be tuned by operating on the polarity of the gate voltage. This type of behavior is linked with the

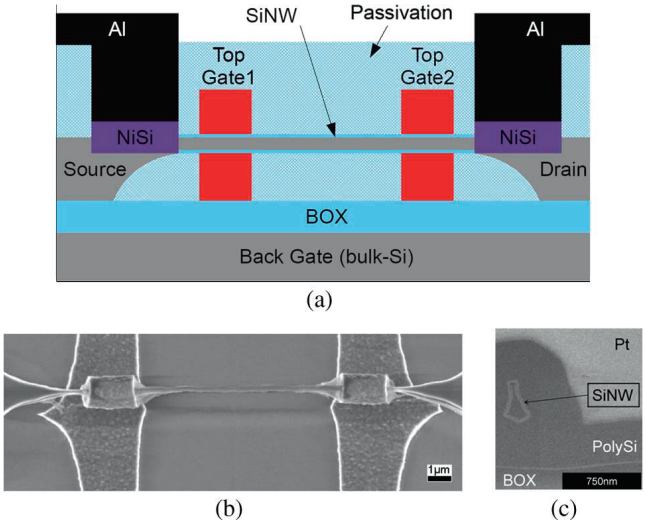


Fig. 17. *(a) Schematic cross section of a dual-gate device with NiSi source and drain regions on SOI substrate. (b) A 20-μm-long SiNW with two parallel GAA polysilicon gates having 4-μm gate lengths. (c) A FIB cut cross-section image showing the SiNW channel surrounded by a 500-nm polysilicon top gate.*

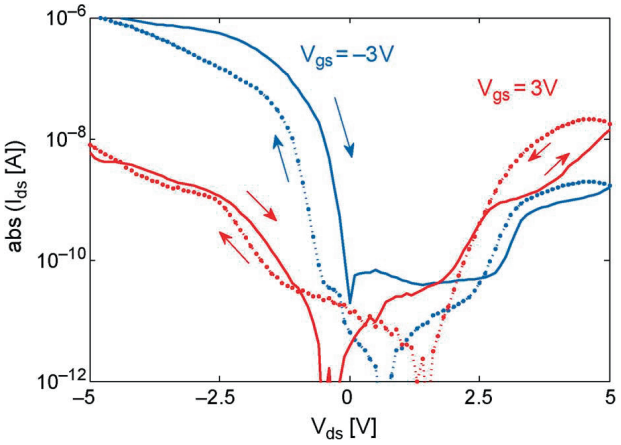


Fig. 18. ***Controlled memristance for fixed top and back gate voltages $V_{bf} = -5$ V.***

double conductance, for holes and electrons. As described in [44] for SB carbon-nanotube (CNT) FETS, the ambipolarity can be controlled by using an additional control gate, such that it blocks one type of carrier conductance. Following this principle, four-terminal memristive SB SiNW FETs can be built (see Fig. 17). In the following, two modes of operation are reported, depending on the nature of the controlling signal applied at the Si nanowire channel.

A. Voltage-Controlled Four-Terminal Memristive Device

A voltage-controlled four-terminal memristive Schottky barrier SiNW FET is obtained by using a dual-gate configuration such that one of the two gates is controlling a portion of the channel that is between the source/drain contacts and the main gate. This configuration is exploited to control the ambipolarity imbalance, such as for CNT FETs [44]. Since the back-gate voltage

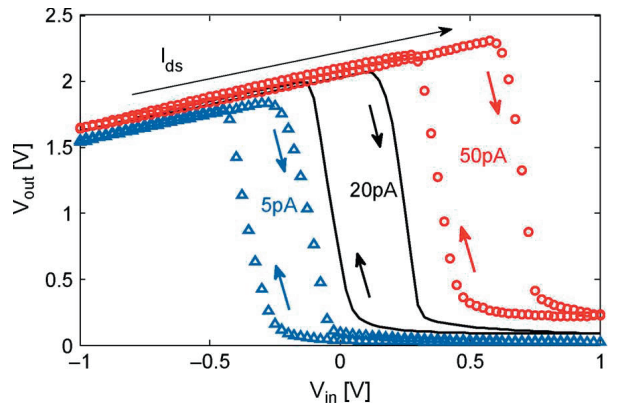


Fig. 19. ***Current-controlled memristive Schottky barrier SiNW FET hysteresis loop.***

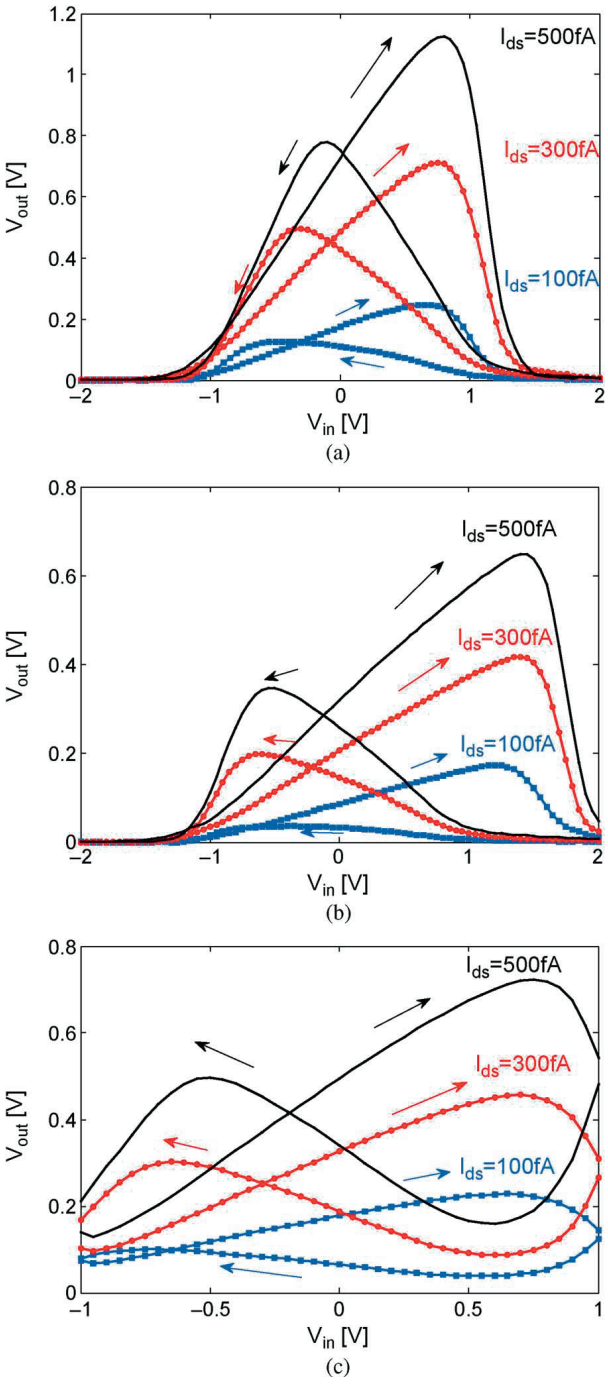


Fig. 20. ***V_{out} voltages for increasing with I_{ds} current bias. In all the figures I_{ds} bias values are 100, 300, and 500 fA. Notice the output voltage hysteresis narrows for increasing frequency sweep: (a) 24 s; (b) 6 s; and (c) 0.5 s.***

modifies the ambipolar conductance, this fact can be used in ambipolar memristive devices to limit the current levels for one of the carriers. A fixed back-gate voltage $V_{bg} = 0$ V leads to imbalanced bistable hysteresis loops under different V_{gs} voltages. By applying a negative $V_{bg} = -5$ V this imbalance is toggled for the negative side of the characteristics, giving a complementary effect (Fig. 18).

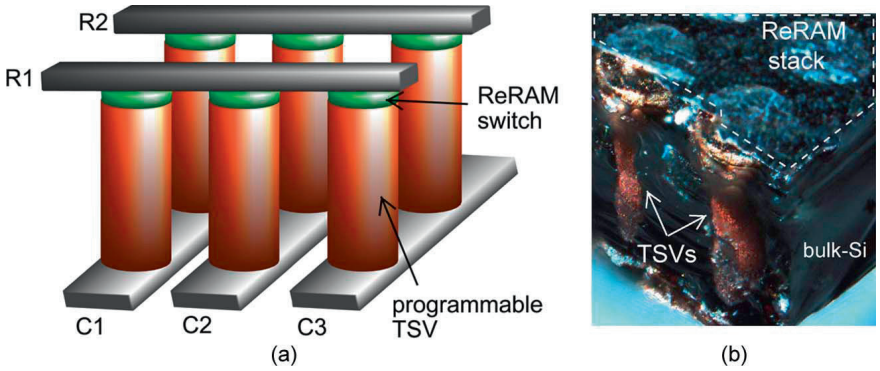


Fig. 21. *(a) A crossbar architecture with programmable TSVs made of ReRAM stacks [21]. (b) Reconstructed 3-D photograph of the TSV-ReRAM stack. The die is cleaved in order to reveal the TSV and the ReRAM layer deposited on top.*

Finally, a $V_{\rm bg} = +5$ V levels off the conductances of electrons and holes, giving a pretty symmetric hysteresis.

B. Current-Controlled Four-Terminal Memristive Devices

A current-controlled version of the four-terminal memristive Schottky barrier SiNW FET is obtained by using a current I_{ds} bias instead of a V_{ds}. The output voltage is then compared with V_{gs} (Fig. 19). The obtained hysteresis can be used as a latch device, whose position in the $V_{\rm out} - V_{\rm in}$ plane can be adjusted by using a different value of the current bias. A similar behavior has been exploited with three-terminal Schottky-barrier polysilicon nanowire FETs circuits to build a new logic family based on precharge and evaluation scheme [45]. Moreover, a similar scheme has been demonstrated for DRAM type of memory [46] and for pA current and temperature detection [47]. Similarly, SB Si nanowire transistors fabricated with a low thermal budget process and biased in current-controlled mode shows a similar hysteresis. Moreover, polycrystalline SiNWs SB FETs can give a hysteretic transfer characteristic (Fig. 20) very similar to the one reported for crystilline SiNW SB FETs fabricated with a low thermal budget process [39]. As is shown in Fig. 20, the maximum output voltage in the transfer characteristics increases with the $I_{\rm ds}$ bias current. From Fig. 20(a)–(c), the sweep time is reduced. Similarly to what was discussed for the three-terminal SB SiNW FET memristive device, the sweeping time impacts on the amount of charge that traps at the gate oxide/channel interface, thus influencing the conductance state of the nanowire channel. A faster sweeping time outbalances the charge trapping/detrapping mechanism, resulting in lower output voltages [see Fig. 20(a) and (b) compared with Fig. 20(c)].

VI. APPLICATIONS

Very different applications belonging to signal processing, memory, and sensing are envisaged for multiterminal memristive devices. The possibility to build very dense crossbar arrays of two-terminal memristive devices is often seen as a disruptive technology for ultradense ReRAM or write at once (WORM) nonvolatile memory storage [48]. In this concern, all the nonvolatile two-terminal memristive technologies are suitable candidates to replace flash memory in the future, given their higher density storage per cost. This feature is especially interesting because it can be utilized to stack nonvolatile memory elements in the back-end-of-the-line, increasing both density and access speed among logic and memory layers. Good examples are the recently proposed hybrid semiconductor/nanowire/molecular (CMOL) integrated circuits [49], as well as 3-D field-programmable gate array (FPGA) architectures with programmable through silicon vias (TSVs) [21] (see Fig. 21). The two-terminal memristive crossbars can also be integrated into programmable logic array architectures to compute Boolean logic functions. The memristive crossbar architecture can be exploited to reprogram itself. For instance, in [50], a very dense nanowire crossbar with TiO_2 memristive junctions was used to perform logic functions and to store the result into another portion of the same crossbar. Moreover, memristive switches can be used to perform material implication function[1] and exploited to build latches that use resistance in place of voltage or charges as physical state variable [6]. Another application that can exploit the memristive functionality is related to the design of cellular neural networks [8]. The Hodgkin–Huxley model for the synapse was one of the earlier examples reported by Chua and Kang [5] of systems that can be modeled with the memristor. Recently, the use of two-terminal memristive devices in combination with digital-to-analog converters demonstrated a way of reproducing the associative memory of animals [51]. The modification of the memristive characteristic to environmental condition can also be utilized for different types of

[1]Here for material implication it is meant a fundamental Boolean logic operation on two variables "p" and "q" such that pIMPq is equivalent to (NOTp)ORq.

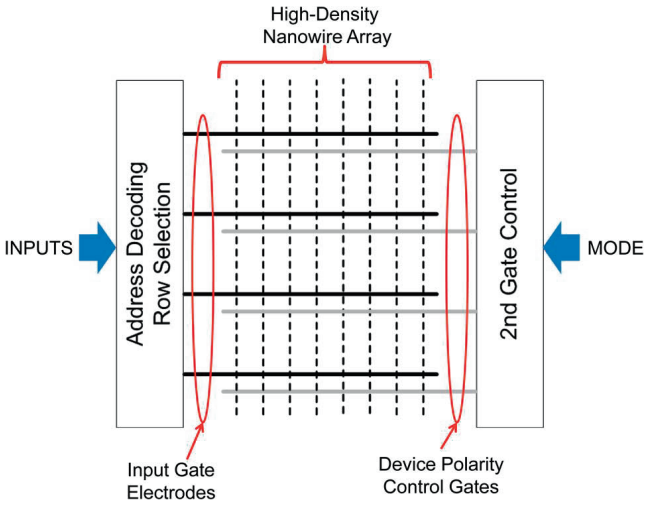


Fig. 22. ***A crossbar architecture with polarity control and address decoding made with high-density four-terminal memristive SiNW arrays.***

sensing. For instance, functionalization of nanowires with redox active molecules give rise to the typical memristive pinched hysteresis loop [52]. Another example can be the sensing of temperature with spintronic memristor [53]. The temperature change can cause a variation of the domain-wall mobility that in turn is sensed thanks to a positive feedback loop electronics. This type of sensor has been reported to be very compact ($\leq 1\ \mu m^2$ cell size) and to operate with very low power.

Multiterminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [32] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for biomolecule detection in dry environment [30]. More specifically, in [30], the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authors [47]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [45]. For instance, in [45], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR, and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing a hysteretical negative differential resistance [46]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel. In Section IV, it is shown that a similar hysteresis can also be obtained independently on the phase state of the Si nanowire channel. Similarly, the same structure can exploit the functionality of an additional gate to tune the polarity of an SB SiNW FET, thus giving even more functionality (Section IV). A very high expressive power architecture can be made of four-terminal memristive devices arranged in a crossbar implementation that exploits the high density of the SiNW arrays (Fig. 22).

VII. CONCLUSION

A general overview on multiterminal memristive devices is reported. The functionality of the devices can be used for logic, memory and sensing applications. Ultradense memristive ReRAMs crossbar arrays can be used for ultradense nonvolatile memory storage. It was shown that three- and four-terminal memristive devices can be used for both logic and memory applications. In particular, Schottky-barrier silicon nanowire FETs are very interesting devices due to their CMOS compatibility and ease of fabrication. Disruptive applications exploiting the high expressive power of four-terminal memristive devices arranged in crossbar arrays are foreseen as a significant advance in the electronic computation. ■

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Davide Sacchetto received the B.S. degree in physics engineering from Politecnico di Torino, Torino, Italy, in 2007 and the jointed M.S. degree in micro and nano technologies for integrated systems from École Polytechnique Fédérale de Lausanne (EPFL), the Institut National Polytechnique de Grenoble, and the Politecnico di Torino, in 2008. Currently, he is working towards the Ph.D. degree at the Microelectronic System Laboratory (LSM) and the Integrated System Laboratory (LSI), EPFL.

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Giovanni De Micheli (Fellow, IEEE) is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He is program leader of the Nano-Tera.ch program. Previously, he was Professor of Electrical Engineering at Stanford University. He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), a M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983).

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Prof. De Micheli is the recipient of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He received also the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000, the D. Pederson Award for the best paper on the IEEE Transactions on CAD/ICAS in 1987, and several Best Paper Awards, including DAC (1983 and 1993), DATE (2005) and Nanoarch (2010).

He has been serving IEEE in several capacities, namely: Division 1 Director (2008-9), co-founder and President Elect of the IEEE Council on EDA (2005–2007), President of the IEEE CAS Society (2003), Editor in Chief of the IEEE Transactions on CAD/ICAS (1987–2001). He has been Chair of several conferences, including DATE (2010), pHealth (2006), VLSI SOC (2006), DAC (2000) and ICCD (1989). He is a founding member of the ALaRI institute at Universita' della Svizzera Italiana (USI), in Lugano, Switzerland, where he is currently scientific counselor.



Yusuf Leblebici (Fellow, IEEE) received his B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, in 1984 and in 1986, respectively, and his Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1990.

Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000–2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, Dr. Leblebici has been a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the coauthor of 6 textbooks, namely, *Hot-Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers, 1993), *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications* (Springer, 2007), *Fundamentals of High Frequency CMOS Analog Integrated Circuits* (Cambridge University Press, 2009), *Extreme Low-Power Mixed Signal IC Design* (Springer, 2010) and *Reliability of Nanoscale Circuits and Systems* (Springer, 2011), as well as more than 250 articles published in various journals and conferences.

He has served as an Associate Editor of IEEE Transactions on Circuits and Systems (II), and IEEE Transactions on Very Large Scale Integrated (VLSI) Systems. He has also served as the general co-chair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference (ESSCIRC/ESSDERC). He is a Fellow of IEEE and has been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.

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PROFILE

Pro-Active R&D engineer with strong motivation in seeking novel nanotechnology solutions for cutting-edge products. Profound knowledge in clean room technologies and device prototyping in a team or independent work. Expertise in lithography, dry etching and thin-films deposition. Design of experiments for the development of semiconductor device technology and process optimization. Very good presentation skills sharpened through experience at international conferences.

Process optimization, design of experiment, lithography, etching, thin-films, teamwork, communication

WORK EXPERIENCE

Research Assistant (2008-2013)
EPFL, Switzerland

- Involved in at least 4 successful project definition and proposals writing for research funding
- Experience with micro- and nano- fabrication tools within a class 100 clean room environment
- Research project planning and team management
- Design, Fabrication and Characterization of ambipolar Vertically-stacked Si nanowire platform
- Demonstration of novel bio-sensing method exploiting memory effects in ambipolar Si nanowires
- Fabrication and characterization of novel resistive RAM concepts for standalone memories and for FPGA applications
- Lecturer and assistant in technical projects for classes of 60+ M.Sc. students
- Advisor of 3 M.Sc. projects involving successful fabrication of Si nanowire resonators and bio-sensors.
- Author of more than 25 scientific publications in international conferences and journals

Exceptional Performance Award of the faculty of engineering at EPFL, 2010
Best Paper Award at Nanoarch 2012

EDUCATION

Doctor of philosophy (PhD) of sciences in Micro-Systems and Micro-Technologies
2008- 2013 (expected)
Thesis title: Multi-Terminal Am-Bipolar Memristive Devices for Emerging Logic and Memory Architectures
Advisors: Prof. Yusuf Leblebici and Prof. Giovanni De Micheli

Master in Micro and Nanotechnologies for the ITCs (2006-2008)
EPFL-Switzerland, INP Grenoble-France, Politecnico di Torino-Italy
Dissertation: Fabrication and Characterization of Vertically-Stacked Si nanowire transistors

Master Project (2008, 6months)
EPFL, Switzerland

- Definition of a top-down fabrication flow for vertically-stacked Si nanowire N-FETs
- Design of photolithographic masks with Cadence Virtuoso
- Fabrication and Characterization of vertically-stacked Si nanowire N-FETs

Summer Internship (2007, 3months)
X-Lab, Chivasso, Italy

- Development of a polymeric Lab-On-a-Chip
- Hot Embossing of PC, PMMA, COC and realization of microfluidics with PDMS bonding and interconnects

Bachelor in Physics Engineering (2003-2007)
Politecnico di Torino – Italy
Dissertation: Nuclear physics in fission reactors and technological considerations

Authored publications

[1] D. Sacchetto, P.-E. Gaillardon, M. Zervas, S. Carrara, G. De Micheli, and Y. Leblebici, "Applications of Multiterminal Memristive Nanowire Devices for Logic and Memory: A Review," accepted for publication in *Circuits and Systems Magazine*, 2013

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[5] D. Sacchetto, S. Xie, V. Savu, M. Zervas, G. De Micheli, J. Brugger, and Y. Leblebici, "Vertically-Stacked Gate-All-Around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography," *Microelectronic Engineering*, vol. 98, pp. 355–358, 2012.

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[9] D. Sacchetto, M. De Marchi, G. De Micheli, and Y. Leblebici, "Alternative Design Methodologies for the Next Generation Logic Switch (Invited)," in *Computer-Aided Design (ICCAD), 2011 IEEE/ACM International Conference on*. IEEE, 2011, pp. 231–234.

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Co-authored publications

[1] P.-E. Gaillardon, L. G. Amarù, S. K. Bobba, M. De Marchi, D. Sacchetto, and G. De Micheli, "Nanosystems: Technology and Design (invited paper)," *Philosophical Transactions of the Royal Society of London. A*, 2013.

[2] P.-E. Gaillardon, S. Bobba, L. Amàru, M. De Marchi, D. Sacchetto, Y. Leblebici, and G. De Micheli, "Vertically Stacked Double Gate Nanowires FETs with Controllable Polarity: From Devices to Regular ASICs," in *Proceedings of the Design, Automation & Test in Europe Conference (DATE 2013)*, 2013.

[3] P.-E. Gaillardon, D. Sacchetto, G. B. Beneventi, M. H. Ben Jamaa, L. Perniola, F. Clermidy, I. O'Connor, and G. De Micheli, "Design and architectural assessment of 3-d resistive memory technologies in fpgas," *IEEE Transactions on Nanotechnology*, vol. 12, pp. 40–50, Jan. 2013.

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