Ambipolar Logic Circuit Design and Synthesis

I. O'Connor, K. Jabeur, S. Le Beux, D. Navarro

Lyon Institute of Nanotechnology
Ecole Centrale de Lyon, France

ian.oconnor@ec-lyon.fr

Ambipolar nanofabrics

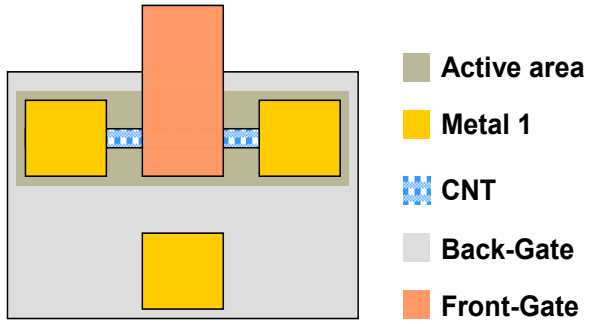
- At nanoscale, only regular fabrics are viable for systematic variability (e.g. OPC) and for self-assembly
- Still random variability – need device-level tuning and system-level reconfigurability
- Multi-gate devices can offer this level of flexibility
- Ambipolar double gate devices in regular nanofabrics could offer a means to solve many problems at the same time
- This work: based on CNT fabric
- Techniques also applicable to SiNW, GNR …

Nanograin architecture

- Layer of aligned semiconducting CNTs
- CMOS-type interconnect layers
- Fine-grain reconfigurable cells
- Fixed intra-matrix interconnect
- Reconfigurable inter-matrix interconnect

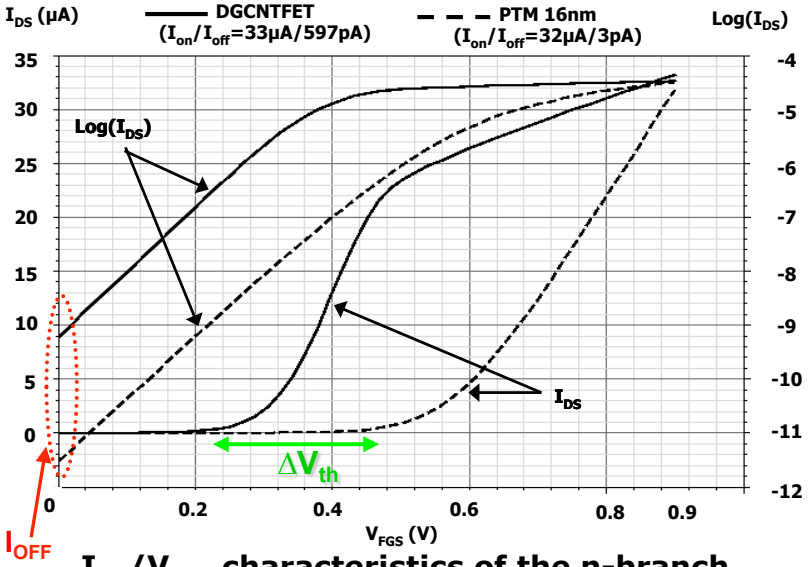
Device and model data

M. H. Ben Jamaa et al, ECS Transactions, 34 (1) 1005-1010 (2011)

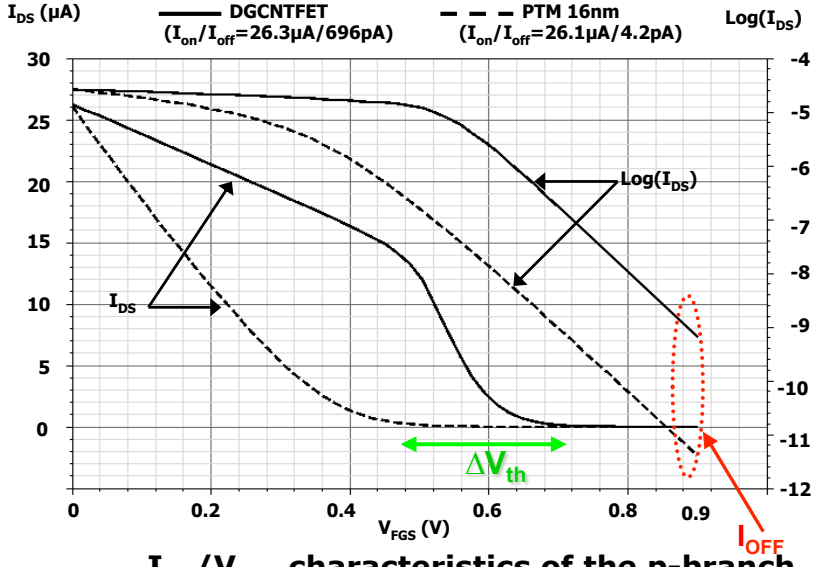


DG-CNTFET: top view

Parameters	DG CNFET	PTM 16nm LP
Drain access channel length	50nm	0
Source access channel length	50nm	0
Inner channel	20nm	16nm
Width	50nm	56nm(n-type)/80nm(p-type)
Chirality (n,m)	(11, 0)	-
Nb of nanotubes	12	-
Diameter of 1 nanotube	0.86nm	-
Supply voltage	0.9 V	0.9 V



I_{DS}/V_{FGS} characteristics of the n-branch (V_{BG}-V_S = +V = +0.9V)



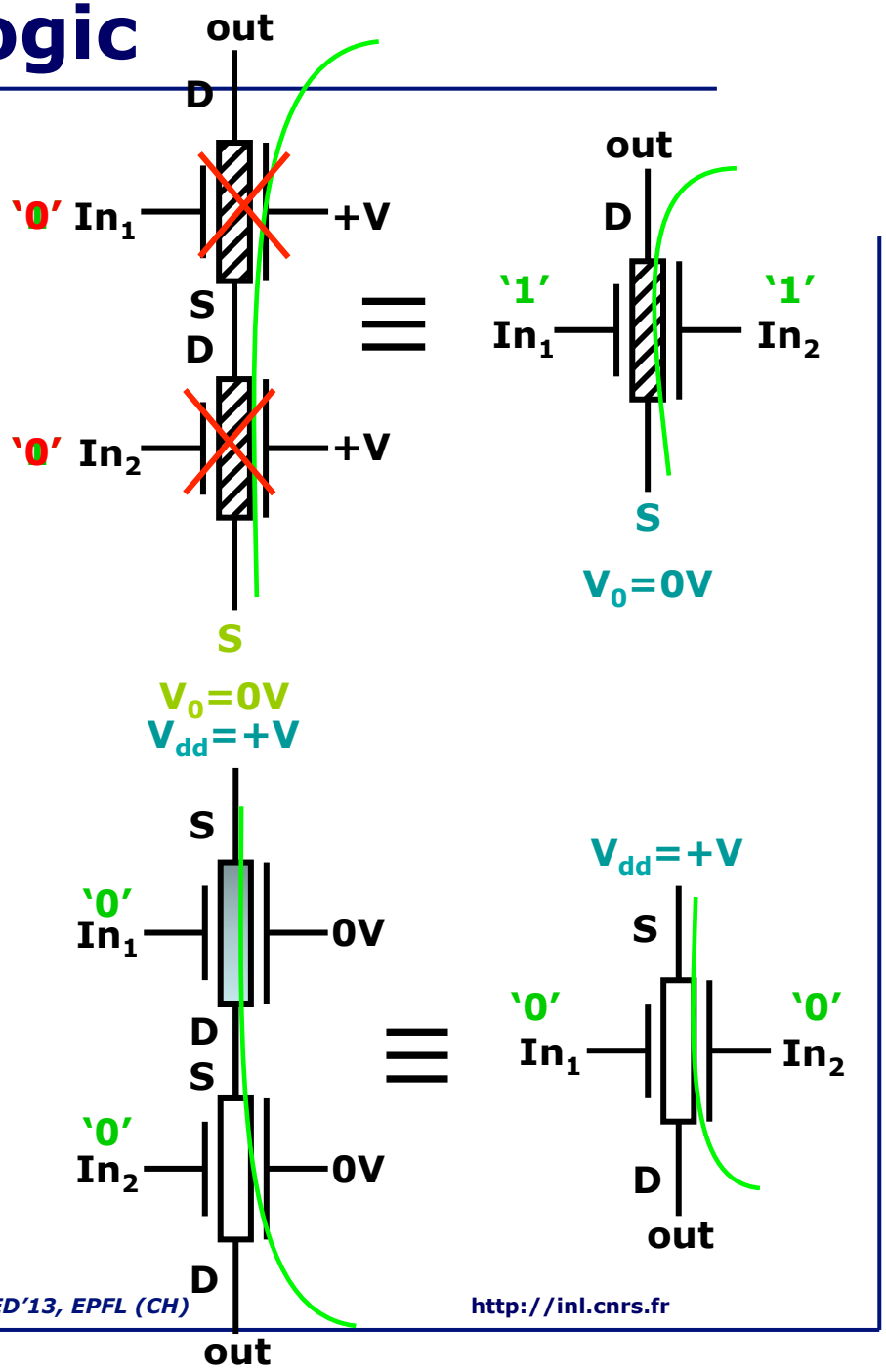
I_{DS}/V_{FGS} characteristics of the p-branch (V_{BG}-V_S = -V = -0.9V)

Agenda

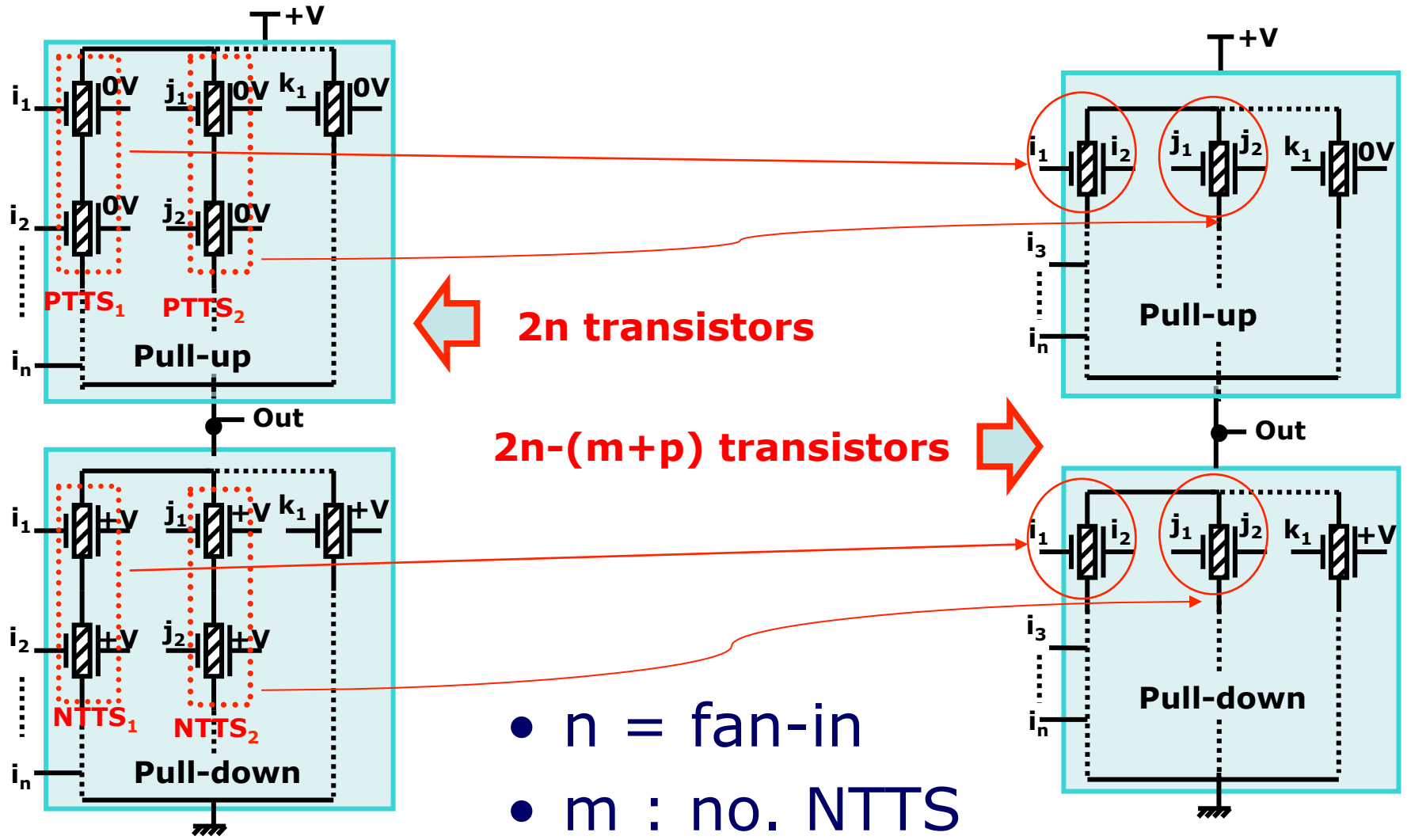
- Compact ambipolar logic
  - TTS structure primitive
  - Double-Gate static logic: principle and evaluation
  - Double-Gate dynamic logic: principle and evaluation
- Reconfigurable logic gates
  - Am-ICDGFET transmission gate primitive
  - x-function logic cell synthesis methodology
  - Performance comparison
- Conclusion

Compact ambipolar logic

- Basic idea: use Am-ICDGFET device to replace two transistors in series (TTS) structures
- critical for path resistance and gate capacitance optimization, with consequent impact on delay, power and area



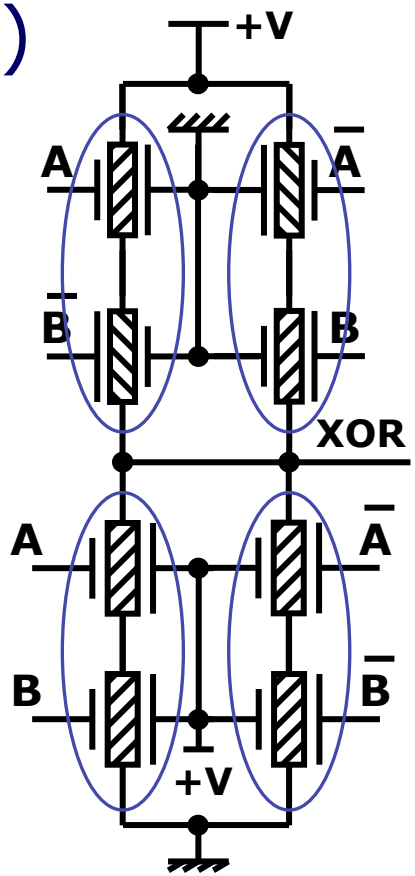
Static Logic structures

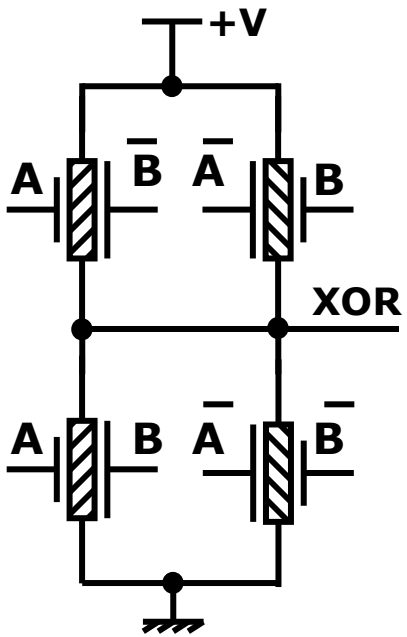


- n = fan-in
- m : no. NTTS
- P : no. PTTS

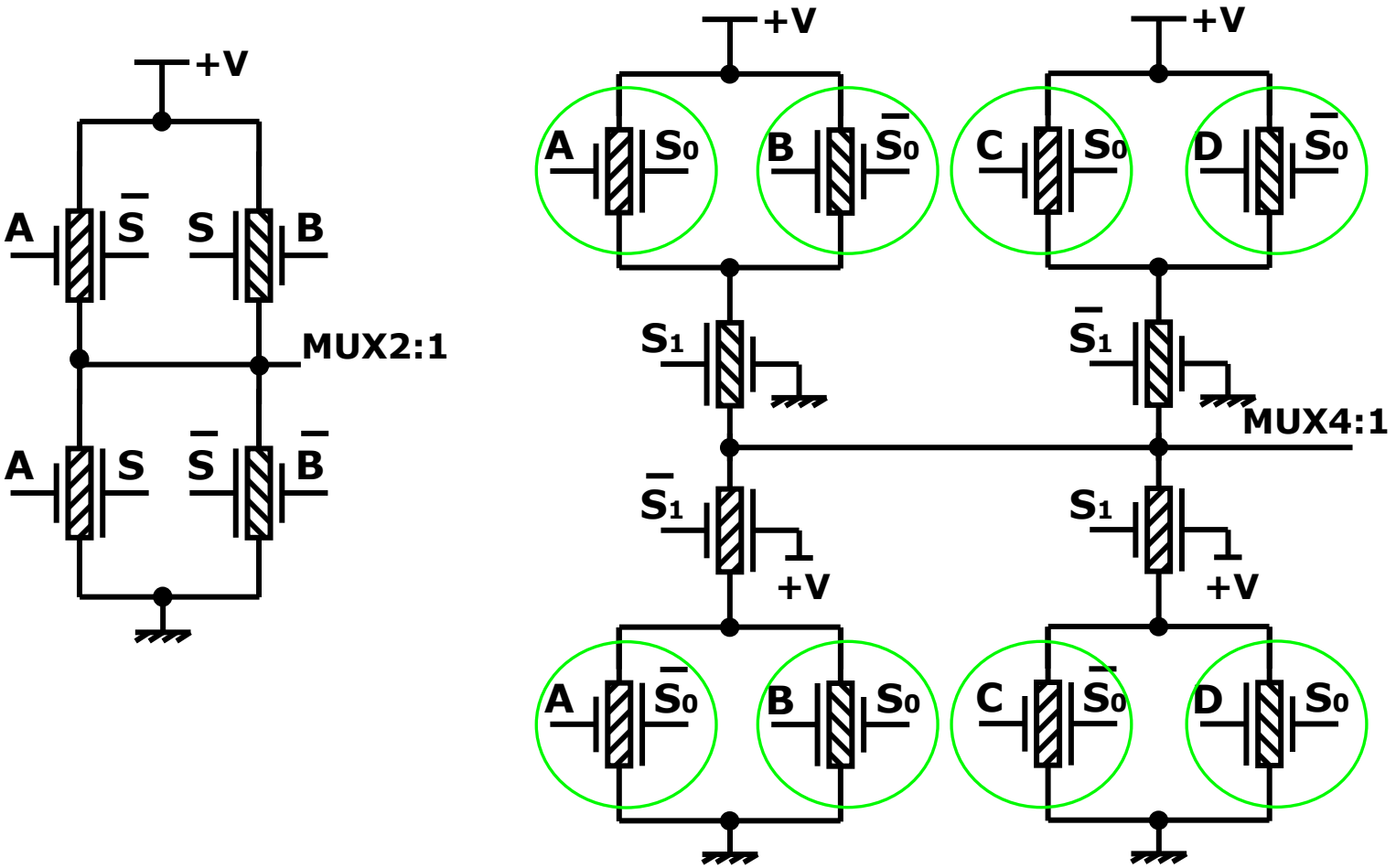
Example: XOR

- Applicable to any complementary static logic gate containing TTS structures
- efficient with complex gates (XOR/XNOR, MUXs…)

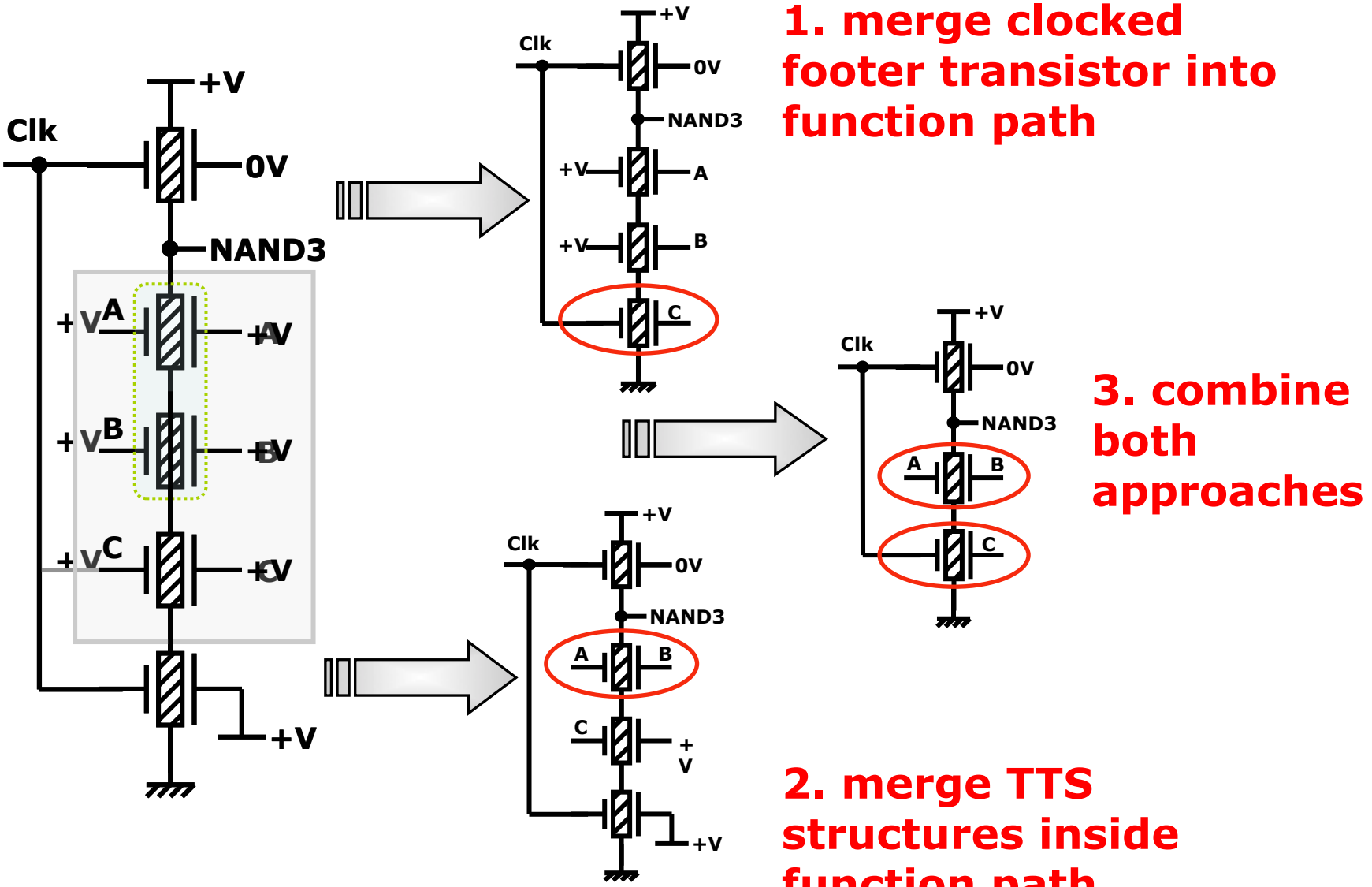




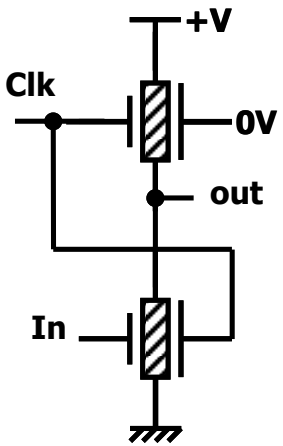
Example: 2:1 and 4:1 MUX



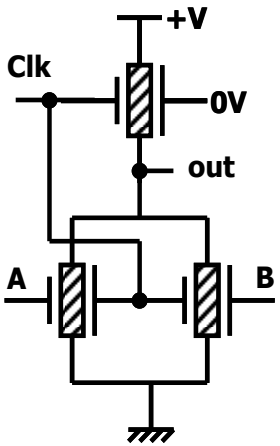
Dynamic Logic structures: 3 approaches



Examples



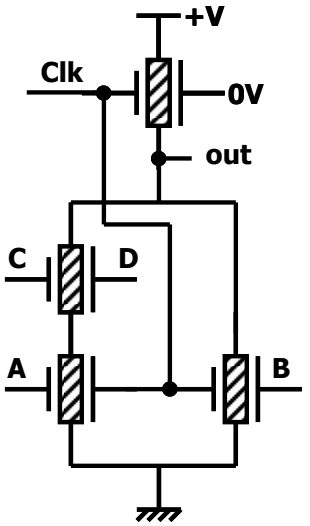
INV



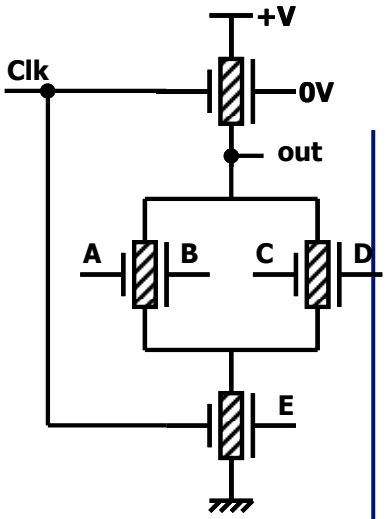
NOR 2

1.

n+1 transistors



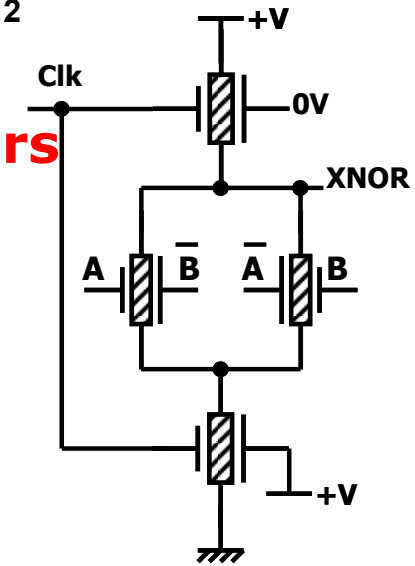
¬ ((A∧ C∧D)∨B)



¬ ((A ∧B)∨(C∧D))∧E

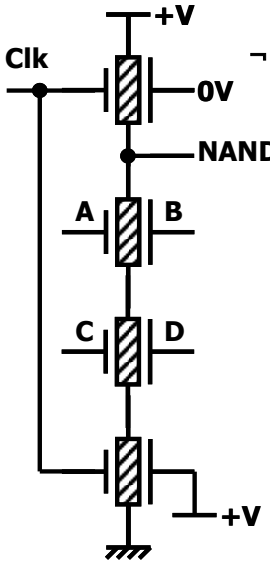
3.

n+1-m transistors



XOR 2

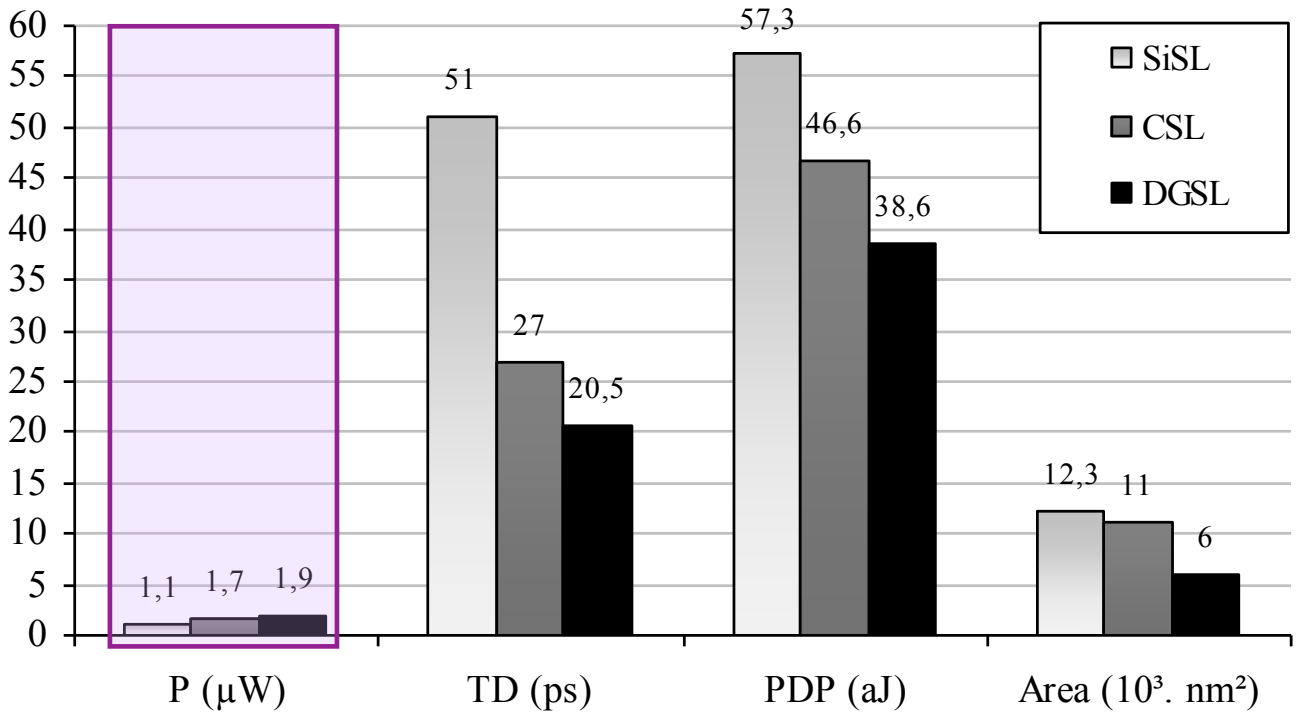
2.



NAND 4

n+2-m transistors

Performance Comparison



f_{clk}=1GHz

t_r=t_f=20ps

C_L=C_{inv4}

SiSL: 16nm conventional static logic

CSL: CNT conventional static logic

DGSL: CNT DG static logic

- **1.7X power consumption**
- **0.4X time delay**
- **0.7X PDP**
- **0.5X area**

Figures averaged over:

XOR

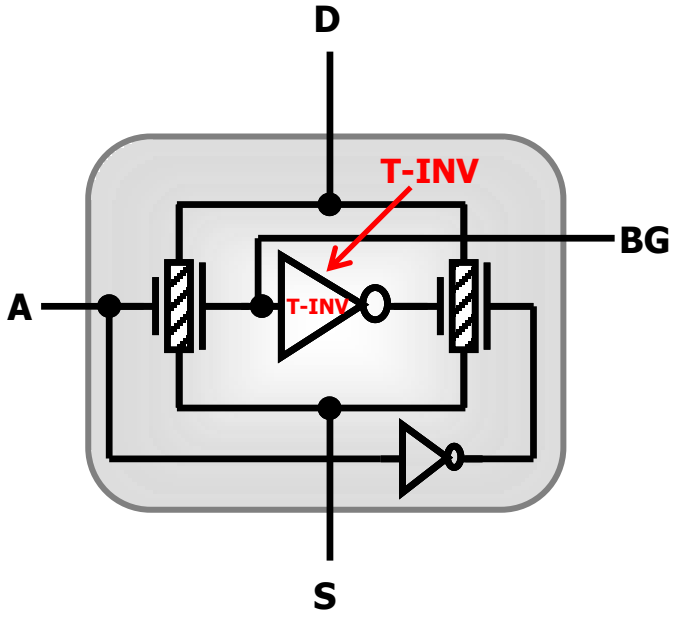
XNOR

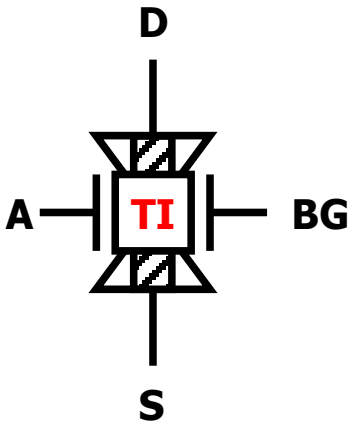
2:1 MUX

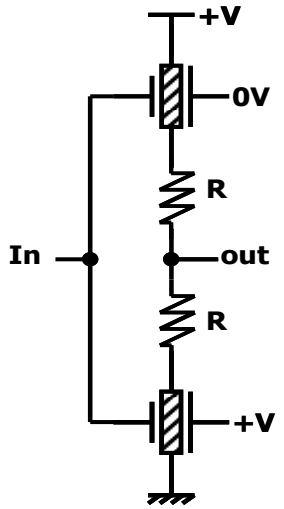
4:1 MUX

Reconfigurable logic gates

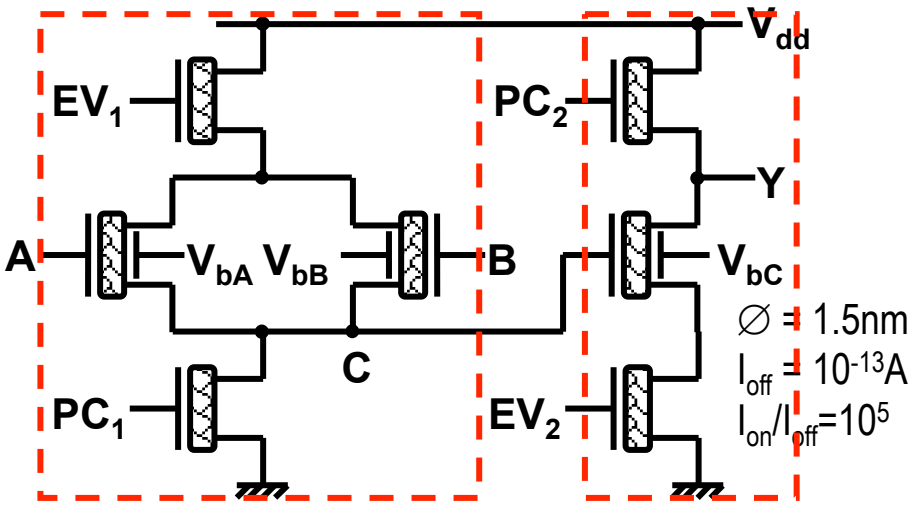
- Basic idea: configure switching properties of logic networks with back gate voltages
- Requires transmission gates to propagate logic levels with no degradation and for a wide range of data and control voltage combinations
- Also requires gate synthesis methodology for tunable functionality







Reconfigurable logic cell CNT-DR7T



- boolean data inputs A and B (logic level at V_{ss}=0V and V_{dd}=1V) + circuit output Y
- four-phase non-overlapping clock signals
  - two pre-charge inputs PC_1, PC_2
  - two evaluation inputs EV_1, EV_2
- control inputs V_{bgA}, V_{bgB}, V_{bgC} to configure circuit to 1 of 14 functions (back-gate bias -1V / p-type and +1V / n-type)

V_{bgA}	V_{bgB}	V_{bgC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	-V	A+B
+V	-V	+V	$\overline{A}$.B
+V	-V	-V	A+$\overline{B}$
-V	+V	+V	A.$\overline{B}$
-V	+V	-V	$\overline{A}$+B
-V	-V	+V	A.B
-V	-V	-V	$\overline{A.B}$
+V	0	+V	$\overline{A}$
+V	0	-V	A
0	+V	+V	$\overline{B}$
0	+V	-V	B
0	0	0	1
0	0	-V	0

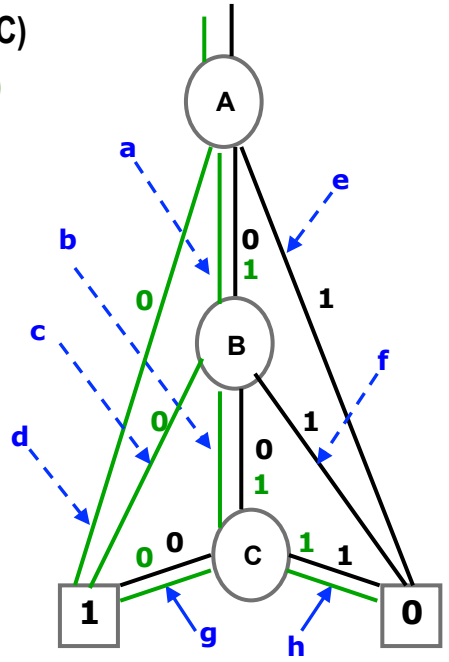
I. O'Connor et al., IEEE TCAS, 2007

Am-BDD design technique

1. Define output functions
2. Map their BDDs in a common Am-BDD
3. Label every edge connecting two different nodes
4. Trace the configuration table and identify correlations
5. Pass-transistor logic circuit implementation

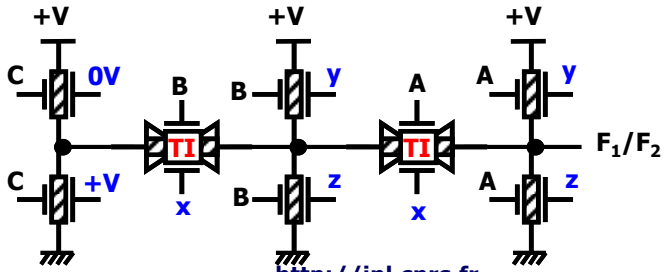
F1= ¬(A+B+C)

F2= ¬(A.B.C)

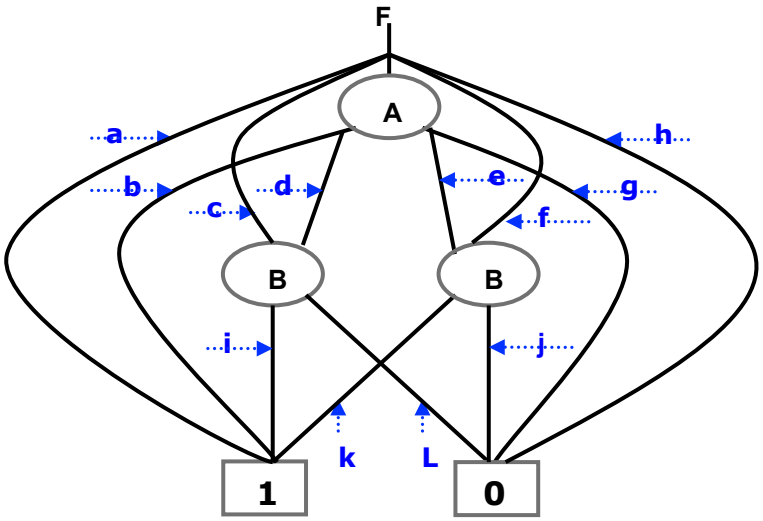


F	a	b	c	d	e	f
F_1=¬ (A+B+C)	0V	0V	V/2	V/2	+V	+V
F_2=¬ (A.B.C)	+V	+V	0V	0V	V/2	V/2

X Y Z



16-function (complete operator set)



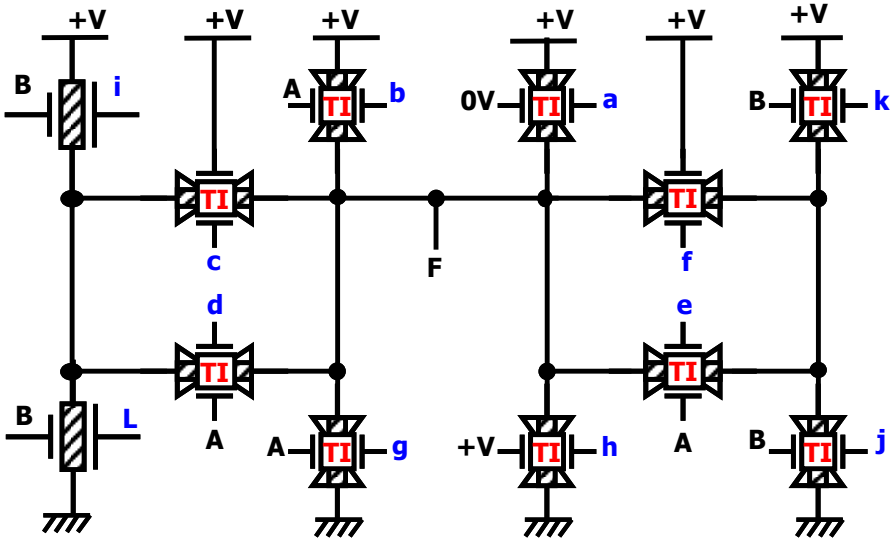


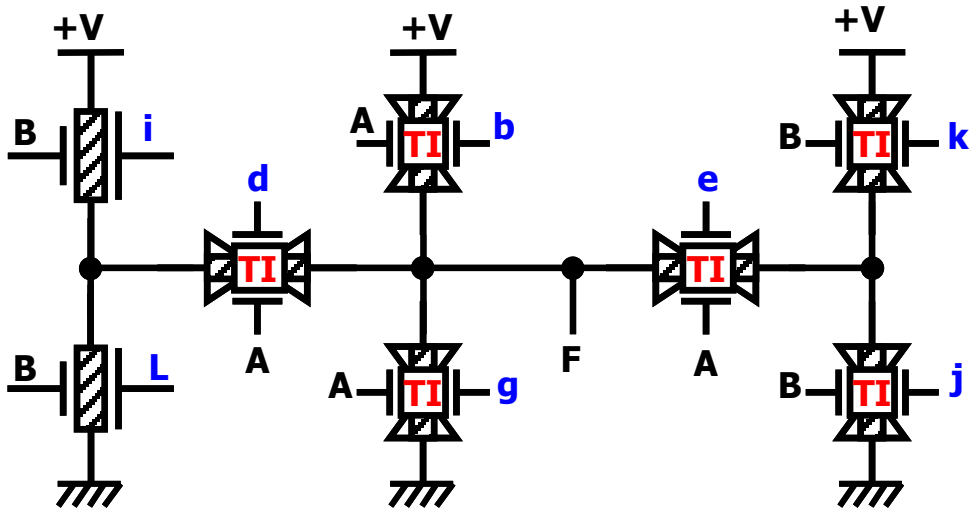
TABLE II. 16-FUNCTIONS CONFIGURATION TABLE

a	b	c	d	e	f	g	h	i	j	k	l	F
0	0	0	-V	0	0	+V	0	-V	0	0	+V	$\overline{A+B}$
0	+V	0	0	-V	0	0	0	0	-V	+V	0	$A+B$
0	-V	0	0	+V	0	0	0	0	-V	+V	0	$\overline{A}+B$
0	0	0	+V	0	0	-V	0	-V	0	0	+V	$A\bullet\overline{B}$
0	+V	0	-V	0	0	0	0	-V	0	0	+V	$A+\overline{B}$
0	0	0	0	-V	0	+V	0	0	-V	+V	0	$B\bullet\overline{A}$
-V	0	0	0	0	0	0	0	0	0	0	0	$\top$
0	0	0	0	0	0	0	+V	0	0	0	0	$\bot$
0	0	0	0	+V	0	-V	0	0	-V	+V	0	$A\bullet B$
0	-V	0	+V	0	0	0	0	-V	0	0	+V	$\overline{A\bullet B}$
0	+V	0	0	0	0	-V	0	0	0	0	0	A
0	-V	0	0	0	0	+V	0	0	0	0	0	$\overline{A}$
0	0	+V	0	0	0	0	0	-V	0	0	+V	$\overline{B}$
0	0	0	0	0	+V	0	0	0	-V	+V	0	B
0	0	0	-V	+V	0	0	0	-V	-V	+V	+V	$\overline{A\oplus B}$
0	0	0	+V	-V	0	0	0	-V	-V	+V	+V	$A\oplus B$

12 configuration signals!

12-function

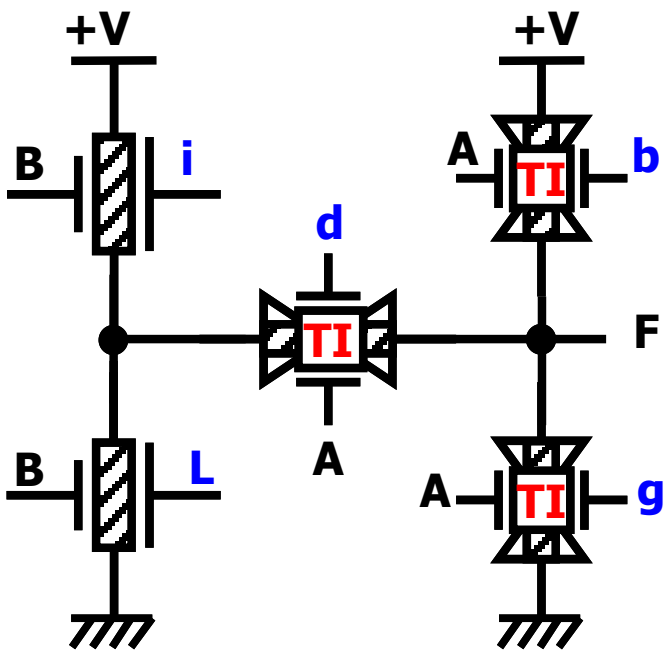
- Tune the functionality
- Remove T, ⊥, B, !B



b	d	e	g	i	j	k	l	F
V/2	0V	V/2	+V	0V	V/2	V/2	+V	$\overline{A+B}$
+V	V/2	0V	V/2	V/2	0V	+V	V/2	$A+B$
0V	V/2	+V	V/2	V/2	0V	+V	V/2	$\bar{A}+B$
V/2	+V	V/2	0V	0V	V/2	V/2	+V	$A\bullet\bar{B}$
+V	0V	V/2	V/2	0V	V/2	V/2	+V	$A+\bar{B}$
V/2	V/2	0V	+V	V/2	0V	+V	V/2	$B\bullet\bar{A}$
V/2	V/2	+V	0V	V/2	0V	+V	V/2	$A\bullet B$
0V	+V	V/2	V/2	0V	V/2	V/2	+V	$\overline{A\bullet B}$
+V	V/2	V/2	0V	V/2	V/2	V/2	V/2	A
0V	V/2	V/2	+V	V/2	V/2	V/2	V/2	$\bar{A}$
V/2	0V	+V	V/2	0V	0V	+V	+V	$\overline{A\oplus B}$
V/2	+V	0V	V/2	0V	0V	+V	+V	$A\oplus B$

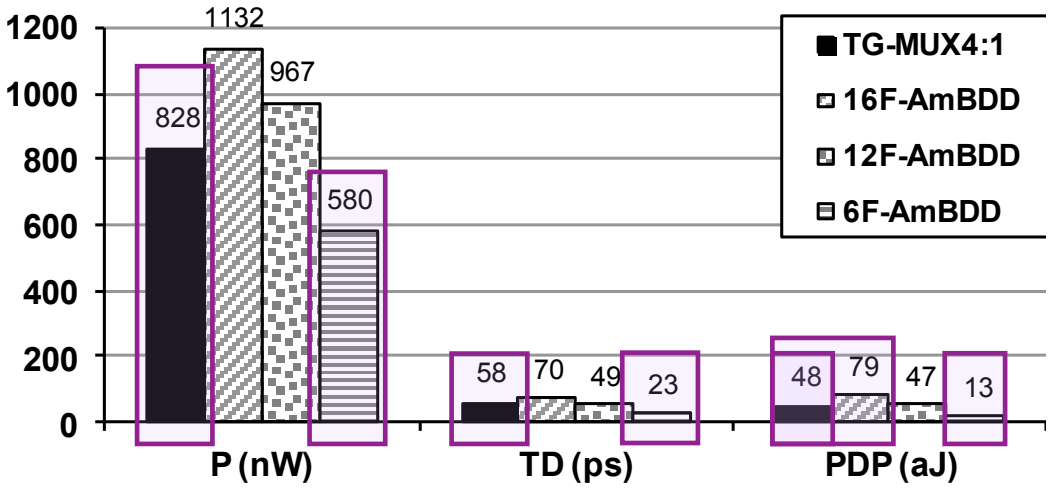
6-function

- Strip down to NAND, NOR, INV, BUF

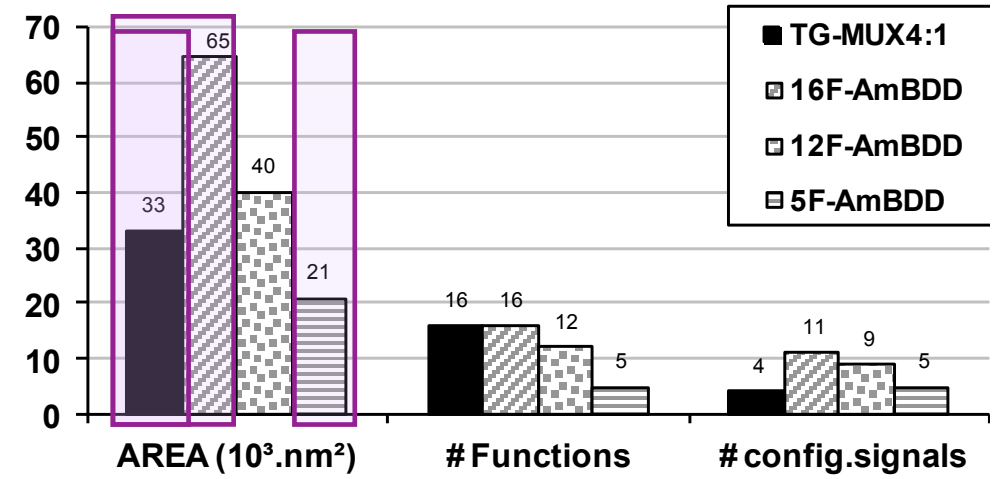


b	d	g	i	l	F
V/2	0V	+V	0V	+V	$\overline{A+B}$
V/2	+V	0V	0V	+V	$A \bullet \overline{B}$
+V	0V	V/2	0V	+V	$A+\overline{B}$
0V	+V	V/2	0V	+V	$\overline{A \bullet B}$
+V	V/2	0V	V/2	V/2	A
0V	V/2	+V	V/2	V/2	$\overline{A}$

Performance comparison



- 16F-AmBDD vs 2-LUT:
  - 1X functionality
  - 1.6X PDP
  - 2X area
  - 2.8X config



- 6F-AmBDD vs 2-LUT:
  - 0.4X functionality
  - 0.3X PDP
  - 0.6X area
  - 1.3x config

Conclusion and perspectives

- Compact logic gates:
  - Merge TTS structures in function path (+footer) using back gate
  - Fewer transistors : 2n-(m+p) or n+2-m
  - Improved time delay : low V_{TH}, low branch resistance
  - Increased power consumption : low V_{TH}
- Reconfigurable logic gates
  - Am-BDD logic synthesis method
  - Full 16F functionality has worse PDP and area
  - Better results achieved for basic 6F cell
- Towards synthesis flows for reduced functionality cells and static interconnect