Auto-Reconfiguration in Statically Interconnected CNTFET-based Cells

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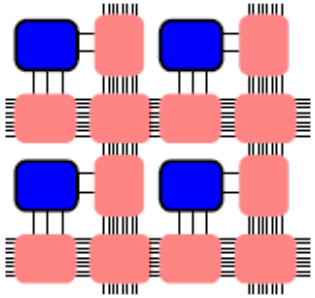
Design challenges and contribution

- Semiconductor industry design challenges:

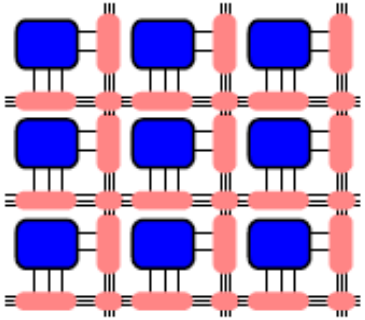
design reliability, manufacturing yield



more routing flexibility

Contradictory!

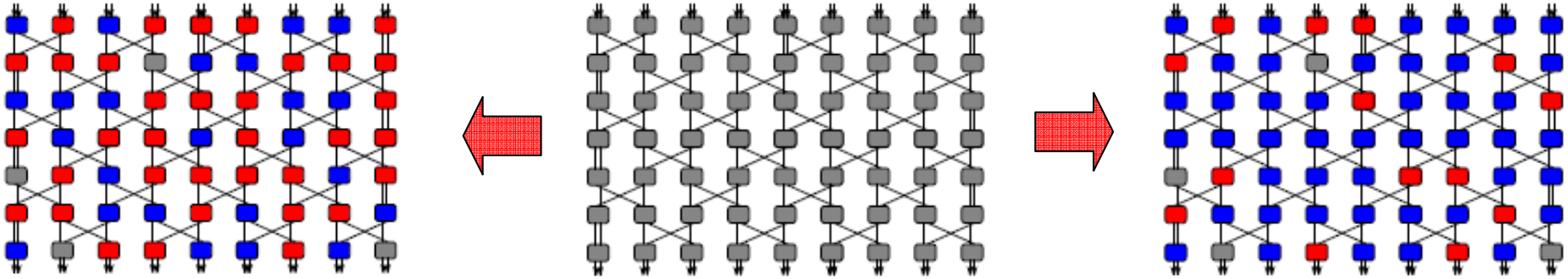
scalability and low power circuits



less routing resources

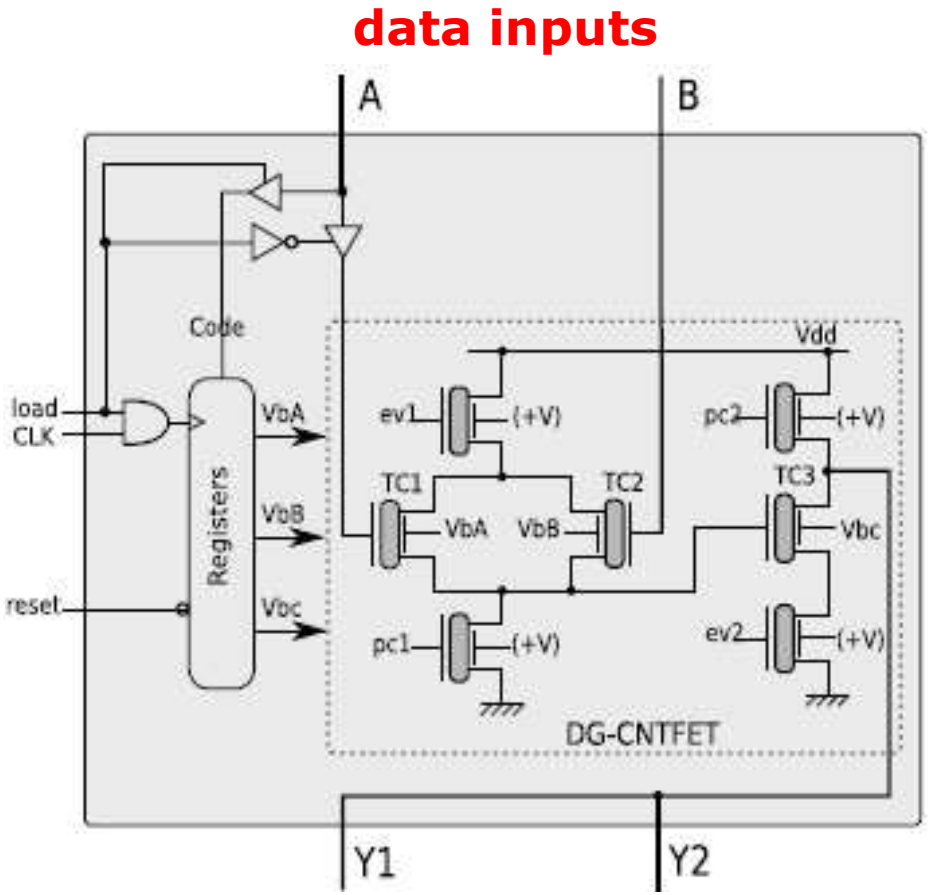
- Contribution : static interconnect-based fault tolerant architecture

cell: **computing** or **data routing**



Reconfigurable Cell

double gate based cell



Truth Table

VbgA	VbgB	VbgC	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	-V	$A+B$
+V	0	+V	$\overline{A}$
+V	0	-V	A
-V	-V	+V	$A \bullet B$
-V	-V	-V	$\overline{A \bullet B}$
+V	-V	+V	$\overline{A}B$
+V	-V	-V	$A+\overline{B}$
0	+V	+V	$\overline{B}$
0	+V	-V	B
0	0	0	1
0	0	-V	0
-V	+V	+V	$A\overline{B}$
-V	+V	-V	$B+\overline{A}$

Mapping methodology

- Free of faulty cells matrix
- Genetic algorithm used to optimize
  - Area
  - Power
  - Latency

- Example:

Truth table (application)

Ci	X2	X1	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

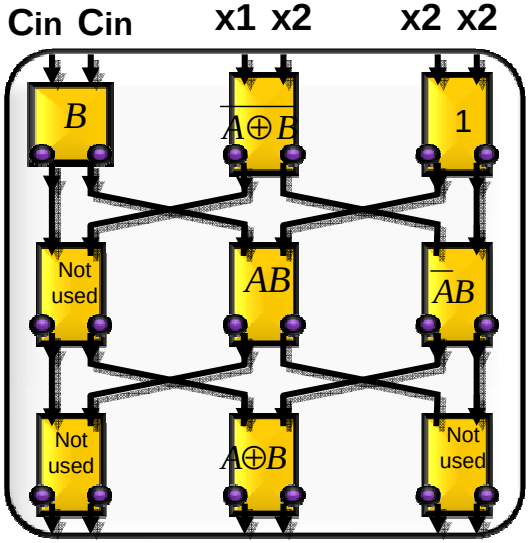
Individual (coding)

e.g. cell is off or on, internal function

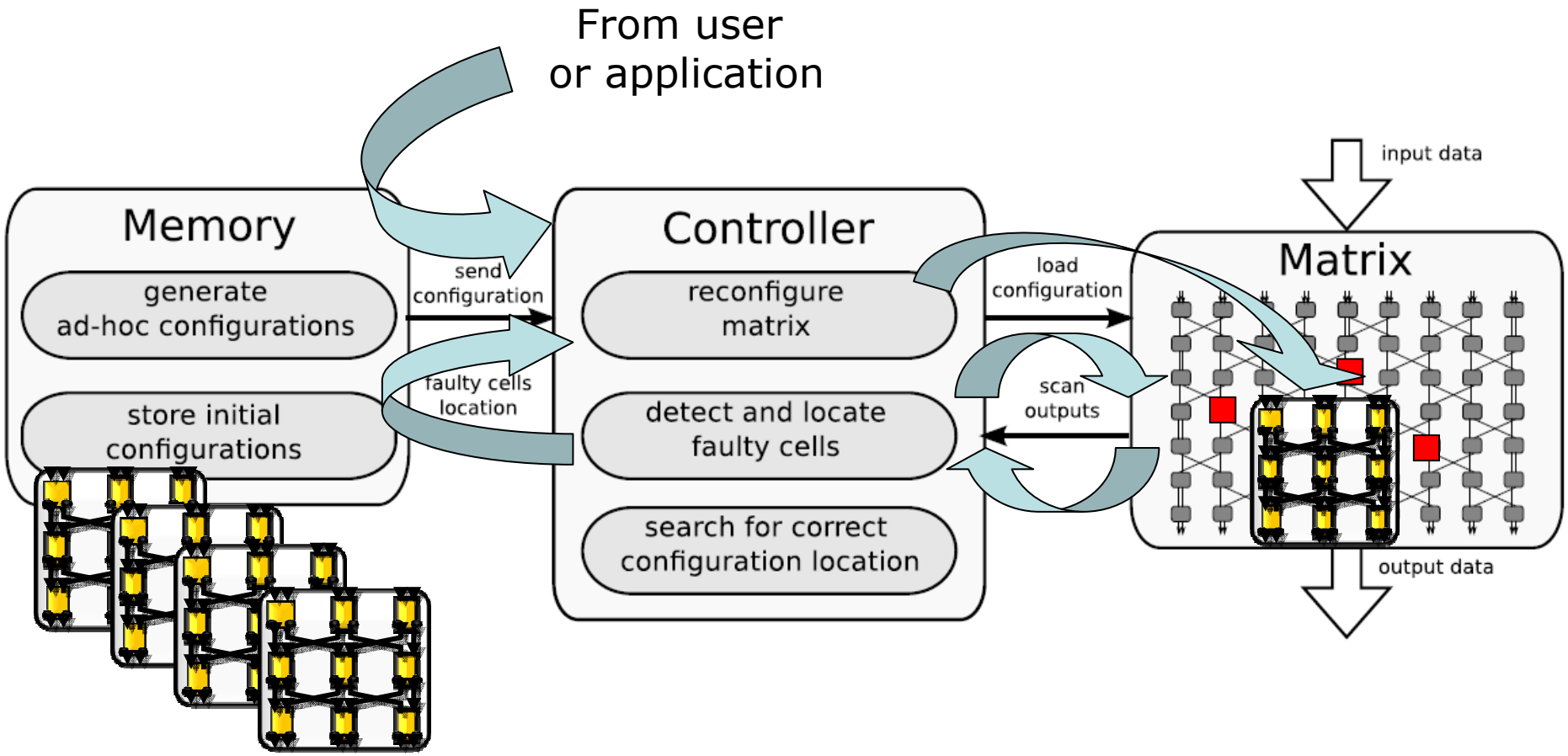
011…10 1…0 0…0 0…1

Gene 1 2 3 4

Matrix (resulting mapping)

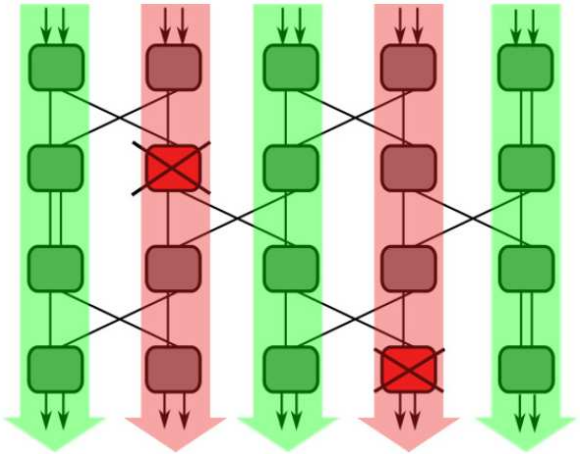


Proposed Architecture

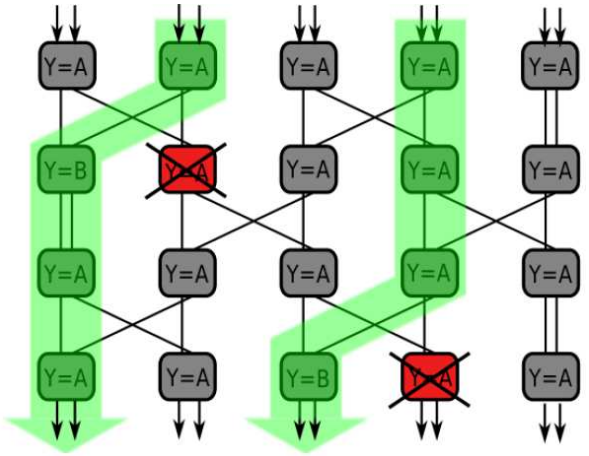


Controller features

- Faulty cells detection

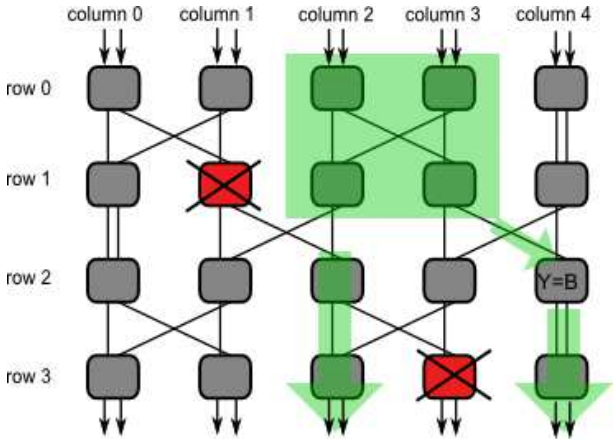


Column detection

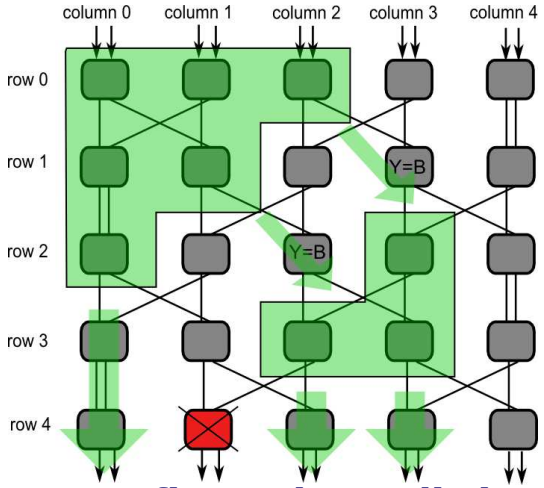


Raw detection

- Mapping correction:



configuration shifting

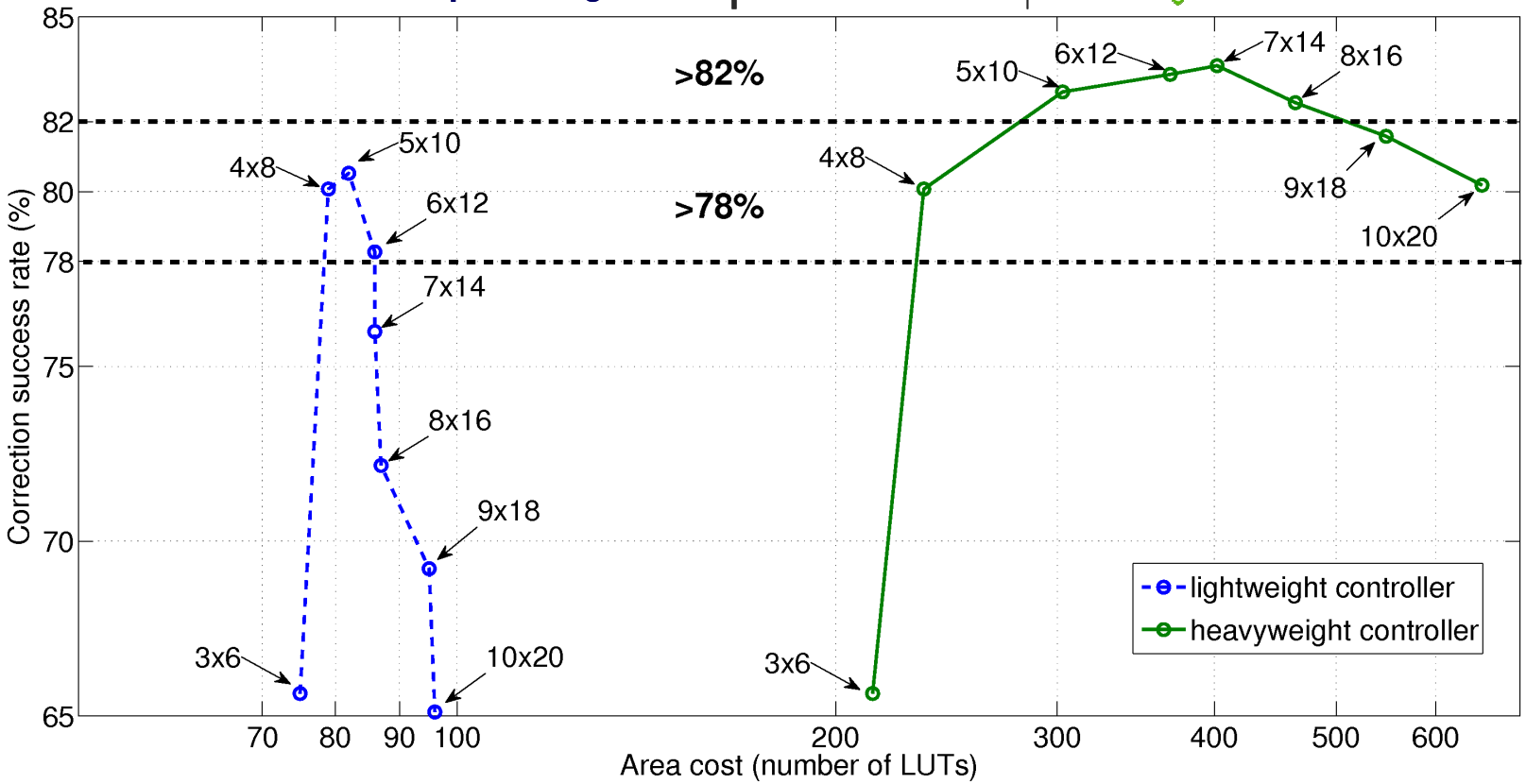


configuration splitting

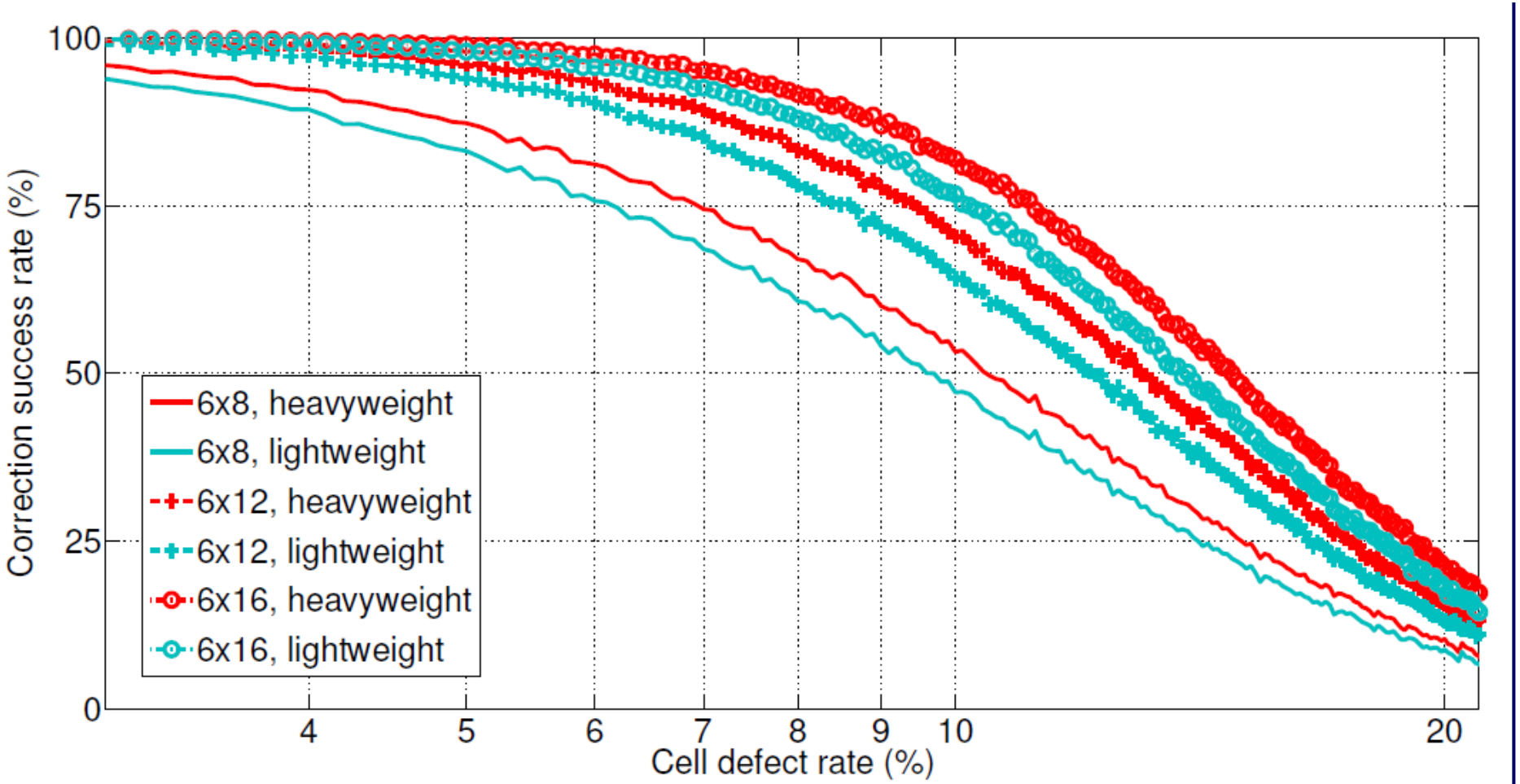
Controller design tradeoffs

- CNT manufacturing yield : 96%
- Two controllers:

Feature	Lightweight controller	Heavyweight controller
Column detection	✓	✓
Raw detection		✓
Shift configuration	✓	✓
Split configuration		✓



Correction success rate vs defect rate



Conclusion

- Statically interconnected cells
  - Potential for reliable and power efficient architectures
  - Multi-objective optimization
  - Heavyweight and lightweight controllers

- Future works
  - Distributed and hierarchical approaches
  - Focus on other technologies e.g. TFET, nanowires