Polarity control at Runtime in Double Gate, Gate-All-Around, Vertically Stacked Nanowire FETs

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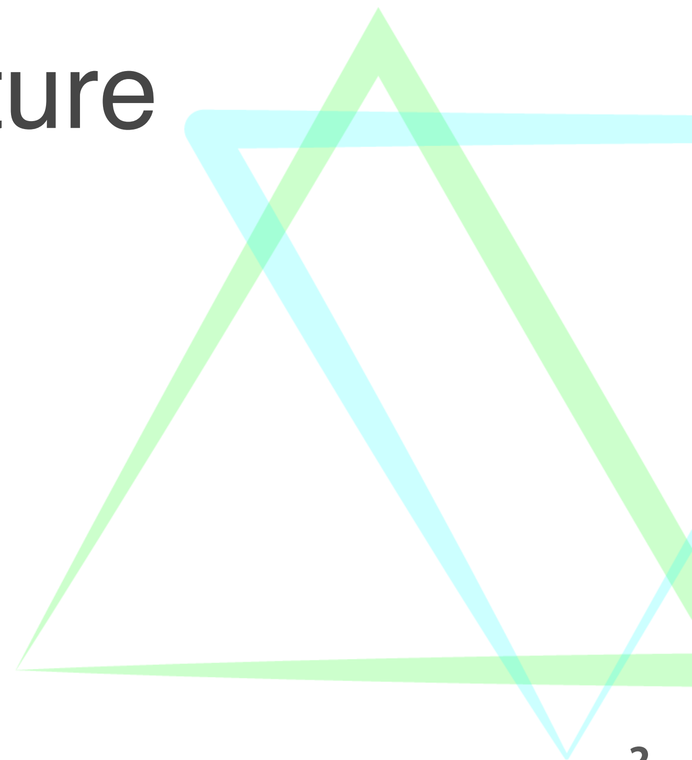
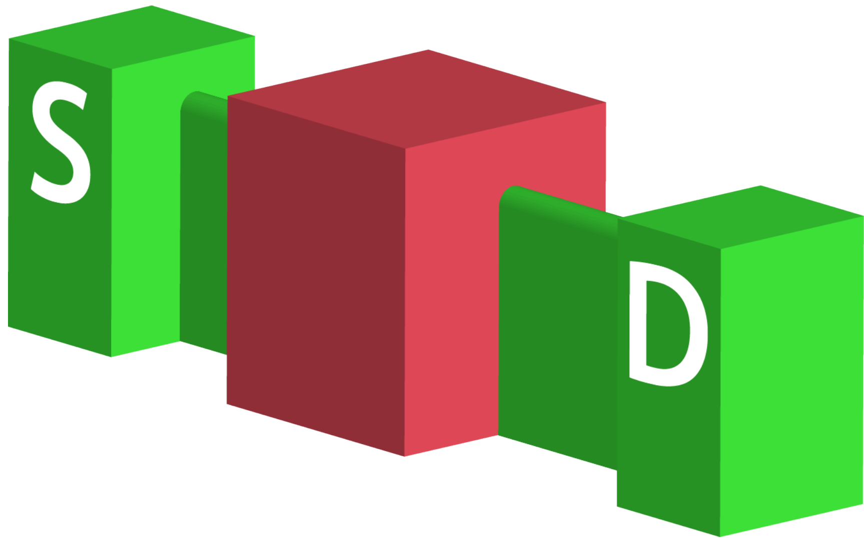
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Our idea

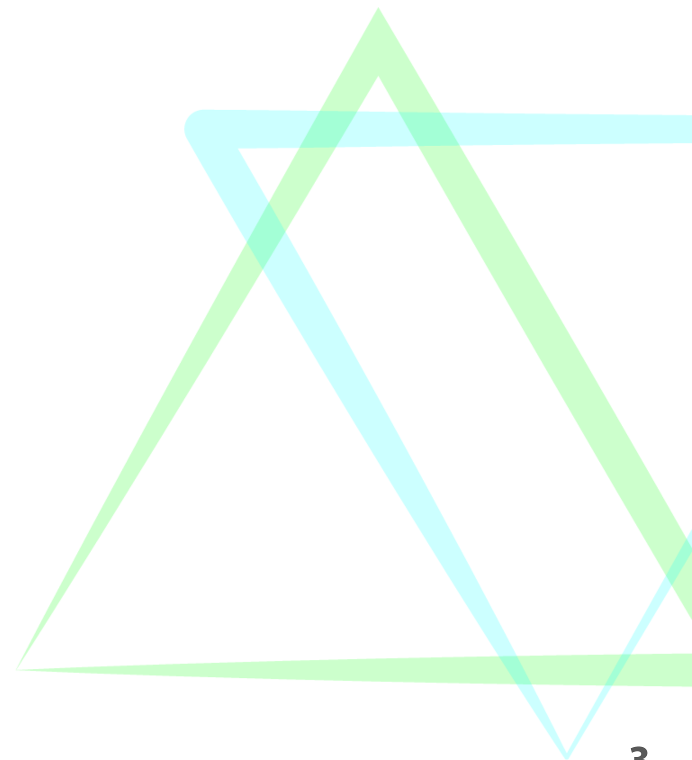
- Programmable polarity device
- Stacked nanowire channel
- Gate-all-around structure
- VLSI compatible



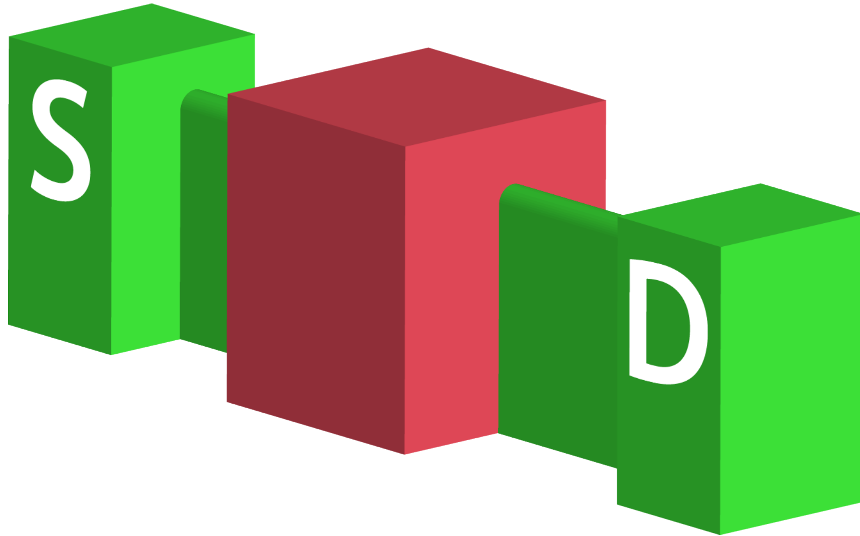
FinFET to Nanowire FET

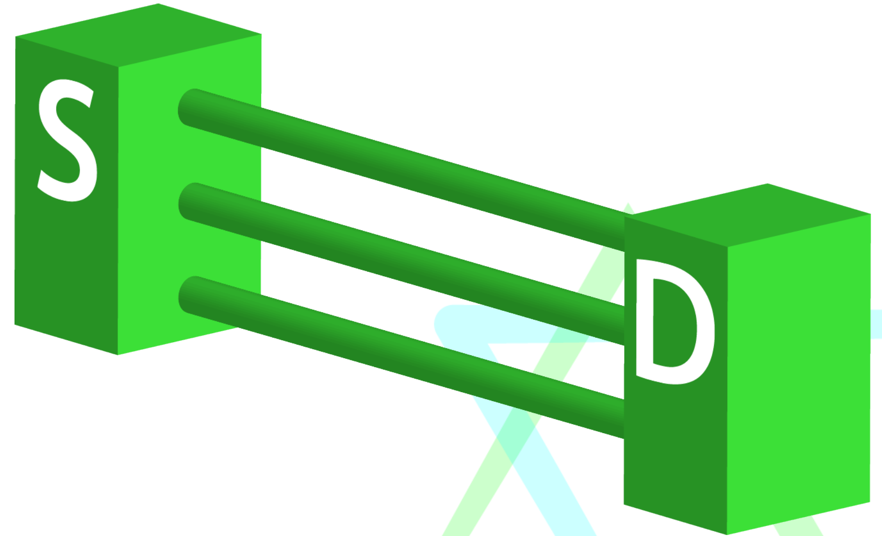


FinFET



FinFET to Nanowire FET

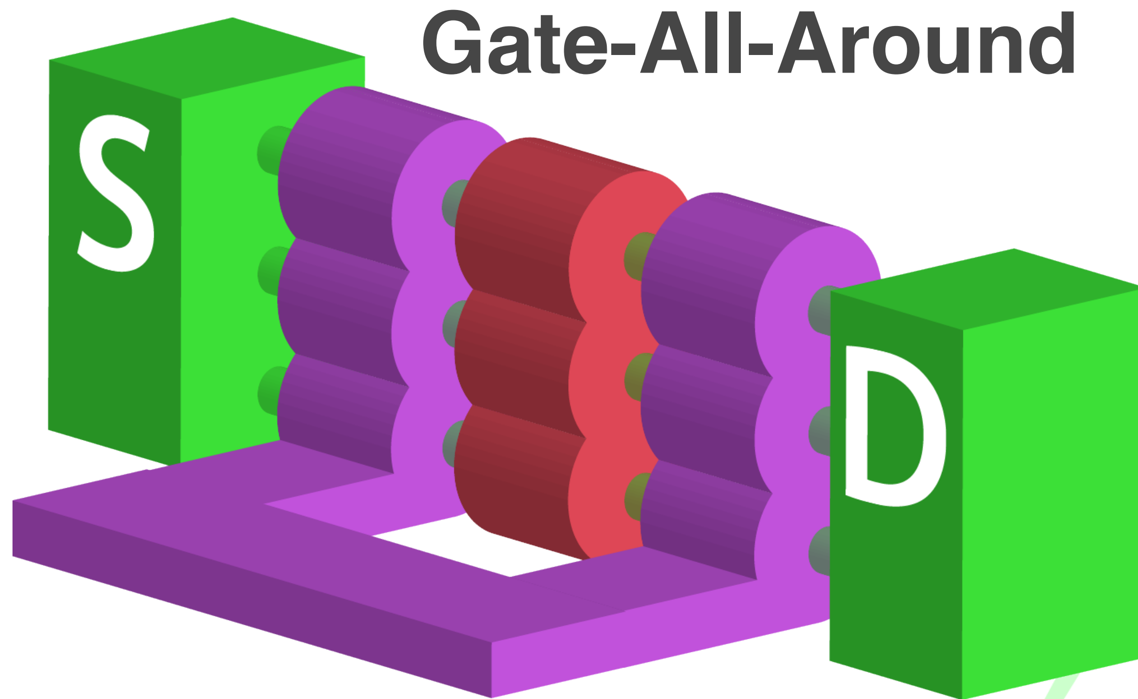




FinFET

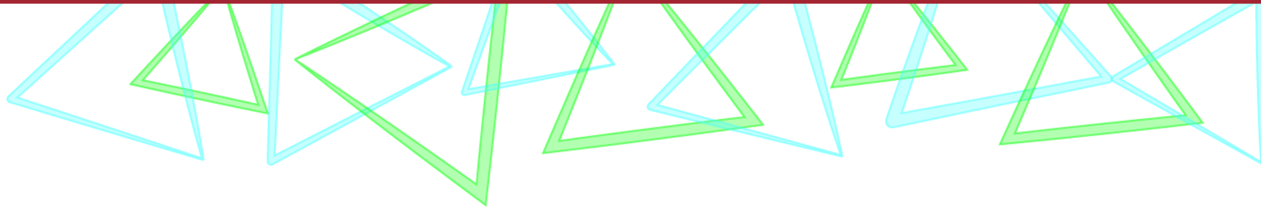
NW FET

Our Nanowire FET

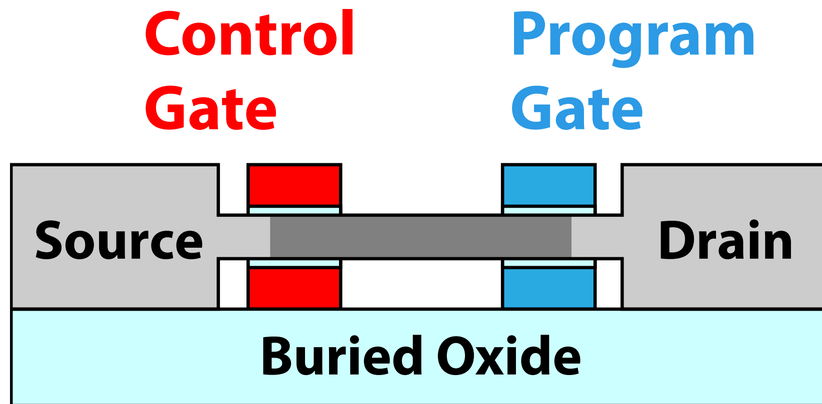


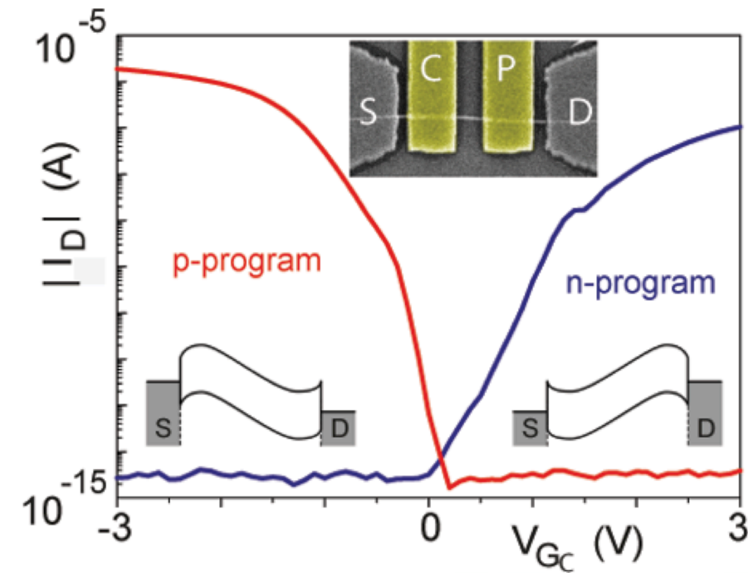
NW FET

Circuit design methodology



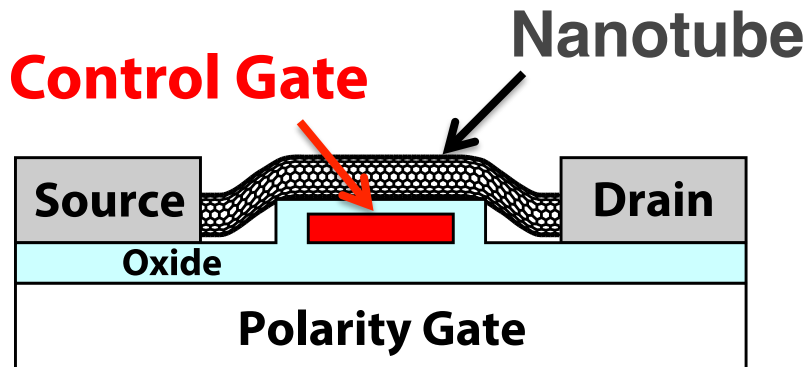
Programmable polarity SiNWFET

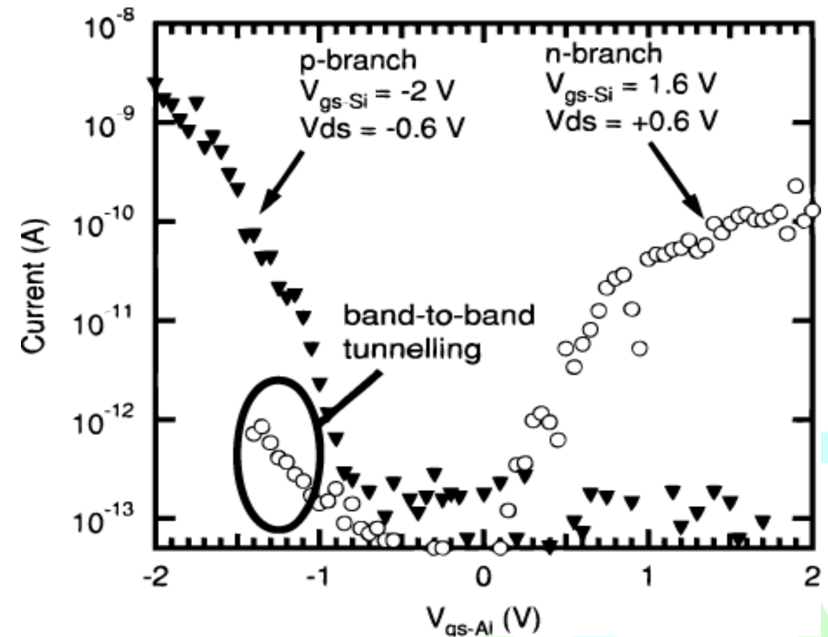




A. Heinzig *et al.*, Nano Letters 2012

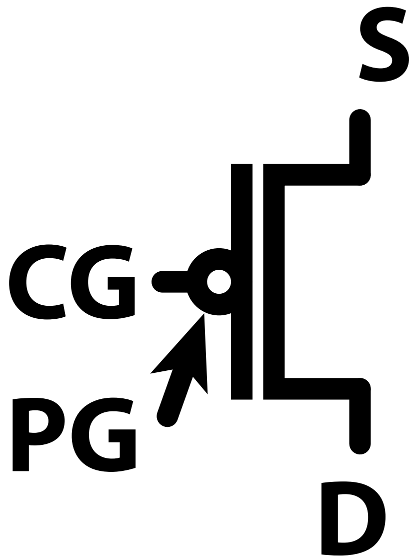
Ambipolar Carbon Nanotube FET

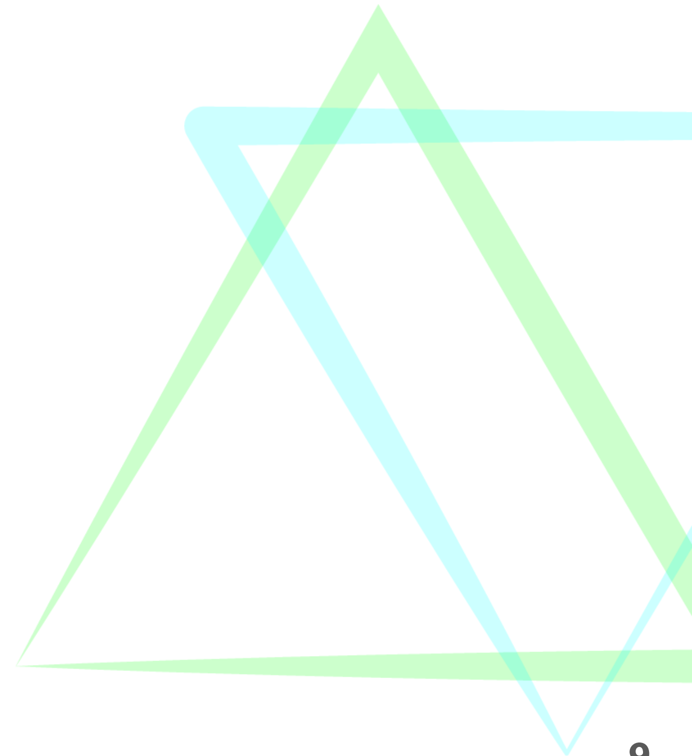




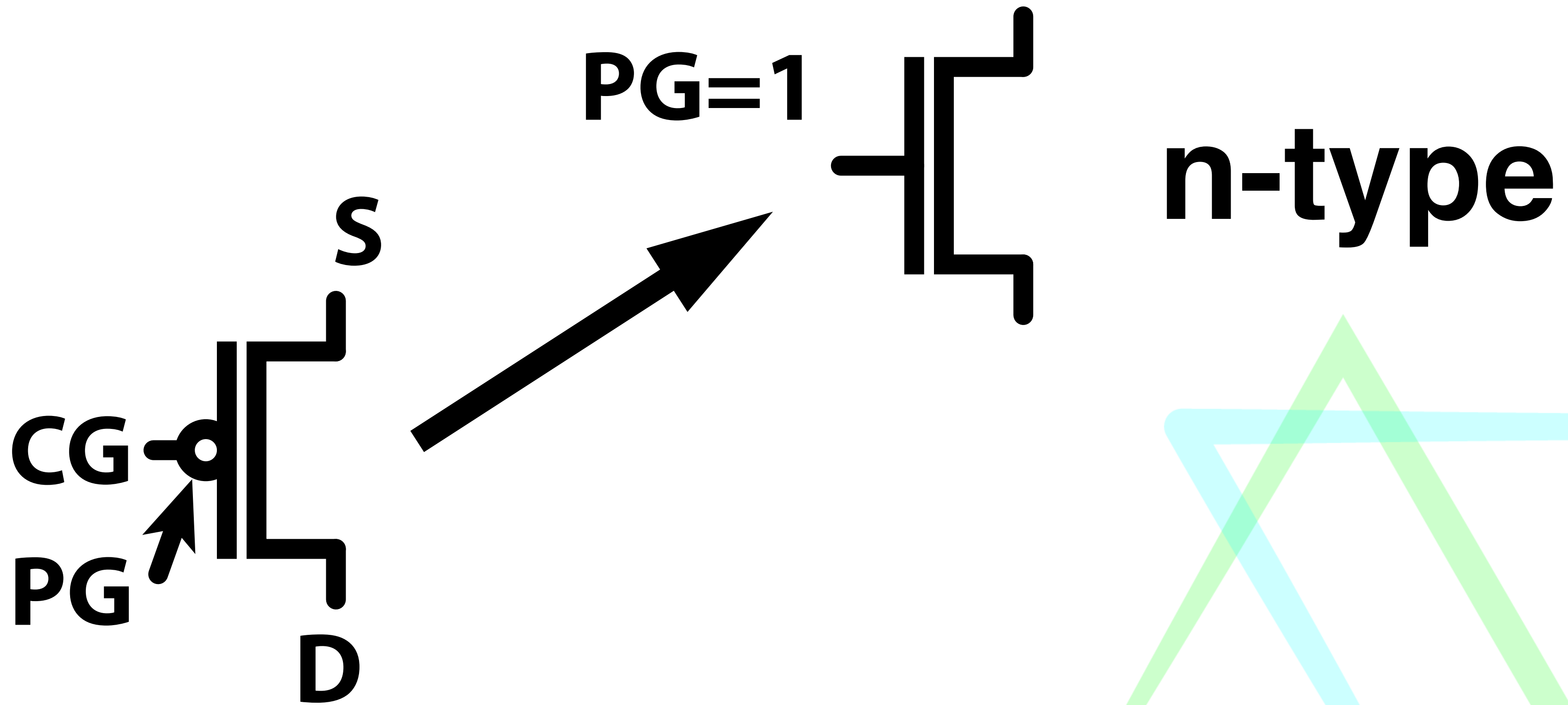
Y.-M. Lin *et al.*, IEEE Trans. on Nanotechnology, 2005.

Polarity control: circuit symbol

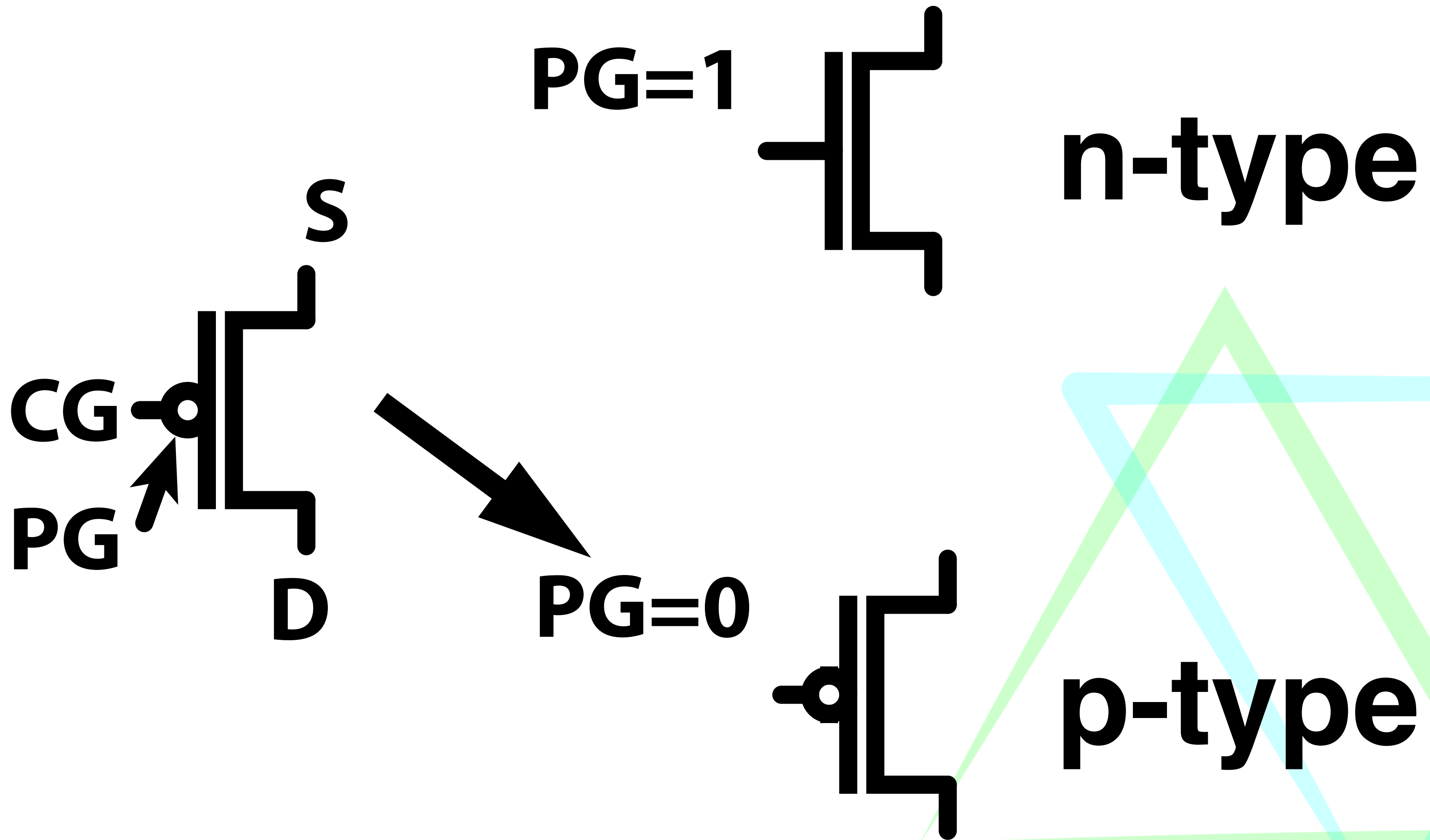




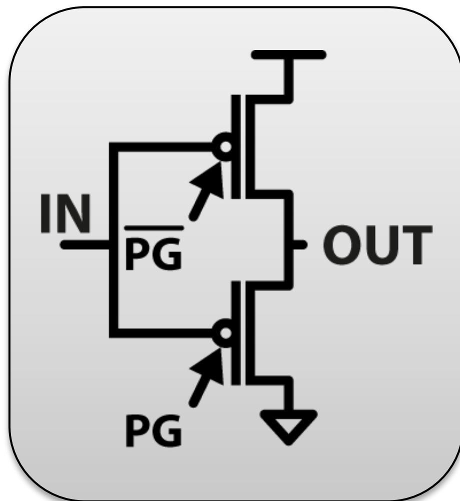
Polarity control: circuit symbol

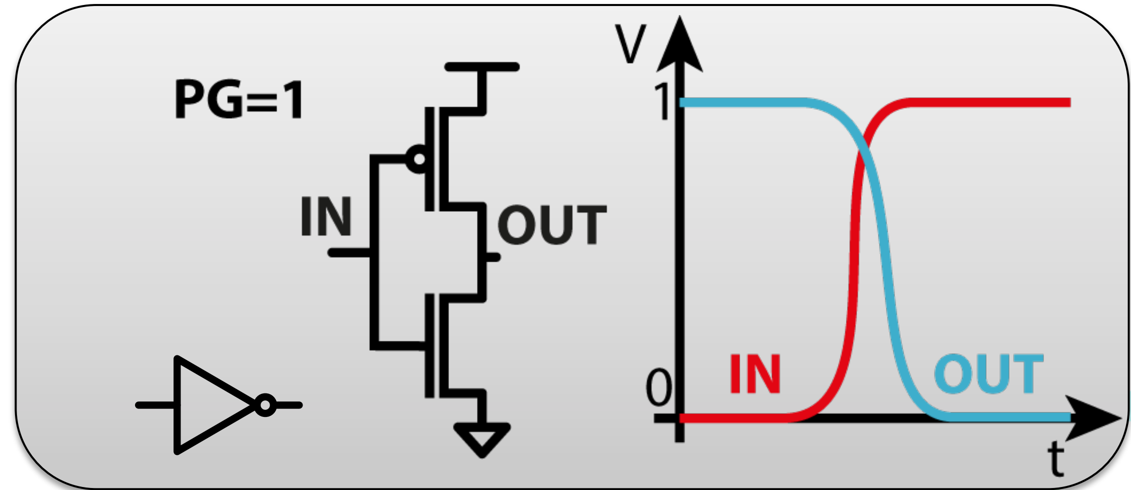


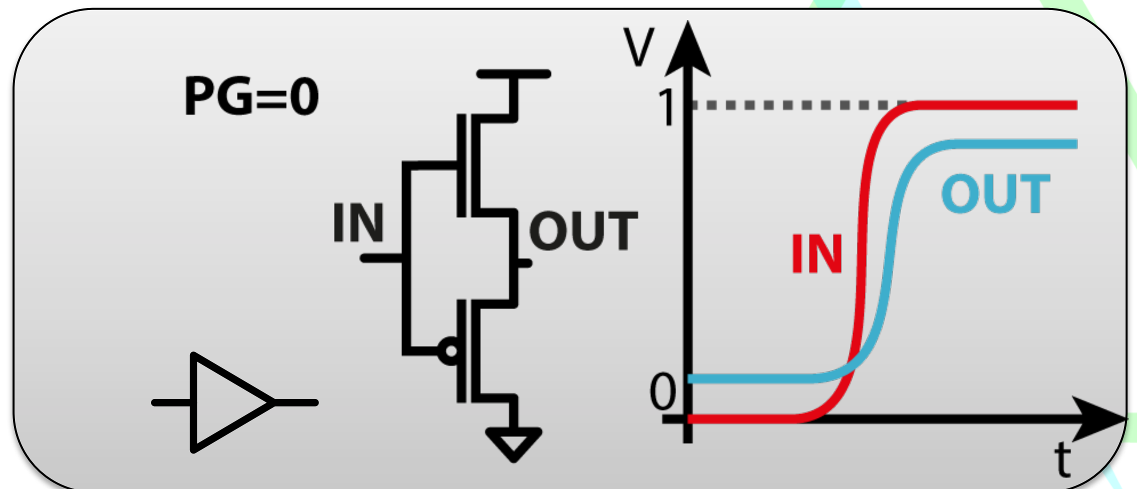
Polarity control: circuit symbol



Inverter / buffer circuit

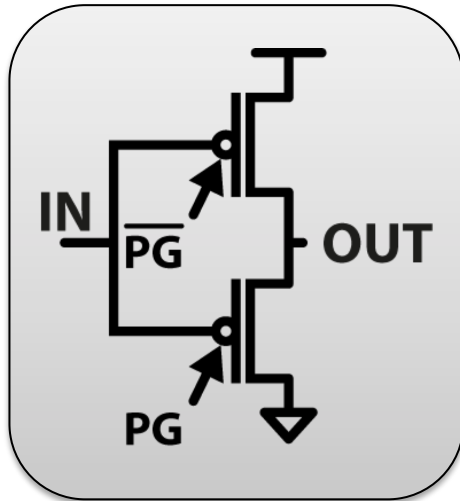


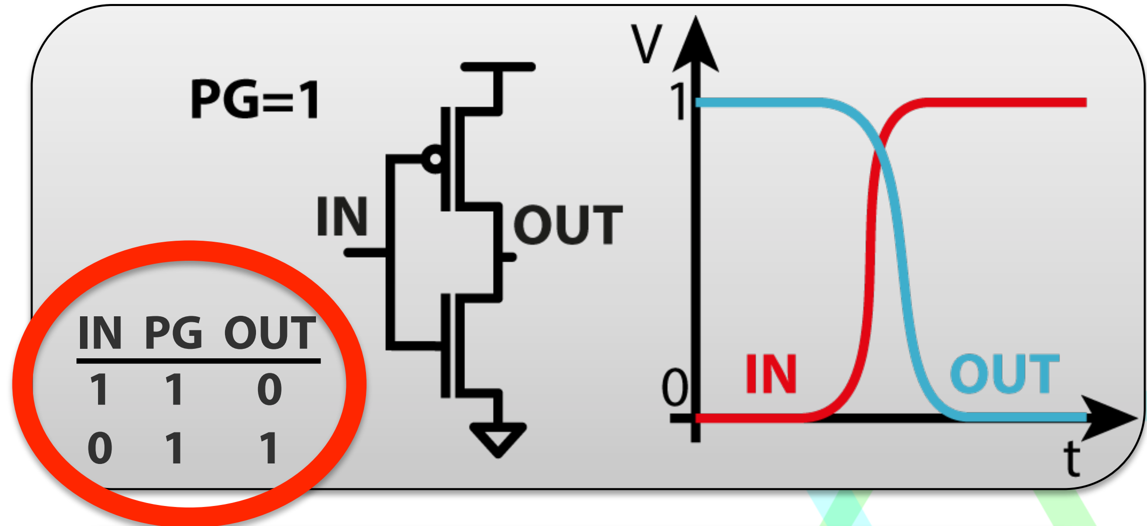




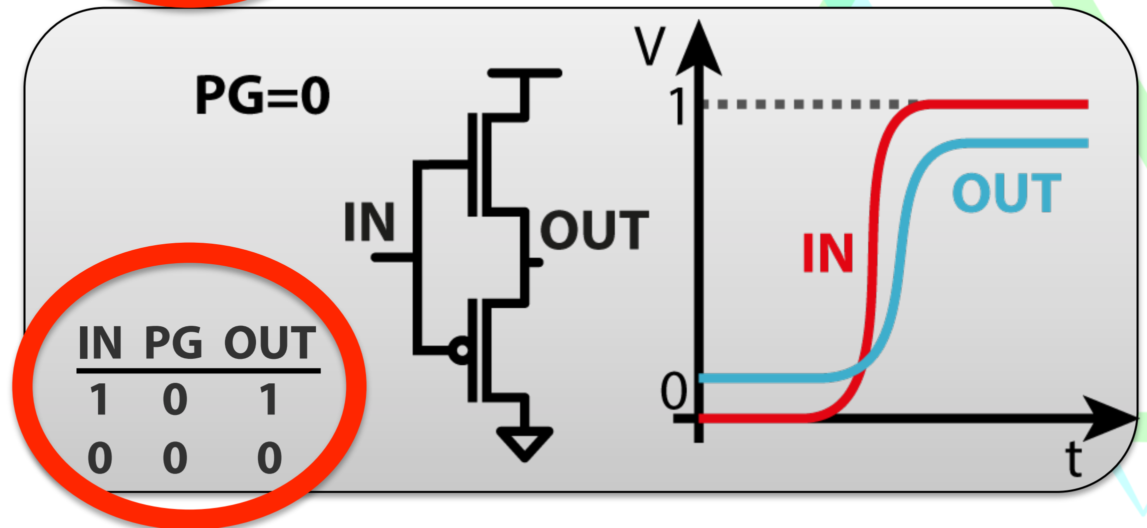
H. Ben Jamaa et al., DATE 2009
M. De Marchi et al., NANOARCH 2010

Inverter / buffer circuit





IN	PG	OUT
1	1	0
0	1	1



IN	PG	OUT
1	0	1
0	0	0

H. Ben Jamaa et al., DATE 2009
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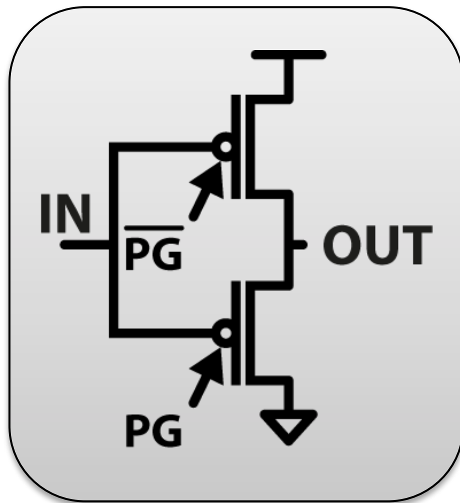
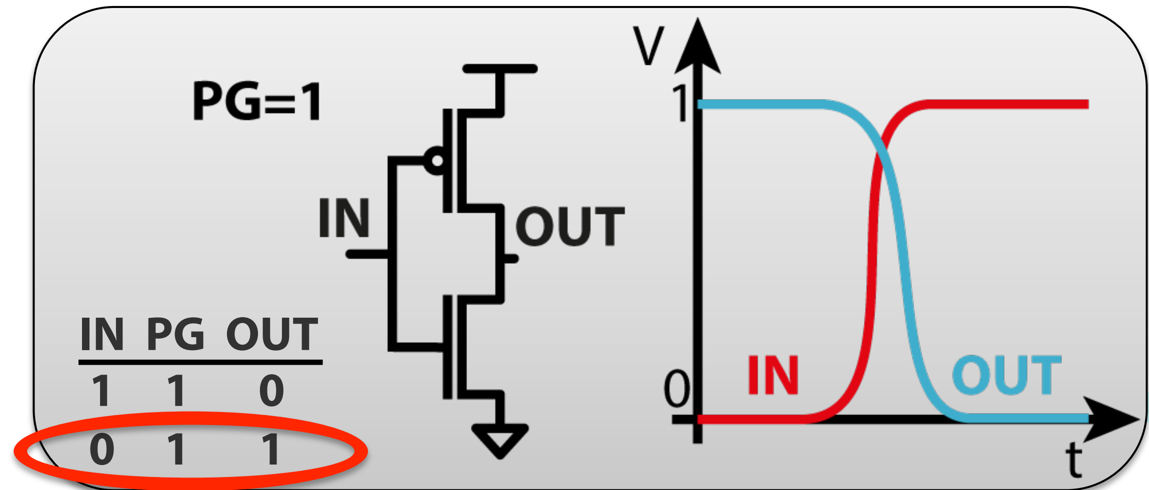
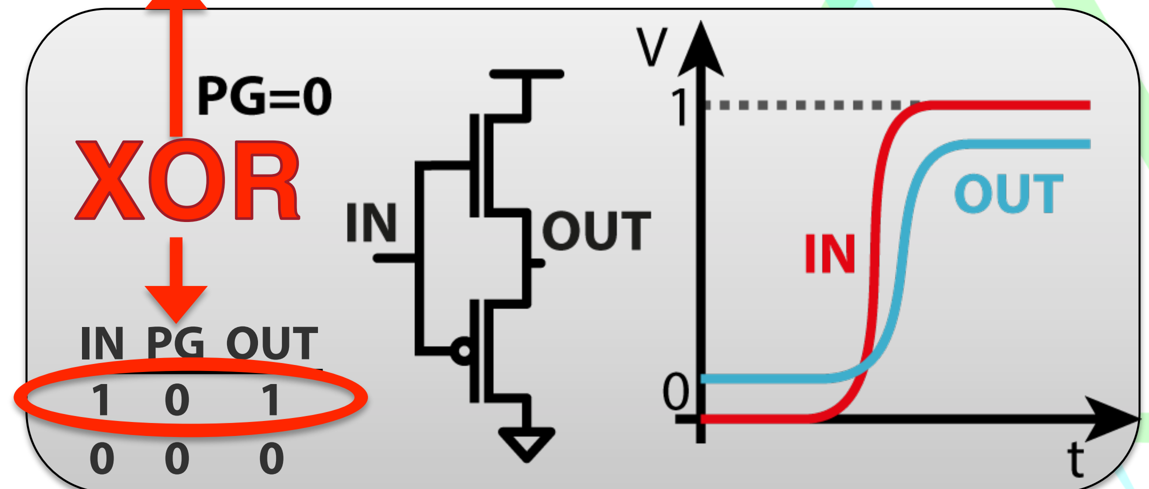
Inverter / buffer circuit







H. Ben Jamaa et al., DATE 2009
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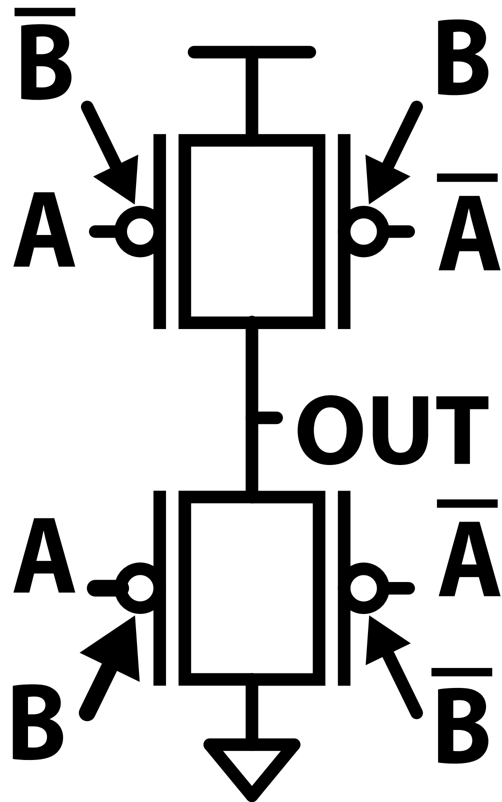
Full swing XOR circuit



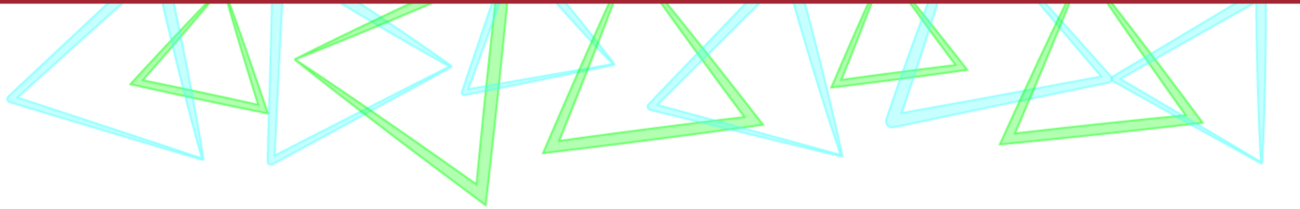
(B=0)
1
OUT
(B=1)
0
0 A 1

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

XOR

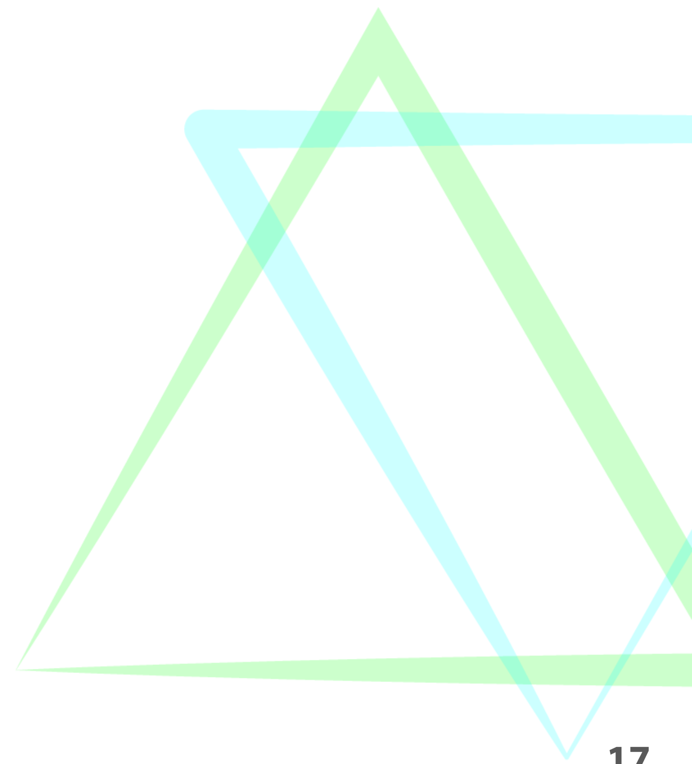
H. Ben Jamaa et al., DATE 2009
M. De Marchi et al., NANOARCH 2010

The device

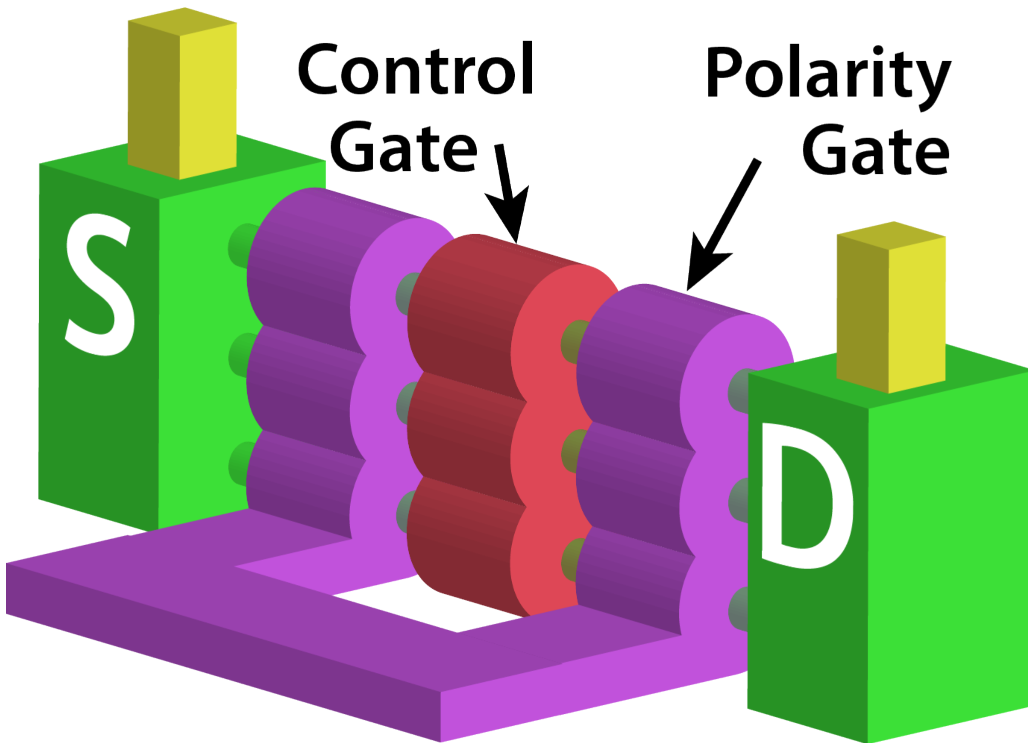


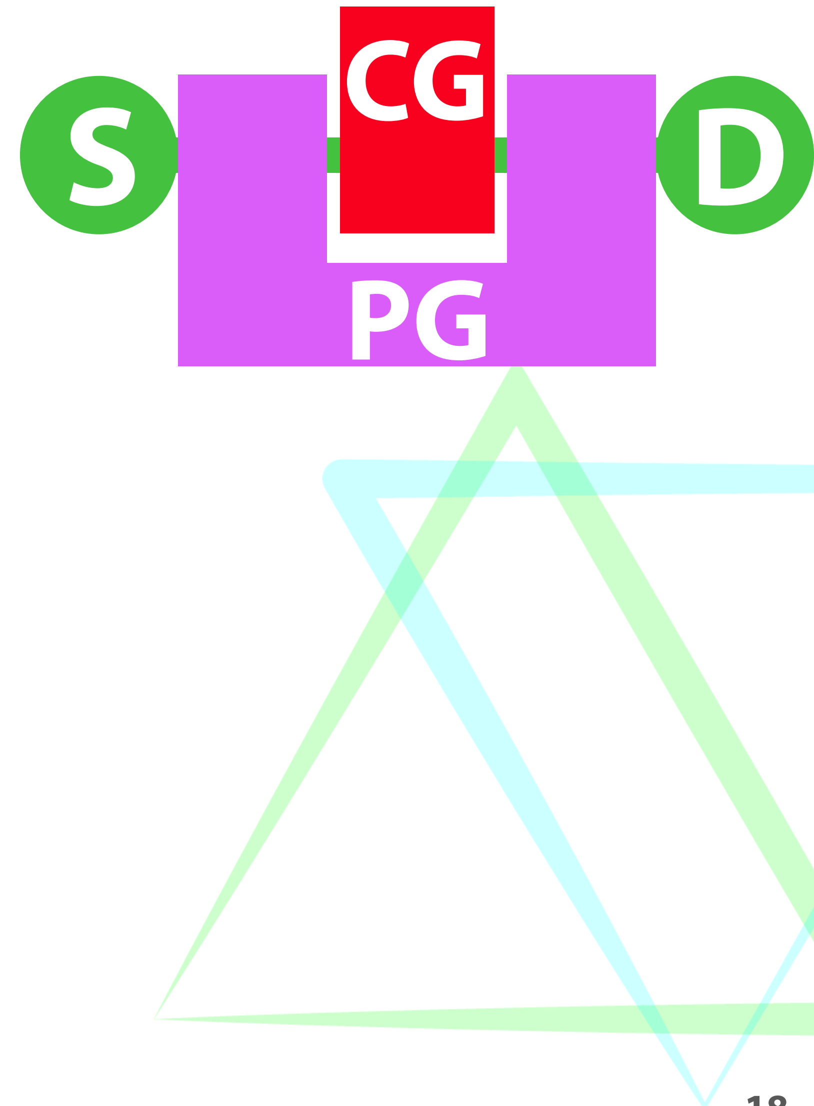
Features we need

- Polarity control
- Symmetric operation
- p-type for PG=0V
- VLSI capability

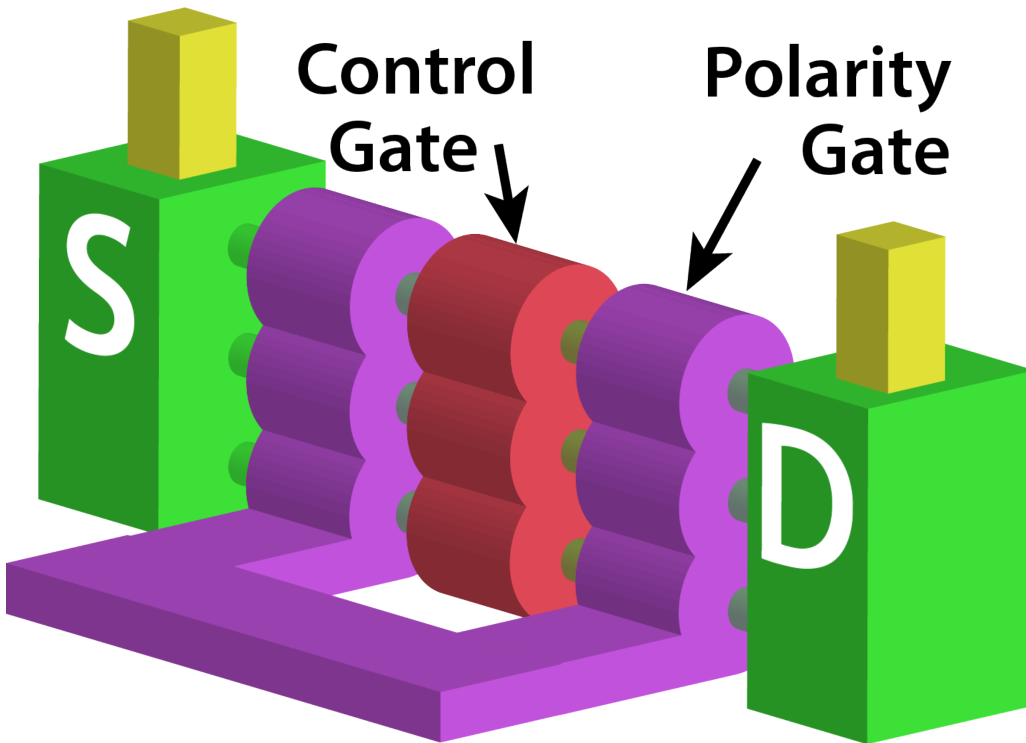


Complete device structure



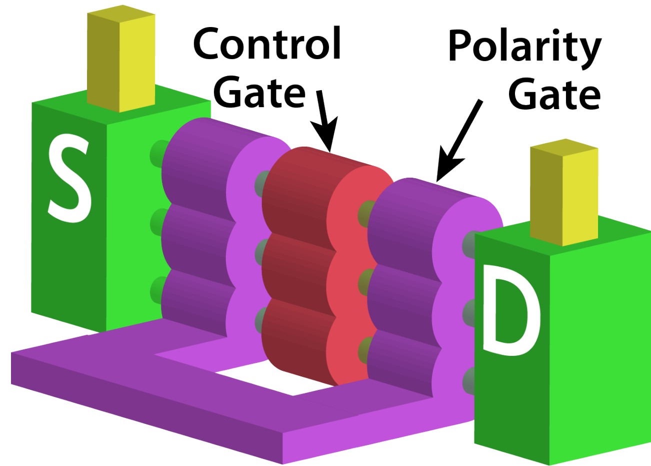


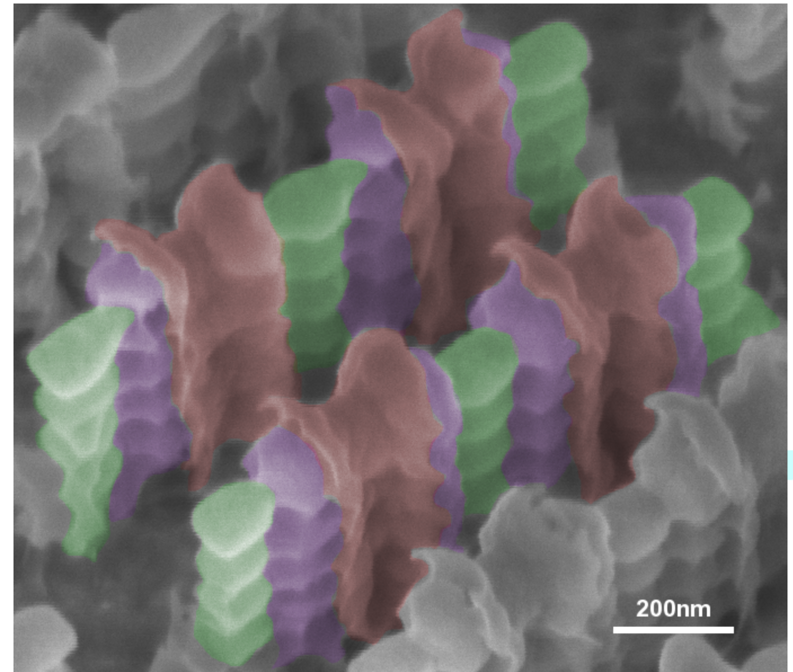
Complete device structure

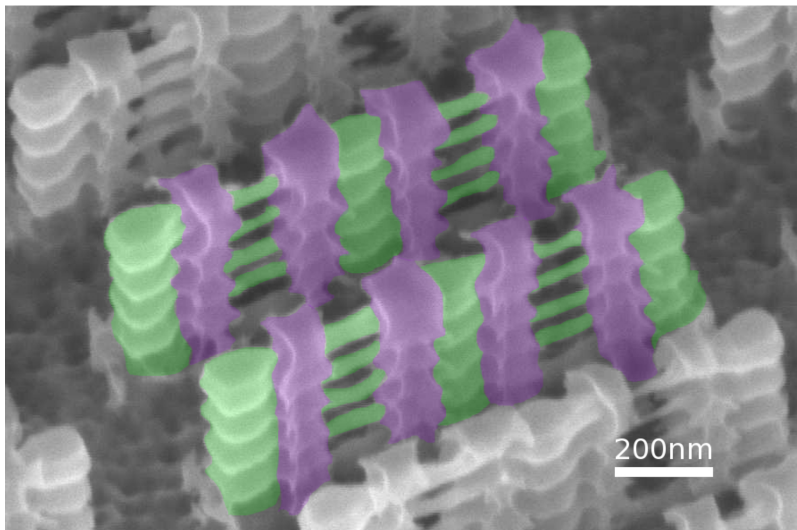


- Si NW stack
- Low p-doped NWs
- Polysilicon gates
- Midgap NiSi S/D contacts

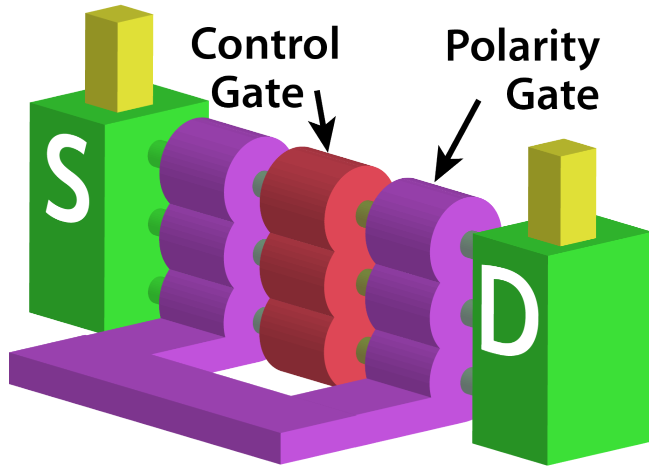
Fabricated device view

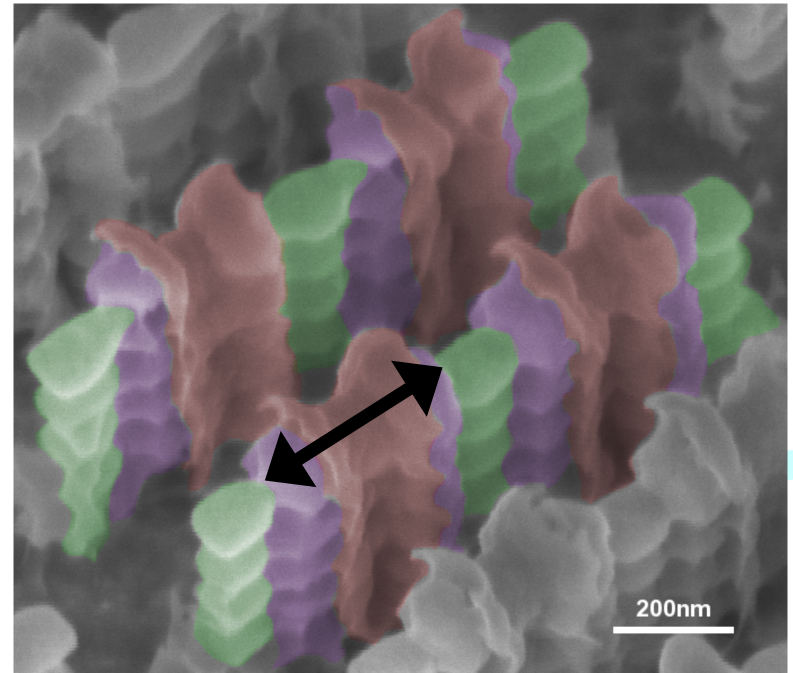




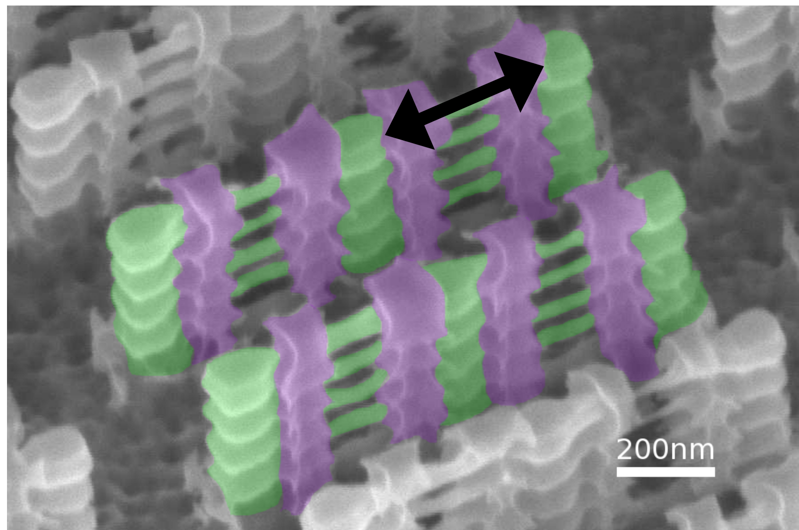


Fabricated device view

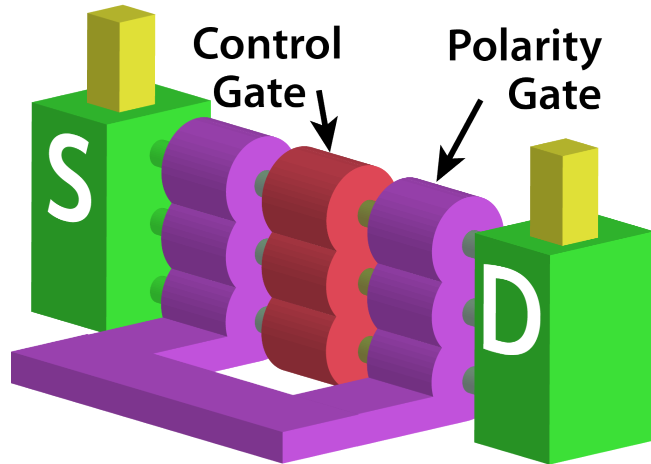


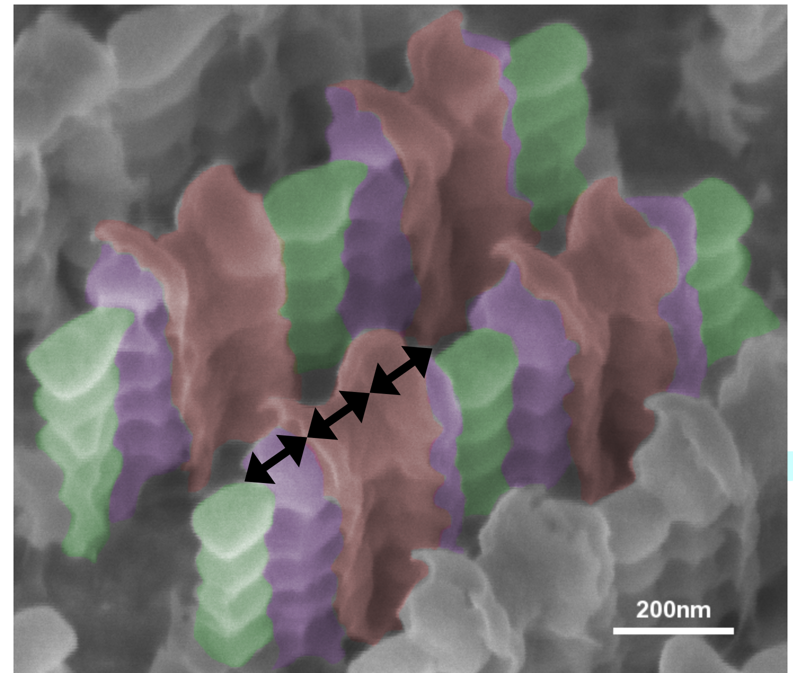


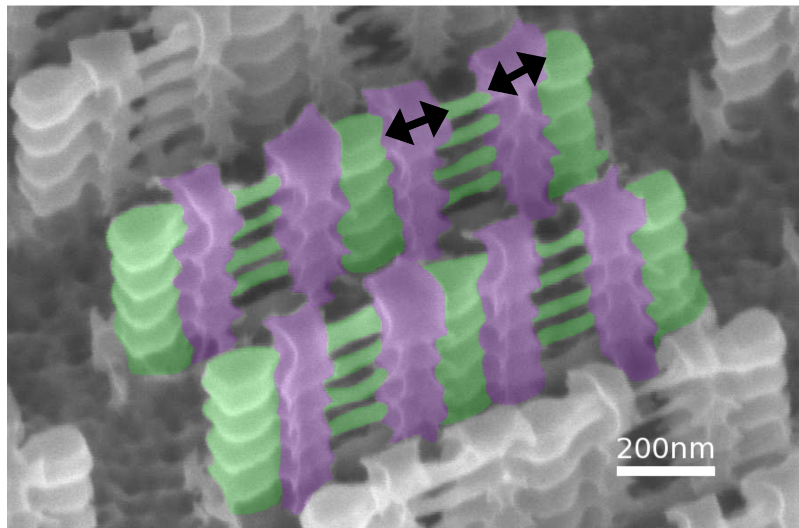
▲350nm long channel



Fabricated device view

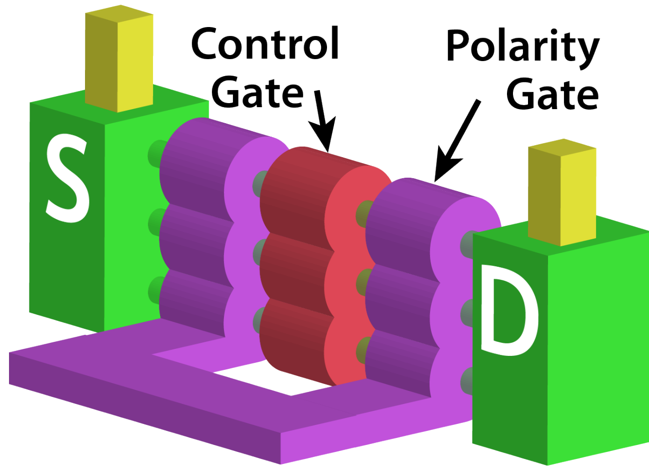


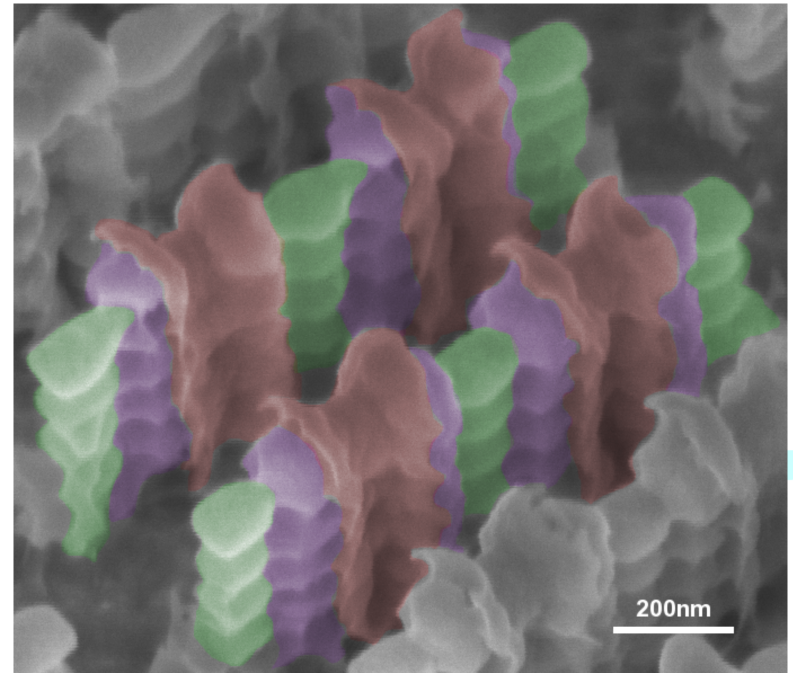


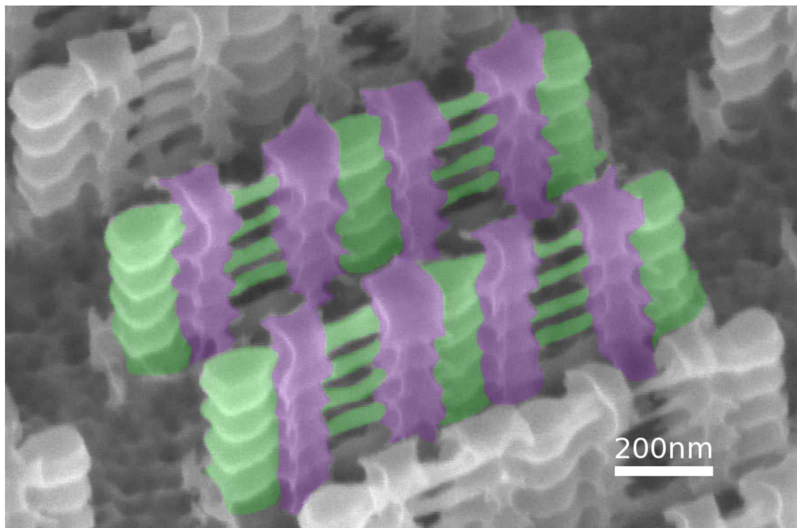


- 350nm long channel
- 100nm gate segments

Fabricated device view

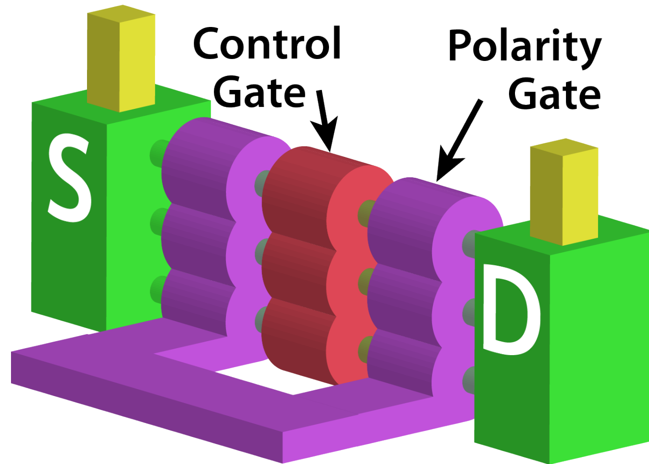


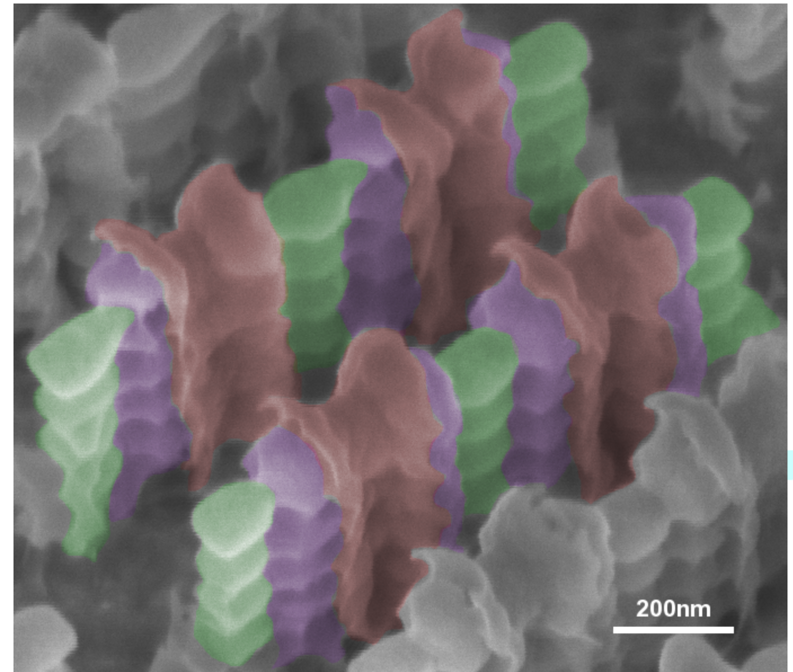


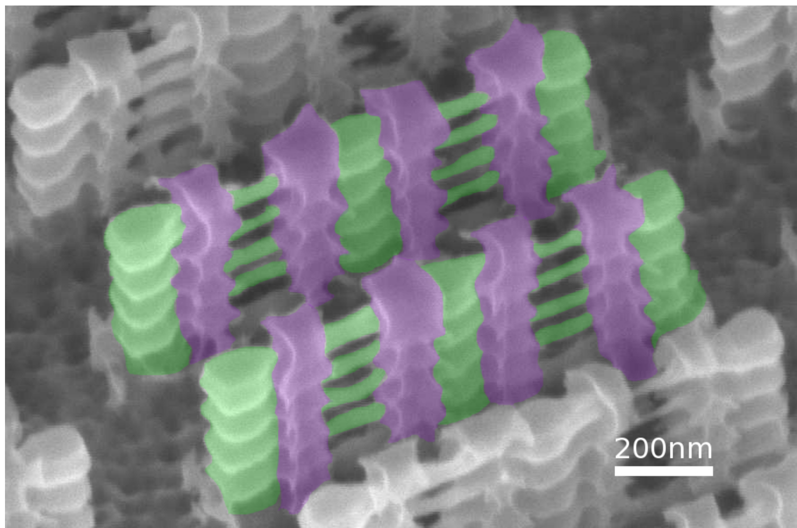


- 350nm long channel
- 100nm gate segments
- 20–40nm wire diameter

Fabricated device view

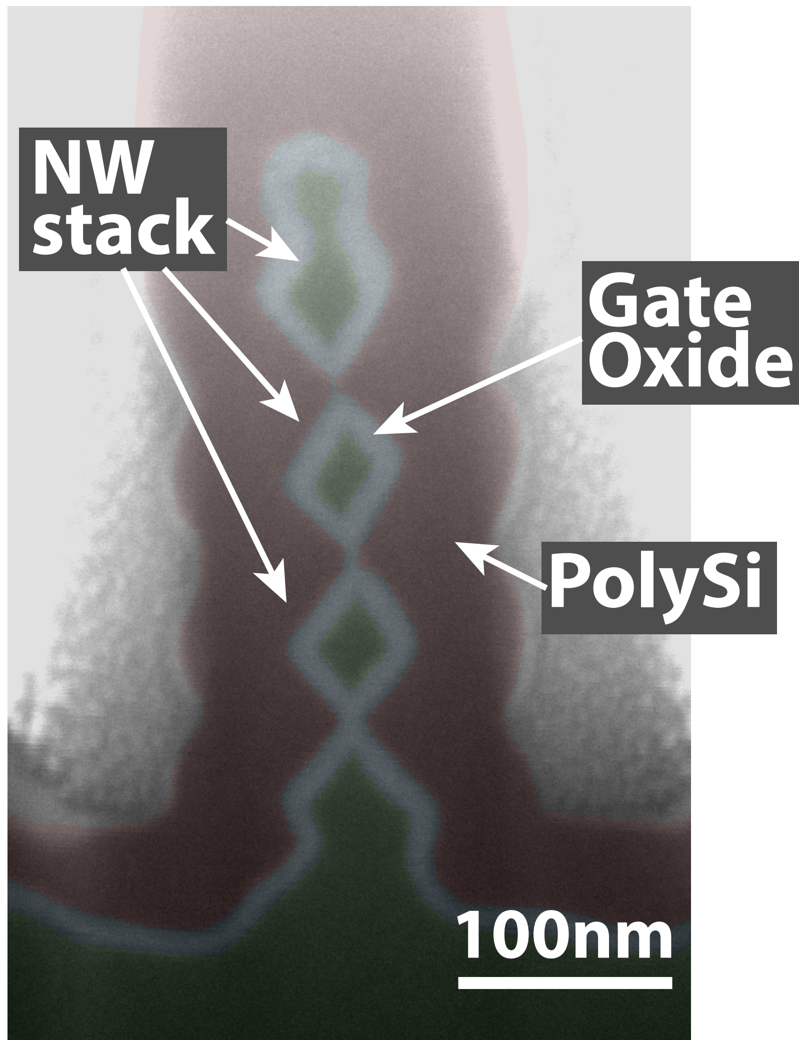


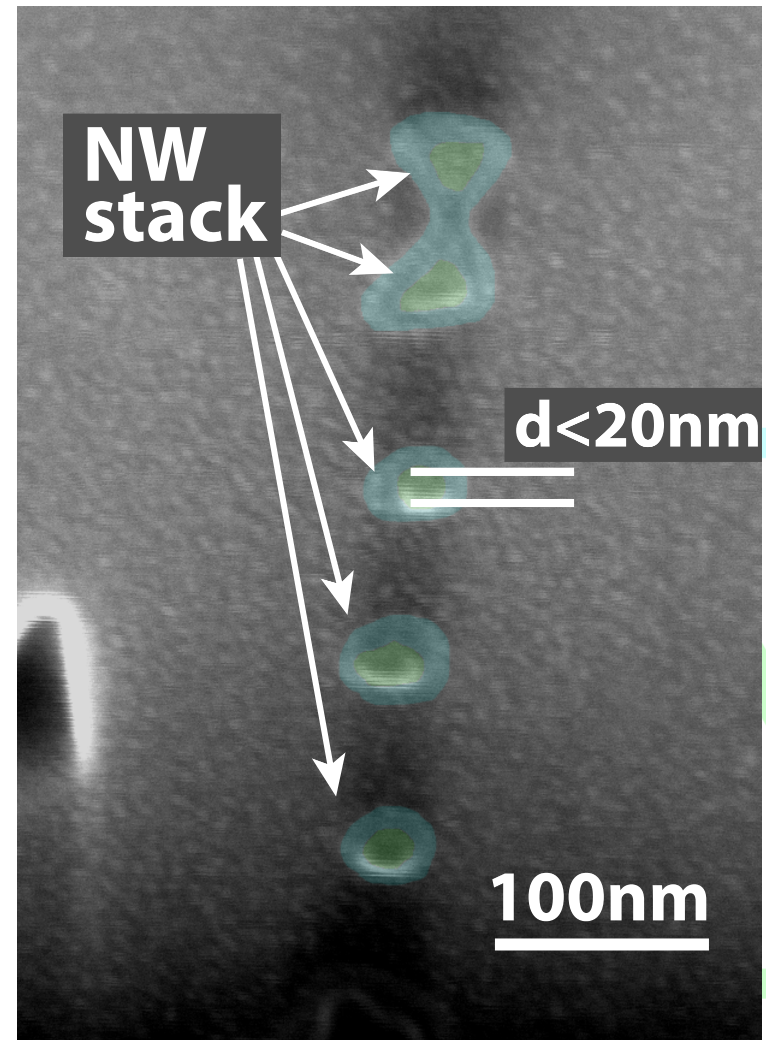




- 350nm long channel
- 100nm gate segments
- 20–40nm wire diameter
- Self-aligned CG

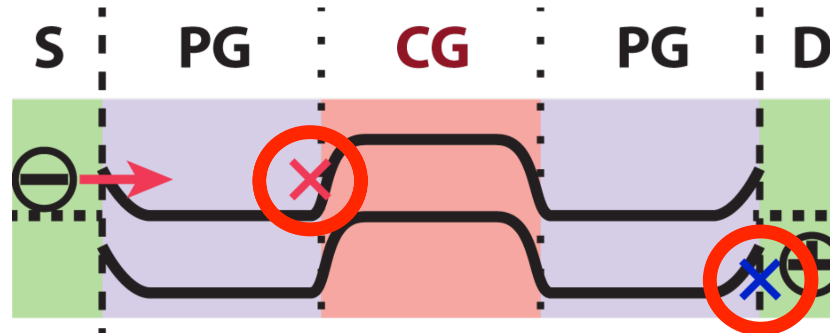
Device cross sections





Device working principle

PG = 1→ n-type
CG = 0



OFF

PG = 1→ n-type
CG = 1

ON

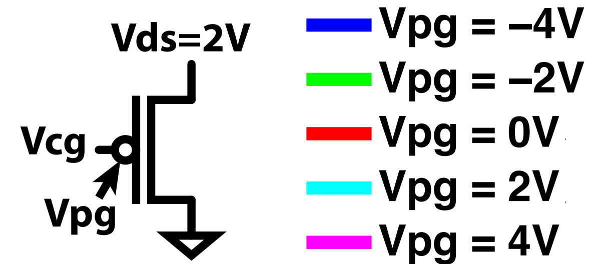
PG = 0→ p-type
CG = 1

OFF

PG = 0→ p-type
CG = 0

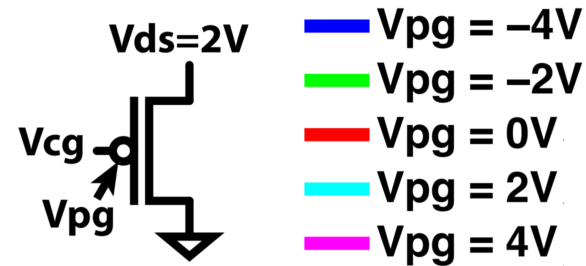
ON

Device I_d-V_{cg}



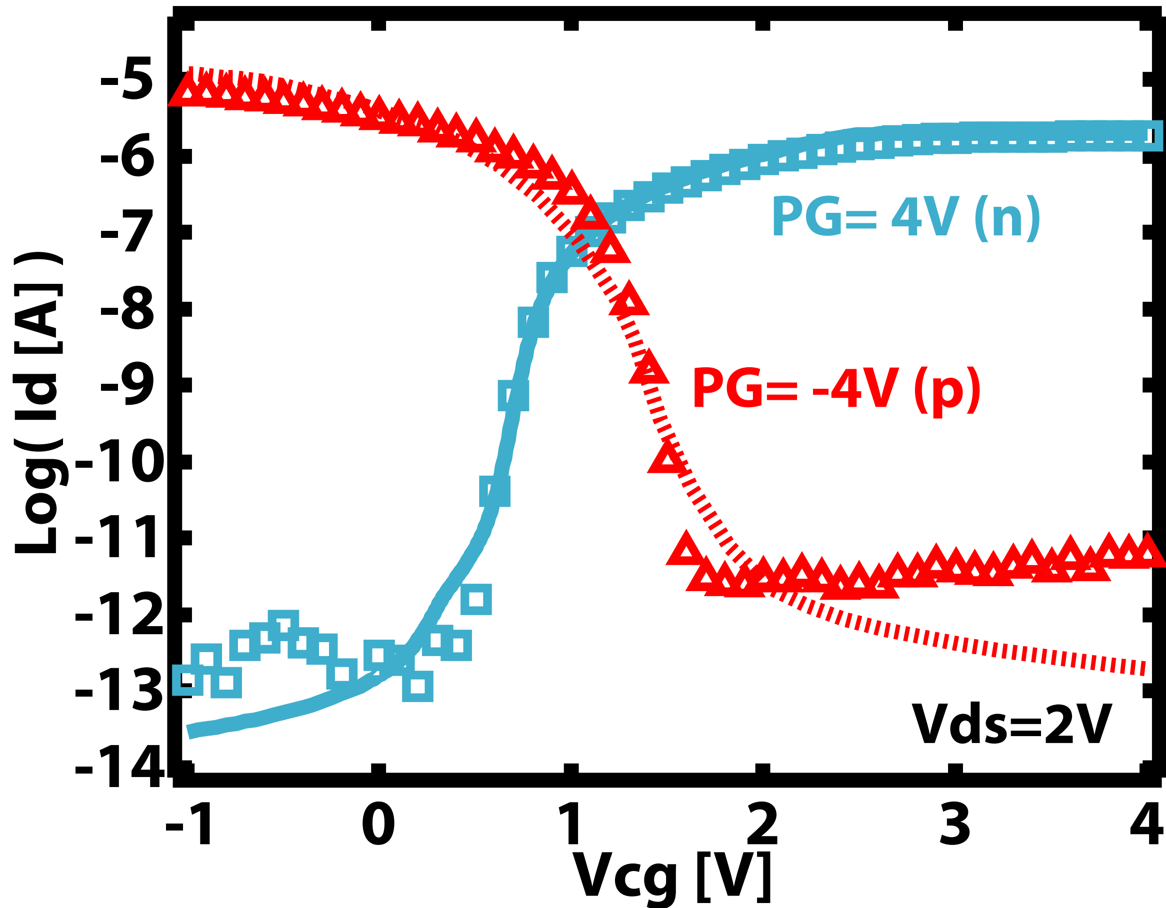
- Crossing > 0V
- PG=0V→p-type
- Symmetry

Device I_d-V_{cg}



- Crossing > 0V
- PG=0V→p-type
- Symmetry
- $I_{ON}/I_{OFF} > 10^6$
- S~64mV/Dec

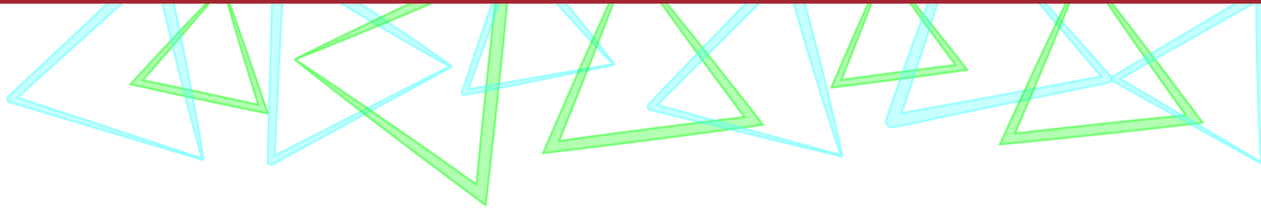
TCAD model validation



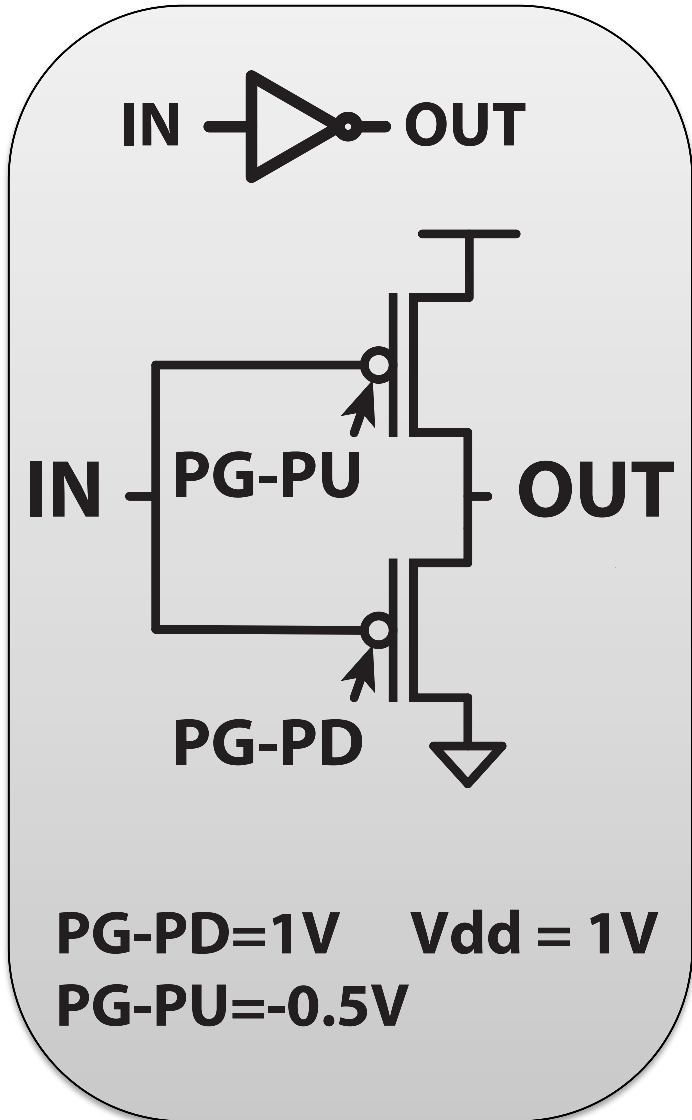
Symbols: Measurement
Lines: TCAD simulation

Simulation consistent with measurement

Fabricated circuits



2 FET inverter configuration



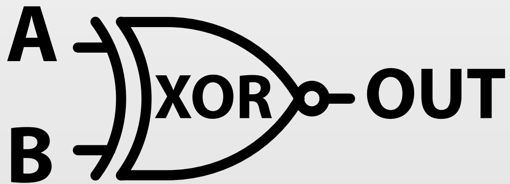
OUT [V]

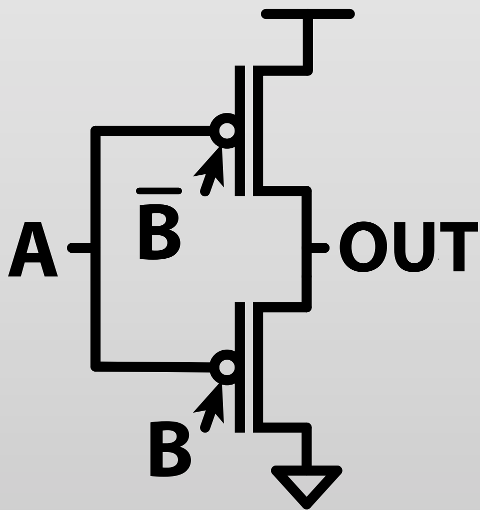
1
0.8
0.6
0.4
0.2
0

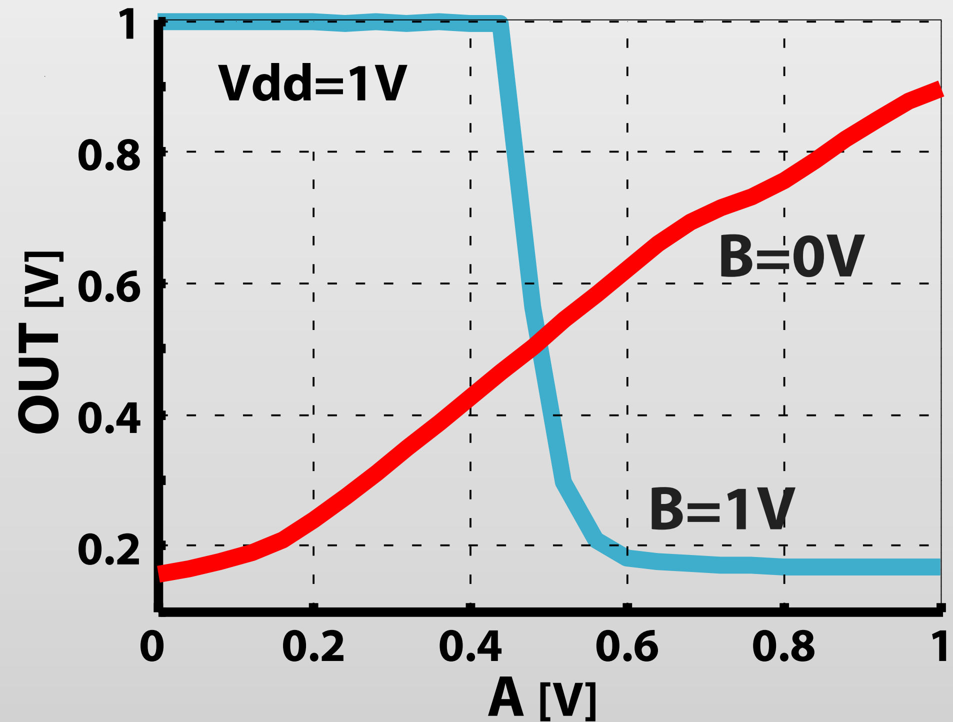
0 0.2 0.4 0.6 0.8 1

IN [V]

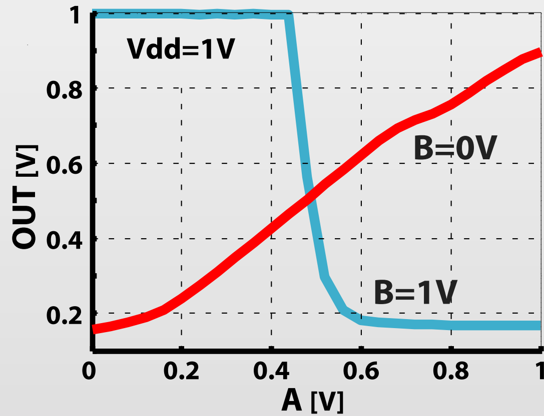
2 transistor XOR circuit

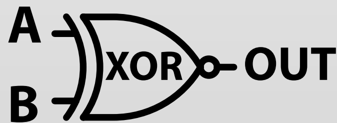


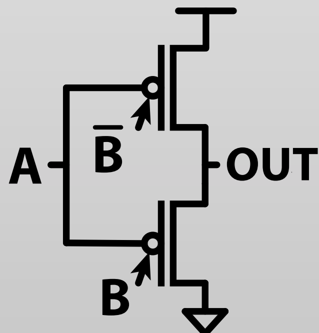


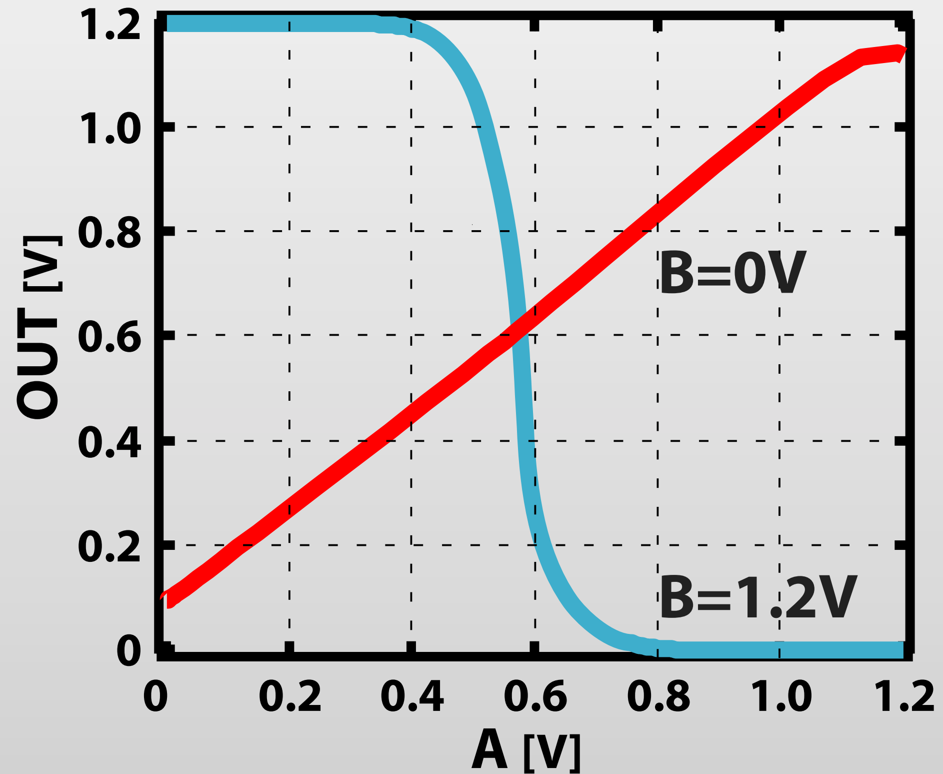


XOR TCAD simulation



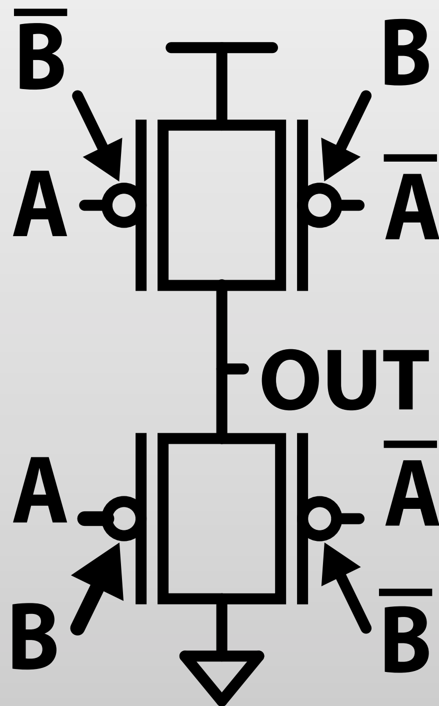


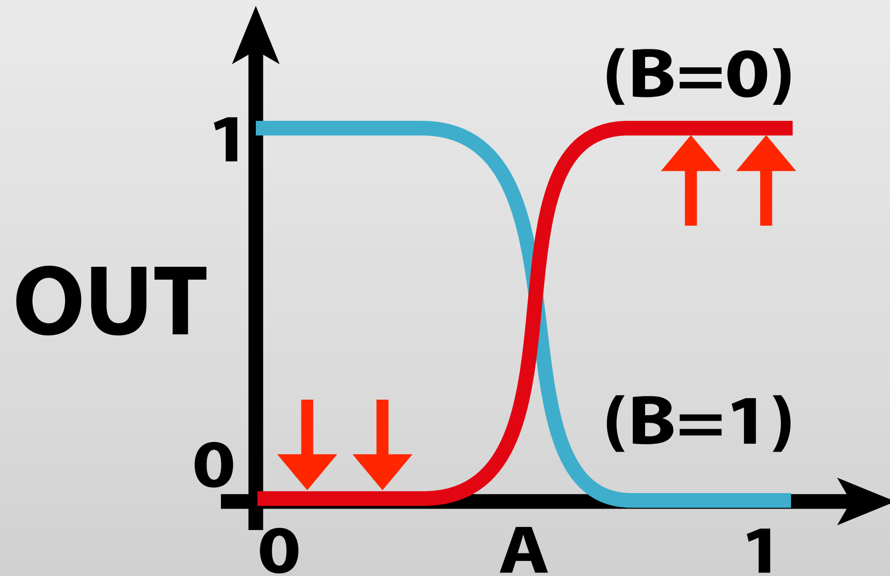




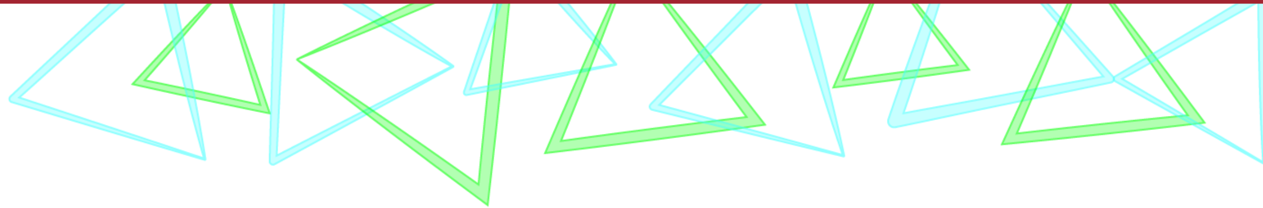
Buffer fixed by adding 2T

Full swing XOR circuit

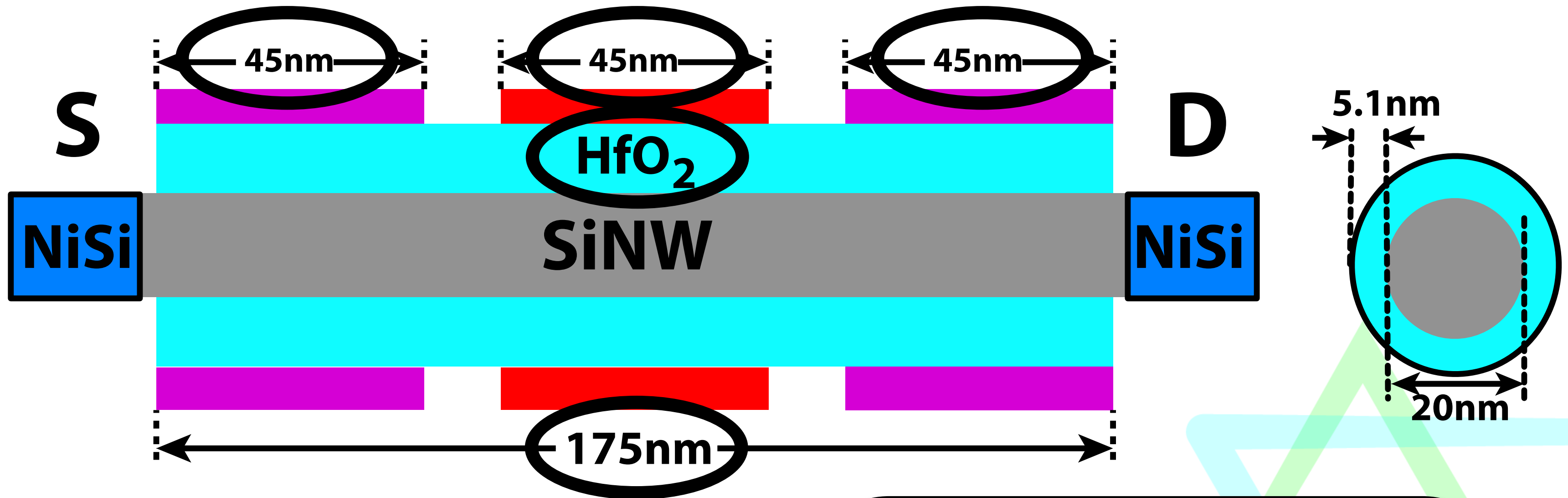


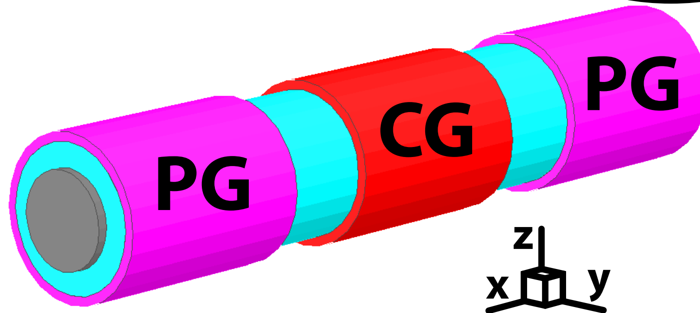


Predicted performance



Device optimization

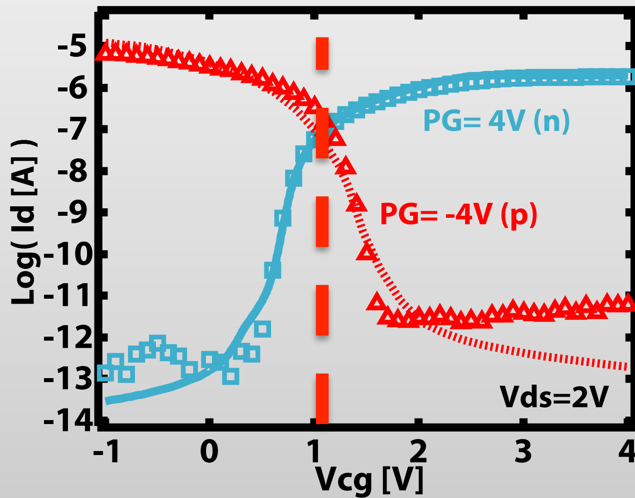


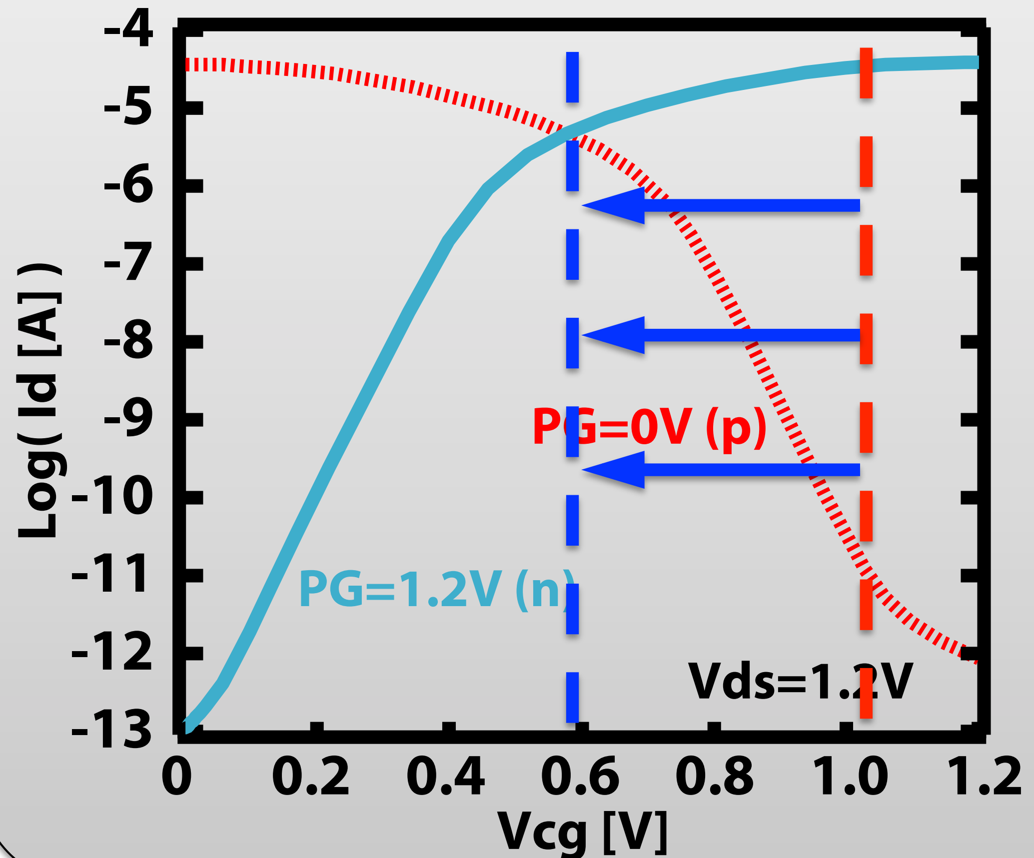


TCAD model

- Reduced dimensions
- High-κ dielectric (EOT = 0.8 nm)

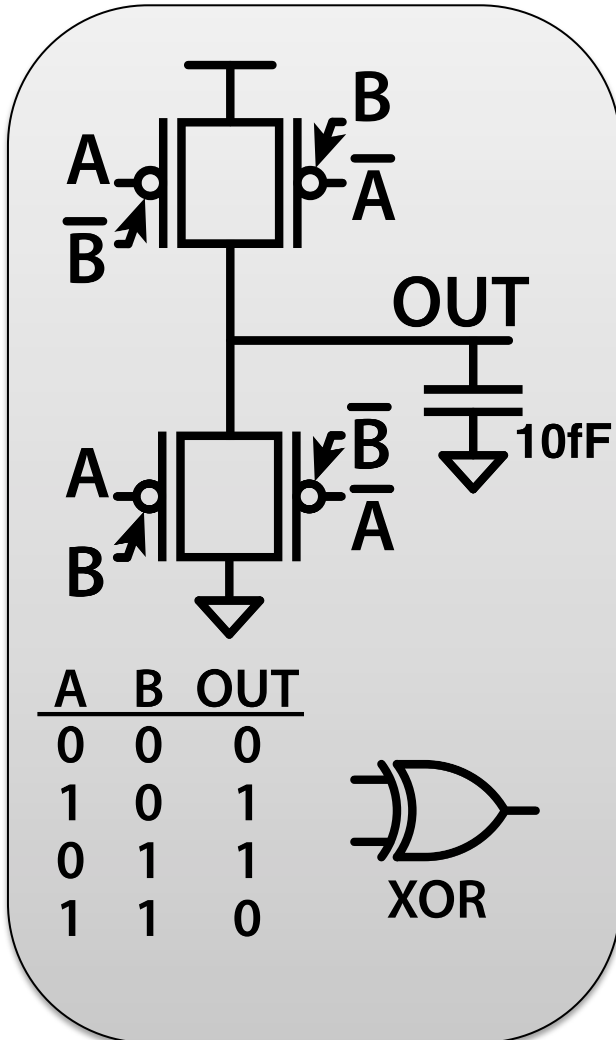
Predicted I_d-V_{cg}





- Crossing shifts left
- Lower V_{dd}

4 transistor XOR simulation



A	B	OUT
0	0	0
1	0	1
0	1	1
1	1	0

A [V]
1.2
0.6
0.0
0 1 0 1

B [V]
1.2
0.6
0.0
0 0 1 1

OUT [V]
1.2
0.6
0.0
0 1 1 0

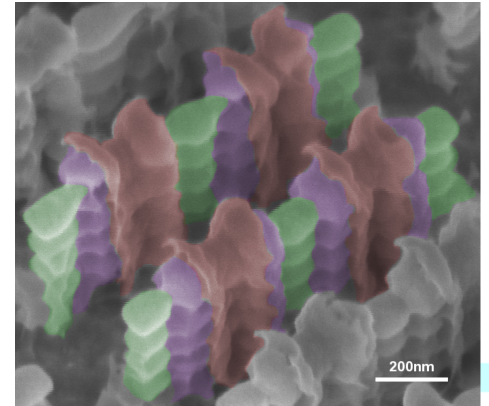
0 10 20

Time [ns]

Simulated with Hspice

Conclusion

- ▲ **Fabricated device**
  - ▽ Top-down stacked nanowires
  - ▽ Gate-All-Around
  - ▽ p-type for PG=0V
  - ▽ Symmetric behavior
- ▲ **Demonstrated circuits**
  - ▽ Configurable inverter
  - ▽ 2 Transistor XOR



Thank you