FROM RESEARCH TO INDUSTRY

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Modularity study of ultra-fine grain FPGA based on DG-CNTFET

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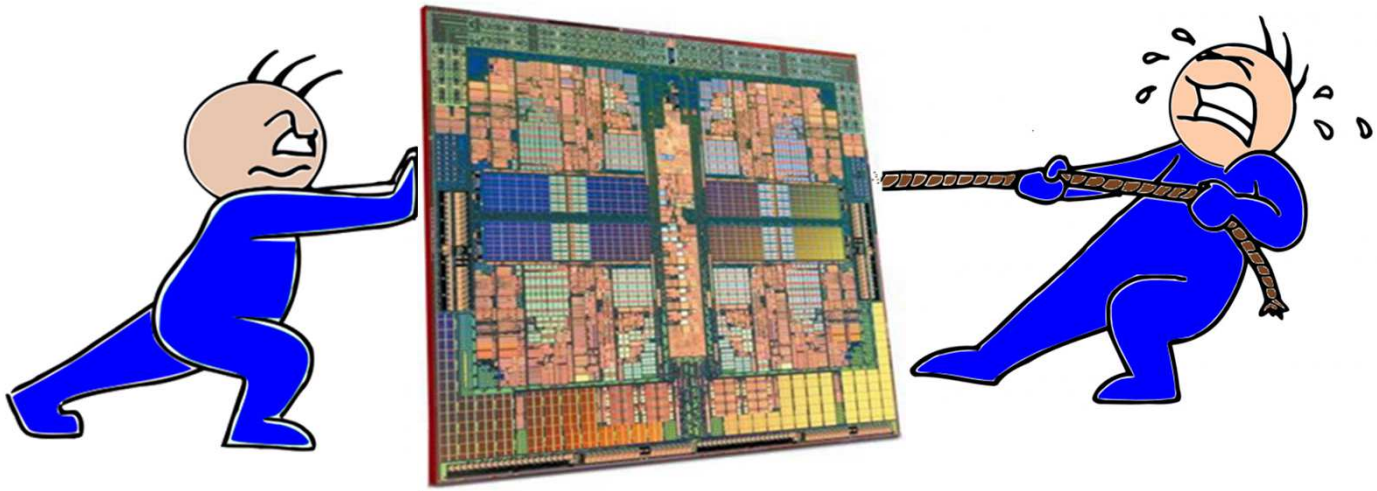
www.cea.fr

leti & list

FPGA versus Von Neumann architectures



Technology Push

Moore's Law

Development Costs ↑

Reliability ↓

Emerging Technologies

Efficiency ↑

Power consumption ↓

Reliability

Architecture Pull

Von Neumann Architectures

Complexity ↑

Power consumption ↑

Reconfigurable Architectures

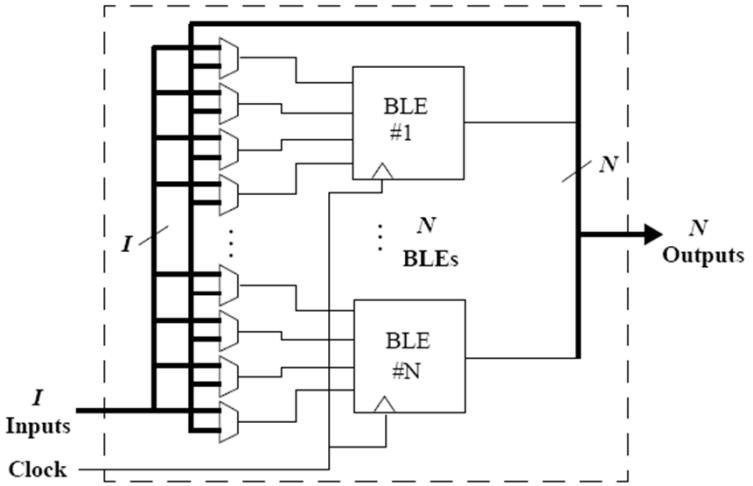
Cost ↓

Regularity ↑

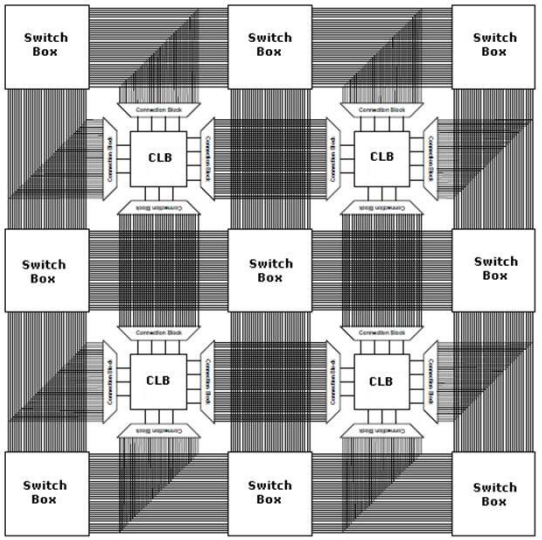
Outline

- **FPGA & NANOGRAIN project**
- DG-CNTFET reconfigurable cell
- Solving the interconnect issue
- Conclusion

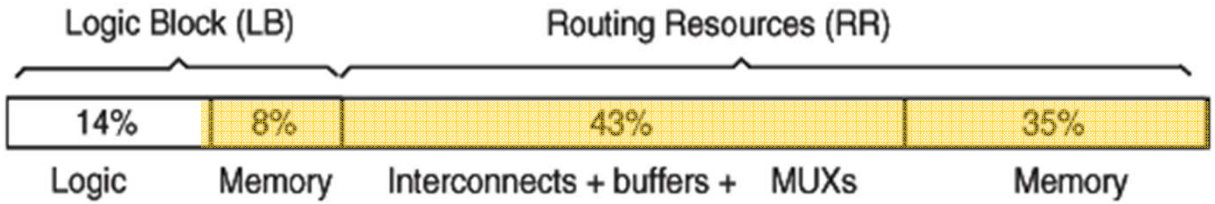
Field Programmable Gate Array



Ahmed et al., 2001



Logic element = CLB

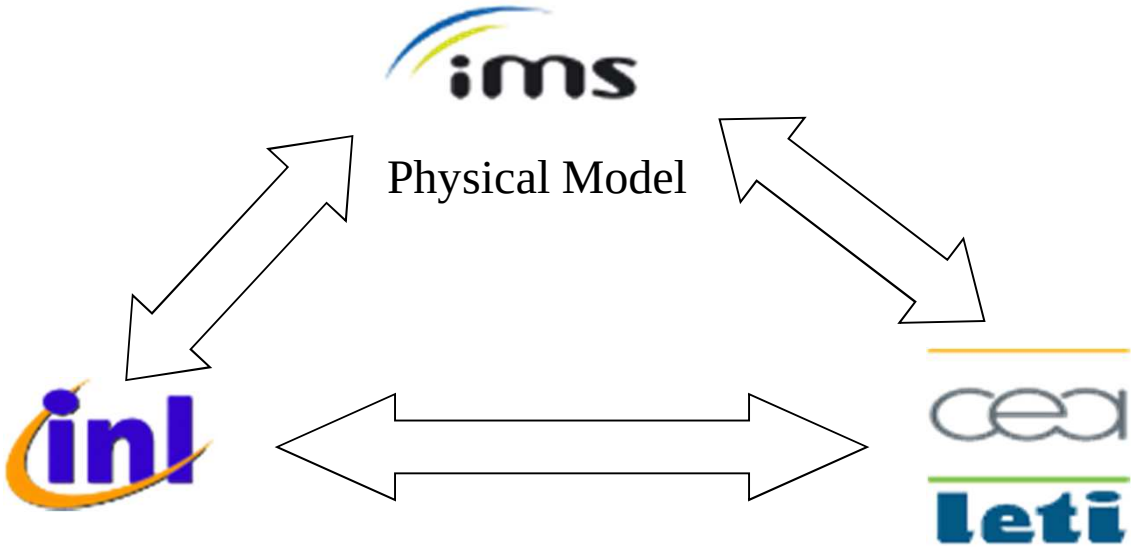


Lin et al., 2007

Low computing efficiency

NANOGRAIN Project

- Ultra-fine grain reconfigurable architectures based on nano-components



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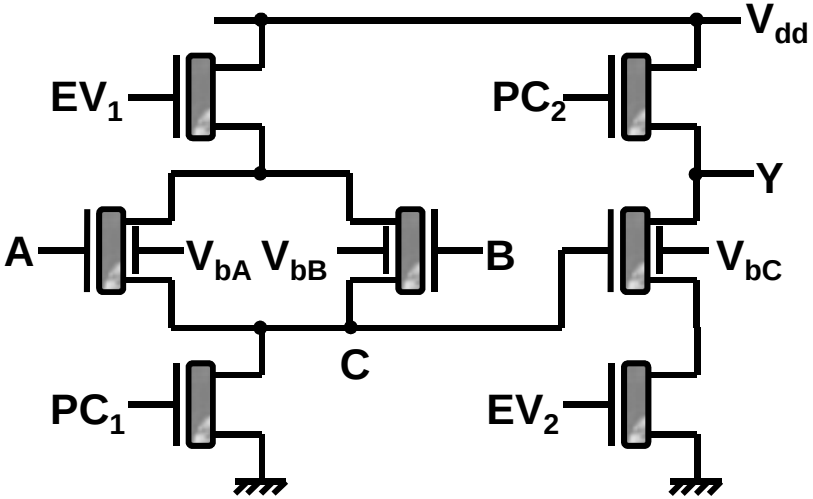
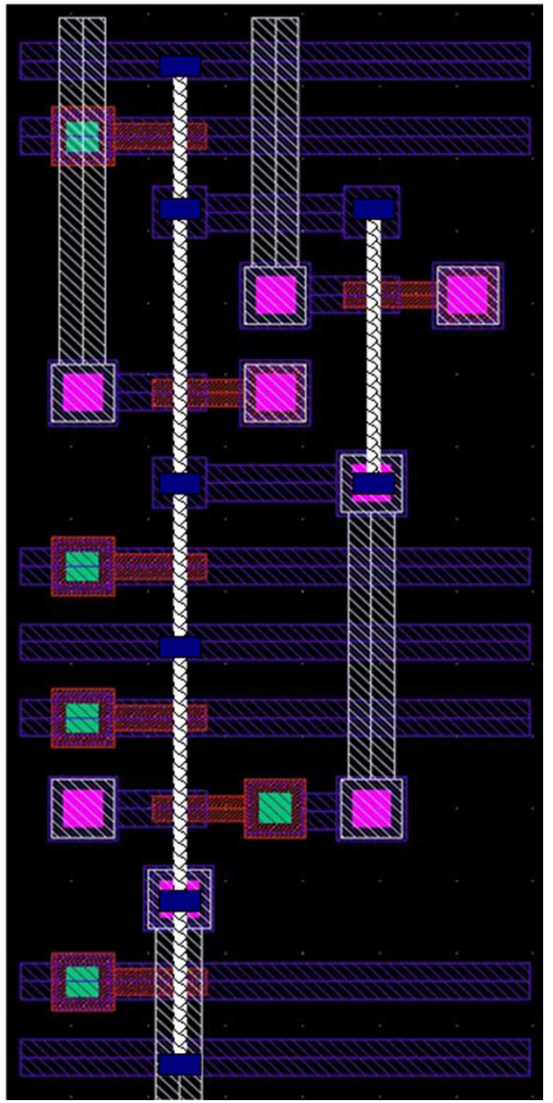
Objective

- Increase computing density for FPGA
- Leveraging on Ambipolar property of CNTFET
- (Questions on reconfigurable cell are for INL…)

DG-CNTFET logic cell

- Cell:





- Layout:

Extrapolation to 22nm

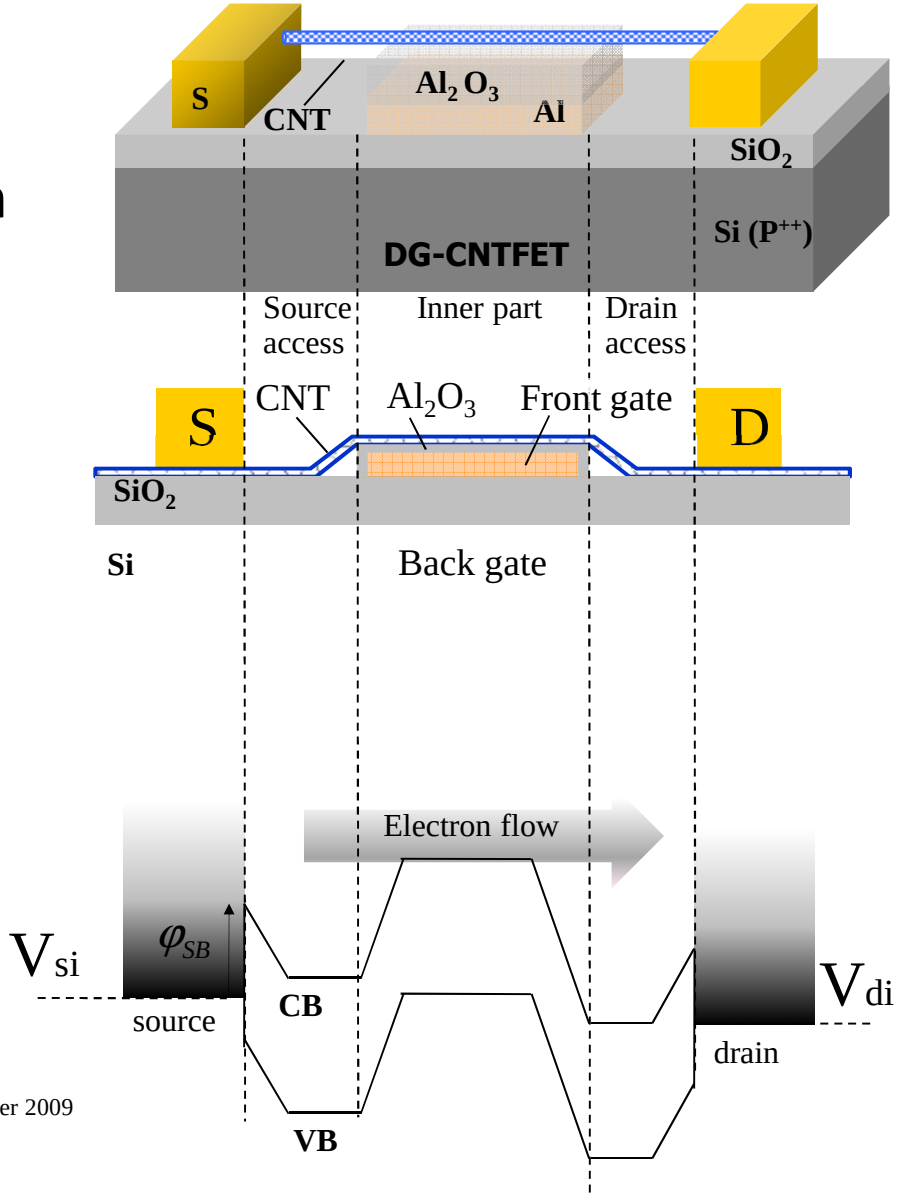
Consider NT alignement

DG-CNTFET Model

- Physical model
- Quasi-ballistic approach

=> Landauer equations

- Charges modeling
- Electrostatic modeling: front and back gates capacities
- Schottky and PN Junctions Capacities modeling (DIBL)



[1] S. Frégonèse, C. Maneux, T. Zimmer, IEEE TED, October 2009.
[2] S. Frégonèse, C. Maneux, T. Zimmer, IEEE ISDRS, Washington DC, December 2009
[3] S. Frégonèse, C. Maneux, T. Zimmer, SSE, accepted with revision

Results

	CMOS (ASIC)	DG-CNTFET	CB-NWFET
Functionality	1	0.875	1
Density	1	25.5	114,9
Performances	1	2,1	1,6
Power reduction	1	243.2	9.5

- Different choices possible depending on tradeoff : density versus power
  - DG-CNTFET → Power gain thanks to carbon electronic
  - CB-NWFET → Density gain thanks to sub-lithographic process

Outline

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- **Solving the interconnect issue**
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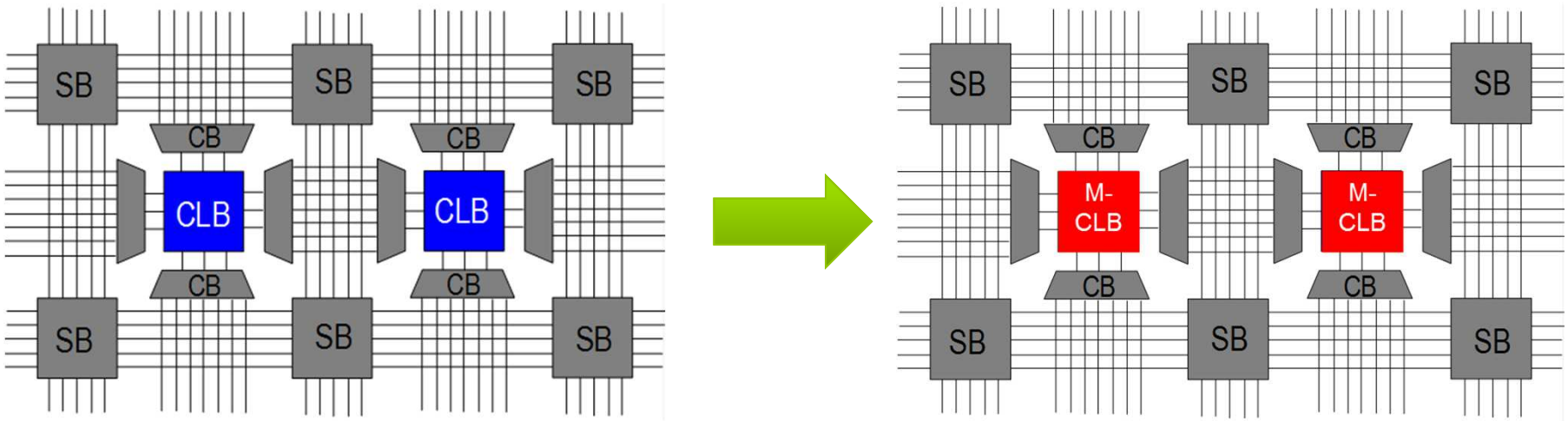
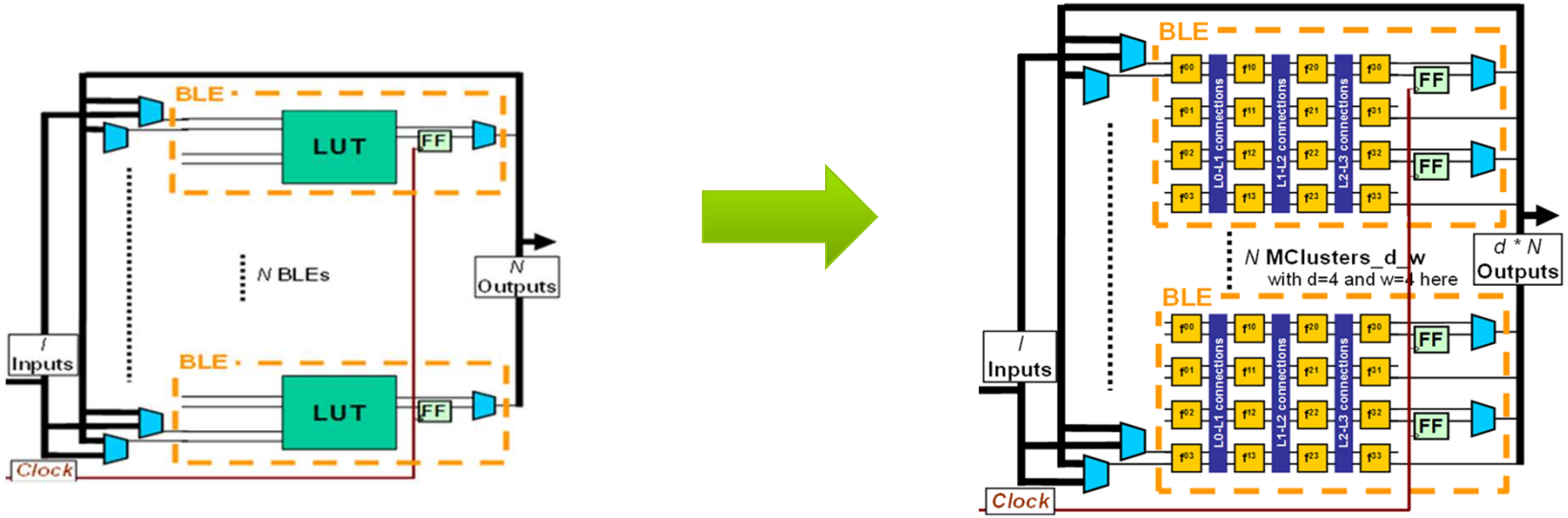
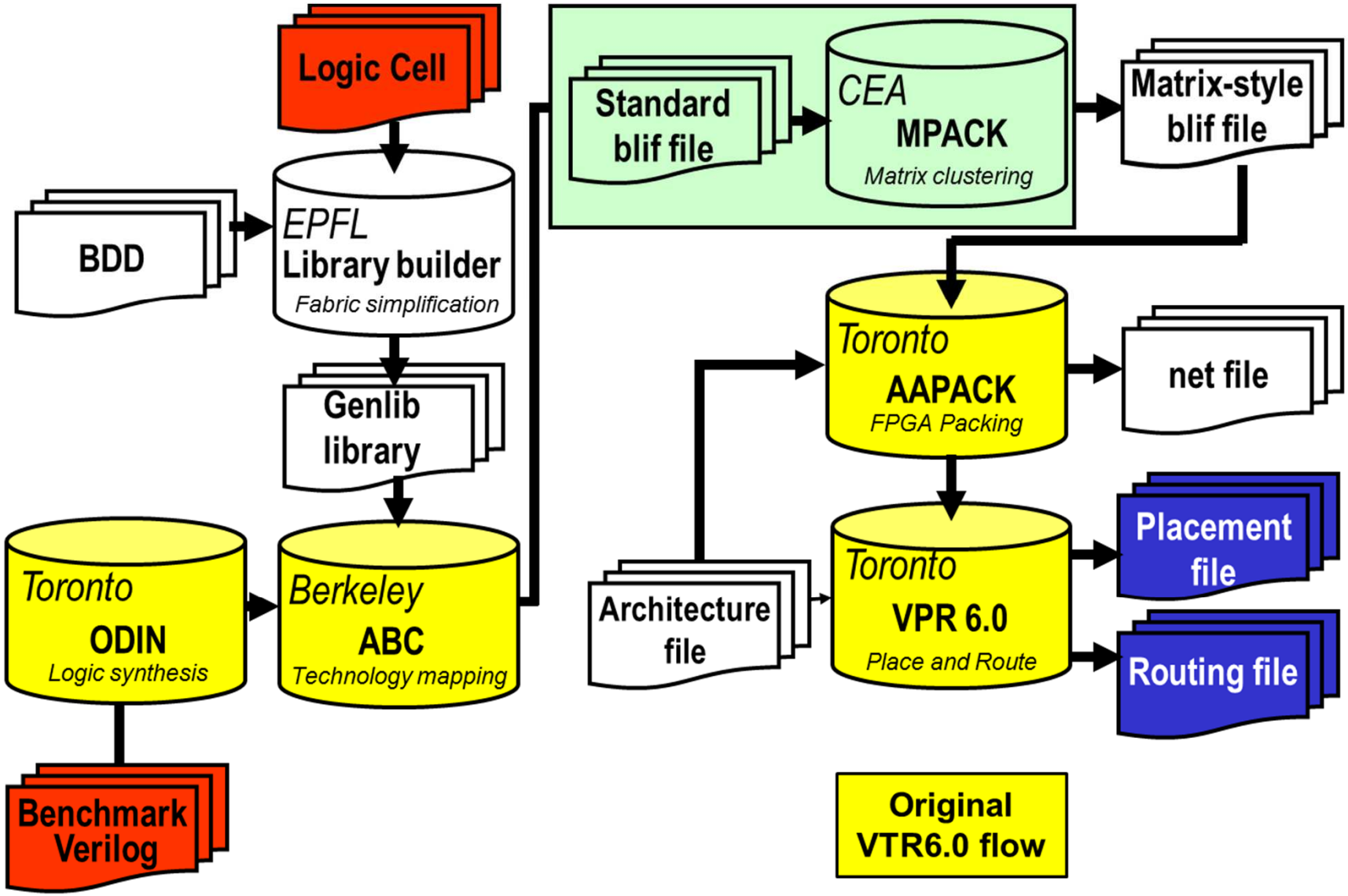
Main idea: modifying FPGA hierarchy

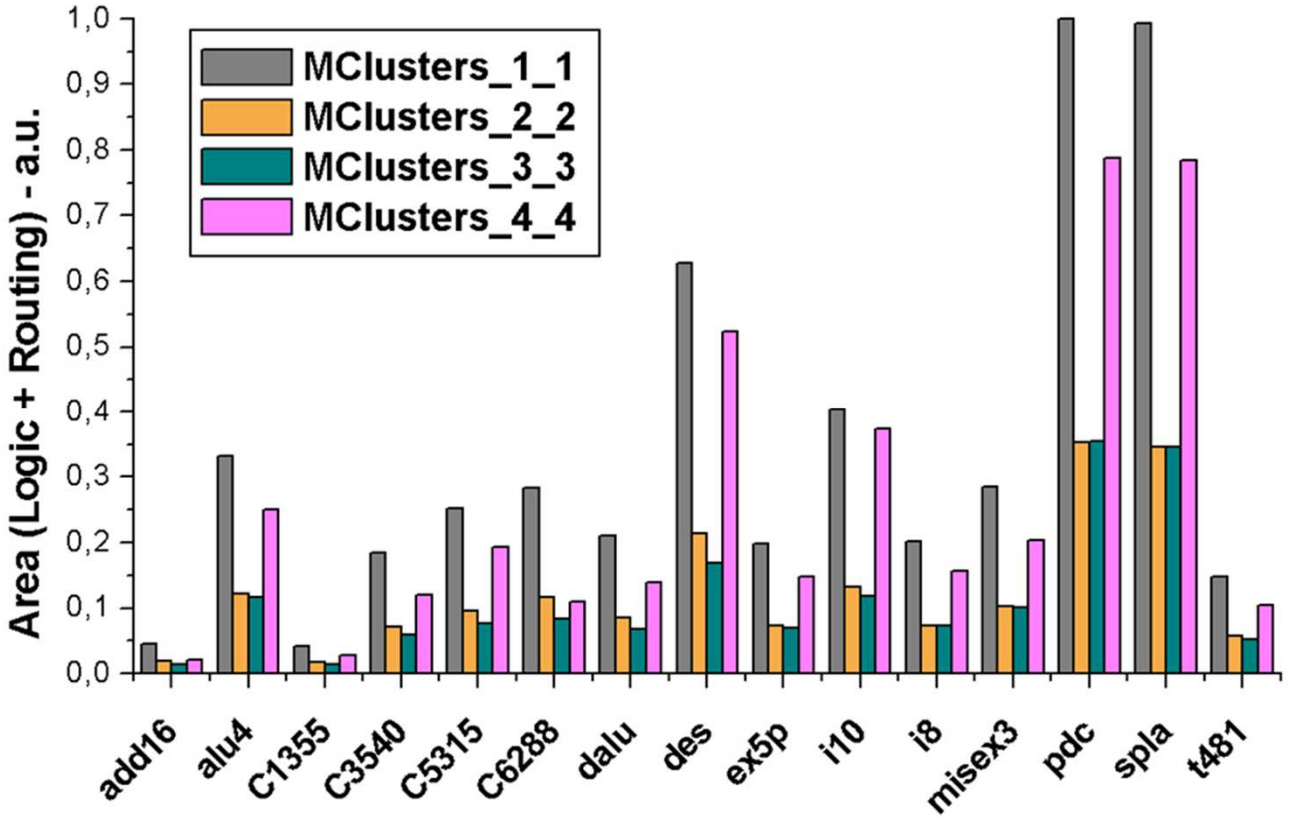




Benchmarking flow

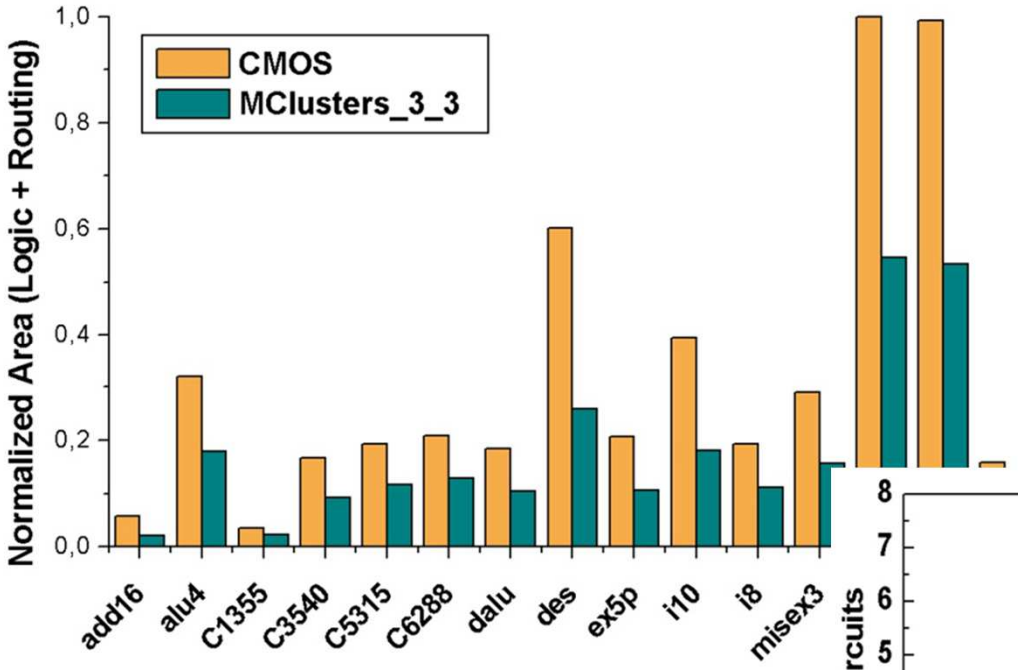


Results: Mcluster granularity



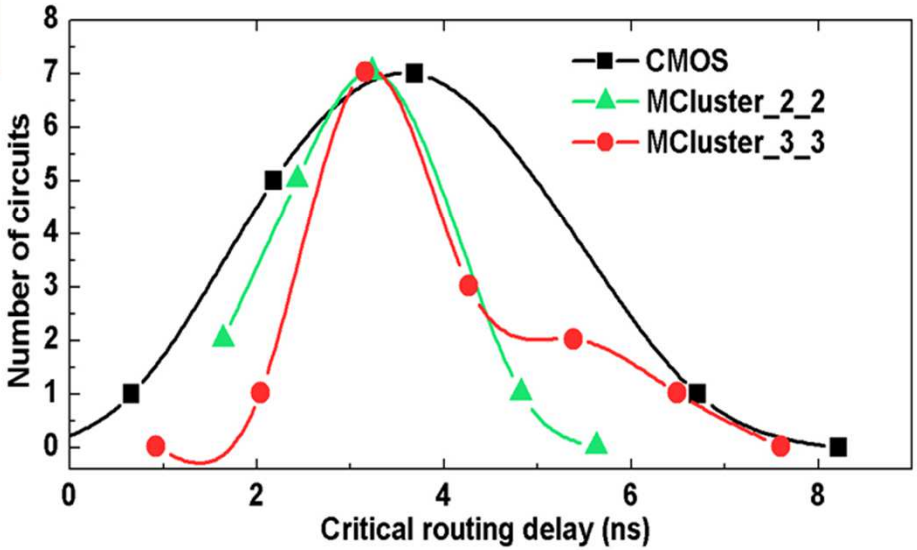
4-input LUTs, 10BLEs, 22 inputs

Results: gains versus CMOS



Gains versus CMOS

Mapping distribution



Conclusion

- Reconfigurable logic well suited for taking advantage of emerging technologies
- But need to re-think classical architectures
- … and now prototyping for convincing

Questions?

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