

## Publications (as of April 17, 2025)

### Books

1. G. De Micheli, A. Sangiovanni-Vincentelli and P. Antognetti, Editors, *Design Systems for VLSI Circuits: Logic Synthesis and Silicon Compilation*, Martinus Nijhoff, 1987.
2. D. Ku and G. De Micheli, *High-Level Synthesis of ASICs Under Timing and Synchronization Constraints*, Kluwer Academic Publishers, 1992.
3. G. De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994.
4. G. De Micheli and M. Sami, Editors, *Hardware/Software Co-design*, Kluwer Academic Publishers, 1996.
5. L. Benini and G. De Micheli, *Dynamic Power Management of Circuits and Systems: Design Techniques and CAD Tools*, Kluwer Academic Publishers, 1998.
6. G. De Micheli, R. Ernst and W. Wolf, *Readings in Hardware/Software Co-Design*, Morgan Kaufmann, 2001.
7. G. De Micheli and L. Benini *Networks on Chips* Morgan Kaufmann, 2006
8. G. De Micheli, Giovanni, S. Mir and R. Reis, Editors *VLSI-SoC: Research Trends in VLSI and Systems on Chip*, Springer 2008.
9. G. De Micheli, M. Gijs, Y. Leblebici and J. Vörös, Editors, *Nanosystems Design and Technology*, Springer, 2009.
10. A. Leblebici, P. Mayor, M. Rajman and G. De Micheli *Nano-Tera.ch - Engineering the Future of Systems for Health, Environment and Energy*. Springer, 2019.
11. C. Metzler, P.E. Gaillardon, G. De Micheli, C. Silva-Cardenas and R. Reis, Editors *VLSI-SOC: New Technology Enabler*, Springer, 2020

### Book Chapters (fully refereed)

12. G. De Micheli, M. Hofmann, A. R. Newton and A. Sangiovanni-Vincentelli, "A Design System for PLA-based Digital Circuits," in A. Sangiovanni-Vincentelli, Editor, *Advances in Computer Engineering Design*, Jai Press, 1985, pp. 285-364.
13. G. De Micheli, "Design of Control Systems," in G. De Micheli, A. Sangiovanni-Vincentelli and P. Antognetti, Editors, *Design Systems for VLSI Circuits: Logic Synthesis and Silicon Compilation*, Martinus Nijhoff, 1987, pp. 327-364 and *IBM Research Report*, No. RC 12062.
14. G. De Micheli, H.Y. Hsieh and I. Hajj, "Decomposition Techniques for Large Scale Circuits," in A. Ruehli, Editor, *VLSI Circuit Analysis, Simulation and Design*, North Holland, 1987, Vol. 2, pp. 1-39 and *IBM Research Report*, No. RC 11712.
15. R. Brayton, R. Camposano, G. De Micheli, R. Otten and J. Van Eijndhoven, "The Yorktown Silicon Compiler System," in D. Gajski, Editor, *Silicon Compilation*, pp. 204-310, Addison Wesley, 1988, and *IBM Report*, No. RC 12500.
16. M. Damiani and G. De Micheli, "Efficient Computation of the Exact and Approximate Observability Don't Care Sets in Multiple-Level Logic Synthesis," in P. Michel and G. Saucier, Editors, *Logic and Architecture Synthesis*, North Holland, 1991, pp. 209-218, and *CSL Report* CSL- TR-90-424.
17. D. Ku and G. De Micheli, "High-level Synthesis and Optimization Strategies in Hercules and Hebe," in P. Michel and G. Saucier, Editors, *Logic and Architecture Synthesis*, North Holland, pp. 111-120, 1991. (Cross-listed as Conference Proceedings No. 409.)
18. D. Ku and G. De Micheli, "Synthesis of ASICs with Hercules and Hebe," in R. Camposano and W. Wolf Editors, *Trends in High-Level Synthesis*, Kluwer, 1991, pp. 177-203 and *Stanford University Report*, CSL-TR-91-461, February 1991.
19. G. De Micheli, "High-Level Synthesis of Digital Circuits," in M. Yovits, Editor, *Advances in Computers*, Vol. 37, pp. 208-285, Academic Press, 1992 and *Stanford University Report*, CSL-TR-92-551, November 1992.
20. G. De Micheli, "Hardware/Software Co-design: Application Domains and Design Technologies," in G. De Micheli and M. Sami, Editors, *Hardware/Software Co-design*, Kluwer Academic Publishers, 1996, pp. 1-28.

21. C. Coelho and G. De Micheli, "Modeling and Synthesis of Synchronous System-Level Specifications," in J. Bergé, O. Levia and J. Rouillard, Editors, *Models in System Design*, Vol.9, Kluwer Academic Publishers, 1997, pp. 1-47.
22. G. De Micheli, L. Benini, and A. Bogliolo, "Dynamic Power Management of Electronic Systems," in A. Jerraya and J. Mermet, Editors *System-level Synthesis*, Kluwer, pp. 263-292, 1999.
23. G. De Micheli, "Cell-based logic optimization," in E. Boerger Editor *Architecture Design and Validation Methods*, Springer, pp.49-88, 2000.
24. L. Benini and G. De Micheli, "Logic Synthesis for Low Power," in S. Hassoun and T. Sasao, Editors, *Logic Synthesis and Verification*, Kluwer, pp. 197-223, 2002.
25. L. Benini and G. De Micheli, "Energy-efficient System-level design," in J. Rabaey and M. Pedram, Editors, *Power-Aware Design Methodologies*, Kluwer, pp. 473-516.
26. D. Bertozzi, L. Benini and G. De Micheli, "Error Control Schemes for On-chip Interconnection Networks: Reliability versus Energy Efficiency," in A. Jantsch and H. Tenhunen, Editors, *Networks on Chip*, Kluwer, 2003.
27. L. Benini and G. De Micheli, "Networks on Chip: A new paradigm for component-based MPSoC design," in A. Jerraya and W. Wolf Editors, *Multiprocessors Systems on Chips*, Morgan Kaufman, 2004, pp. 49-80.
28. L. Benini, D. Bertozzi and G. De Micheli, "Energy Efficient Network-on-chip Design," in E. Macii, Editor, *Ultra Low-Power Electronics and Design*, Kluwer, 2004, pp. 214-232.
29. D. Bertozzi, L. Benini and G. De Micheli, "Network-on-chip Design for Gigascale Systems-on-chip," in R. Zurawski, Editor, *Industrial Technology Handbook*, CRC Press, 2004, pp. 95-1, 95-18.
30. T. Ye, L. Benini and G. De Micheli, "Networks on Chips: Energy-efficient Design of SoC Interconnect," in C. Piguet Editor, *Low-Power Electronics Design*, CRC Press, 2004, pp. 30.1-30.16.
31. G. De Micheli, "Networking Chip Subsystems," in YearBook 2004, McGraw-Hill, pp. 224-226.
32. S. Yoon, L. Benini and G. De Micheli, "A Pattern-Mining Method for High-Troughput Lab-on-Chip Data Analysis", in K. Chakrabarty and J. Zeng Editors, *Design Automation Methods and Tools for Microfluidic-Based Chips*, Springer, 2006. (Cross-listed as Journal No. 135.)
33. F. Gilabert, D. Bertozzi, L. Benini and G. De Micheli, "Networks on chip: an interconnect Fabric for Multi-Processors Systems on Chip," in R. Zurawski Editors, *Embedded Systems Handbook*, CRC Press, 2008
34. G. De Micheli, "Nanosystems," in G. De Micheli, M. Gijs, Y. Leblebici and J. Vörös, Editors, *Nanosystems Design and Technology*, Springer, 2009.
35. H. Ben Jamaa, B. K. Boroujeni, G. De Micheli, Y. Leblebici, C. Piguet, A. Schmid, and M. Stanisavljevic, "Design Technologies for Nanoelectronic Systems Beyond Ultimately Scaled CMOS", in G. De Micheli, M. Gijs, Y. Leblebici and J. Vörös, Editors, *Nanosystems Design and Technology*, Springer, 2009.
36. V. Rana, D. Atienza, M. D. Santambrogio, D. Sciuto, and G. De Micheli, "A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication," in D. Soudris, C. Piguet, and R. Reis, Editors, *VLSI-SOC: Design Methodologies for SoC and SiP*, Vol. 1, pages 1-20. Springer, Boston, 2010.
37. C. Seiculescu, S. Murali, L. Benini and G. De Micheli. 3D Network on Chip Topology Synthesis: Designing Custom Topologies for Chip Stacks , in 3D Integration for NoC-based SoC Architectures, num. 3, p. 193-223, 2011.
38. C. Seiculescu, S. Murali, L. Benini and G. De Micheli. Design and Analysis of NoCs for Low-Power 2D and 3D SoCs , in Low Power Networks-on-Chip, num. 3, p. 199-222, 2011.
39. H. Ben Jamaa and G. De Micheli. Reliable Circuit Design with Nanowire Arrays, in Nanoelectronic Circuit Design, p. 153-188, 2011.
40. C. Baj-Rossi, G. De Micheli and S. Carrara. P450-Based Nano-Bio-Sensors for Personalized Medicine, in Biosensors for Health, Environment and Biosecurity, Book 1, 2011.
41. G. De Micheli, "Electronic Systems for Health Management, in S. Carrara and K. Iniewski Editors, *Handbook of Bioelectronics: Directly Interfacing Electronics and Biological Systems*, Part VIII, Chapter 42, p. 543-549, Cambridge Press, 2015.
42. A. Cavallini, C. Boero, G. De Micheli and S. Carrara. "CNT and proteins for bioelectronics in personalized medicine", in S. Carrara and K. Iniewski Editors, *Hand Book of Bioelectronics: Directly Interfacing Electronics and Biological Systems, Part II*, Chapter 9, p. 109-121, Cambridge Press, 2015.

43. X. Tang, S. Rahimian Omam, P. Meinerzhagen, P.-E. Gaillardon and G. De Micheli. "Low Power FPGAs based on Resistive Memories", in *Reconfigurable Logic: Architecture, Tools and Applications*, pp. 399-432, Devices, Circuits and Systems, 2015.
44. I. Taurino, A. Sanginario, G. De Micheli, D. Demarchi and S. Carrara. "Carbon Nanomaterials for Electrochemical and Electrochemiluminescent Medical Sensors", in *Carbon for Sensing Devices*, Chapter 6, pp. 133-152, 2015
45. P.-E. Gaillardon, J. Zhang, L. Amaru and G. De Micheli. "Multiple-Independent-Gate Nanowire Transistors: From Technology to Advanced SoC Design", in *Nano-CMOS and Post-CMOS Electronics: Devices and Modeling*, Volume 1, 2015.
46. H. Riener, R. Ehlers, B. Schmitt and G. De Micheli, "Exact Synthesis of ESOP Forms", in R. Dreschler and M. Soeken Editors, *Advanced Boolean Techniques*, Springer 2019.
47. I. Tzouvadaki, G. De Micheli and S. Carrara, "Memristive Biosensors for Ultrasensitive Diagnostics and Therapeutics," in M. Suri, Editor, *Applications of Emerging Memory Technology*, Springer 2019.
48. S.-Y. Lee, H. Riener, and G. De Micheli, "External Don't Cares in Logic Synthesis", in R. Drechsler and S. Huhn Editors, *Advanced Boolean Techniques* Springer 2023
49. R. Bairakulov, Alessandro Tempia Calvino and Giovanni De Micheli, Synthesis of SFQ Circuits with Compound Gates, in I. Elfadel and L. Albasha Editors, *VLSI-SoC 2023: Innovations for Trustworthy Artificial Intelligence*, Springer 2024.

#### Journals (fully refereed)

50. V. Amoia, G. De Micheli and M. Santomauro, "Computer Aided Formulation of Transition Rate Matrices via Kronecker Algebra," *IEEE Transactions on Reliability*, pp. 123-132, June 1981.
51. G. De Micheli and A. L. Sangiovanni-Vincentelli, "Characterization of Integration Algorithms for the Timing Analysis of MOS VLSI Circuits," *International Journal on Circuit Theory and Applications*, Vol. 10, pp. 299-309, October 1982.
52. G. De Micheli, "Progetto di Sistemi VLSI Assistito da Calcolatore," *PIXEL*, No.2, pp. 17-21, April 1982 (in Italian).
53. L. Dadda, G. De Micheli and M. G. Sami, "Prospettive di Sviluppo della Microelettronica. La Progettazione dei Circuiti VLSI," *L'Elettrotecnica*, Vol. 69, No. 7, pp. 613-622, July 1982 (in Italian).
54. G. De Micheli, A. Newton and A. Sangiovanni-Vincentelli, "Symmetric Displacement Algorithms for the Timing Analysis of Large Scale Circuits," *IEEE Transactions on CAD/ICAS*, Vol. 2, No. 3, pp. 167-180, July 1983.
55. G. De Micheli and M. Santomauro, "SMILE: A Computer Program for Partitioning of Programmed Logic Array," *Computer Aided Design*, No. 2, pp. 89-97, March 1983 and *Memorandum UCB/ERL*, No. 82/74.
56. G. De Micheli and A. Sangiovanni-Vincentelli, "Multiple Constrained Folding of Programmable Logic Arrays: Theory and Applications," *IEEE Transactions on CAD/ICAS*, Vol. 2, No. 3, pp. 151-167, July 1983, and *Memorandum UCB/ERL*, No. 82/57.
57. G. De Micheli and A. Sangiovanni-Vincentelli, "PLEASURE: A Computer Program for Simple-Multiple Constrained-Unconstrained Folding of Programmable Logic Arrays," *Computer Aided Design*. No. 1, pp. 2-12, January 1984. (Cross-listed as Conference Proceedings No. 387.)
58. G. De Micheli, R. Brayton and A. Sangiovanni-Vincentelli, "Optimal State Assignment for Finite State Machines," *IEEE Transactions on CAD/ICAS*, Vol. CAD-4, No. 3, pp. 269-284, July 1985 and *IBM Research Report*, No. RC 10599.
59. G. De Micheli, "Symbolic Design of Combinational and Sequential Circuits Implemented by Two-level Logic Macros," *IEEE Transactions on CAD/ICAS*, October 1986, pp. 597-616 and *IBM Research Report*, No. RC 11672 and reprinted in A. R. Newton, Editor, *Logic Synthesis for Integrated Circuit Design*, IEEE Press, pp. 84-103, 1987. (IEEE/CAS 1986 CAD-Transactions Best Paper Award.)
60. G. De Micheli, "Performance-Oriented Synthesis of Large Scale Domino CMOS Circuits," *IEEE Transactions on CAD/ICAS*, Vol. CAD-6, No. 5, pp. 751-765, September 1987 and *Stanford University Report*, CSL-TR-87-330, May 1987.
61. G. De Micheli, "Computer Aided Design and Optimization of Control Units for VLSI Processors," *International Journal of Circuit Theory and Applications*, Vol. 16, pp. 347-369, October 1988, and *Stanford University Report*, No. CSL-TR-88-356.

62. G. De Micheli, D. Ku, F. Mailhot, and T. Truong, "The Olympus Synthesis System for Digital Design," *IEEE Design & Test*, pp. 37-53, October 1990.
63. G. De Micheli, "Synchronous Logic Synthesis: Algorithms for Cycle-Time Minimization," *IEEE Transactions on CAD/ICAS*, Vol 10, No. 1, pp. 63-73, January 1991.
64. D. Ku, and G. De Micheli, "Optimal Synthesis of Control Logic from Behavioral Specifications," *Integration: the VLSI Journal*, Vol. 10, No.3, pp. 271-298, February 1991, and *Stanford Report CSL-TR-89-402*, November 1989.
65. P. Song, and G. De Micheli, "Circuit and Architecture Trade-offs for High-Speed Multiplication," *IEEE Journal on Solid State Circuits*, Vol. 26, No. 9, pp. 1184-1198, September 1991.
66. D. Ku and G. De Micheli, "Constrained Resource Sharing and Conflict Resolution in Hebe," *Integration: the VLSI Journal*, Vol. 12, No. 2, December 1991, pp. 131-166.
67. D. Ku and G. De Micheli, "Relative Scheduling Under Timing Constraints: Algorithms for High-Level Synthesis of Digital Circuits," *IEEE Transactions on CAD/ICAS*, Vol. 11, No. 6, June 1992, pp. 696-718.
68. D. Wong, G.De Micheli and M.Flynn, "A Bipolar Population Counter using Wave Pipelining to Achieve a 2.5X Normal Clock Frequency," *IEEE Journal on Solid State Circuits*, Vol. 27, No. 5, pp. 745-753, May 1992.
69. D. Filo, D. Ku and G. De Micheli, "Optimizing Control Through the Resynchronization of Operations," *Integration: the VLSI Journal*, Vol. 13, No. 3, pp.231-258, 1992 and *CSL Report*, CSL-TR-91-494, 1991.
70. D. Wong, G.De Micheli and M.Flynn, "Algorithms for Designing High-Performance Digital Circuits Using Wave Pipelining," *IEEE Transactions on CAD/ICAS*, Vol. 12, No. 1. January 1993, pp. 25-46.
71. M. Damiani and G. De Micheli, "Don't Care Specifications in Combinational and Synchronous Logic Circuits," *IEEE Transactions on CAD/ICAS*, Vol.12, No. 3, March 1993, pp. 365-388 and *CSL Report*, CSL-TR-92-531, 1992.
72. R. Gupta and G. De Micheli, "Hardware-Software Co-synthesis for Digital Systems," *IEEE Design & Test*, Vol. 10, No. 3, pp. 29-41, September 1993.
73. F.Mailhot and G. De Micheli, "Algorithms for Technology Mapping Based on Binary decision Diagrams and on Boolean Operations," *IEEE Transactions on CAD/ICAS*, Vol. 12, No. 5, May 1993, pp.599-620, *CSL Report*, CSL-TR-91-486, 1991.
74. G.De Micheli "Optimization of Sequential Synchronous Digital Circuits using Structural Models," *IEICE Transactions on Information and Systems*, Vol E76-D, No. 9, September 1993, pp. 1018-1029.
75. D.Filo, D. Ku, C.Coelho and G.De Micheli, "Interface Optimization for Concurrent Systems Under Timing Constraints," *IEEE Transactions on VLSI*, Vol.1, No. 3, pp. 268-281, September 1993.
76. R. Gupta, C. Coelho and G. De Micheli, "Program Implementation Schemes for Hardware-Software Systems," *IEEE Computer*, Vol. 27, No. 1, January 1994, pp. 48-55. (Cross-listed as Workshop Proceedings No. 899.)
77. G. De Micheli, "Computer-Aided Hardware/Software Co-design," *IEEE Micro*, pp.11-16, August 1994.
78. L. Benini, P. Siegel and G. De Micheli "Saving Power by Synthesizing Gated Clocks for Sequential Circuits," *IEEE Design & Test*, Winter 1994, pp. 32-41.
79. G.De Micheli, M.G.Sami and D.Sciuto, "Progetto di Sistemi Digitali Dedicati," *Automazione e Strumentazione*, No. 2, February 1995, pp. 35-39 (in Italian).
80. L.Benini and G. De Micheli "State Assignment for Low Power Dissipation," *IEEE Journal of Solid State Circuits*, Vol. 30, No. 3, pp. 258-268, March 1995.
81. G. De Micheli, "A Survey of Problems and Methods for Computer-Aided Hardware/Software Co-design," *Journal of Information Processing Society of Japan*, Vol. 37, No. 7, pp. 605-613, July 1995. (In Japanese: translation of Conference Proceedings No. 77 ).
82. R. Gupta and G. De Micheli "A Co-synthesis Approach to Embedded Systems Design Automation," *Design Automation of Embedded Systems*, Vol 1, No. 2, January 1996, pp. 69-120.
83. M. Damiani, J. Yang and Giovanni De Micheli "Optimization of Combinational Logic Circuits based on Compatible Gates," *IEEE Transactions on CAD/ICAS*, Vol.14, No. 11, November 1995, pp. 1316-1327.
84. J. Yang, G. De Micheli and M. Damiani, "Scheduling and Control Generation with Environmental Constraints," *IEEE Transactions on CAD/ICAS*, Vol. 15, No. 2, February 1996, pp.166-183.

85. L. Benini and G. De Micheli "Transformation and Synthesis of FSMs for Low-Power Gated-Clock Implementation," *IEEE Transactions on CAD/ICAS*, Vol. 15, No. 6, June 1996, pp. 630-643.
86. C.Coelho and G.De Micheli, "Analysis and Synthesis of Concurrent Digital Circuits Using Control-Flow Expressions," *IEEE Transactions on CAD/ICAS*, Vol. 15, No. 8, August 1996, pp. 854-876, and *CSL Report*, CSL-TR-96-694, 1996.
87. G. De Micheli "Progetto Concorrente di Hardware e Software," *Alta Frequenza*, Vol. 8, No. 3, May-June 1996, Vol.8, No.3, pp. 39-43 (in Italian).
88. R. Gupta and G. De Micheli, "Hardware/Software Co-design," *IEEE Proceedings*, Vol. 85, No. 3, March 1997, pp.349-365.
89. L. Benini, A. Bogliolo, P. Vuillod and G. De Micheli, "Clock Skew Optimization for Peak Current Reduction," *Journal of VLSI Signal Processing Systems*, Vol. 16, Issues 2 & 3, June 1997, pp.5-18.
90. R. Gupta and G. De Micheli, "Specification and Analysis of Timing Constraints for Embedded Systems", *IEEE Transactions on CAD/ICAS*, Vol. 16, No.3, pp. 240-256, March 1997.
91. R. Gupta and G. De Micheli, "Constrained Software Synthesis for Embedded Applications", *Journal of System Architecture*, Vol. 43, No.8, May 1997, pp 557-586.
92. A. Bogliolo, L.Benini, G. De Micheli and B. Riccò, "Gate-Level Power and Current Simulation of CMOS Integrated Circuits," *IEEE Transactions on VLSI*, Vol.5, No.4, December 1997, pp.473-488.
93. L. Benini and G. De Micheli, "A Survey of Boolean Matching Techniques for Library Binding," *TODAES, ACM Transactions on Design Automation of Electronic Systems*, Vol. 2, No. 3, July 1997, pp. 193-226.
94. L. Benini, E. Macii, M. Poncino and G. De Micheli, "Telescopic Units: A New Paradigm for Performance Optimization of VLSI Designs," *IEEE Transactions on CAD/ICAS*, Vol. 17, No. 3, March 1998, pp.220-231.
95. L. Benini, P. Vuillod and G. De Micheli, "Iterative re-mapping for logic circuits," *IEEE Transactions on CAD/ICAS*, Vol. 17, No. 10, October 1998, pp. 948-964.
96. L. Benini, A. Bogliolo, M. Favalli and G. De Micheli, "Regression Models for behavioral Power Estimation", *Integrated Computer-Aided Engineering*, Vol. 5, No. 2, 1998, pp. 95-106.
97. L. Benini, G. De Micheli, E. Macii, M. Poncino and S. Quer, "Power Optimization of Core-Based Systems by Address Bus Encoding," *IEEE Transactions on VLSI*, Vol. 6, No. 4, December 1998, pp. 554-562.
98. H. Kapadia, L. Benini and G. De Micheli, "Reducing Switching Activity on Datapath Buses with Control-Signal Gating," *IEEE Solid State Journal*, Vol. 34, No. 3, March 1999, pp. 405-414.
99. L. Benini, A. Bogliolo, G. Paleologo and G. De Micheli, "Policy Optimization for Dynamic Power Management," *IEEE Transactions on CAD*, Vol. 18, No. 6, June 1999, pp. 813-833.
100. L. Benini, G. De Micheli, A. Liroy, E. Macii, G. Odasso and M. Poncino, "Automatic Synthesis of Large Telescopic Units Based on Near-Minimum Timed Supersampling," *IEEE Transactions on Computers*, Vol. 48, No. 8, August 1999, pp. 769-779.
101. A. Bogliolo, L. Benini, B. Riccò and G. De Micheli, "Controllo Dinamico del Consumo di Potenza in Sistemi a Microprocessore," *Alta Frequenza*, Vol. 11, No. 1, Gennaio-Marzo 1999, pp. 29-41 (In Italian).
102. L. Benini, G. De Micheli, E. Macii, M. Poncino, R. Scarsi, "Symbolic Synthesis of Clock-Gating Logic for Power Optimization of Synchronous Networks," *TODAES, ACM Transaction on Design Automation of Electronic Systems.*, Vol.4, No.4, October 1999 , pp. 351-375.
103. L. Benini, G. De Micheli, E. Macii, M. Poncino, R. Scarsi "A Multi-Level Engine for Fast Power Simulation of Realistic Input Streams," *IEEE Transactions on CAD/ICAS*, Vol. 18, No. 4, pp. 459-472, April 2000.
104. L. Benini, G. De Micheli, A. Macii, E. Macii, M. Poncino, "Automatic selection of instruction op-codes of low-power core processors," *IEE Proceedings. Computers and Digital Techniques*, vol. 146, no. 4, pp. 173-178, July 1999.
105. L. Benini, G. De Micheli, A. Macii, E. Macii, M. Poncino and R. Scarsi, "Glitch Power Minimization by Selective Gate Freezing," *IEEE Transactions on VLSI*, pp.287-298, June 2000.
106. L. Benini, A. Bogliolo and G. De Micheli, "A Survey of Design Techniques for System-Level Dynamic Power Management," *IEEE Transactions on VLSI*, June 2000, pp. 299-316.
107. L. Benini and G. De Micheli "System-Level Power Optimization: Techniques and Tools," *TODAES, ACM Transactions on Design Automation of Electronic Systems*, Vol.5, No . 2, pp.115-192, April 2000.

108. L. Benini, and G. De Micheli, "Synthesis of Low-Power Selectively-Clocked Systems from High-Level Specifications," *TODAES, ACM Transactions on Design Automation of Electronic Systems*, Vol.5, No. 3, July 2000, pp. 311-321.
109. A. Bogliolo, L. Benini and G. De Micheli, "Regression-Based Behavioral Power Modeling," *TODAES, ACM Transactions on Design Automation of Electronic Systems*, Vol.5, No. 3, July 2000, pp. 337-372.
110. L. Séméria and G. De Micheli, "Resolution, Optimization and Encoding of Pointer Variables for the Behavioral Synthesis from C," *IEEE Transactions on CAD/ICAS*, February 2001, pp. 213-233.
111. L. Benini, E. Macii and G. De Micheli, "Designing Low Power Circuits: Practical Recipes", *IEEE Circuit and System Magazine*, Vol. 1, No. 1, First Quarter 2001, pp. 6-25.
112. V. Mooney and G. De Micheli, "Hardware/Software Co-Design of Run-Time Schedulers for Real-Time Systems," *Design Automation of Embedded Systems*, Vol. 6, No. 1, pp. 89-144, September 2000.
113. T. Šimunić, L. Benini and G. De Micheli, "Energy-Efficient Design of Battery-Powered Systems," *IEEE Transactions on VLSI*, Vol. 9, No. 1, pp. 15-28, February 2001.
114. Y.-H. Lu and G. De Micheli, "Comparing System-Level Power Management Policies," *IEEE Design and Test*, Vol. 18, No. 2, pp. 10-19, March-April 2001.
115. L. Benini, G. De Micheli, A. Liyo, E. Macii, G. Odasso, M. Poncino, "Synthesis of Power-Managed Sequential Components Based on Computational Kernel Extraction," *IEEE Transactions on CAD/ICAS*, September 2001, pp. 1118-1131.
116. T. Šimunić, L. Benini, P. Glynn, G. De Micheli, "Event-driven Power Management," *IEEE Transactions on CAD/ICAS*, Vol. 20, No. 7, pp. 840-857, July 2001
117. L. Séméria, K. Sato and G. De Micheli, "Synthesis of Hardware Models in C with Pointers and Complex Data Structures," *IEEE Transactions on VLSI*, Vol.9, No. 6, pp.743-756, December 2001.
118. J. Smith and G. De Micheli, "Polynomial Circuit Models for Component Matching in High-Level Synthesis," *IEEE Transactions on VLSI*, Vol.9, No. 6, pp. 783-800, December 2001.
119. L. Benini and G. De Micheli "Networks on Chips: A New SoC Paradigm," *IEEE Computers*, January 2002, pp. 70-78.
120. Y. Lu, L. Benini and G. De Micheli "Power Aware Operating Systems for Interacting Systems," *IEEE Transactions on VLSI*, April 2002, pp. 119-134.
121. E.Y. Chung, L. Benini, G. De Micheli, G. Luculli and M. Carilli, "Value-sensitive Automatic Code Specialization for Embedded Software," *IEEE Transactions on CAD/ICAS*, Vol. 21, No.9, September 2002, pp. 1051-1067. (Cross-listed as Other 918.)
122. E.Y. Chung, L. Benini, A. Bogliolo and G. De Micheli "Dynamic Power Management for Non-Stationary Service Requests," *IEEE Transactions on Computers*, Vol 51, No. 11, November 2002, pp. 1345-1361.
123. Y. Lu, L. Benini, and De Micheli, "Dynamic Frequency Scaling with Buffer Insertion for Mixed Workloads," *IEEE Transactions on CAD/ICAS*, Vol. 21, No. 11, November 2002, pp. 1284-1305.
124. A. Peymandoust, T. Šimunić and G. De Micheli, "Complex Instruction and Software Library Mapping for Embedded Software Using Symbolic Algebra," *IEEE Transactions on CAD/ICAS*, Vol. 22, No. 8, August 2003, pp. 964-975.
125. A. Peymandoust G. De Micheli, "Application of Symbolic Computer Algebra in High-Level Data-Flow Synthesis," *IEEE Transactions on CAD/ICAS*, Vol. 22, No. 9, September 2003, pp.1154-1165.
126. A. Bogliolo, L. Benini, E. Lattanzi and G. De Micheli, "Specification and Analysis of Power-Managed Systems," *IEEE Proceedings*, Vol. 92, No. 8, August 2004, pp. 1306-1346.
127. F. Worm, P. Ienne, P. Thiran and G. De Micheli, "On-chip Self-calibrating Communication Robust to Electrical Parameter Variations," *IEEE Design and Test*, Vol. 21, No. 6, pp. 524-535, Nov/Dec 2004.
128. T. Ye, L. Benini and G. De Micheli, "Packetization and Routing Analysis of On-Chip Multiprocessor Networks," *JSA - Journal of System Architecture*, Vol 50, February 2004, pp. 81-104
129. F. Worm, P. Ienne, P. Thiran and G. De Micheli, "A Robust Self-calibrating Transmission Scheme for On-chip Networks," *IEEE Transactions on VLSI*, Vol. 13, No. 1, January 2005, pp. 126-139.
130. D. Bertozzi, A. Jalabert, S. Murali, R. Tamhankar, S. Stergiou, L. Benini, G. De Micheli, "NoC Synthesis Flow for Customized Domain Specific Multiprocessor Systems-on-Chip", *IEEE Transactions on Parallel and Distributed Systems*, Vol. 16, No. 2, February 2005, pp. 113-129.

131. D.Bertozzi, L.Benini, G. De Micheli, "Error control schemes for on-chip communication links: the energy - reliability trade-off," *IEEE Transactions on CAD*, Vol. 24, No. 6, pp.818-831, 2005.
132. S. Murali, T. Theocharides, N. Vijaykrishnan, M.J. Irwin, L. Benini and G. De Micheli, "Analysis of Error Recovery Schemes for Networks on Chips", *IEEE Design and test of Computers*, Vol. 22, No. 5, September 2005, pp. 434-442.
133. P. Pande, C. Grecu, A. Inavnov, R. Saleh and G. De Micheli, "Design, Synthesis and Test of Networks on Chips", *IEEE Design and Test of Computers*, Vol. 22, No. 5, September 2005, pp. 404-413.
134. S. Yoon, C. Nardini, L. Benini and G. De Micheli, "Discovering Coherent Biclusters from Gene Expression Data Using Zero-Suppressed Binary Decision Diagram", *IEEE Transactions on Computational Biology and Bioinformatics*, Vol. 2, No. 4, pp. 339-354, 2005.
135. S. Yoon, L. Benini and G. De Micheli, "A Pattern-Mining Method for High-Throughput Lab-on-Chip Data Analysis", *IEEE Transactions on CAD*, Vol. 25, No. 2, February 2006, pp. 353-380. (Cross-listed as Book Chapters No. 32.)
136. A. K. Coskun, T. Simunic Rosing, K. Mihic, G. De Micheli, and Y. Leblebici, "Analysis and Optimization of MPSoC Reliability," *J. Low Power Electronics*, vol. 2, no. 1, pp. 56-69, 2006.
137. S. Yoon and G. De Micheli, "Computational Identification of MicroRNAs and their Targets," *Birth Defects Research*, Vol. 78, No. 2, pp. 118-128, June 2006.
138. C. Nardini, L. Benini, and G. De Micheli, "Circuits and Systems for High-Throughput Biology," *IEEE Circuits and Systems*, pp. 10-20, 2006.
139. S. Carrara, F. Grkaynak, C. Guiducci, C. Stagni, L. Benini, Y. Leblebici, B. Samor, and G. De Micheli, "Interface Layering Phenomena in Capacitance Detection of DNA with Biochips," *Sensors & Transducers Journal*, vol. 76, no. 2, pp. 969-977, 2007.
140. K. Mihic, T. Simunic and G. De Micheli, "Power and Reliability Management of SoCs", *IEEE Transactions on VLSI*, Vol. 15, No.4, pp.391-403.
141. S. Yoon, J. C. Ebert, E.-Y. Chung, G. De Micheli, and R. B. Altman. "Clustering protein environments for function prediction: finding PROSITE motifs in 3D". *BMC Bioinformatics*, 2007, 8(Suppl 4):S10 (22 May 2007)
142. S. Murali, L. Benini and G. De Micheli, "An Application-Specific Design Methodology for On-chip Crossbar Generation", *IEEE Transactions on CAD*, Vol. 26, No.7, pp. 1283-1296, 2007.
143. R. Tamhankar, S. Murali, S. Stergiou, A. Pullini, F. Angiolini, L. Benini and Giovanni De Micheli, "A Timing Error Tolerant Design Methodology for Networks on Chips", *IEEE Transactions on CAD*, Vol. 26, No.7, pp. 1297, 1310, 2007.
144. S. Murali, P. Meloni, D. Atienza, S. Carta, L. Benini, G. De Micheli, and L. Raffo. "Synthesis of Predictable Networks-on-Chip Based Interconnect Architectures for Chip Multi-Processors", *IEEE Transactions on VLSI*, 2007, Vol. 15, No. 8, pp. 869-880, August 2007.
145. D. Atienza, P. Del Valle, G. Paci, F. Poletti, L. Benini, G. De Micheli, J. Mendias and R. Hermida, "HW-SW Emulation Framework for Temperature-Aware Design in MPSoCs", *ACM Transactions on Design Automation for Embedded Systems (TODAES)*, Vol. 12, Nr. 3, pp. 1-26, August 2007.
146. A. E. Susu, M. Magno, A. Acquaviva, D. Atienza, and G. De Micheli, "Reconfiguration Strategies for Environmentally Powered," *Transaction on HiPEAC-1, Lecture Notes in Computer Science (LNCS)*, vol. 4050, Springer-Verlag Berlin Heidelberg New York, no. ISBN: 978-3-540-71527-6, ISSN: 0302-9743, pp. 341-360, 2007.
147. S. Yoon, J. Ebert C, E.-Y. Chung, G. De Micheli, and Altman B, "Clustering protein environments for function prediction: finding PROSITE motifs in 3D," *BMC Bioinformatics*, vol. ISSN 1471-2105, no. 8 (Suppl 4):S10 (22 May 2007), pp. doi:10.1186/1471-2105-8-S4-S10, 2007.
148. N. Genko, D. Atienza, G. De Micheli, and L. Benini, "NoC emulation: a tool and design flow for MPSoC," *Circuits and Systems Magazine, IEEE*, vol. 7, no. issue 4, pp. 42 - 51, 2007.
149. A. Pullini, F. Angiolini, S. Murali, D. Atienza, G. De Micheli, and L. Benini, "Bringing NoCs to 65nm," *IEEE Micro Magazine*, vol. 12, no. 5, September/October, pp. 75 - 85, ISSN: 0272-1732, 2007.
150. A. Di Cara, A. Garg, G. De Micheli, I. Xenarios, and L. Mendoza, "Dynamic simulation of regulatory networks using SQUAD," *BMC Bioinformatics* no. 8:462, 2007.
151. S. Yoon, L. Benini and G. de Micheli, "Co-clustering: A versatile Tool for Data Analysis in Biomedical Informatics", *IEEE Transactions on Information Technology in Biomedicine*, Vol 11, No. 4, pp. 493-494, 2007

152. S. Murali, D. Atienza, L. Benini, and G. De Micheli. "A Method for Routing Packets Across Multiple Paths in NoCs with In-Order Delivery and Fault-Tolerance Guarantees", *VLSI-Design Journal*, Hindawi Publications, 2007.
153. D. Atienza, F. Angiolini, S. Murali, A. Pullini, L. Benini, and G. De Micheli, "Network-On-Chip Design and Synthesis Outlook," *Integration-The VLSI Journal*, 41(2, February, ISSN: 0167-9260), 2008.
154. D. Atienza, P. Raghavan, J.-L. Ayala, G. De Micheli, F. Catthoor, D. Verkest, and M. Lopez-Vallejo, "Joint Hardware-Software Leakage Minimization Approach for the Register File of VLIW Embedded Architectures," *Integration-The VLSI journal, Elsevier Science* vol. 41, no. 1, pp. 38-48, 2008.
155. A. Garg, A. Di Cara, I. Xenarios, L. Mendoza, and G. De Micheli, "Synchronous versus asynchronous modeling of gene regulatory networks," *BIOINFORMATICS*, vol. 24, no. 17, pp. 1917-1925, 2008.
156. M. H. Ben Jamaa, K. E. Moselund, D. Atienza, D. Bouvet, Ionescu Adrian M, Y. Leblebici, and G. De Micheli, "Variability-Aware Design of Multilevel Logic Decoders for Nanoscale Crossbar Memories," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 11, pp. 2053-2067, 2008.
157. K. E. Moselund, D. Bouvet, M. H. Ben Jamaa, D. Atienza, Y. Leblebici, G. De Micheli, and M. A. Ionescu, "Prospects for logic-on-a-wire," *Microelectronic Engineering*, vol. 85, no. 5-6, pp. 1406-1409, 2008.
158. E. Ficarra, G. De Micheli, S. Yoon, L. Benini, and E. Macii, "Joint co-clustering: Co-clustering of genomic and clinical bioimaging data," *Computers & Mathematics With Applications*, vol. 55, pp. 938-949, 2008.
159. A. Mutapcic, S. Boyd, S. Murali, D. Atienza, G. De Micheli, and R. Gupta, "Processor Speed Control with Thermal Constraints," *IEEE Transactions on Circuits and Systems I*, Vol. 56, No. 9, pp. 1994-2007, September 2009.
160. G. De Micheli, "An Outlook on Design Technologies for Future Integrated Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 28, No. 6, pp. 777-790, 2009.
161. F. Mulas, D. Atienza, A. Acquaviva, S. Carta, L. Benini, and G. De Micheli, "Thermal Balancing Policy for Multiprocessor Stream Computing Platforms," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 28, No. 12, pp. 1870-1882, 2009.
162. T. Tao Ye and G. De Micheli, "On-chip implementation of multiprocessor networks and switch fabrics," *International Journal Embedded Systems*, 2009, Vol. 3, No.4, pp.209-218.
163. H. Ben-Jamaa, K. Mohanram, and G. De Micheli, "An Efficient Gate Library for Ambipolar CNTFET Logic," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2010.
164. H. Ben-Jamaa, G. Cerofolini, G. De Micheli, and Y. Leblebici, "Poly-Silicon Nanowire Transistors and Arrays Fabricated with the Multi-Spacer Technique," *IEEE Transactions on Nanotechnology*, 2010.
165. S. Carrara, A. Cavallini, Y. Leblebici, G. De Micheli, V. Bhalla, F. Valle, B. Samor, L. Benini, B. Ricc, I. Vikholm-Lundin, and T. Munter, "Capacitance DNA bio-chips improved by new probe immobilization strategies," *MicroelectronicsJournal*, no. 41, pp. 711-717, 2010.
166. J. Olivo, S. Carrara, and G. De Micheli, "Energy Harvesting and Remote Powering for Implantable Biosensors," *IEEE Sensors Journal*, 2010.
167. C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, "SunFloor 3D: A Tool for Networks on Chip Topology Synthesis for 3D Systems on Chips," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 12, pp. 1987-2000, 2010.
168. C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, "Comparative Analysis of NoCs for Two-Dimensional Versus Three-Dimensional SoCs Supporting Multiple Voltage and Frequency Islands," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 5, pp. 364 - 368, 2010.
169. S. Carrara, A. Cavallini, Y. Maruyama, E. Charbon, and G. De Micheli, "A new ethylene glycol-silane monolayer for highly-specific DNA detection on Silicon Chips," *Surface Science Letters*, 2010.
170. D. Sacchetto, G. De Micheli and Y. Leblebici. "Ambipolar Gate-Controllable SiNW FETs for Configurable Logic Circuits With Improved Expressive Capability", in *IEEE Electron Device Letters*, 2011.
171. M. Zervas, D. Sacchetto, G. De Micheli and Y. Leblebici. "Top-down fabrication of very-high density vertically stacked silicon nanowire arrays with low temperature budget", in *Microelectronic Engineering*, vol. 88, num. 10, p. 3127-3132, 2011.
172. C. Boero, S. Carrara, G. Del Vecchio, L. Calza and G. De Micheli. "Highly Sensitive Carbon Nanotube-Based Sensing for Lactate and Glucose Monitoring in Cell Culture", in *IEEE Transactions on Nanobio-science*, vol. 10, p. 59-67, 2011.



173. C. Boero, S. Carrara, G. Del Vecchio, L. Calza and G. De Micheli. "Targeting of multiple metabolites in neural cells monitored by using protein-based carbon nanotubes", in *Sensors And Actuators B-Chemical*, vol. 157, p. 216-224, 2011.
174. D. Sacchetto, A. V. Savu, G. De Micheli, J. Brugger and Y. Leblebici, "Ambipolar silicon nanowire FETs with stenciled-deposited metal gate", in *Microelectronic Engineering*, vol. 88, p. 2732-2735, 2011.
175. I. Taurino, S. Carrara, M. Giorelli, A. Tagliaferro and G. De Micheli. "Comparing Sensitivities of Differently Oriented Multi-walled Carbon Nanotubes Integrated on Silicon Wafer for Electrochemical Biosensors", in *Sensors and Actuators B: Chemica* vol. B 160, p. 327-333, 2011.
176. L. Zhu, G. Del Vecchio, G. De Micheli, Y. Liu, S. Carrara, S. Calzà and S. Carrara, "Biochips for Regenerative Medicine: Real-time Stem Cell Continuous Monitoring as Inferred by High-Throughput Gene Analysis", in *BioNanoScience*, vol. 1, num. 4, p. 183-191, 2011.
177. B. Jamaa, M. Haykel, G. Cerofolini, G. De Micheli and Y. Leblebici. "Polysilicon Nanowire Transistors and Arrays Fabricated With the Multispacer Technique", in *IEEE Transactions on Nanotechnology*, vol. 10, num. 4, p. 891-899, 2011.
178. J. Olivo, S. Carrara and G. De Micheli. "Biofuel Cells and Inductive Powering as Energy Harvesting Techniques for Implantable Sensors", in *Science of Advanced Materials*, vol. 3, num. 3, p. 420-425, 2011.
179. H. Ben-Jamaa, P.-E. Gaillardon, F. Clermidy, I. O'Connor, D. Sacchetto, G. De Micheli and Y. Leblebici, "Silicon Nanowire Arrays and Crossbars: Top-Down Fabrication Techniques and Circuit Applications", in *Science of Advanced Materials*, vol. 3, p. 466476, 2011.
180. D. Sacchetto, M.-A. Doucey, G. De Micheli, Y. Leblebici and S. Carrara, "New Insight on Bio-sensing by Nano-fabricated Memristors", in *BioNanoScience*, vol. 1, num. 1-2, p. 1-3, 2011.
181. F. Zanini, M. M. S. Aly, D. Atienza Alonso and G. De Micheli. "Hierarchical Thermal Management Policy for High-Performance 3D Systems with Liquid Cooling", in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, p. 88-101, 2011.
182. S. Carrara, A. Cavallini, V. Erokhin and G. De Micheli. "Multi-panel drugs detection in human serum for personalized therapy", in *Biosensors and Bioelectronics*, vol. 26, num. 9, p. 3914-3919, 2011.
183. B. Jamaa, M. Haykel, P.-E. Gaillardon, S. Frègonèse, M. De Marchi, G. De Micheli, T. Zimmer, I. O'Connor and F. Clermidy, "FPGA Design with Double-Gate Carbon Nanotube Transistors", in *Electrochemical Society Transactions - CSTIC 2011*, vol. 34, num. 1, p. 1005-1010, 2011.
184. D. Sacchetto, A. V. Savu, G. De Micheli, J. Brugger and Y. Leblebici, "Ambipolar Silicon Nanowire FETs with Stenciled-Deposited Metal Gate", in *Microelectronic Engineering*, vol. 88, num. 8, p. 2732-2735, 2011.
185. H. Ben-Jamaa, K. Mohanram and G. De Micheli, "An Efficient Gate Library for Ambipolar CNTFET Logic", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, num. 2, p. 242-255, 2011.
186. J. Olivo, S. Carrara and G. De Micheli, "Energy Harvesting and Remote Powering for Implantable Biosensors", in *IEEE Sensors Journal*, vol. 11, num. 7, p. 1573 - 1586, 2011.
187. A. Dimonte, S. Frache, V. Erokhin, G. Piccinini, D. Demarchi, F. Milano, G. De Micheli and S. Carrara, "Nanosized Optoelectronic Devices Based on Photoactivated Proteins", in *ACS BioMacromolecules*, vol. 13, num. 11, p. 3503-3509, 2012.
188. I. Taurino, S. Carrara, M. Giorelli, A. Tagliaferro and G. De Micheli, "Carbon Nanotubes With Different Orientations for Electrochemical Biodevices", in *IEEE Sensors Journal*, vol. 12, num. 12, p. 3356-3362, 2012.
189. C. Boero, J. Olivo, S. Carrara and G. De Micheli, "A Self-Contained System With CNTs-Based Biosensors for Cell Culture Monitoring", in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, num. 4, p. 658-671, 2012.
190. I. Taurino, G. De Micheli and S. Carrara, "Multiwalled Carbon Nanotubes for Amperometric Array-Based Biosensors", in *BioNanoScience*, vol. 2, num. 4, p. 185-195, 2012.
191. F. Zanini, D. Atienza Alonso, C. Jones, L. Benini and G. De Micheli, "Online Thermal Control Methods for Multi-Processor Systems", in *ACM Transactions on Design Automation of Electronic Systems*, vol. 18, num. 1, p. 6:1 - 6:26, 2012.
192. D. Sacchetto, S. Xie, V. Savu, M. Zervas, G. De Micheli, J. Brugger and Y. Leblebici, "Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-micron gates patterned by nanostencil lithography", in *Microelectronic Engineering*, vol. 98, p. 355-358, 2012.

193. S. Carrara, S. S. Ghoreishizadeh, J. Olivo, I. Taurino, C. Baj-Rossi, A. Cavallini, M. Op de Beek, C. De Hollain, W. Bursleson and G. Francis, "Fully Integrated Biochip Platforms for Advanced Healthcare", in *Sensors*, vol. 12, num. 8, p. 11013-11060, 2012.
194. J. Ghaye, G. De Micheli and S. Carrara, "Simulated Biological Cells for Receptor Counting in Fluorescence Imaging", in *BioNanoScience*, vol. 2, num. 2, p. 94-103, 2012.
195. C. Baj-Rossi, G. De Micheli and S. Carrara, "Electrochemical Detection of Anti-Breast-Cancer Agents in Human Serum by Cytochrome P450-Coated Carbon Nanotubes", in *Sensors*, vol. 12, num. 5, p. 6520-6537, 2012.
196. S. Carrara, D. Sacchetto, M.-A. Doucey, C. Baj-Rossi, G. De Micheli and Y. Leblebici, "Memristive-Biosensors: A New Detection Method by Using Nanofabricated Memristors", in *Sensors and Actuators B*, vol. 171-172, p. 449-457, 2012.
197. D. Sacchetto, G. De Micheli and Y. Leblebici, "Multiterminal Memristive Nanowire Devices for Logic and Memory Applications: A Review", in *Proceedings of the IEEE*, vol. 100, num. 6, p. 2008-2020, 2012.
198. S. Rahimian Omam, V. Pavlidis and G. De Michel, "Inter-Plane Communication Methods for 3-D ICs", in *Journal of Low Power Electronics*, vol. 8, num. 2, p. 170-181, 2012.
199. J. M. Ghaye, G. De Micheli and S. Carrara, "Simulated biological cells for receptor counting in fluorescence imaging", in *BioNanoScience*, vol. 2, num. 2, p. 94-103, 2012.
200. A. S. Kumar, M. P. Kumar, S. Murali, V. Kamakoti, L. Benini and G. De Micheli, "A Buffer-Sizing Algorithm for Network-on-Chips with Multiple Voltage-Frequency Islands", in *Journal of Electrical and Computer Engineering*, vol. 2012, 2012.
201. F. Zanini, D. Atienza Alonso, C. Jones, L. Benini and G. De Micheli, "A Combined Sensor Placement and Convex Optimization Approach for Thermal Management in 3D-MPSoC with Liquid Cooling", in *Integration, the VLSI Journal*, vol. 46, num. 1, p. 33-43, 2012.
202. H. Xu, V. Pavlidis and G. De Micheli, "Effects of Process Variations on 3-D Global Clock Distribution Networks", in *ACM Journal on Emerging Technologies in Computing Systems*, vol. 8, num. 3, 2012.
203. D. Sacchetto, G. De Micheli and Y. Leblebici, "Ambipolar Gate-Controllable SiNW FETs for Configurable Logic Circuits With Improved Expressive Capability", in *IEEE Electron Device Letters*, vol. 33, num. 2, p. 143-145, 2012.
204. I. Taurino, S. Carrara, M. Giorcelli, A. Tagliaferro and G. De Micheli, "Comparison of Two Different Carbon Nanotube-based Surfaces with Respect to Potassium Ferricyanide Electrochemistry", in *Surface Science*, vol. 606, num. 3-4, p. 156-160, 2012.
205. D. Sacchetto, M. Zervas, Y. Temiz, G. De Micheli and Y. Leblebici, "Resistive Programmable Through Silicon Vias for Reconfigurable 3D Fabrics", in *IEEE Transactions on Nanotechnology*, vol. 11, num. 1, p. 8-11, 2012.
206. C. Boero, J. Olivo, S. Carrara and G. De Micheli, "New Approaches for Carbon Nanotubes-Based Biosensors and Their Application to Cell Culture Monitoring," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, num. 5, p. 479-485, 2012.
207. E. Kyriakides, S. Carrara, G. De Micheli and J. Georgiou, "Low-cost, CMOS compatible, Ta2O5-based hemi-memristor for neuromorphic circuits", in *Electronics Letters*, vol. 48, num. 23, p. 1451-1452, 2012.
208. S. Rahimian, V. F. Pavlidis, X. Tang and G. De Micheli, "An Enhanced Design Methodology for Resonant Clock Trees", in *Journal of Low Power Electronics*, vol. 9, num. 2, p. 198-206, 2013.
209. J. Joven, A. Marongiu, F. Angiolini, L. Benini and G. De Micheli, "An integrated, programming model-driven framework for NoC-QoS support in cluster-based embedded many-cores", in *Parallel Computing*, vol. 39, num. 10, p. 549-566, 2013.
210. C. Baj-Rossi, G. De Micheli and S. Carrara, "A Linear Approach to Multi-Panel Sensing in Personalized Therapy for Cancer Treatment", in *IEEE Sensors Journal*, vol. 13, num. 12, p. 4860-4865, 2013.
211. I. Taurino, A. Magrez, F. Matteini, L. Forr, S. Carara and G. De Micheli, "Direct growth of nanotubes and graphene nanoflowers on electrochemical platinum electrodes", in *Nanoscale*, vol. 5, num. 24, p. 12448-12455, 2013.
212. I. Taurino, V. Van Hoof, G. De Micheli and S. Carrara, "Superior sensing performance of multi-walled carbon nanotube-based electrodes to detect unconjugated bilirubin", in *Thin Solid Films*, vol. 548, p. 546-550, 2013.

213. W. You, A. Simalatsar, N. Widmer and G. De Micheli, "Personalized Drug Administrations Using Support Vector Machine", in *BioNanoScience*, 2013.
214. J. Olivo, S. Carrara and G. De Micheli, "A Study of Multi-Layer Spiral Inductors for Remote Powering of Implantable Sensors", in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, num. 4, p. 536-547, 2013.
215. J. Joven, A. Bagdia, F. Angiolini, P. Strid, E. Fernandez, J. Carrabina, D. Castells-Rufas and G. De Micheli, "QoS-Driven Reconfigurable Parallel Computing for NoC-Based Clustered MPSoCs", in *IEEE Transactions on Industrial Informatics*, vol. 9, num. 3, p. 1613-1624, 2013.
216. I. Taurino, R. Reiss, M. Richter, M. Fairhead and L. Thoeny-Meyer, S. Carrara and G. De Micheli, "Comparative study of three lactate oxidases from *Aerococcus viridans* for biosensing applications", in *Electrochimica Acta*, vol. 93, p. 72-79, 2013.
217. J. M. Ghaye, M. Avinash Kamat, L. Corbino-Giunta, P. Silacci, G. Vergres, S. Carrara and G. De Micheli, "Image thresholding techniques for localization of sub-resolution fluorescent biomarkers", in *Cytometry*, vol. 83, num. 11, p. 1001-1016, 2013.
218. L. Amar, P.-E. Gaillardon, J. Zhang and G. De Micheli, "Power-Gated Differential Logic Style Based on Double-Gate Controllable-Polarity Transistors", in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, num. 10, p. 672-676, 2013.
219. G. Kkl, J. Ghaye, R. Etienne-Cummings, Y. Leblebici, S. Carrara and G. De Micheli et al, "Empowering Low-Cost CMOS Cameras by Image Processing to Reach Comparable Results with Costly CCDs", in *BioNanoScience*, vol. 3, num. 4, p. 403-414, 2013.
220. C. Seiculescu, D. Rahmati, S. Murali, L. Benini, H. Sarbazi-Azad and G. De Micheli et al. , "Designing Best Effort Networks-on-Chip to Meet Hard Latency Constraints", in *ACM Transactions on Embedded Computing Systems*, vol. 12, num. 4, 2013.
221. D. Sacchetto, P.-E. J. M. Gaillardon, M. Zervas, S. Carrara, Y. Leblebici and G. De Micheli et al. , "Applications of Multi-Terminal Memristive Devices: A Review", in *IEEE Circuits and Systems Magazine*, vol. 13, num. 2, p. 23-41, 2013.
222. F. Mastrantonio, F. Valgimigli, L. Grassi, P. Cappa, S. Carrara and G. De Micheli , "Comparative Performance of Different Nanostructured Electrochemical Sensors on Insulin Detection", in *BioNanoScience*, vol. 3, num. 3, p. 285-288, 2013.
223. S. Carrara, L. Bolomey, C. Boero, A. Cavallini, E. Meurville, G. de Micheli, T. Rezzonico, M. Proietti and F. Grassi , "Remote System for Monitoring Animal Models With Single-Metabolite Bio-Nano-Sensors", in *IEEE Sensors Journal*, vol. 13, num. 3, p. 1018 - 1024, 2013.
224. H. Xu, V. Pavlidis, X. Tang, W. Burleson and G. De Micheli. , "Timing Uncertainty in 3-D Clock Trees due to Process Variations and Power Supply Noise", in *IEEE Transactions on Very Large Scale Integration Systems*, vol. 21, num. 12, p. 2226-2239, 2013.
225. P.-E. Gaillardon, D. Sacchetto, G. Betti Beneventi, H. Ben Jamaa, L. Perniola , F. Clermidy, I. O'Connor and G. De Micheli , "Design and Architectural Assessment of 3-D Resistive Memory Technologies in FPGAs", in *IEEE Transactions on Nanotechnology*, vol. 12, num. 1, p. 40-50, 2013.
226. S. Bobba, A. Chakraborty, O. Thomas, P. Batude and G. De Micheli, "Cell Transformations and Physical Design Techniques for 3D Monolithic Integrated Circuits", in *ACM Journal on Emerging Technology in Computing Systems*, vol. 9, num. 3, p. 19:1 - 19:28, 2013.
227. F. Zanini, D. Atienza Alonso and G. De Micheli, "A Combined Sensor Placement and Convex Optimization Approach for Thermal Management in 3D-MPSoC with Liquid Cooling", in *Integration, the VLSI Journal*, vol. 46, num. 1, p. 33-43, 2013.
228. D. Rahmati, S. Murali, L. Benini, F. Angiolini, H. Sarbazi-Azad and G. De Micheli, "Computing Accurate Performance Bounds for Best Effort Networks-on-Chip,,", in *IEEE Transactions on Computers*, vol. 62, num. 3, p. 452-467, 2013.
229. M. De Marchi, D. Sacchetto, J. Zhang, S. Frache, P.-E. Gaillardon, Y. Leblebici and G. De Micheli , "Top-Down Fabrication of Gate-All-Around Vertically-Stacked Silicon Nanowire FETs with Controllable Polarity", in *IEEE Transactions on Nanotechnology*, vol. 13, num. 6, p. 1029 - 1038, 2014.
230. I. Kazi, P. Meinerzhagen, P.-E. Gaillardon, D. Sacchetto, Y. Leblebici, A. Burg and G. De Micheli. , "Energy/Reliability Trade-Offs in Low-Voltage ReRAM-Based Non-Volatile Flip-Flop Design", in *IEEE Transactions on Circuits and Systems Part 1 Regular Papers*, vol. 61, num. 11, p. 3155 - 3164, 2014.

231. J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici and G. De Micheli, “Polarity-Controllable Silicon Nanowire Transistors with Dual Threshold Voltages”, in *IEEE Transactions on Electron Devices*, vol. 61, num. 11, p. 3654 - 3660, 2014.
232. S. S. Ghoreishizadeh, C. Baj-Rossi, A. Cavallini, S. Carrara and G. De Micheli, “An Integrated Control and Readout Circuit for Implantable Multi-Target Electrochemical Biosensing”, in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, num. 6, p. 891 - 898, 2014.
233. C. Baj-Rossi, E. G. Kilin, S. S. Ghoreishizadeh, D. Casarino, T. Rezzonico Jost, C. DeHollain, F. Grasi, L. Pastorini, G. De Micheli and S. Carrara, “Full Fabrication and Packaging of an Implantable Multi-panel Device for Monitoring of Metabolites in Small Animals”, in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, num. 5, p. 636-647, 2014.
234. I. Taurino, V. Van Hoof, A. Magrez, L. Forró, G. De Micheli and S. Carrara, “Efficient voltammetric discrimination of free bilirubin from uric acid and ascorbic acid by a CVD nanographite-based microelectrode,” *Elsevier, Talanta, The International Journal of Pure and Applied Analytical Chemistry* vol. 130, num. December, p. 423-426, 2014.
235. L. Amarú, P.-E. Gaillardon and G. De Micheli, “Biconditional Binary Decision Diagrams: A Novel Canonical Representation Form”, in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, num. 4, p. 487-500, 2014.
236. C. Boero, M. A. Casulli, J. Olivo, L. Foglia, E. Orso, M. Mazza, S. Carrara and G. De Micheli, “Design, development, and validation of an in-situ biosensor array for metabolite monitoring of cell cultures”, in *Biosensors and Bioelectronics*, vol. 61, p. 251-259, 2014.
237. I. Taurino, A. Magrez, F. Matteini, A. Cavallini, L. Forr, G. De Micheli and S. Carrara, “High-Performance Multipanel Biosensors Based on a Selective Integration of Nanographite Petals”, in *ACS Nano Letters*, vol. 14, num. 6, p. 3180-3184, 2014.
238. L. Amarù, P.-E. Gaillardon and G. De Micheli, “A Circuit Synthesis Flow for Controllable-Polarity Transistors”, in *IEEE Transactions on Nanotechnology*, vol. 13, num. 6, p. 1074-1083, 2014.
239. M. De Marchi, J. Zhang, S. Frache, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici and G. De Micheli, “Configurable Logic Gates Using Polarity Controlled Silicon Nanowire Gate-All-Around FETs”, in *IEEE Electron Device Letters*, vol. 35, num. 8, p. 880-882, 2014.
240. J. Zhang, X. Tang, P.-E. Gaillardon and G. De Micheli, “Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs”, in *IEEE Transactions on Circuits and Systems Part 1 Regular Papers*, vol. 61, num. 10, p. 2851-2861, 2014.
241. P. D. Duben, J. Joven, A. Lingamneni, H. McNamara, G. De Micheli, K. Palem and T. Palmer, “On the use of inexact, pruned hardware in atmospheric modelling”, in *Proceedings of the Royal Society of London A*, vol. 372, num. 2018, 2014.
242. A. Simalatsar, W. You, V. Gotta, N. Widmer and G. De Micheli, “Representation of Medical Guidelines with a Computer Interpretable Model”, in *International Journal on Artificial Intelligence Tools (IJAIT)*, vol. 23, num. 3, 2014.
243. F. Puppo, S. Carrara, M. Di Ventra and G. De Micheli, “Memristive sensors for pH measure in dry conditions”, in *Surface Science Journal*, vol. 624, num. June, p. 76-79, 2014.
244. J. Olivo, S. Carrara and G. De Micheli, “Micro-fabrication of high-thickness spiral inductors for the remote powering of implantable biosensors”, in *Microelectronic Engineering*, vol. 113, p. 130-135, 2014.
245. S. Carrara, C. Baj-Rossi, C. Boero and G. De Micheli, “Do Carbon Nanotubes Contribute to Electrochemical Biosensing?”, in *Electrochimica Acta*, vol. 128, p. 102-112, 2014.
246. F. Puppo, A. Dave, M.-A. Doucey, D. Sacchetto, C. Baj-Rossi, Y. Leblebici, G. De Micheli and S. Carrara, “Memristive Biosensors Under Varying Humidity Conditions”, in *IEEE Transactions on Nanobioscience*, vol. 13, num. 1, pp. 19-30, 2014.
247. S. Bobba, J. Zhang, P.-E. Gaillardon, H.-S. P. Wong, S. Mitra and Giovanni De Micheli, “System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits”, in *ACM Journal on Emerging Technologies in Computing Systems*, vol. 10, num. 4, 2014.
248. C. Baj-Rossi, T. Rezzonico Jost, A. Cavallini, F. Grassi, G. De Micheli and S. Carrara, “Continuous monitoring of Naproxen by a cytochrome P450-based electrochemical sensor”, in *Biosensors and Bioelectronics*, vol. 53, p. 283-287, 2014.

249. P.-E. Gaillardon, L. G. Amarù, S. K. Bobba, M. De Marchi, D. Sacchetto and G. De Micheli , “Nanowire systems: technology and design”, in *Philosophical Transactions of the Royal Society of London A*, vol. 372, num. 2012, 2014.
250. I. Taurino, G. Sanzo, F. Mazzei, G. Favero, G. De Micheli and S. Carrara, “Fast synthesis of platinum nanopetals and nanospheres for highly-sensitive non-enzymatic detection of glucose and selective sensing of ions”, in *Scientific Reports*, vol. 5, num. Article number: 15277, 2015.
251. S. Bobba and G. De Micheli. “Layout Technique for Double-Gate Silicon Nanowire FETs With an Efficient Sea-of-Tiles Architecture”, in *IEEE Transactions on very Large Scale Integration (VLSI) Systems*, vol. 23, num. 10, p. 2103-2115, 2015.
252. H. Ghasemzadeh, P.-E. Gaillardon and G. De Micheli. “From Defect Analysis to Gate-Level Fault Modeling of Controllable-Polarity Silicon Nanowires”, *IEEE Transactions on Nanotechnology*, vol. 14, num. 6, p. 1117-1126, 2015.
253. J. Zhang, P.-E. Gaillardon and G. De Micheli. “On Temperature Dependency of Steep Subthreshold Slope in Dual-Independent-Gate FinFET”, accepted in *IEEE Journal of the Electron Devices Society*, vol. 3, num. 6, p. 452-456, 2015.
254. C. Baj-Rossi, C. Mueller, U. von Mandach, G. De Micheli and S. Carrara. “Faradic Peaks Enhanced by Carbon Nanotubes in Microsomal Cytochrome P450 Electrodes”, in *Electroanalysis*, vol. 27, num. 6, p. 1507-1515, 2015.
255. I. Tzouvadaki, C. Parrozzani, A. Galotta, G. De Micheli and S. Carrara. “Memristive Biosensors for PSA-IgM Detection”, accepted in *BioNanoScience*, 2015.
256. E. G. Kilin, C. Baj-Rossi, S. Ghoreishizadeh, S. Riario, F. Stradolini, C. Boero, G. De Micheli, F. Maloberti, S. Carrara, and C. Dehollain. “A System for Wireless Power Transfer and Data Communication of Long-Term Bio-Monitoring”, in *IEEE Sensors Journal*, vol. 15, num. 11, p. 6559-6569, 2015.
257. F. Puppo, M.-A. Doucey, J.-F. Delaloye, T. S. Y. Moh, G. Pandraud, P. Sarro, G. de Micheli and S. Carrara, “SiNW-FET in-Air Biosensors for High Sensitive and Specific Detection in Breast Tumor Extract”, accepted in *IEEE Sensors Journal*, 2015.
258. I. Tzouvadaki, F. Puppo, G. De Micheli and S. Carrara. “Computational Study on the Electrical Behavior of Silicon Nanowire Memristive Biosensors”, in *IEEE Sensors Journal*, vol. 15, num. 11, p. 6208-6217, 2015.
259. Y. Bi, K. Shamsi, J.-S. Yuan, P.-E. Gaillardon, G. De Micheli, X. Yin, X. Hu , M. Niemier and Y. Yin. “Emerging Technology Based Design of Primitives for Hardware Security”, accepted in *ACM Journal on Emerging Technologies in Computing Systems*, 2015.
260. L. Amarù, P.-E. Gaillardon, S. Mitra and G. De Micheli. “New Logic Synthesis As Nanotechnology Enabler”, *Proceedings of the IEEE*, vol. 103, num. 11, p. 2168-2195, 2015.
261. P.-E. Gaillardon, E. Beigné, S. Lesecq and G. De Micheli. “A Survey on Low-Power Techniques with Emerging Technologies: From Devices to Systems”, in *ACM Journal on Emerging Technologies: From Devices to Systems*, vol. 12, num. 2, p. 12:1 - 12:26, 2015.
262. J. Sandrini, M. V. Thammassack, T. Demirci, P.-E. J. M. Gaillardon, D. Sacchetto, G. De Micheli and Y. Leblebici. “Heterogeneous Integration of ReRAM Crossbars in 180nm CMOS BEoL Process”, in *Microelectronic Engineering*, vol. 145, num. 9, p. 62-65, 2015.
263. N. Aliakbari, I. Taurino, J. Pravin, A. Tagliaferro , G. Piccinini, G. De Micheli and S. Carrara. “Electrochemical nanostructured biosensors: carbon nanotubes versus conductive and semi-conductive nanoparticles”, in *Chemical Papers*, vol. 69, num. 1, p. 134-142, 2015.
264. A. Cavallini, T. Rezzonico Jost, S. S. Ghoreishizadeh, J. Olivo and M. Op de Beeck, B. Gorissen, F. Grassi, G. De Micheli and S. Carrara. “A Subcutaneous Biochip for Remote Monitoring of Human Metabolism: Packaging and Biocompatibility Assessment”, in *IEEE Sensors Journal*, vol. 15, num. 1, p. 417-424, 2015.
265. K. Kang, L. Benini and G. De Micheli. “Cost-Effective Design of Mesh-of-Tree Interconnect for Multi-Core Clusters with 3-D Stacked L2 Scratchpad Memory”, in *IEEE Transactions on Very Large Scale Integration Systems*, vol. 23, num. 9, p. 1828-1841, 2015.
266. P.-E. Gaillardon, X. Tang, G. Kim and G. De Micheli. “A Novel FPGA Architecture based on Ultra-Fine Grain Reconfigurable Logic Cells”, accepted in *IEEE Transactions on Very Large Scale Integration Systems*, vol. 23, num. 10, p. 2187-2197, 2015.

267. C. Baj-Rossi, A. Cavallini, E. G. Kilin, F. Stradolini, T. Rezzonica Jost, M. Progetti, G. De Micheli, C. Dehollain and S. Carrara, "In-Vivo Validation of Fully Implantable Multi-Panel Devices for Remote Monitoring of Metabolism," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, num. 5, p. 955-962, 2016.
268. A. Vallero, I. Tzouvadaki, F. Puppo, M.-A. Doucey, J.-F. Delaloye, G. De Micheli and S. Carrara, "Memristive Biosensors Integration With Microfluidic Platform", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, num. 12, pp. 2120-2127, 2016.
269. I. Tzouvadaki, N. Madaboosi, I. Taurino, V. Chu, J. P. Conde, Giovanni De Micheli and S. Carrara, "Study on the bio-functionalization of memristive nanowires for optimum memristive biosensors", in *Journal of Materials Chemistry B*, num. 4, p. 2153-2162, 2016.
270. A. Antidormi, S. Frache, M. Graziano, P.-E. Gaillardon, G. Piccinini and G. De Micheli "Computationally Efficient Multiple-Independent-Gate Device Model," in *IEEE Transactions on Nanotechnology*, vol. 15, num. 1, p. 2-14, 2016.
271. F. Puppo, F. L. Traversa, M. Di Ventra, G. De Micheli and S. Carrara. "Surface trap mediated electronic transport in biofunctionalized silicon nanowires", in *Nanotechnology*, vol. 27, num. 34, p. 345503, 2016.
272. G. Sanzo, I. Taurino, R. Antiochia, L. Gorton, G. Favero, F. Mazzei, G. De Micheli and S. Carrara, "Bubble electrodeposition of gold porous nanocorals for the enzymatic and non-enzymatic detection of glucose", in *Bioelectrochemistry*, vol. 112, num. December, p. 125-131, 2016.
273. G. Massicotte, S. Carrara, G. De Micheli and M. Sawan. "A CMOS Amperometric System for Multi-Neurotransmitter Detection", in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, num. 3, p. 731-741, 2016.
274. I. Tzouvadaki, P. Jolly, X. Lu, S. Ingebrandt, G. De Micheli, P. Estrela and S. Carrara, "Label-Free Ultrasensitive Memristive Aptasensor", in *ACS Nano Letters*, vol. 16, num. 7, p. 4472-4476, 2016.
275. N. Aliakbari, G. De Micheli and S. Carrara. "Enzymatic and Nonenzymatic Electrochemical Interaction of Abiraterone (Antiprostata Cancer Drug) with Multiwalled Carbon Nanotube Bioelectrodes", in *Analytical Chemistry*, vol. 88, num. 19, p. 9347-9350, 2016.
276. G. V. Resta, S. Sutar, Y. Balaji, D. Lin, P. Raghavan, I. Radu, F. Catthoor, A. Thean, P.E. Gaillardon and G. De Micheli, "Polarity control in WSe<sub>2</sub> double-gate transistors", in *Scientific Reports*, vol. 6, num. 29448, 2016.
277. F. Stradolini, S. Riario, C. Boero, C. Baj-Rossi, I. Taurino, G. Surrel, G. De Micheli and S. Carrara, "Wireless Monitoring of Endogenous and Exogenous Biomolecules on an Android Interface", in *IEEE Sensors Journal*, vol. 16, num. 9, p. 3163-3170, 2016.
278. I. Taurino, G. Sanzo, R. Antiochia, C. Tortolini, F. Mazzei, G. Favero, G. De Micheli and S. Carrara, "Recent advances in Third Generation Biosensors based on Au and Pt Nanostructured Electrodes", in *TrAC Trends In Analytical Chemistry*, vol. 79, num. May 2016, p. 151-159, 2016.
279. I. Taurino, S. Massa, G. Sanzo, J. Aleman, B. Flavia, S-R Shin, Y-S Zhang, M. Dokmeci, G. De Micheli and S. Carrara, "Platinum nanopetal-based potassium sensors for acute cell death monitoring", in *RSC Advances*, vol. 6, num. 46, p. 40517-40526, 2016.
280. H. Ghasenzadeh Mohammadi, P.-E. Gaillardon and G. De Micheli. "Efficient Statistical Parameter Selection for Nonlinear Modeling of Process/Performance Variation", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, num. 12, p. 1995 - 2007, 2016.
281. C. Baj-Rossi, S. Ghoreishzadeh, S. Carrara and G. De Micheli. "An Innovative System of Membranes for the Monitoring of Endogenous and Exogenous Metabolites", in *BioNanoScience*, vol. 6, num. 2, p. 85-92, 2016.
282. G. Beanato, A. Cevrero, G. De Micheli and Y. Leblebici. "Impact of Data Serialization over TSVs on Routing Congestion in 3D-Stacked Multi-Core Processors," in *Microelectronics Journal*, vol. 51, num. May, p. 38-45, 2016.
283. X. Tang, G. Kim, P.-E. Gaillardon and G. De Micheli. "A Study on the Programming Structures for RRAM-based FPGA Architectures," in *IEEE Transactions on Circuits and Systems - I*, vol. 63, num. 4, p. 503-516, 2016.
284. L. Amarú, P.-E. Gaillardon, A. Chattopadhyay and G. De Micheli. "A Sound and Complete Axiomatization of Majority-n Logic," in *IEEE Transactions on Computers*, vol. 65, num. 9, p. 2889 - 2895, 2016.

285. A. Antidormi, S. Frache, M. Graziano, P.-E. Gaillardon, G. Piccinini and G. De Micheli “Computationally Efficient Multiple-Independent-Gate Device Model,” in *IEEE Transactions on Nanotechnology*, vol. 15, num. 1, p. 2-14, 2016.
286. J. Sandrini, M. Barlas, M. Thammasack, T. Demirci, M. De Marchi, D. Sacchetto, P.E. Gaillardon, G. De Micheli and Y. Leblebici “Co-design of ReRAM Passive Crossbar Arrays Integrated’ in 180nm CMOS Technology, in *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 6, num. 3, p. 339-351, 2016.
287. L. Amaru, P.-E. Gaillardon and G. De Micheli. “Majority-Inverter Graph: A New Paradigm for Logic Optimization’, in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, num. 5, p. 806-819, 2016.
288. F. Puppo, M.-A. Doucey, J.-F. Delaloye, T. S. Y. Moh and G. Pandraud, P. Sarro. G. de Micheli and S. Carrara. “SiNW-FET in-Air Biosensors for High Sensitive and Specific Detection in Breast Tumor Extract’, in *IEEE Sensors Journal*, vol. 16, num. 10, p. 3374-3381, 2016.
289. Y. Bi, K. Shamsi, J.-S. Yuan, P.-E. Gaillardon, G. De Micheli, X.Yin, S. Hu, M.Niemier and Y. Jin, “Emerging Technology Based Design of Primitives for Hardware Security’, in *ACM Journal on Emerging Technologies in Computing Systems*, vol. 13, num. 1, p. 3:1-3:19, 2016.
290. P. Mayor, M. Rajman and G. De Micheli. “Nano-Tera.ch: Information Technology for Health, Environment, and Energy”, in *IEEE Design and Test*, vol. 34, num. 6, p. 109-118, 2017.
291. M. Thammasack, G. De Micheli and P.-E. Gaillardon. “Effect of O2 migration in Pt/HfO2/Ti/Pt structure”, in *Journal of Electroceramics*, vol. 39, num. 1-4, p. 137-142, 2017.
292. G. Sanz, I. Taurino, F. Puppo, R. Antiochia, L. Gorton, G. Favero, F. Mazzei, S. Carrara, G. De Micheli. “A bimetallic nanocoral Au decorated with Pt nanoflowers (bio)sensor for H2O2 detection at low potential”, in *Methods*, vol. 129, num. October, p. 89-95, 2017.
293. I. Tzouvadaki, N. Aliakbarinodehi, G. De Micheli and S. Carrara. “The memristive effect as a novelty in drug monitoring”, in *Nanoscale*, vol. 9, num. 27, p. 9676-9684, 2017.
294. A. Ibrahim, P. A. Hager, A. Bartolini, F. Angiolini, M. Arditi, J.-Ph. Thiran, L. Benini and G. De Micheli, “Efficient Sample Delay Calculation for 2-D and 3-D Ultrasound Imaging”, in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, num. 4, p. 815-831, 2017.
295. S. Ghoreishizadeh, I. Taurino, G. De Micheli, S. Carrara and P. Georgiou. “A Differential Electrochemical Readout ASIC with Heterogeneous Integration of Bio-nano Sensors for Amperometric Sensing,” in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, num. 5, p. 1148-1159, 2017.
296. G. De Micheli. “Cyber-Medical Systems: Requirements, Components Design Examples,” accepted in *IEEE Transactions on Circuits and Systems Part 1 Regular Papers*, 2017.
297. G. De Micheli and L. Benini. “Networks on Chips: 15 Years Later”, in *Computer*, vol. 50, num. 5, p. 10-11, 2017.
298. M. Soeken, P.-E. Gaillardon, S. Shirinzadeh, R. Drechsler and G. De Micheli. “A PLiM Computer for the Internet of Things”, in *Computer*, vol. 50, num. 6, p. 35-40, 2017.
299. G. Resta, T. Agarwal, D. Lin, I. P. Radu, F. Catthoor, P.-E. Gaillardon and G. De Micheli. “Scaling trends and performance evaluation of 2-dimensional polarity-controllable FETs”, in *Scientific Reports*, vol. 7, num. 45556, 2017.
300. N. Aliakbari, P. Jolly, N. Bhalla, A. Miodek, G. De Micheli, P. Estrela and S. Carrara. “Aptamer-based Field-Effect Biosensor for Tenofovir Detection”, in *Scientific Reports*, vol. 7, num. 44409, 2017.
301. N. Aliakbarinodehi, G. De Micheli and S. Carrara. “Highly sensitive enzymatic MWCNTs-based biosensors for detection of abiraterone in human serum”, accepted in *BioNanoScience*, 2017.
302. D.-Y. Jeon, J. Zhang, J. Trommer, S. J. Park, P.-E. Gaillardon, G. De Micheli, T. Mikolajick, M. Walter. “Operation regimes and electrical transport of steep slope Schottky Si-FinFETS,” in *Journal of Applied Physics*, vol. 121, num. 6, 2017.
303. T.-H. Lin, T. Margossian, M. De Marchi, M. Thammasack, D. Zemlyanov, S. Kumar, J. Jagielski, L-Q Zheng, C-J. Shih, R. Zenobi, G. De Micheli, D. Baudouin, P.-E. Gaillardon, and C. Copret. “Low Temperature Wet Conformal Nickel Silicide Deposition for Transistor Technology through an Organometallic Approach,” in *ACS Applied Materials & Interfaces*, vol. 9, num. 5, p. 4948-4955, 2017.
304. M. Soeken, L. Amaru, P.-E. Gaillardon and G. De Micheli. “Exact Synthesis of Majority-Inverter Graphs and Its Applications”, in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, num. 11, p. 1842-1855, 2017.

305. X. Tang, E. Giacomini, G. De Micheli and P.-E. Gaillardon. "Circuit Designs of High-Performance and Low-Power RRAM-Based Multiplexers Based on 4T(ransistor)1R(RAM) Programming Structure", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, num. 5, p. 1173-1186, 2017.
306. X. Tang, G. De Micheli and P.-E. Gaillardon. "A High-performance FPGA Architecture Using One-Level RRAM-based Multiplexers", *IEEE Transactions on Emerging Topics in Computing*, Vol.5 Issue 2, 2017.
307. J. Tranchant, J. Sandrini, E. Janod, D. Sacchetto, B. Corraze, M.-P. Besland, J. Ghanbja, G. De Micheli, P.-E. Gaillardon and L. Cario. "Control of Resistive Switching in Mott Memories Based on TiN/AM4Q8/TiN MIM Devices", in *ECS Transactions*, vol. 75, num. 32, p. 3-12, 2017.
308. H. Ghasemzadeh-Mohammadi, P.-E. Gaillardon, J. Zhang, G. De Micheli, E. Sanchez and M. Sanzo-Reorda. "A Fault Tolerant Ripple-Carry Adder with Controllable-Polarity Transistors", in *ACM Journal on Emerging Technologies in Computing Systems*, vol. 13, num. 2, 2017.
309. S. Skalistis, F. Angiolini, A. Simalatsar, G. De Micheli. "Safe and Efficient Deployment of Data-Parallelisable Applications on Many-Core Platforms: Theory and Practice", *IEEE Design and Test*, 2018.
310. A. Biscontinini, M. Thammasack, G. De Micheli and P.-E. Gaillardon. "An FPGA-Based Test System for RRAM Technology Characterization", in *IEEE Transactions on Nanotechnology*, vol. 17, num. 1, pp. 177-183, 2018.
311. N. Aliakbarinodehi, P. Jolly, N. Bhalla, A. Miodek, G. De Micheli, P. Estrela, S. Carrara, "Aptamer-based Field-Effect Biosensor for Tenofovir Detection", *Scientific Reports*, vol. 7, num. 44409, 2018
312. N. Aliakbarinodehi, F. Stradolini, S.A. Nakhjavani, I. Tzouvadaki, I. Taurino, G. De Micheli, S. Carrara, "Performance of Carbon Nano-Scale Allotropes in Detecting Midazolam and Paracetamol in Undiluted Human Serum", *IEEE Sensors Journal*, vol. 18, num. 12, pp. 5073-5081. 2018.
313. F. Criscuolo, I. Taurino, F. Stradolini, S. Carrara, G. De Micheli, "Highly-stable Li<sup>+</sup> ion-selective electrodes based on noble metal nanostructured layers as solid-contacts", *Analytica Chimica Acta* vol. 1027, pp. 22-32. 2018.
314. A. Ibrahim, S. Zhang, F. Angiolini, M. Arditi, S. Kimura, S. Goto, J.P. Thiran, G. De Micheli, "Towards Ultrasound Everywhere: A Portable 3D Digital Back-End Capable of Zone and Compound Imaging", *IEEE Transactions on Biomedical Circuits and Systems* vol. 12, num. 5, pp. 968-981. 2018.
315. T.-H. Lin, T. Margossian, L. Q. Zheng, S. Kumar, I. Morozau, O. Sereda, D. Zemlyanov, C.-J. Shih, R. Zenobi, D. Baudouin, G. De Micheli, P.-E. Gaillardon, C. Copéret, "Conformal Deposition of Conductive Single-Crystalline Cobalt Silicide Layer on Si Wafer via a Molecular Approach", *Chemistry of Materials*, vol. 30, num. 6, pp 2158-2173. 2018.
316. G.V. Resta, Y. Balaaji, D. Lin, I.P. Radu, F. Catthoor, P.-E. Gaillardon, G. De Micheli, "Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors". *ACS Nano* vol. 12, num. 7, p. 7039-7047. 2018.
317. S. Shirinzadeh, M. Soeken, P.-E. Gaillardon, R. Drechsler, "Logic Synthesis for RRAM-Based In-Memory Computing", *IEEE Transactions on Computer-aided design of integrated Circuits and Systems*, vol. 37, num. 7, pp.1422-1435. 2018.
318. M. Soeken, E. Testa, A. Mishchenko, G. De Micheli, "Pairs of majority-decomposing functions", *Information Processing Letters*, vol. 139, pp. 35-38. 2018.
319. F. Stradolini, T. Kilic, A. Di Consiglio, A., M. Ozsoz, G. De Micheli, S. Carrara, "Long-term Monitoring of Propofol and Fouling Effect on Pencil Graphite Electrodes", *Electroanalysis*, vol. 30, num. 7, pp. 1363-1369. 2018.
320. F. Stradolini, T. Kilic, I. Taurino, G. De Micheli, G. Boero, "Cleaning strategy for carbon-based electrodes: Long-term propofol monitoring in human serum, *Sensors and Actuators B*, vol. 269, pp. 304-313. 2018.
321. F. Stradolini, A. Tuoheti, T. Kilic, S. L. Ntella, N. Tamburrano, Z. Huang, G. De Micheli, D. Demarchi, S. Carrara, "An IoT Solution for Online Monitoring of Anesthetics in Human Serum Based on an Integrated Fluidic Bioelectronic System", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, num. 5, pp. 01-09. 2018.
322. X. Tang, E. Giacomini, G. De Micheli, P.-E. Gaillardon, "FPGA-SPICE: A Simulation-Based Architecture Evaluation Framework for FPGAs" *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, pp. 1-14. 2018.
323. X. Tang, E. Giacomini, G. De Micheli, P.-E. Gaillardon, "Post-P&R Performance and Power Analysis for RRAM-based FPGAs", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 8, num. 3, pp. 639-650. 2018.



324. E. Testa, M. Soeken, L. Amaru, W. Haaswijk, G. De Micheli, "Mapping Monotone Boolean Functions into Majority", *IEEE Transactions on Computers*, 2018.
325. I. Tzouvadaki, N. Aliakbarinodehi, D. Dvila Pineda, G. De Micheli, S. Carrara, "Graphene nanowalls for high-performance chemotherapeutic drug sensing and anti-fouling properties", *Sensors and Actuators B: Chemical*, vol. 262, p. 395-403. 2018.
326. E. Testa, M. Soeken, L.G. Amaru, G. De Micheli, "Logic Synthesis for Established and Emerging Computing", *Proceedings of the IEEE*. vol. 107, num. 1, pp 165-184. 2019.
327. F. Criscuolo, I. Taurino, V. A. Dam, F. Catthoor, M. Zevenbergen, S. Carrara, G. De Micheli, "Fast Procedures for the Electrodeposition of Platinum Nanostructures on Miniaturized Electrodes for Improved Ion Sensing" *Sensors*, vol. 19, no. 10, p. 2260, January 2019.
328. X. Tang, E. Giacomini, G. D. Micheli, and P. Gaillardon, "FPGA-SPICE: A Simulation-Based Architecture Evaluation Framework for FPGAs", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 3, pp. 637-650, March 2019.
329. I. Tzouvadaki, J. Zapatero-Rodriguez, S. Naus, G. de Micheli, R. OKennedy, and S. Carrara, "Memristive biosensors based on full-size antibodies and antibody fragments" *Sensors and Actuators B: Chemical*, vol. 286, pp. 346-352, May 2019.
330. I. Tzouvadaki, A. Tuoheti, S. Lorrain, M. Quadroni, M.-A. Doucey, G. De Micheli, D. Demarchi, and S. Carrara, "Multi-panel, on-single-chip Memristive Biosensing" *IEEE Sensors Journal*, 2019 (to appear)
331. G. Resta, A. Leondhart, Y. Balaji, S. De Gendt, P.-E. Gaillardon G. De Micheli. "Devices and Circuits using Novel 2-Dimensional Materials: a Perspective for Future VLSI Systems", *IEEE Transaction on Very Large Scale Integration Systems*, 2019 vol. 27, num. 7, pp 1486-1503, July 2019.
332. M. Soeken, M. Roetteler, N. Wiebe, G. De Micheli, LUT-Based Hierarchical Reversible Logic Synthesis, *IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems*, vol. 38, num. 9, pp. 1675-1688, September 2019.
333. I. Ny Hanitra, F. Criscuolo, N. Pankratova, S. Carrara, G. De Micheli, "Multi-Channel Front-End for Electrochemical Sensing of Metabolites, Drugs, and Electrolytes" *IEEE Sensors Journal*, December 2019.
334. M. Soeken, G. Meuli, B. Schmitt, F. Mozafari, H. Riener and G. De Micheli, "Boolean satisfiability in quantum compilation", *Philosophical Transactions of The Royal Society A-Mathematical Physical And Engineering Sciences*. Vol. 378, num. 2164, p. 20190161, 2019 DOI: 10.1098/rsta.2019.0161.
335. W. Haaswijk, M. Soeken, A. Mischenko, G. De Micheli, "SAT-based Exact Synthesis: Encoding, Topology Families and Parallelism", *IEEE Transactions on CAD*, Vol.39, No.4, April 2020.
336. M. I. Ny Hanitra, F. Criscuolo, N. Pankratova, S. Carrara and G. De Micheli, "Multi-Channel Front-End for Electrochemical Sensing of Metabolites, Drugs, and Electrolytes," *IEEE Sensors Journal*. 2020. Vol. 20, num. 7, p. 3636-3645. DOI: 10.1109/JSEN.2019.2959885.
337. G.De Micheli, A. Domic, M. Di Ventra, M. Roettler and J. Cong, Roundtable Discussion at DAC 2019: Evolutionary Computing or Heuristic Forever?, *IEEE Design and Test*, Vol. 37, No. 3, pp. 100-114, May-June 2020
338. S. Aiassa, Ny Hanitra, G. Sandri, T. Totu, F. Grassi, F. Criscuolo, G. De Micheli, S. Carrara and G. De Micheli, "Continuous monitoring of propofol in human serum with fouling compensation by support vector classifier", *Biosensors and Bioelectronics*, 171, 2020.
339. Z. Chu, M. Soeken, Y. Xia, L. Wang, G. De Micheli, "Advanced Functional Decomposition Using Majority and Its Applications" *Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 39, Issue 8, 2020
340. E. Testa, L. Amaru, M. Soeken, A. Mischchenko, P. Vuillod, P.E. Gaillardon and G. De Micheli, "Extending Boolean Methods for Scalable Logic Synthesis", *IEEE Access*, December 2020.
341. F. Criscuolo, I. Ny Hanitra, S. Aiassa, I. Taurino, N. Oliva, S. Carrara and G. De Micheli, "Wearable multifunctional sweat-sensing system for efficient healthcare monitoring", *Sensors and Actuators B: Chemical*, Volume 328, February 2021.
342. F. Criscuolo, F. Cantu, I. Taurino, S. Carrara, and G. De Micheli, "Wearable electrochemical sensing system for non-invasive monitoring of lithium drug in bipolar disorders", *IEEE Sensors Journal*, vol. 21, no. 8, pp. 9649-9656, April 2021.
343. D. S. Marakkalage, E. Testa, H. Riener, A. Mishchenko, M. Soeken and G. De Micheli, "Three-Input Gates for Logic Synthesis", *IEEE Transactions on CAD*, Vol. 40, No. 10, October 2021, pp. 2184-2188.

344. M.I. Ny Hanitra, F.Criscuolo, S. Carrara and G. De Micheli, "Multi-ion-sensing emulator and multivariate calibration optimization by machine learning models, *IEEE Access*, March 2021.
345. M.I. Ny Hanitra, F.Criscuolo, S. Carrara and G. De Micheli, "Real-Time Multi-Ion Monitoring Front-end with Interface Compensation by Multi-Output Support Vector Regressor," *IEEE Transactions on Biomedical Circuits and Systems (TBIOCAS)*, Vol 15, No. 5, pp.1-12, 2021
346. F. Mozafari, H. Riener, M. Soeken and G. De Micheli, Efficient Boolean Methods for Preparing Uniform Quantum States *IEEE Transactions on Quantum Engineering*, Vol. 2, pp. 1-12, 2021
347. F.Criscuolo, M.I.Ny Hanitra, S.Carrara and G. De Micheli, "All-solid-state ion-selective electrodes: a tutorial for correct practice", *IEEE Sensors*, Vol. 21, No. 20, October 15, 2021
348. G. De Micheli, The emerging majority: Technology and design for superconducting electronics, *IEEE Design and Test*, Vol. 38, No. 6, pp. 79-87, December 2021.
349. G. De Micheli, J.-H. R. Jiang, R. Rand, K. Smith and M. Soeken, "Advances in Quantum Computation and Quantum Technologies: A Design Automation Perspective", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 12, No.3, 2022, pp. 584-601.
350. G. Meuli, M. Soeken and G. De Micheli, "XOR-AND-Inverter Graphs for Quantum Compilation, *Nature partner journal on Quantum Information* 8, 7, January 2022.
351. S.Y. Lee, A. Mishchenko, H. Riener and G. De Micheli, "A Simulation-Guided Paradigm for Logic Synthesis and Verification", *IEEE TCAD* vol. 41, no. 8, pp. 2573-2586, Aug. 2022.
352. F. Mozafari, G. De Micheli, and Y. Yang, "Efficient deterministic preparation of quantum states using decision diagrams", *Physical review A* 106,022617 - Published 29 August 2022
353. S. Rai, A. Tempia Calvino, H. Riener and G. De Micheli, "Utilizing XMG-based Synthesis to Preserve Self-Duality for RFET-Based Circuits", *IEEE TCAD*, Vol. 452, No. 3, March 2023, pp. 914-927.
354. A.Costamagna and G.De Micheli, "Accuracy recovery: A Decomposition Procedure for the Synthesis of Partially-Specified Boolean Functions", *Integration, the VLSI Journal*, 89, 2003, pp.248-260.
355. G. De Micheli, "Strange Loops in Design and Technology: 59th DAC Keynote Speech," in *IEEE Design & Test*, vol. 40, no. 5, pp. 96-103, Oct. 2023.
356. S-Y. Lee, C. L. Ayala and G. De Micheli, "Impact of Sequential Design on The Cost of Adiabatic Quantum-Flux Parametron Circuits," in *IEEE Transactions on Applied Superconductivity*, Vol. 33, No. 8, pp1-9, October 2023.
357. S.-Y. Lee and G. De Micheli, "Heuristic Logic Resynthesis Algorithms at the Core of Peephole Optimization", *IEEE Transactions on Computer Aided Design (TCAD)* Vol. 33, No. 8, pp1-9, October 2023.
358. M. Yu, D. Marakkellage and G. De Micheli, "Logic Synthesis Unleashes Efficient Secure Computation", *MPDI Cryptography*, 2023, 7, 61.
359. D. Marakkellage and G. De Micheli, "Fanout-Bounded Logic Synthesis for Emerging Technologies", *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 43. No. 5, May 2024, pp. 1415-1428.
360. R. Bairakulov and Giovanni De Micheli, Superconductive Electronics a 25-year review, *IEEE CAS Magazine*, Second Quarter 2024.
361. F. Meng et al., "Benchmarking of Scaled Majority-Logic-Synthesized Spintronic Circuits Based on Magnetic Tunnel Junction Transducers," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, (to appear)
362. A.Tempia Calvino, G. De Micheli, A. Mishchenko and R. Brayton, Enhancing Delay-driven LUT Mapping with Boolean Decomposition, *IEEE Transactions on Computer Aided Design (TCAD)* (to appear)
363. C.Meng, A. Mischchenko, W. Quian and G. De Micheli, Efficient Resubstitution-Based Approximate Logic Synthesis, *IEEE Transactions on Computer Aided Design (TCAD)*, (early access)
364. S.-Y. Lee, A. Tempia-Calvino, R. Riener and G. De Micheli, Technology Legalization and Optimization for Adiabatic Quantum-Flux Parametron, *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 44, No. 1, January 2025, pp. 186-199.
365. A. Costamagna, A. Tempia Calvino, A. Mishchenko and G. De Micheli, "Area-Oriented Resubstitution for Networks of Look-Up Tables" *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 44, No.1, January 2025, pp. 186-199 (early access).
366. F. Meng S.-Y. Lee, O.Zografos, et al., "Benchmarking of Scaled Majority-Logic-Synthesized Spintronic Circuits Based on Magnetic Tunnel Junction Transducers," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 72, No.1, January 2025, pp. 135-142.

367. A. Tempia Calvino, G. De Micheli, A. Mishchenko and R. Brayton, "Enhancing Delay-driven LUT Mapping with Boolean Decomposition", *IEEE TCAD* Vol 44, No. 3, March 2025, pp. 1017-1030

#### Editorials (invited papers)

368. G. De Micheli, "High-Level Synthesis of Digital Circuits," Editorial, *IEEE Design & Test*, October 1990, pp. 6-7.
369. G. De Micheli, "Computer-Aided Design for Hardware/Software Co-design," *IEEE Computer*, January 1993, pp. 85-87.
370. G. De Micheli, "Hardware/Software Co-design," Editorial, *IEEE Micro*, pp.9-10, August 1994.
371. G. De Micheli "Progettazione di Sistemi Digitali Assistita da Calcolatore," *Alta Frequenza*, Vol. 8, No. 3, May-June 1996, Vol.8, No. 3, p. 3 (in Italian).
372. G. De Micheli, "Scanning the Issue: Hardware/Software Co-design," Editorial, *IEEE Proceedings*, Vol. 85, No. 3, March 1997, pp.347-348.
373. A. Ivanov and G. De Micheli, "The network on Chip paradigm in Practice and Research", *IEEE Design and test of Computers*, Vol. 22, No. 5, September 2005, pp. 399-403.
374. G. De Micheli and A. Acquaviva, "Resource Management for MPSoCs - Is Our Software Ready for it?," *Frontier Journal* Vol. 4, No. 3, March 07.
375. G. De Micheli, "Designing Micro- and Nanosystems for a Safer and Healthier Tomorrow," *IEEE Design & Test of Computers*, vol. 25, no. 5, pp. 488-494, 2008.
376. P. Mayor, P. Bradley, and G. De Micheli, "Nano-Tera.ch: Engineering Complex Systems for Health, Security, and the Environment," *Solid-State Circuits Magazine*, vol. 2 Issue 3, Summer 2010, pp. 87-92, 2010.
377. G. De Micheli, "Chip Challenge," *IEEE Solid-State Circuits Magazine*, vol. 2, no. 4, pp. 22-26, 2010.
378. G. De Micheli, S. Mitra and M. Ogorzalek. "Editorial: Special Issue on Nanocircuits and Systems", in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, num. 4, p. 653-657, 2012.
379. G. De Micheli, C. Boero and S. Carrara, "Implantable devices: the future of blood monitoring? (Editorial)", in *FSG Future Medicine Clinical Practice*, vol. 10, num. 4, p. 385-388, 2013.
380. P.-E. Gaillardon, G. De Micheli, I. O'Connor, S. Mitra and T. Ernst, "Introduction to the Special Section on Functionality-Enhanced Devices", in *IEEE Transactions on Nanotechnology*, vol. 13, num. 6, p. 1019-1019, 2014.
381. S. Basu, R. Bryant, G. De Micheli, T. Theis and L. Whitman, "NonSilicon, Non-von Neumann Computing - Part 1", *Proceedings of IEEE*, Vol 107, No.1, January 2019, pp. 11-18.
382. S. Basu, R. Bryant, G. De Micheli, T. Theis and L. Whitman, "NonSilicon, Non-von Neumann Computing - Part 2", *Proceedings of IEEE*, Vol 108, No. 8, August 2020, pp 121-1217.
383. G. De Micheli, J.-H. R. Jiang, R. Rand, K. Smith and M. Soeken, "Editorial: Design and Automation for Quantum Computation and Quantum Technologies", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 12, No.3, 2022, pp. 581-583.

#### Conference Proceedings (fully refereed and with unlimited distribution)

384. G. De Micheli, A. Sangiovanni-Vincentelli and A. Newton, "New Algorithms for Timing Analysis of Large Circuits," *ISCAS, Proceedings of the International Symposium on Circuit and Systems*, Houston, TX, April 1980, pp. 439-443.
385. G. De Micheli and A. L. Sangiovanni-Vincentelli, "Numerical Properties of Algorithms for the Timing Analysis of MOS VLSI Circuits," *Proceedings of the European Conference on Circuit Theory and Design*, Den Haag (NL), August 1981, and *Memorandum UCB/ERL*, No. 81/25.
386. G. De Micheli and A. Sangiovanni-Vincentelli, "Multiple Folding of Programmable Logic Arrays," *ISCAS, Proceedings of the International Symposium on Circuits and Systems*, Newport Beach, CA, May 1983, pp. 1026-1029.
387. G. De Micheli and A. Sangiovanni-Vincentelli, "PLEASURE: A Computer Program for Simple-Multiple Constrained-Unconstrained Folding of Programmable Logic Arrays," *DAC, Proceedings of the 20th Design Automation Conference*, Miami Beach, FL, June 1983, pp. 530-537. (DAC 83 Best Paper Award). (Cross-listed as Journal No. 57.)

388. G. De Micheli and M. Santomauro, "Topological Partitioning of Programmable Logic Arrays," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, September 1983, pp.182-184.
389. G. De Micheli and A. L. Sangiovanni-Vincentelli and T. Villa, "Computer Aided Synthesis of PLA-based Finite State Machines," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, September 1983, pp. 154-157.
390. G. De Micheli, "Optimal Encoding of Control Logic," *ICCD, Proceedings of the International Conference on Circuits and Computer Design*, Rye, NY, October 1984, pp. 16-22.
391. G. De Micheli, R. Brayton and A. Sangiovanni-Vincentelli, "KISS: A Program for Optimal State Assignment of Finite State Machines," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1984, pp. 209-211.
392. R. Rudell, A. Sangiovanni-Vincentelli and G. De Micheli, "A Finite-State Machine Design System," *ISCAS, Proceedings of the International Symposium on Circuits and Systems*, Kyoto, Japan, June, 1985, pp. 647-650.
393. R. Brayton, N. Brenner, C. Chen, G. De Micheli, C. McMullen and R. Otten, "The Yorktown Silicon Compiler," *ISCAS, Proceedings of the International Symposium on Circuits and Systems*, Kyoto, Japan, June, 1985, pp. 391-394.
394. R. Brayton, C. Chen, G. De Micheli, J. Katzenelson, C. McMullen, R. Otten and R. Rudell, "A Microprocessor Design Using the Yorktown Silicon Compiler," *ICCD, Proceedings of the International Conference on Circuits and Computer Design*, Rye, NY, October 1985, pp. 225-231.
395. G. De Micheli, "Symbolic Minimization of Logic Functions," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1985, pp. 293-296.
396. G. De Micheli, "Performance-oriented Synthesis in the Yorktown Silicon Compiler," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1986, pp. 138-142.
397. G. De Micheli and D. Ku, "Hercules, a System for High-Level Synthesis," *DAC, Proceedings of the Design Automation Conference*, Anaheim, CA, June 1988, pp. 483-488.
398. F. Mailhot and G. De Micheli, "Automatic Layout and Optimization of Static CMOS Cells," *ICCD, Proceedings of the International Conference on Circuit and Computer Design*, Rye, NY, October 1988, pp. 180-185.
399. G. Bewick, P. Song, G. De Micheli and M. Flynn, "Approaching a Nanosecond: A 32 Bit Adder," *ICCD, Proceedings of the International Conference on Circuit and Computer Design*, Rye, NY, October 1988, pp. 221-226.
400. V. Rampa and G. De Micheli, "Computer Aided Synthesis of a Bi-dimensional Discrete Transform Chip," *ISCAS, Proceedings of the International Symposium on Circuit and Systems*, Portland, OR, May 1989, pp.220-225, and *CSL Report*, CSL-TR-88-363.
401. T. Klein and G. De Micheli, "Algorithms for Synchronous Logic Synthesis," *ISCAS, Proceedings of the International Symposium on Circuit and Systems*, Portland, OR, pp. 756-761, May 1989.
402. M. Ligthart, A. Bechtolsheim, G. De Micheli and A. El Gamal, "Design of a Digital Audio Input Output Chip," *CICC, Proceedings of the Custom Integrated Circuit Conference*, San Diego, CA, May 1989, pp. 15.1.1-15.1.6.
403. G. De Micheli, "Synthesis Systems for Digital Design," *SBMICRO, Proceedings of the Brazilian Microelectronic Conference*, Porto Alegre, Brazil, July 1989, pp. 481-495.
404. D. Wong, G. De Micheli and M. Flynn, "Designing High-Performance Digital Circuits using Wave Pipelining," *VLSI 89 Conference*, Munchen, W. Germany, August 1989, pp 241-252.
405. D. Wong, G. De Micheli and M. Flynn, "Inserting Active Delay Elements for Wave Pipelining," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1989, pp. 270-273, and *CSL Report*, CSL-TR-89-386.
406. G. De Micheli, and R. Yip, "Logic Transformations for Synchronous Logic Synthesis," *IEEE Hawaii Conference on System Science*, Kona, HI, January 1990, pp. 407-415.
407. F. Mailhot, and G. De Micheli, "Technology Mapping with Boolean Matching," *European Design Automation Conference*, Glasgow, Scotland, March 1990, pp. 212-216.
408. M. Damiani and G. De Micheli, "Synchronous Logic Synthesis: Circuit Specification and Optimization Algorithms," *ISCAS, Proceedings of the International Symposium on Circuit and Systems*, New Orleans, May 1990, pp. 2566-2570.

409. D. Ku and G. De Micheli, "High-level Synthesis and Optimization Strategies in Hercules and Hebe," *Eurasic, Proceedings of the European Conference on ASIC Design*, Paris, May 1990, pp. 124-129. (Cross-listed as Book Chapter No. 17.)
410. D. Ku and G. De Micheli, "Relative Scheduling Under Timing Constraints," *Design Automation Conference*, Orlando, Florida, June 1990, pp. 59-64 and *CSL Report*, CSL-TR-89-40.
411. M. Damiani and G. De Micheli, "Observability Don't Cares and Boolean Relations," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1990, pp. 502-506.
412. R. Gupta and G. De Micheli, "Partitioning of Functional Models of Synchronous Digital Systems," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1990, pp. 216-220.
413. D. Filo, J. Yang, F. Mailhot and G. De Micheli, "Technology Mapping for a Multiple-Output RAM-Based Field Programmable Gate Array," *EDAC, Proceedings of the European Design Automation Conference*, Amsterdam, February 1991, pp. 534-538.
414. G. De Micheli, "Technology Mapping for Digital Circuits," *COMPEURO, Proceedings of the European Computer Conference*, Bologna, Italy, May 1991, pp. 580-586.
415. D. Ku, D. Filo and G. De Micheli, "Optimizing Control by Resynchronization of Operations," *Design Automation Conference*, San Francisco, June 1991, pp. 366-371.
416. S. Ercolani and G. De Micheli, "Technology Mapping for Electrically Programmable Gate Arrays," *Design Automation Conference*, San Francisco, June 1991, pp. 234-239.
417. D. Kastle and G. De Micheli, "An Image Decoding ASIC for Space Based Applications," *Eurasic 91*, Paris, May 1991, pp. 86-91.
418. M. Ishikawa and G. De Micheli, "A Module Selection Algorithm for High-Level Synthesis," *ISCAS, Proceedings of the International Symposium on Circuit and Systems*, Singapore, June 1991, pp. 1777-1780.
419. D. Wong, G. De Micheli, M. Flynn and R. Huston, "A Bipolar Population Counter Using Wave Pipelining to Achieve 2.5x Normal Clock Frequency," *ISSC, Proceedings of the International Solid State Conference*, San Francisco, February 1992, pp. 56-57.
420. M. Damiani and G. De Micheli, "Synthesis and Optimization of Synchronous Logic Circuits from Recurrence Equations," *EDAC, Proceedings of the European Design Automation Conference*, Brussels, March 1992, pp. 226-231.
421. R. Gupta and G. De Micheli, "System-level Synthesis using Re-programmable Components," *EDAC, Proceedings of the European Design Automation Conference*, Brussels, March 1992, pp. 2-7.
422. M. Damiani and G. De Micheli, "Recurrence Equations and the Optimization of Synchronous Logic Circuits," *DAC, Proceedings of the Design Automation Conference*, Anaheim, June 1992, pp. 556-561.
423. R. Gupta, C. Coelho and G. De Micheli, "Synthesis and Simulation of Digital Systems Containing Interacting Hardware and Software Components," *DAC, Proceedings of the Design Automation Conference*, Anaheim, June 1992, pp. 225-230.
424. P. Siegel, G. De Micheli and D. Dill, "Automatic Technology Mapping for Generalized Fundamental-Mode Asynchronous Designs," *DAC, Proceedings of the Design Automation Conference*, Dallas, June 1993, pp. 61-67, and *CSL Report* CSL-TR-93-580. (DAC 93 Best Paper Award).
425. M. Damiani, J. Yang and G. De Micheli, "Optimization of Combinational Logic Circuits Based on Compatible Gates," *DAC, Proceedings of the Design Automation Conference*, Dallas, June 1993, pp. 631-636.
426. J. Burch, D. Dill, E. Wolf and G. De Micheli, "Modeling Hierarchical Combinational Circuits," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, Santa Clara, CA, November 1993, pp. 612-617.
427. J. Yang, M. Damiani and G. De Micheli, "Scheduling with Environmental Constraints Based on Automata Representations," *EDAC, Proceedings of the European Conference on Computer Aided Design*, Paris, 1994, pp. 495-501.
428. L. Benini and G. De Micheli, "State Assignment for Low Power Dissipation," *CICC, Proceedings of the Custom Integrated Circuit Conference*, San Diego, CA, May 1994, pp. 7.4.1-7.4.4.
429. J. Fron, J. Yang, M. Damiani and G. De Micheli, "A Synthesis Framework Based on Trace and Automata Theory," *ISCAS, Proceedings of the International Symposium on Circuits and Systems*, London (UK), May 1994, pp. 291-294.

430. R. Gupta, and G. De Micheli, "Constrained Software Generation for Hardware-Software Systems," *Proceedings of ACM/IEEE Hardware-Software Co-design*, September 1994 pp.56-64.
431. D. Filo, J. Yang, V. Mooney, and G. De Micheli, "Redesigning Hardware-Software Systems," *Proceedings of ACM/IEEE Hardware-Software Co-design*, September 1994 pp. 116-123.
432. C.Coelho and G. De Micheli, "Dynamic Scheduling and Synchronization Synthesis of Concurrent Digital Systems Under System-level Constraints," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1994, pp. 175-181.
433. P. Siegel and G. De Micheli, "Decomposition Methods for Library Binding of Speed-Independent Synchronous Designs," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1994, pp 558-565.
434. L. Benini and G. De Micheli, "Transformation and Synthesis of FSMs for Low-Power Gated-Clock Implementation," *Proceedings of the International Symposium on Low Power Design*, pp. 21-26, April 1995, and reprinted in A. Chandrakasan and R. Brodersen, *Low-Power CMOS Design*, pp. 554-559.
435. A.Bogliolo, B. Riccò, L. Benini and G. De Micheli, "Accurate Logic-Level Power Estimation," *Digest of the International Symposium on Low Power Electronics*, San Jose, CA, pp. 40-41, October 1995.
436. M.Favalli, L. Benini, and G.De Micheli, "Design for Testability for Gated Clock FSMs," *EDTC, Proceedings of the European Design and Test Conference*, Paris, 1996, pp.589-596.
437. A Bogliolo, L. Benini, G. De Micheli and B. Riccò, "Gate-Level Current Waveform Simulation of CMOS Integrated Circuits," *Digest of the International Symposium on Low Power Electronics and Design*, Monterey, 1996, pp. 109-112.
438. P. Vuillod, L. Benini, A. Bogliolo and G. De Micheli, "Clock Skew Optimization for Peak Current Reduction," *Digest of the International Symposium on Low Power Electronics and Design*, Monterey, 1996, pp. 265-270.
439. L. Benini, A. Bogliolo, M. Favalli and G. De Micheli, "Regression Models for Behavioral Power Estimation", *PATMOS - Power Timing Modeling Optimization Simulation Workshop*, Bologna, 1996, pp. 179-188.
440. V. Mooney, T. Sakamoto, C.Coelho and G. De Micheli "Synthesis from Mixed Specifications," *EURODAC, Proceedings of the European Design Automation Conference*, Geneva, 1996, pp. 114-119.
441. L. Benini, A. Bogliolo and G. De Micheli, "Distributed EDA Tool Integration: the PPP Paradigm," *ICCD, Proceedings of the International Conference on Circuits and Computer Design*, Austin, TX, October 1996, pp. 448-453.
442. L. Benini, P.Vuillod, C.Coelho and G. De Micheli, "Synthesis of Low-Power Selectively-Clocked systems from High-Level Specifications," *ISSS, Proceedings of the International Symposium on System Synthesis*, La Jolla, CA, November 1996, pp.57-64.
443. L. Benini, G. De Micheli, E. Macii, D. Sciuto and C.Silvano, "Asymptotic Zero-Transition Activity Encoding for Address Busses in Low-Power Microprocessor-Based Systems," *Proceedings of the Great Lakes Symposium on VLSI*, March 1997, pp.77-82.
444. L. Benini, G. De Micheli, E. Macii, M. Poncino and R.Scarsi, "Symbolic Synthesis of Clock-Gating Logic for Power Optimization of Control-Oriented Synchronous Networks", *EDTC, Proceedings of the European Design and Test Conference*, Paris, 1997, pp. 514-520.
445. A. Bogliolo, L. Benini and G. De Micheli, "Adaptive Least Mean Square Behavioral Power Modeling", *EDTC, Proceedings of the European Design and Test Conference*, Paris, 1997, pp. 404-410.
446. V. Mooney, T. Sakamoto, and G. De Micheli "Run-Time Scheduler Synthesis for Hardware-Software Systems and Application to Robot Control Design," *CODES/CASHE, Proceedings of the International Workshop on Hardware/Software Co-design*, Braunschweig, 1997, pp. 95-99.
447. L. Benini, G. De Micheli, E. Macii, M. Poncino and S. Quer, "System-Level Power Optimization of Special Purpose Applications: The Beach Solution," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 1997, pp. 24-29.
448. P. Vuillod, L. Benini and G. De Micheli, " Re-mapping for Low Power under Timing Constraints," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 1997, pp. 287-292.
449. C. Coelho, A. Fernandes and G.De Micheli, "Reducing Coding Style Effects in High-Level Specifications," *SBCCI Proceedings of X Brazilian Symposium on Integrated Circuit Design*, Gramado (Brazil), pp. 273-282, 1997.

450. V. Mooney and G. De Micheli, "Real Time Analysis and Priority Scheduler Generation for Hardware-Software Systems with a Synthesized Run-Time System," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1997, pp. 605-612.
451. P.Vuillod, L.Benini and G. De Micheli, "Generalized Matching from Theory to Applications," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1997, pp.13-20.
452. L.Benini, G. De Micheli, E. Macii, M. Poncino, and R.Scarsi, "Fast power estimation for deterministic input streams," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1997, pp. 494-501.
453. L. Benini, G. De Micheli, A. Macii, E. Macii, M. Poncino, "Reducing Power Consumption of Dedicated Processors Through Instruction Set Encoding", *GLS-VLSI-98: IEEE/ACM 8th Great Lakes Symposium on VLSI*, pp. 8-12, Lafayette, Louisiana, February 1998.
454. L. Benini, G. De Micheli, A. Liyo, E. Macii, G. Odasso, M. Poncino, "Timed Supersetting and the Synthesis of Large Telescopic Units", *GLS-VLSI-98: IEEE/ACM 8th Great Lakes Symposium on VLSI*, pp. 331-337, Lafayette, Louisiana, February 1998.
455. A. Bogliolo, L. Benini and G. De Micheli, "Characterization-Free Behavioral Power Modeling," *DATE, Proceedings of the Design, Automation and Test in Europe Conference*, 1998, pp. 767-773.
456. L. Benini, G. De Micheli, E. Macii, D. Sciuto and C. Silvano, "Address Bus Encoding Techniques for System-Level Power Optimization," *DATE, Proceedings of the Design, Automation and Test in Europe Conference*, 1998, pp. 861-866.
457. H. Kapadia, G. De Micheli and L. Benini, "Reducing Switching Activity on Datapath Buses with Control-Signal Gating," *CICC - Proceedings of the Custom Integrated Circuit Conference*, pp. 589-592, 1998.
458. L. Benini, F. Vermeulen and G. De Micheli, "Finite-State Machine partitioning for low power," *ISCAS, Proceedings of the International Symposium on Circuits and Systems*, Vol II, pp. 5-9, June 1998.
459. G. Paleologo, L. Benini, A. Bogliolo and G. De Micheli, "Policy Optimization for Dynamic Power Management," *DAC - Proceedings of the Design Automation Conference*, 1998, pp. 182-187.
460. J. Smith and G. De Micheli, "Automated Composition of Hardware Components," *DAC - Proceedings of the Design Automation Conference*, 1998, pp.14-19.
461. L. Benini, G. De Micheli, A. Liyo, E. Macii, G. Odasso, M. Poncino, "Computational Kernels and their Application to Sequential Power Optimization," *DAC - Proceedings of the Design Automation Conference*, 1998, pp.764-769.
462. M. Platzner and G. De Micheli, "Acceleration of Satisfiability Algorithms by Reconfigurable Hardware," *FPL '98, Proceedings International Workshop of Field Programmable Logic and Applications*, published as R. Hartenstein and Andres, Editors, Lecture Notes in Computer Science, No. 1482, Springer, 1998, pp. 69-78.
463. V. Mooney, D. Ruspini, O. Kathib and G. De Micheli, "Hardware/Software Run-Time Systems and Robotics: A Case Study," *Proceedings of EUROMICRO Conference*, Västerås, Sweden, 1998, pp. 162-167.
464. S. Minato and G. De Micheli, "Finding all Simple Disjunctive Decompositions Using Irredundant Sum-of-Products Forms," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1998, pp. 111-117.
465. L. Séméria and G. De Micheli, "SpC: Synthesis of Pointers in C, Application of Pointer Analysis to the Behavioral Synthesis from C," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1998, pp. 340-346.
466. J. Smith and G. De Micheli, "Polynomial Methods for Component Matching and Verification," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1998, pp. 678-685.
467. L. Benini, A. Bogliolo and G. De Micheli, "Dynamic Power Management of Electronic Systems," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1998, pp. 696-702.
468. J. Smith and G. De Micheli, "Polynomial Methods for Allocating Complex Components," *DATE, Proceedings of the Design, Automation and Test in Europe Conference*, 1999, pp. 217-222.
469. Eui-Young Chung, L. Benini and G. De Micheli, "Dynamic Power Management for Non-Stationary Service Requests," *DATE, Proceedings of the Design, Automation and Test in Europe Conference*, 1999, pp. 77-81.

470. L. Benini, G. De Micheli, A. Macii, E. Macii and R. Scarsi, *Glitch Power Minimization by Gate Freezing*, DATE, Proceedings of the Design, Automation and Test in Europe Conference, 1999, pp. 163-167.
471. G. De Micheli, *Hardware Synthesis from C/C++ Models*, DATE, Proceedings of the Design, Automation and Test in Europe Conference, 1999, pp.382-383.
472. Yung-Hsiang Lu and G. De Micheli, "Adaptive Hard Disk Power Management on Personal Computers," *Proceedings of the IEEE Great Lakes Symposium*, 1999, pp. 50-53.
473. Yung-Hsiang Lu, T. Šimunić and G. De Micheli, "Software Controlled Power Management," *CODES, Proceedings of the IEEE Hardware/Software C-design Workshop*, 1999, pp. 157-161.
474. T. Šimunić, L. Benini and G. De Micheli, "Cycle-Accurate Simulation of Energy Consumption in Embedded Systems," *DAC - Proceedings of the Design Automation Conference*, 1999, pp. 867-872.
475. L. Benini, G. De Micheli, E. Macii, G. Odasso and M. Poncino, "Kernel-based Power Optimization of RTL Components: Exact and Approximate Extraction Algorithms," *DAC - Proceedings of the Design Automation Conference*, 1999, pp. 247-252.
476. T. Šimunić, L. Benini and G. De Micheli, "Energy-Efficient Design of Battery-Powered Embedded Systems," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 1999, pp. 212-217.
477. A. Bogliolo, L. Benini, G. De Micheli and B. Riccò, "Efficient Switching Activity Computation During High-level Synthesis of Control-Dominated Designs," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 1999, pp. 127-132.
478. L. Benini, G. De Micheli, "System-Level Power Optimization: Techniques and Tools," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 1999, pp. 288-293.
479. J. Smith and G. De Micheli, "A Methodology for Synthesis with Re-usable Components from Arithmetic Specifications," *ECCTD, Proceedings of the European Conference on Circuit Theory and Design*, Stresa, 1999, Vol. 2, pp. 1195-1198.
480. Y. Sasaki and G. De Micheli, "Cross-talk Delay Analysis using Relative Window Method," *IEEE International ASIC/SOC Conference* 1999, pp. 9-13.
481. E.Y. Chung, L. Benini and G. De Micheli, "Dynamic Power Management using Adaptive Learning Tree," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 1999, pp. 274-279.
482. T. Šimunić, L. Benini, and G. De Micheli, "Event-Driven Power Management of Portable Systems," *ISSS, Proceedings of International Symposium on System Synthesis*, pp. 18-23, November 1999.
483. Y. Lu, E.Y. Chung, T. Šimunić, L. Benini and G. De Micheli, "Quantitative Comparison of Power Management Algorithms," *DATE, Proceedings of Design Automation and Test in Europe*, pp.20-26, March 2000.
484. T. Šimunić, L. Benini, P. Glynn and G. De Micheli, "Dynamic Power Management of Portable Systems Using Semi-Markov Decision Processes," *DATE, Proceedings of Design Automation and Test in Europe*, p. 736, March 2000.
485. L. Séméria, K. Sato and G. De Micheli, "Resolution of Dynamic Memory Allocation and Pointers for the Behavioral Synthesis from C," *DATE, Proceedings of Design Automation and Test in Europe*, pp. 312-319, March 2000.
486. Y. Lu, L. Benini and G. De Micheli, "Low-Power Task Scheduling for Multiple Devices," *CODES, Proceedings of the IEEE Hardware/Software C-design Workshop*, pp. 39-43, 2000.
487. Y. Lu, L. Benini, and G. De Micheli, "Operating-System Directed Power Reduction," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 2000, pp. 37-42.
488. T. Šimunić, H. Vikalo, P. Glynn and G. De Micheli "Energy Efficient Design of Portable Wireless Systems," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 2000, pp. 49-54.
489. T. Šimunić, L. Benini, P. Glynn and G. De Micheli, "Dynamic Power Management for Portable Systems," *MOBICOM, Proceedings of International Conference on Mobile Computing and Networking*, August 2000, pp. 11-19.
490. T. Šimunić, L. Benini, G. De Micheli and M. Hans, "Source Code Optimization and Profiling of Energy Consumption in Embedded Systems," *ISSS, Proceedings of International Symposium on System Synthesis*, September 2000, pp. 193-198.
491. Y. Lu, L. Benini, and G. De Micheli "Requester-Aware Power Reduction," *ISSS, Proceedings of International Symposium on System Synthesis*, September 2000. pp 18-23.



492. T.T Ye and G. De Micheli, "Data Path Placement with Regularity," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 2000, pp. 264-270
493. T.Zhang, G. De Micheli and L. Benini, "Component Selection and Matching for IP-Based Design," *DATE, Proceedings of Design Automation and Test in Europe*, March 2001, pp.40-46.
494. T. Šimunić, L. Benini, A. Acquaviva, P. Glynn and G. De Micheli, "Dynamic Voltage Scaling and Power Management for Portable Systems," *DAC - Proceedings of the Design Automation Conference*, June 2001, pp. 524-529.
495. A. Peymandoust and G. De Micheli, "Using Symbolic Algebra in Algorithmic DSP Synthesis," *DAC - Proceedings of the Design Automation Conference*, 2001, pp. 277-282.
496. E.Y. Chung, L. Benini and G. De Micheli, "Automatic Source Code Specialization for Energy Reduction," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 2001, pp. 80-83.
497. L. Benini and G. De Micheli, "Powering Networks on Chips: Energy-efficient and reliable interconnect design for SoCs," *ISSS, Proceedings of the International Symposium on System Synthesis*, Montreal, October 2001, pp. 33-38.
498. E.Y. Chung, L. Benini and G. De Micheli, "Source Code Transformation based on Software Cost Analysis," *ISSS, Proceedings of the International Symposium on System Synthesis*, Montreal, October 2001, pp. 153-158.
499. P. Panda, L. Séméria and G. De Micheli, "Cache-Efficient Memory Layout of Aggregate Data-Structures," *ISSS, Proceedings of the International Symposium on System Synthesis*, Montreal, October 2001, pp. 101-106.
500. A. Peymandoust and G. De Micheli, "Symbolic Algebra and Timing-Driven Data-Flow Synthesis," *ICCAD, Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 2001, pp. 300-305.
501. L. Benini and G. De Micheli, "Networks on Chip: A New Paradigm for Systems on Chip Design," *DATE, International Conference on Design and Test Europe Paris*, 2002, pp. 418-419.
502. D. Bertozzi, L. Benini and G. De Micheli, "Low-Power Error-Resilient Encoding for On-chip Data Busses," *DATE, International Conference on Design and Test Europe Paris*, 2002, pp. 102-109.
503. A. Peymandoust, T. Šimunić and G. De Micheli, "Low-Power Embedded Software Optimization using Symbolic Algebra," *DATE, International Conference on Design and Test Europe Paris*, 2002, pp. 1052-1058.
504. A. Peymandoust, T. Šimunić and G. De Micheli, "Complex Library Mapping for Embedded Software using Symbolic Algebra," *DAC - Proceedings of the Design Automation Conference*, 2002, pp. 325-330.
505. T. Ye and G. De Micheli, "Analysis of Power Consumption on Switch Fabrics in Network Routers," *DAC - Proceedings of the Design Automation Conference*, 2002, pp. 524-530.
506. E.Y. Chung, L. Benini and G. De Micheli, "Contents Provider assisted Dynamic Voltage Scaling for Low Energy MultiMedia Applications," *ISLPED, IEEE Symposium on Low Power Electronics and Design*, 2002, pp. 42-47.
507. T. Ye, S. Chaudhuri, H. Savoj and G. De Micheli, "Physical Synthesis for ASIC Datapath Circuits," *ISCAS, International Symposium on Circuits and Systems*, Vol. 3, pp. 365-368, Tempe, 2002.
508. F. Worm, P. Ienne, P. Thiran and G. De Micheli, "An Adaptive Low-power Transmission Scheme for On-chip Networks," *ISSS, Proceedings of the International Symposium on System Synthesis*, Kyoto, October 2002, pp. 92-100.
509. G. De Micheli "Designing Robust System with Uncertain Information," *ASPDAC, Proceedings of the Asian Pacific Design Automation Conference*, pp. vi-vii, January 2003.
510. T. Ye, L. Benini and G. De Micheli, "Packetized On-Chip Interconnect Communication Analysis," *DATE, International Conference on Design and Test Europe*, 2003, pp. 344-349.
511. T. Taoe Ye and G. De Micheli, "Physical Planning for On-Chip Multiprocessor Networks and Switch Fabrics," *ASAP, Proceedings of the International Conference on Application-specific Systems, Architectures and Processors*, den Haag, 2003, pp.97-107.
512. A. Peymandoust, L. Pozzi, P. Ienne and G. De Micheli, "Automatic Instruction Set Extension and Utilization for Embedded Processors," *ASAP, Proceedings of the International Conference on Application-specific Systems, Architectures and Processors*, den Haag, 2003, pp. 108-118.

513. G. De Micheli "Robust System Design with Uncertain Information," *Memocode, Proceedings of the IEEE/ACM Conference on Methods and Models for Co-Design*, p. 283, June 2003.
514. A. Jalabert, S. Murali, L. Benini, G.De.Micheli, "XpipesCompiler: A Tool for Instantiating Application Specific Networks on Chip," *DATE, International Conference on Design and Test Europe*, 2004, pp. 884-889.
515. S. Murali, G.De Micheli, "Bandwidth Constrained Mapping of Cores onto NoC Architectures," *DATE, International Conference on Design and Test Europe*, 2004, pp.896-901.
516. S. Yoon, C. Nardini, L. Benini and G. De Micheli "Enhanced pClustering and its Applications to Gene Expression Data," *BIBE*, 2004, pp. 275-282.
517. G. De Micheli, "Reliable Communication in Systems on Chip," *DAC, Design Automation Conference*, 2004, p. 77.
518. S. Murali and G. De Micheli, "SUNMAP: A tools for Automatic Topology Selection and Generation for NOCs," *DAC, Design Automation Conference*, 2004, pp. 914-919.
519. K. Mihic, T. Šimunić, and G. De Micheli, "Reliability and Power Management of Integrated Systems," *DSD - Euromicro Symposium on Digital System Design*, 2004, pp. 5-11.
520. S. Yoon and G.De Micheli, "An Application of Zero-Suppressed Binary Decision Diagrams to Clustering Analysis of DNA Microarray Data," *EMBS - Proceedings of the 26th Annual International Conference*, 2004, pp. 2925-2929.
521. T. Simunic, W. Qadeer, G. De Micheli, "Managing Heterogeneous Wireless Environments via Hotspot Servers" *MMCN - Proceedings of the Multimedia Computing and Networking Conference*, pp. 110-123, 2005.
522. R. Tamhankar, S. Murali and G. De Micheli, "Performance Driven reliable Link for Networks on Chip," *ASPDAC - Proceedings of the Asian Pacific Conference on Design Automation*, Shahghai, 2005, pp. 749-754.
523. S. Murali, L. Benini and G. De Micheli, "Mapping and Physical Planning of Networks on Chip Architectures with Quality of Service Guarantees," *ASPDAC - Proceedings of the Asian Pacific Conference on Design Automation*, Shahghai, 2005, pp. 27-32.
524. S.Stergios, S. Murali, F. Angiolini, D. Bertozzi, S. Carta, L. Raffo and G. De Micheli, "xPipesLite: A Synthesis-Oriented Design Flow for Networks on Chip," *DATE, International Conference on Design and Test Europe*, 2005, pp. 1188-1193.
525. N. Genko, D.Atienza, J. Mendias, R. Hermida, G. De Micheli and F. Catthoor, "A Complete Network-on-Chip Emulation Framework," *DATE, International Conference on Design and Test Europe*, 2005, pp. 246-251.
526. S. Murali and G. De Micheli, "An Application-Specific Design Methodology for ST-Bus Crossbar Generation," *DATE, International Conference on Design and Test Europe*, 2005, pp. 1176-1181.
527. N. Genko, D. Atienza, G. De Micheli, L. Benini, J. Mendias, R. Hermida, and F. Catthoor, "A Novel Approach for Network on Chip Emulation," *ISCAS - International Symposium on Circuits and Systems*, Kobe, 2005, pp. 2365-2368.
528. S. Yoon, L. Benini, and G. De Micheli, "Finding Co-Clusters of Genes and Clinical Parameters," *EMBC - Engineering in Medicine and Biology Conference*, no. 11.3.1.4, 2005.
529. S. Yoon and G. De Micheli, "Prediction and Analysis of Human MicroRNA Regulatory Modules," *EMBC - Engineering in Medicine and Biology Conference*, no. 11.3.2.6, 2005.
530. S. Yoon and G. De Micheli, "Prediction of Regulatory Modules Comprising MicroRNAs and Target Genes," *ECCB - European Conference on Computational Biology* 2005, Vol. 21, Supp.2 pp. ii93-ii100
531. T. Simunic, K. Mihic, and G. De Micheli, "Optimization of Reliability and Power Consumption in Systems on a Chip," *PATMOS - Power Area Timing Worksop for MOS circuits*, pp. 237-246, 2005.
532. A. Coskun, T.Simunic, Y. Leblebici and G. De Micheli, "A Simulation Methodology for Reliability Analysis in Multi-Core SoCs," *GLSVLSI - Proceedings of the Great lake Symposium on VLSI*, April 2006, pp. 95-99.
533. C. Nardini, D. Masotti, S. Yoon, E. Macii, M.D. Kuo, G. De Micheli, L. Benini, "Mining gene sets for measuring similarities," *ISCC, Proceedings of IEEE Symposium on Computers and Communications*, 2006, pp. 227-232.
534. E. Ficarra, E. Macii, G. De Micheli, and L. Benini, "Computer-aided evaluation of protein expression in pathological tissue images," *Computer-Based Medical Systems - CBMS*, pp. 413 - 418, 2006.

535. S. Murali, M. Coenen, A. Radulescu, K. Goossens, and G. De Micheli, "Mapping and Configuration Methods for Multi-Use-Case Networks on Chips," *ASPDAC - Asia and South Pacific Design Automation Conference*, pp. 146-151.
536. S. Murali, M. Coenen, A. Radulescu, K. Goossens and G. De Micheli, "A Methodology for Mapping Multiple Use-Cases onto Networks on Chips", *Proc. DATE*, March 2006, pp. 118-123.
537. S. Murali, D. Atienza, L. Benini, G. De Micheli, "A Multi-Path Routing Strategy with Guaranteed In-order Packet Delivery and Fault Tolerance for Networks on Chips", *Proc. DAC*, July 2006, pp. 845-848.
538. D. Atienza, P. Garcia Del Valle, G. Paci, F. Poletti, L. Benini, G. De Micheli, and J. Mendias, "A Fast HW/SW FPGABased Thermal Emulation Framework for MultiProcessor SystemonChip," in *DAC- Design Automation Conference*, pp. 618-623, 2006.
539. F. Angiolini, D. Atienza, S. Murali, L. Benini and G. De Micheli, "Reliability Support for On-chip Memories Using Networks-on-Chips", *ICCD*, October 2006.
540. S. Murali, P. Meloni, F. Angiolini, D. Atienza, S. Carta, L. Benini, De Micheli and L. Raffo, "Designing Message-Dependent Deadlock Free Networks on Chips for Application-Specific Systems on Chips", *VLSI-SoC*, October 2006, pp. 158-163.
541. P. Del Valle, D. Atienza, I. Magan, J. Flores, E. Perez, J. Mendias, L. Benini, and G. De Micheli, "A Complete Multi-Processor System-on-Chip FPGA-Based Emulation Framework," i *IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SoC*, pp. 140-145, October 2006.
542. M. Coenen, S. Murali, A. Radulescu, K. Goossens and G. De Micheli, "A buffer sizing Algorithm for Networks on Chip using TDMA and credit based end to end Flow Control", *CODES+ISSS*, October 2006.
543. S. Murali, R. Tamhankar, F. Angiolini, A. Pullini, D. Atienza, L. Benini and G. De Micheli, "Comparison of a Timing-Error Tolerant Scheme with a Traditional Re-transmission Mechanism for Networks on Chips", *International Symposium on Systems on Chips*, November 2006, pp. 130-135.
544. D. Atienza, P. Raghavan, J. Ayala, G. De Micheli, F. Catthoor, D. Verkest, and M. Lopez-Vallejo, "Compiler-Driven Leakage Energy Reduction in Banked Register Files," in J. Vounckx, N. Azemard and P. Maurine, Editors, *Integrated Circuit and System Design: Power and Timing Modelling, Optimization and Simulation (PATMOS)*, Springer, 2006, pp. 107-116.
545. I. Folcarelli, T. Kluther, A. E. Susu, A. Acquaviva, and G. De Micheli, "An Opportunistic Reconfiguration Strategy for Environmentally Powered Devices," *ACM International Conference on Computing Frontiers*, 2006, pp. 171-176.
546. S. Murali, P. Meloni, F. Angiolini, D. Atienza, S. Carta, L. Benini, G. De Micheli and L. Raffo, "Design of Application-Specific Networks on Chips with Floorplan Information", *ICCAD*, November 2006, pp.355-362.
547. P. Del Valle, D. Atienza, I. Magan, J. Flores, E. Perez, J. Mendias, L. Benini, and G. De Micheli, "Architectural Exploration of MPSoC Designs Based on an FPGA Emulation Framework", *DCIS- XXI Conference on Design of Circuits and Integrated Systems*, pp. 12-18, 2006.
548. S. Yoon, A. Garg, E.-Y. Chung, H. S. Park, W. Y. Park, and G. De Micheli, "Exploiting Binary Abstractions in Deciphering Gene Interactions," in *Engineering in Medicine and Biology Society, EMBS '06*, pp. 5858-5863, 2006.
549. S. Carta, A. Acquaviva, P. G. Del Valle, M. Pittau, D. Atienza, F. Rincon, G. De Micheli, L. Benini, and J. M. Mendias. "Multi-Processor Operating System Emulation Framework with Thermal Feedback for Systems-on-Chip" *17th ACM Great Lakes Symposium on VLSI*, 2007, pp. 311-316.
550. J. Ayala, P. Raghavan, D. Atienza, F. Catthoor, G. De Micheli, and M. Lopez-Vallejo, "Reduction of Register File Delay Due to Process Variability in VLIW Architectures", *IEEE International Symposium on Circuits and Systems (ISCAS)*, New Orleans, USA, pp.121-124, 2007.
551. A. Garg, I. Xenarios, L. Mendoza, and G. De Micheli, "An Efficient Method for Dynamic Analysis of Gene Regulatory Networks and in silico Gene Perturbation Experiments," in *11th Annual International Conference on Research in Computational Molecular Biology, RECOMB 2007*, Lecture Notes in Computer Science, Springer, 2007.
552. A. Garg, L. Mendoza, I. Xenarios, and G. De Micheli, "Modeling of Multiple Valued Gene Regulatory Networks," in *29th Annual International Conference of the IEEE. EMBS, 2007*, vol. IEEE CNS, pp. 1398 - 1404, 2007.
553. S. Murali, A. Mutapcic, D. Atienza, R. Gupta, S. P. Boyd, and G. De Micheli, "Temperature-Aware Processor Frequency Assignment for MPSoCs Using Convex Optimization," in *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, ISBN: 978-1-59593-824-4/07/0009, pp. 111-116, 2007.

554. F. J. Rincn, A. E. Susu, M. Snchez-lez, D. Atienza, and G. De Micheli, "A Simulation Model for Wireless Sensor Networks Based on TOSSIM," in *XXII Conference on Design of Circuits and Integrated Systems (DCIS)*, no. ISBN: 978-84690-86929-2, (Barcelona), pp. pp. 278-283, IMSE, 2007.
555. P. G. Del Valle, D. Atienza, G. Paci, F. Poletti, L. Benini, G. De Micheli, J. M. Mendias, and R. Hermida, "Application of FPGA Emulation to SoC Floorplan and Packaging Exploration," in *XXII Conference on Design of Circuits and Integrated Systems*, no. ISBN: 978-84690-86929-2, (Barcelona), pp. 236-240, Departament d'Electrnica-Universitat de Barcelona, Spain, 2007.
556. A. Pullini, F. Angiolini, P. Meloni, D. Atienza, S. Murali, L. Raffo, G. De Micheli, and L. Benini, "NoC Design and Implementation in 65 nm Technology," in *First International Symposium on Networks-on-Chips (NoC)*, pp. 273-282, 2007.
557. H. Ben Jamaa, K. Moselund, D. Atienza, D. Bouvet, A. Ionescu, Y. Leblebici, and G. De Micheli, "Fault-Tolerant Multi-Level Logic Decoder for Nanoscale Crossbar Memory Arrays," in *International Conference on Computer-Aided Design (ICCAD)*, no. ISBN: 1-4244-1382-6/07, pp. 765-772, 2007.
558. F. Angiolini, H. Ben Jamaa, D. Atienza, L. Benini, and G. De Micheli, "Improving the Fault Tolerance of Nanometric PLA Designs," in *Design Automation and Test in Europe (DATE)*, no. ISBN: 978-3-9810801-2-4, pp. 570-575, 2007.
559. S. Carrara, F. K. Grkaynak, C. Guiducci, C. Stagni, L. Benini, Y. Leblebici, B. Samor and G. De Micheli, "Interface Layering Phenomena in Capacitance Detection of DNA with Biochips *Sensors & Transducers Journal*, Vol. 76 (2007), 969-977.
560. D. Atienza, S. Bobba, M. Poli, G. De Micheli and L. Benini, "System-Level Design for Nano-Electronics," *Proceedings ICECS*, pp. 747-751, 2001.
561. D. Atienza, G. De Micheli, L. Benini, J. Ayala, P. Del Valle, M. DeBole, and V. Narayanan, "Reliability-Aware Design for Nanometer-Scale Devices," in *Asia and South Pacific Design Automation Conference (ASP-DAC)*, no. ISSN: 1530-1591/05, pp. 549 - 554, 2008.
562. F. Rincon, M. Paselli, J. Recas, Q. Zhao, M. Sanchez-Elez, D. Atienza, J. Penders, and G. De Micheli, "OS-Based Sensor Node Platform and Energy Estimation Model for Health-Care Wireless Sensor Networks," in *Design, Automation and Test in Europe (DATE '08)*, 2008.
563. F. Mulas, M. Buttu, M. Pittau, S. Carta, D. Atienza, A. Acquaviva, L. Benini, and G. De Micheli, "Thermal Balancing Policy for Streaming Computing on Multiprocessor Architectures," in *Design, Automation and Test in Europe (DATE '08)*, 2008.
564. S. Murali, D. Atienza, L. Benini, and G. De Micheli, "Temperature Control of High Performance Multicore Platforms Using Convex Optimization," in *Design, Automation and Test in Europe (DATE '08)*, 2008.
565. A. Garg, D. Banerjee, and G. De Micheli, "Implicit Methods for Probabilistic Modeling of Gene Regulatory Networks," in *30th IEEE EMBS Annual International Conference 2008*, Vancouver, Canada, 2008.
566. V. Rana, D. Atienza, M. D. Santambrogio, D. Sciuto, and G. De Micheli, "A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication," in *16th IFIP/IEEE International Conference on Very Large Scale Integration*, pp. 321-326, 2008.
567. S. Carrara, A. Cavallini, G. De Micheli, J. Olivo, L. Benini, V. V. Shumyantseva, and A. I. Arhakov, "Circuits Design and Nano-Structured Electrodes for Drugs Monitoring in Personalized Therapy," in *BioCAS 2008, Biomedical Circuits and Systems Conference*, 2008.
568. H. Ben Jamaa, D. Atienza, Y. Leblebici, and G. De Micheli, "Programmable Logic Circuits based on Ambipolar CNFET," in *45th Design Automation Conference*, 2008.
569. Y. Temiz, F. Gurkaynak, S. Terrettaz, H. Vogel, G. De Micheli, Y. Leblebici, C. Guiducci, and L. Benini, "Real-Time High-Sensitivity Impedance Measurement Interface for Tethered BLM Biosensor Arrays," in *IEEE SENSORS 2008*, pp. 650-653, 2008.
570. A. Susu, A. Acquaviva, A. Atienza, and A. De Micheli, "Stochastic Modeling and Analysis for Environmentally Powered Wireless Sensor Nodes," in *6th Intl. Symposium on Modeling and Optimization in Mobile, Ad Hoc, and Wireless Networks (WiOPT'08)*, vol. 1, pp. 11 - 20, 2008.
571. A. Sathanur, A. Pullini, L. Benini, G. De Micheli, and E. Macii, "Physically clustered Forward Body Biasing for variability compensation in nano-meter CMOS design," in *Design, Automation & Test in Europe, DATE 2009*.
572. F. Zanini, D. Atienza, and G. De Micheli, "A Control Theory Approach for Thermal Balancing of MPSoC," in *14th Asia and South Pacific Design Automation Conference (ASP-DAC 09)*, vol. 1, pp. 7-12, 2009.

573. C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, "SunFloor 3D: A Tool for Networks on Chip Topology Synthesis for 3D Systems on Chip," in *DATE*, 2009.
574. S. Murali, C. Seiculescu, L. Benini, and G. De Micheli, "Synthesis of Networks on Chips for 3D Systems on Chips," in *ASPDAC 2009*, 2009.
575. E. Ngangue, N. Khaled, and G. De Micheli, "An Analytical Model for the Contention Access Period of the Slotted IEEE 802.15.4 with Service Differentiation," in *ICC*, 2009.
576. F. J. Rincon, L. Gutierrez, M. Jimenez, V. Diaz, N. Khaled, D. Atienza, M. Sanchez-Elez, J. Recas, and G. De Micheli, "Implementation of an automated egg-based diagnosis for a wireless body sensor platform," in *International Conference on Biomedical Electronics and Devices*, 2009.
577. S. Bobba, J. Zhang, A. Pullini, D. Atienza, S. Mitra, and G. De Micheli, "Design of Compact Imperfection-Immune CNFET Layouts for Standard-Cell-Based Logic Synthesis," in *Design, Automation & Test in Europe, DATE*, 2009.
578. M. H. Ben Jamaa, D. Atienza, Y. Leblebici, and G. De Micheli, "A Stochastic Perturbative Approach to Design a Defect-Aware Thresholder in the Sense Amplifier of Crossbar Memories," in *14th IEEE/ACM Asia and South Pacific Design Automation Conference*, 2009.
579. S. Carrara, C. Boero, and G. De Micheli, "Quantum Dots and Wires to improve Enzymes-Based Electrochemical Bio-sensing," *Nano-Net 2009*, 2009.
580. S. Carrara, A. Cavallini, Y. Leblebici, G. De Micheli, V. Bhalla, F. Valle, B. Samori, L. Benini, B. Ricco, V. Vikholm-Lundin, and T. Munter, "New probe immobilizations by lipoate-diethalonamine or ethylene-glycol molecules for capacitance DNA chip," in *IWASI*, pp. 9-14, 2009.
581. Y. Temiz, S. Carrara, A. Cavallini, and Y. Leblebici, "3d Architecture and Replaceable Layers for Label-Free DNA Biochips," *IWASI*, pp. 35-40, 2009.
582. C. Boero, S. Carrara, and G. De Micheli, "Sensitivity Enhancement by Carbon Nanotubes: Applications to Stem Cell Cultures Monitoring," *PRIME*, pp. 260-263, 2009.
583. S. Carrara, A. Cavallini, A. Garg, and G. De Micheli, "Dynamical Spot Queries to Improve Specificity in P450s based Multi-Drugs Monitoring," *IEEE/ICME International Conference on Complex Medical Engineering*, pp. 1-6, 2009.
584. D. Sacchetto, M. H. Ben Jamaa, G. De Micheli, and Y. Leblebici, "Fabrication and Characterization of Vertically Stacked Gate-All-Around Si Nanowire FET Arrays," *ESSDERC*, 2009.
585. M. H. Ben Jamaa, S. Carrara, J. Georgiou, N. Archontas, and G. De Micheli, "Fabrication of Memristors with Poly-Crystalline Silicon Nanowires," *IEEE Nano*, 2009.
586. M. H. Ben Jamaa, G. Cerofolini, Y. Leblebici, and G. De Micheli, "Complete Nanowire Crossbar Framework Optimized for the Multi-Spacer Patterning Technique," *CASES*, 2009.
587. V. F. Pavlidis and G. De Micheli, "Power Distribution Paths for 3-D IC," *ACM Great Lakes VLSI Symposium*, pp. 261-268, 2009.
588. I. Savidis, V. F. Pavlidis, E. G. Friedman, and G. De Micheli, "Clock and Power Distribution Networks for 3-D ICs," *ACM/IEEE Conference on Design, Automation, and Test in Europe*, 2009.
589. H. Ben Jamaa, Y. Leblebici, and G. De Micheli, "Decoding Nanowire Arrays Fabricated with the Multi-Spacer Patterning Technique," in *DAC - Design Automation Conference*, 2009.
590. C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, "NoC Topology Synthesis for Supporting Shutdown of Voltage Islands in SoCs," *DAC 2009*, pp. 822-825, 2009.
591. B. Ben Jamaa, K. Mohanram, and G. De Micheli, "Novel Library of Logic Gates with Ambipolar CNTFETs: Opportunities for Multi-Level Logic Synthesis," *Design, Automation and Test in Europe*, pp. 622-627, 2009.
592. F. Zanini, D. Atienza, L. Benini, and G. De Micheli, "Multicore Thermal Management with Model Predictive Control," *European Conference on Circuit Theory and Design (ECCTD 2009)*, vol. 1, (New York), pp. 90-95, IEEE Press, 2009.
593. F. Zanini, D. Atienza, A. K. Coskun, and G. De Micheli, "Optimal Multi-Processor SoC Thermal Simulation via Adaptive Differential Equation Solvers," *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 80-85, IEEE/IFIP Press, 2009.
594. H. Xu, V. Pavlidis, and G. De Micheli, "Repeater Insertion for Two-Terminal Nets in Three-Dimensional Integrated Circuits," in *Nano-Net 2009*.

595. D. Rahmati, S. Murali, L. Benini, F. Angiolini, G. De Micheli, and H. Sarbazi-Azad, "A Method for Calculating Hard QoS Guarantees for Networks-on-Chip," in *Proceedings of the International Conference on CAD (ICCAD)*, 2009.
596. G. De Micheli, "Nano-Tera.ch: Nano-technologies for Tera-scale Problems," *Proceedings IEEE Bipolar Circuit and Technology Meeting*, pp. 142-145, October 2009.
597. A. Garg, K. Mohanram, A. Di Cara, G. De Micheli and I. Xenarios, "Modeling stochasticity and robustness in gene regulatory networks," *Bioinformatics*, Vol 25, pp. i101-i109, 2009.
598. J. Zhang, S. Bobba, N. Patil, A. Lin, H.-S. P. Wong, G. De Micheli, and S. Mitra, "Carbon Nanotube Correlation: Promising Opportunity for CNFET Circuit Yield Enhancement," in *Proceedings of the 47th Design Automation Conference (DAC 2010)*, vol. 1, pp. 889-892, 2010.
599. G. De Micheli, C. Seiculescu, S. Murali, L. Benini, F. Angiolini, and A. Pullini, "Networks on Chips: from Research to Products," in *Proceedings of the 47th Design Automation Conference (DAC 2010)*, vol. 1, pp. 300-305, 2010.
600. D. Sacchetto, H. Ben-Jamaa, S. Carrara, G. De Micheli, and Y. Leblebici, "Memristive Devices Fabricated with Silicon Nanowire Schottky Barrier Transistors," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, vol. 1, pp. 9-12, 2010.
601. D. Sacchetto, H. Ben-Jamaa, G. De Micheli, and Y. Leblebici, "Design Aspects of Carry Lookahead Adders with Vertically-Stacked Nanowire Transistors," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, vol. 1, pp. 1715-1717, 2010.
602. H. Ben Jamaa, K. Mohanram, and G. De Micheli, "Power Consumption of Logic Circuits in Ambipolar Carbon Nanotube Technology," in *DATE, 2010*.
603. F. Zanini, D. Atienza Alonso, G. De Micheli, and S. P. Boyd, "Online Convex Optimization-Based Algorithm for Thermal Management of MPSoCs," in *Proceedings of the 20th ACM Great Lakes Symposium on VLSI (GLSVLSI 2010)*, vol. 1, (New York), pp. 203-208, ACM Press, 2010.
604. C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, "A Method to Remove Deadlocks in Networks-on-Chips with Wormhole Flow Control," in *DATE 2010*, 2010.
605. F. Zanini, D. Atienza, C. N. Jones, and G. De Micheli, "Temperature Sensor Placement in Thermal Management Systems for MPSoCs," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, vol. 1, pp. 1065-1068, IEEE Press, 2010.
606. F. Zanini, C. N. Jones, D. Atienza, and G. De Micheli, "Multicore thermal management using approximate explicit Model Predictive Control," in *Proceedings of the of IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, vol. 1, pp. 3321-3324, IEEE Press, 2010.
607. S. Bobba, S. Carrara, and G. De Micheli, "Design of a CNFET Array for Sensing and Control in P450 based Biochips for multiple drug detection," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, vol. 1, pp. 1065-1068, 2010.
608. N. Archontas, J. Georgiou, H. Ben Jamaa, S. Carrara, and G. De Micheli, "Characterization of Memristive Poly-Si Nanowires via Empirical Physical Modelling," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, vol. 1, pp. 1675-1678, 2010.
609. J. Joven, F. Angiolini, D. Castells-Rufas, G. De Micheli, and J. Carrabina, "QoS-ocMPI: QoS-aware on-chip Message Passing Library for NoC-based Many-Core MPSoCs," in *Proceedings of the 2nd Workshop on Programming Models for Emerging Architectures (PMEA'10)*, 2010.
610. J. Joven Murillo, A. Marongiu, F. Angiolini, L. Benini, and G. De Micheli, "Exploring Programming Model-driven QoS Support for NoC-based Platforms," in *Proceedings of International Conference on Hardware/Software Codesign and System Synthesis (CODES+ ISSS'10)*, pp. 65-74, 2010.
611. S. K. Bobba, A. Chakraborty, O. Thomas, P. Batude, V. Pavlidis, and G. De Micheli, "Performance Analysis of 3-D Monolithic Integrated Circuits," in *Proceedings of the IEEE International 3D System Integration Conference (3DIC'10)*, 2010.
612. S. Carrara, M. D. Torre, A. Cavallini, D. De Venuto, and G. De Micheli, "Multiplexing pH and Temperature in a Molecular Biosensor," in *Proceedings of the IEEE BIOCAS 2010 Conference*, 2010.
613. D. De Venuto, M. D. Torre, C. Boero, S. Carrara, and G. De Micheli, "A Novel Multi-Working Electrode Potentiostat for Electrochemical Detection of Metabolites," in *Proceedings of the IEEE Sensors 2010 Conference*, no. 1, pp. 1572-1577, 2010.

614. J. Olivo, S. Carrara, and G. De Micheli, "Optimal Frequencies for Inductive Powering of Fully Implantable Biosensors for Chronic and Elderly Patients," in *Proceedings of the IEEE Sensors 2010 Conference*, vol. 1, pp. 99-103, 2010.
615. A. Cavallini, S. Carrara, G. De Micheli, and V. Erokhin, "P450-mediated electrochemical sensing of drugs in human plasma for personalized therapy," in *Proceedings of the Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2010 Conference on, pp. 1-4, 2010.
616. A. Biyabani, C. Guiducci, and G. De Micheli, "Regenerative Circuits for Rapid Biosensing," in *17th IEEE International Conference on Electronics, Circuits, and Systems ICECS 2010*, 2010.
617. C. Boero, S. Carrara, G. Del Vecchio, G. D. Albini, L. Calz, and G. De Micheli, "Carbon Nanotubes-Based Electrochemical Sensing for Cell Culture Monitoring," in *Proceedings of the 2010 IEEE/ICME International Conference on Complex Medical Engineering*, vol. 1, pp. 288-293, 2010.
618. M. De Marchi, H. Ben Jamaa, and G. De Micheli, "Regular Fabric Design with Ambipolar CNTFETs for FPGA and Structured ASIC Applications," in *IEEE/ACM International Symposium on Nanoscale Architectures (Nanoarch'10)*, 2010.
619. V. Pavlidis, H. Xu, I. Tsioutsios, and G. De Micheli, "Synchronization and Power Integrity Issues in 3-D ICs," in *Proceedings of Asia Pacific Conference on Circuits and Systems*, pp. 536-539, 2010.
620. I. Tsioutsios, V. Pavlidis, and G. De Micheli, "Physical Design Tradeoffs in Power Distribution Networks for 3-D ICs," in *Proceedings of the 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2010)*, pp. 435-438, 2010.
621. M. De Marchi, S. Bobba, H. Ben Jamaa, and G. De Micheli, "Synthesis of regular computational fabrics with ambipolar CNTFET technology," in *Proceedings of the 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2010)*, 2010.
622. H. Xu, V. Pavlidis and G. De Micheli, "Skew Variability in 3-D ICs with Multiple Clock Domains". *International Symposium on Circuits and Systems (ISCAS)*, 2011 IEEE International Symposium on, Rio de Janeiro, Brazil, 2011.
623. S. Rahimian Omam, V. Pavlidis and G. De Micheli, "Design of Resonant Clock Distribution Networks for 3-D Integrated Circuits". *PATMOS'11, 21st international conference on Integrated circuit and system design: power and timing modeling, optimization, and simulation*, Madrid, 2011.
624. F. Zanini, D. Atienza Alonso and G. De Micheli, "Convex-Based Thermal Management for 3D MPSoCs Using DVFS and Variable-Flow Liquid Cooling". *PATMOS'11, 21st international conference on Integrated circuit and system design: power and timing modeling, optimization, and simulation*, Madrid, 2011.
625. P. Batude, M. Vinet, B. Previtali, C. Tabone, C. Xu, J. Mazurier, O. Weber, F. Andrieu, L. Tosti and L. Brevard, Advances, "Challenges and Opportunities in 3D CMOS Sequential Integration". *IEEE International Electron Devices Meeting (IEDM)*, Washington DC, USA, 2011.
626. D. Sacchetto, M. De Marchi, G. De Micheli and Y. Leblebici, "Alternative Design Methodologies for the Next Generation Logic Switch (invited paper)". *International Conference on Computer-Aided Design*, San Jose, California, USA, 2011.
627. W. You, N. Widmer and G. De Micheli, "Personalized Modeling for Drug Concentration Prediction Using Support Vector Machine". *4th International Conference on Biomedical Engineering and Informatics (BMEI)*, Shanghai, China, 2011.
628. S. Carrara, L. Bolomey, C. Boero, A. Cavallini, E. Meurville, G. De Micheli, T. Rezzonico, M. Proietti and F. Grassi, "Single-Metabolite Bio-Nano-Sensors and System for Remote Monitoring in Animal Models". *IEEE Sensors 2011 Conference*, Limerick, Ireland, 2011.
629. W. You, N. Widmer and G. De Micheli, "Example-based Support Vector Machine for Drug Concentration Analysis". *33rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2011)*, Boston, Massachusetts, USA, 2011.
630. J. Joven Murillo, P. Strid, D. Castells-Rufas, A. Bagdia, J. Carrabina and G. De Micheli, "HW-SW Implementation of a Decoupled FPU for ARM-based Cortex-M1 SoCs in FPGAs". *6th IEEE International Symposium on Industrial Embedded Systems (SIES'11)*, Vasteras, Sweden, 2011.
631. M. Beltrandi, A. Vachoux, S. Carrara, Y. Leblebici and G. De Micheli, "VHDL-AMS Model of an Electrochemical Cell to Design VLSI Bio-Chips". *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, San Diego, California, USA, 2011.

632. D. Sacchetto, S. Xie, A. V. Savu, M. Zervas, G. De Micheli, J. Brugger and Y. Leblebici, "Vertically-Stacked Si Nanowire FETs with sub-micrometer Gate-All-Around polysilicon gates patterned by nanostencil lithography". *37th International Conference on Micro and Nano Engineering (MNE)*, Berlin, Germany, 2011.
633. C. Seiculescu, S. Murali, L. Benini and G. De Micheli, "A DRAM Centric NoC Architecture and Topology Design Approach". *IEEE Computer Society Annual Symposium on VLSI*, Chennai, India, 2011.
634. G. De Micheli, V. Pavlidis, D. Atienza Alonso and Y. Leblebici, "Design Methods and Tools for 3D Integration". *Symposium on VLSI Technology*, Kyoto, Japan, 2011.
635. D. Sacchetto, G. De Micheli and Y. Leblebici, "Ambipolar Si Nanowire Field Effect Transistors for Low Current and Temperature Sensing". *16th International Conference on Solid-State Sensors, Actuators and Microsystems*, Beijing, China, 2011.
636. J. Olivo, S. Carrara and G. De Micheli, "Modeling of Printed Spiral Inductors for Remote Powering of Implantable Biosensors". *5th International Symposium on Medical Information and Communication Technology*, Montreux, Switzerland, 2011.
637. S. K. Bobba, A. Chakraborty, O. Thomas, P. Batude, T. Ernst, O. Faynot, D. Pan and G. De Micheli, "CELONCEL: Effective Design Technique for 3-D Monolithic Integration targeting High Performance Integrated Circuits". *16th Asia and South Pacific Design Automation Conference (ASP-DAC 2011)*, Yokohama, Japan, 2011.
638. F. Zanini, D. Atienza Alonso, L. Benini and G. De Micheli, "Thermal-Aware System-Level Modeling and Management for Multi-Processor Systems-on-Chip". *IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio de Janeiro, Brazil, 2011.
639. G. De Micheli. "Logic Synthesis and Physical Design: Quo Vadis, *Design, Automation and Test in Europe (DATE 2011)*", Grenoble, France, 2011.
640. H. Xu, V. F. Pavlidis and G. De Micheli, "Analytical Heat Transfer Model for Thermal Through-Silicon Vias". *Design, Automation and Test in Europe (DATE 2011)*, Grenoble, France, 2011.
641. G. De Micheli, S. S. Ghoreishizadeh, C. Boero, F. Valgimigli and S. Carrara, "An Integrated Platform for Advanced Diagnostics". *Design, Automation and Test in Europe (DATE 2011)*, Grenoble, France, 2011.
642. G. Beanato, I. Loi, G. De Micheli, Y. Leblebici and L. Benini, "3D-LIN: A Configurable Low-Latency Interconnect for Multi-Core Clusters with 3D Stacked L1 Memory". *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Santa Cruz, California, USA, 2012.
643. J. Ghaye, G. De Micheli and S. Carrara, "Quantification of Sub-resolution Sized Targets in Cell Fluorescent Imaging". *IEEE Biomedical Circuits and Systems Conference (BioCAS 2012)*, Hsinchu, Taiwan, 2012.
644. S. S. Ghoreishizadeh, I. Taurino, S. Carrara and G. De Micheli, "A Current-Mode Potentiostat for Multi-Target Detection Tested with Different Lactate Biosensors". *IEEE Biomedical Circuits and Systems Conference (BioCAS 2012)*, Hsinchu, Taiwan, 2012.
645. A. Cavallini, C. Baj-Rossi, S. Ghoreishizadeh, G. De Micheli and S. Carrara, "Design, fabrication, and test of a sensor array for perspective biosensing in chronic pathologies". *IEEE Biomedical Circuits and Systems Conference (BioCAS 2012)*, Hsinchu, Taiwan, 2012.
646. S. Carrara, A. Cavallini, S. Ghoreishizadeh, J. Olivo and G. De Micheli, "Developing Highly-Integrated Subcutaneous Biochips for Remote Monitoring of Human Metabolism". *IEEE Sensors Conference*, Taipei, Taiwan, 2012.
647. K. Kang, L. Benini and G. De Micheli, "A High-throughput and Low-Latency Interconnection Network for Multi-Core Clusters with 3-D Stacked L2 Tightly-Coupled Data Memory". *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Santa Cruz, California, USA, 2012.
648. P.-E. Gaillardon, D. Sacchetto, S. Bobba, Y. Leblebici and G. De Micheli, "GMS: Generic Memristive Structure for Non-Volatile FPGAs". *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Santa Cruz, California, USA, 2012.
649. A. Simalatsar and G. De Micheli, "Medical Guidelines Reconciling Medical Software and Electronic Devices: Imatinib Case-study." *IEEE 12th International Conference on Bioinformatics and BioEngineering (BIBE'12)*, Larnaca, Cyprus, 2012.
650. W. You, A. Simalatsar, N. Widmer and G. De Micheli, "A Drug Administration Decision Support System". *IEEE International Conference on Bioinformatics and Biomedicine (BIBM)*, Philadelphia, Pennsylvania, USA, 2012.



651. J. M. Ghaye, G. De Micheli and S. Carrara, "Quantification of Sub-resolution Sized Targets in Cell Fluorescent Imaging". *IEEE Biomedical Circuits and Systems*, Hsinchu, Taiwan, 2012.
652. M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. J. M. Gaillardon, Y. Leblebici and G. de Micheli, "Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs". *International Electron Devices Meeting (IEDM)*, San Francisco, California, USA, 2012.
653. C. Seiculescu, L. Benini and G. De Micheli, "A Distributed Interleaving Scheme for Efficient Access to WideIO DRAM Memory". *International Conference on Hardware/Software Codesign and System Synthesis (CODES + ISSS)*, Tampere, Finland, 2012.
654. V. Pavlidis, H. Xu and G. De Micheli, "Enhanced Wafer Matching Heuristics for 3-D ICs". *IEEE 17th European Test Symposium*, Annecy, France, 2012.
655. S. Bobba, P.-E. J. M. Gaillardon, J. Zhang, M. De Marchi, D. Sacchetto, Y. Leblebici and G. De Micheli, "Process/Design Co-optimization of Regular Logic Tiles for Double-Gate Silicon Nanowire Transistors". *IEEE /ACM International Symposium on Nanoscale Architectures (NANOARCH '12)*, Amsterdam, Netherlands, 2012.
656. A. Simalatsar and G. De Micheli, "TAT-based Formal Representation of Medical Guidelines : Imatinib Case-study. *34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2012)*", San Diego, California, USA, 2012.
657. J. Olivo, S. Carrara and G. De Micheli, "IronIC Patch: A Wearable Device for the Remote Powering and Connectivity of Implantable Systems". *IEEE International Instrumentation and Measurement Technology Conference (I2MTC 2012)*, Graz, Austria, 2012.
658. G. De Micheli, C. Boero, C. Baj-Rossi, I. Taurino and S. Carrara, "Integrated Biosensors for Personalized Medicine. *49th Design Automation Conference (DAC)*", San Francisco, California, USA, 2012.
659. G. Kökklü, J. M. Ghaye, R. Beuchat, G. De Micheli, Y. Leblebici and S. Carrara, "Quantitative Comparison of Commercial CCD and Custom-Designed CMOS Camera for Biological Applications". *2012 IEEE International Symposium on Circuits and Systems (ISCAS 2012)*, Seoul, Korea, 2012.
660. S. Bobba, M. De Marchi, Y. Leblebici and G. De Micheli, "Physical Synthesis onto Sea-of-Tiles with Double-Gate Silicon Nanowire Transistors". *49th Design Automation Conference (DAC)*, San Francisco, California, USA, 2012.
661. H. Xu, V. Pavlidis, W. Burleson and G. De Micheli, "The Combined Effect of Process Variations and Power Supply Noise on Clock Skew and Jitter". *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, California, USA, 2012.
662. G. De Micheli, "Engineering Complex Systems for Health, Security and the Environment". *The 17th Asia and South Pacific Design Automation Conference*, Sydney, Australia, 2012.
663. C. Zhang, V. Pavlidis and G. De Micheli, "Voltage Propagation Method for 3-D Power Grid Analysis". *Design, Automation and Test in Europe (DATE 12)*, Dresden, Germany, 2012.
664. S. Volos, C. Seiculescu, B. Grot, N. Khosro, K. Pour, B. Falsafi and G. De Micheli, "CCNoC: Specializing On-Chip Interconnects for Energy Efficiency in Cache-Coherent Servers". *6th International Symposium on Networks-on-Chip*, Lyngby, Denmark, 2012.
665. S. Rahimian, V. Pavlidis and Giovanni De Micheli, "Low-Power Clock Distribution Networks for 3-D ICs," *2012 IEEE 27th Convention of Electrical and Electronics Engineers in Israel*, 2012.
666. S. Rahimian, V. Pavlidis and Giovanni De Micheli, "A Low-Overhead Method for Pre-bond Test of Resonant 3-D Clock Distribution Networks," *IEEE 3rd International Workshop on Testing Three - Dimensional Stacked Integrated Circuits (3D-Test)*, Anaheim, California, USA, 2012.
667. F. Puppo, M.-A. Doucey, T. S. Y. Moh, G. Pandraud, P. M. Sarro, S. Carrara and G. De Micheli "Femto-Molar Sensitive Field Effect Transistor Biosensors Based on Silicon Nanowires and Antibodies" *IEEE Sensors*, Baltimore, Maryland, USA, 2013.
668. H. Ghasemzadeh Mohammadi, P.-E. Gaillardon, M. Yazdani and G. De Micheli. "A Fast TCAD-based Methodology for Variation Analysis of Emerging Nano-Devices," *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, New York City, New York, USA, 2013.
669. A. Simalatsar, W. You, D. Sun, V. Gotta and N. Widmer and G. De Micheli, "A Control Flow Prototype for a Dose Recommending Device for Chronic Myeloid Leukemia Patients," *Medical Cyber Physical Systems Workshop 2013*, Philadelphia, Pennsylvania, USA, 2013.

670. S. S. Ghoreishizadeh, N. Gaurav, S. Carrara and G. De Micheli. "Empirical Study of Noise Dependence in Electrochemical Sensors," *5th International Workshop on Advances in Sensors and Interfaces (IWASI)*, Bari, Italy, 2013.
671. S. S. Ghoreishizadeh, S. Carrara and G. De Micheli. "A Configurable IC to Control, Readout and Calibrate an Array of Biosensors," *2013 European Conference on Circuit Theory and Design (ECCTD)*, Dresden, Germany, 2013.
672. C. Gasnier, P.-E. Gaillardon and G. De Micheli. "SATSoT: A Methodology to Map Controllable-Polarity Devices on a Regular Fabric Using SAT," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Brooklyn, NY, USA, 2013.
673. C. Baj-Rossi, E. Kilin, S. Ghoreishizadeh, D. Casarino, T. Rezzonico Jost, C. De Hollain, F. Grassi, L. Pastorino, S. Carrara and G. De Micheli. "Fabrication and Packaging of a Fully Implantable Biosensor Array," *IEEE Biomedical Circuits and Systems Conference (BIOCAS 2013)*, Rotterdam, the Netherlands, 2013.
674. S. Ghoreishizadeh, E. Kilinc, C. Baj-Rossi, C. Dehollain, S. Carrara and G. De Micheli. "An Implantable Bio-Micro-system for Drug Monitoring," *IEEE Biomedical Circuits and Systems Conference (BIOCAS 2013)*, Rotterdam, the Netherlands, 2013.
675. G. De Micheli, C. Boero and S. Carrara, "Lab-on-a-chip implants: a mini laboratory under the skin," *58me Journes Internationales de Biologie (JIB)*, Paris, France, 2013.
676. W. You, A. Simalatsar and G. De Micheli. "Parameterized SVM for Personalized Drug Concentration Prediction," *35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Osaka, Japan, 2013.
677. G. Koklu, R. Etienne-Cummings, Y. Leblebici, G. D. Micheli and S. Carrara. "Characterization of Standard CMOS Compatible Photodiodes and Pixels for Lab-on-Chip Devices," *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, 2013.
678. L. Amar, P.-E. Gaillardon and G. De Micheli. "Efficient Arithmetic Logic Gates Using Double-Gate Silicon Nanowire FETs, invited paper," *11th IEEE International NEWCAS Conference*, Paris, France, 2013.
679. I. Kazi, P. A. Meinerzhagen, P.-E. J. M. Gaillardon, D. Sacchetto, A. P. Burg and G. De Micheli "A ReRAM-Based Non-Volatile Flip-Flop with Sub-VT Read and CMOS Voltage-Compatible Write," *11th IEEE International NEWCAS Conference*, Paris, France, 2013.
680. P.-E. Gaillardon, M. De Marchi, L. Amaru, S. Bobba, D. Sacchetto, Y. Leblebici and G. De Micheli "Towards Structured ASICs Using Polarity-Tunable SiNW Transistors," *50th Design Automation Conference (DAC 2013)*, Austin, Texas, USA, 2013.
681. L. Amaru, P.-E. Gaillardon and G. De Micheli. "BDS-MAJ: A BDD-based Logic Synthesis Tool Exploiting Majority Logic Decomposition," *50th Design Automation Conference (DAC 2013)*, Austin, Texas, USA, 2013.
682. J. Olivo, S. S. Ghoreishizadeh, S. Carrara and G. De Micheli. "Electronic Implants: Power Delivery and Management," *Design, Automation & Test in Europe Conference (DATE 2013)*, Grenoble, France, 2013.
683. P.-E. Gaillardon, S. Bobba, L. Amru, M. De Marchi, D. Sacchetto, Y. Leblebici and G. De Micheli. "Vertically Stacked Double Gate Nanowires FETs with Controllable Polarity: From Devices to Regular ASICs," *Design, Automation & Test in Europe Conference (DATE 2013)*, Grenoble, France, 2013.
684. P.-E. Gaillardon, H. Ghasemzadeh and G. De Micheli. "Vertically-Stacked Silicon Nanowire Transistors with Controllable Polarity: a Robustness Study," *14th IEEE Latin American Test Workshop (LATW)*, Cordoba, Argentina, 2013.
685. S. K. Bobba, P.-E. Gaillardon, C. Seiculescu, V. Pavlidis and G. De Micheli. "3.5-D Integration: A Case Study," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, 2013.
686. O. Trkylmaz, L. Amar, F. Clermidy, P.-E. Gaillardon and G. De Micheli. "Self-Checking Ripple-Carry Adder with Ambipolar Silicon Nanowire FET," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, 2013.
687. J. Zhang, P.-E. Gaillardon and G. De Micheli. "Dual-threshold-voltage configurable circuits with three-independent gate silicon nanowire FETs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, 2013.
688. L. Amar, P.-E. Gaillardon and G. De Micheli. "Biconditional BDD: A Novel Canonical BDD for Logic Synthesis targeting XOR-rich Functions," *Design, Automation & Test in Europe Conference (DATE 2013)*, Grenoble, France, 2013.

689. L. Amar, P.-E. Gaillardon and G. De Micheli. "MIXSyn: An Efficient Logic Synthesis Methodology for Mixed XOR-AND/OR Dominated Circuits," *18th Asia and South Pacific Design Automation Conference (ASP-DAC 2013)*, Yokohama, Japan, 2013.
690. J. Jung, K. Kang, G. De Micheli and C.-M. Kyung. "Runtime 3-D Stacked Cache Management for Chip-Multiprocessors," *The International Symposium on Quality Electronic Design (ISQED 2013)*, Santa Clara, California, 2013.
691. I. Taurino, A. Magrez, L. Forró, G. De Micheli and S. Carrara. "Direct and selective synthesis of a wide range of carbon nanomaterials by CVD at CMOS compatible temperatures," *14th IEEE International Conference on Nanotechnology*, Toronto, Ontario, Canada, 2014.
692. H. Ghasemzadeh, P.-E. Gaillardon, M. Yazdani and G. De Micheli. "Fast Process Variation Analysis in Nano-Scaled Technologies Using Column-Wise Sparse Parameter Selection," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, Paris, France, 2014.
693. X. Tang, J. Zhang, P.-E. Gaillardon and G. De Micheli. "TSPC Flip-Flop Circuit Design with Three-Independent-Gate Silicon Nanowire FETs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, 2014.
694. O. Zografos, P.-E. Gaillardon and G. De Micheli. "Novel Grid-Based Power Routing Scheme for Regular Controllable-Polarity FET Arrangements," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, 2014.
695. P.-E. Gaillardon, X. Tang and G. De Micheli. "Novel Configurable Logic Block Architecture Exploiting Controllable-Polarity Transistors, (invited)," *9th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC'14)*, Montpellier, France, 2014.
696. P.-E. Gaillardon, L. Amarù and G. De Micheli. "A New Basic Logic Structure for Data-Path Computation," *22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2014)*, Monterey, California, 2014.
697. X. Tang, P.-E. Gaillardon and G. De Micheli. "Pattern-Based FPGA Logic Block and Clustering Algorithm," *24th International Conference on Field Programmable Logic and Applications (FPL)*, Munich, Germany, 2014.
698. J. Sandrini, A. Cevrero, T. Demirci, P.-E. Gaillardon, D. Sacchetto, G. De Micheli and Y. Leblebici, "Heterogeneous integration of ReRAM crossbars in a CMOS foundry chip.," *40th International Micro and Nano Engineering Conference (MNE)*, Lausanne, Switzerland, 2014.
699. X. Tang, P.-E. Gaillardon and G. De Micheli. "A High-Performance Low-Power Near-Vt RRAM-based FPGA," *International Conference on Field-Programmable Technology (FPT)*, Shanghai, China, 2014.
700. J. Zhang, M. De Marchi, P.-E. Gaillardon and G. De Micheli. "A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current," *International Electron Devices Meeting (IEDM14)*, San Francisco, California, USA, 2014.
701. S. Ghoreishizadeh, T. Yalin, A. Pullini, G. De Micheli, W. Burleson and S. Carrara, "A Lightweight Cryptographic System for Implantable Biosensors," *IEEE Biomedical Circuits and Systems Conference (BIOCAS 2014)*, Lausanne, Switzerland, 2014.
702. S. Ghoreishizadeh, C. Boero, A. Pullini, C. Baj-Rossi, S. Carrara and G. De Micheli "Sub-mW Reconfigurable Interface IC for Electrochemical Sensing," *IEEE Biomedical Circuits and Systems Conference (BIOCAS 2014)*, Lausanne, Switzerland, 2014.
703. A. Zaher, F. Puppo, P. Haefliger, G. De Micheli and S. Carrara. "Novel Readout Circuit for Memristive Nanowire Cancer Detection Sensors," *IEEE Biomedical Circuits and Systems Conference (BIOCAS 2014)*, Lausanne, Switzerland, 2014.
704. F. Puppo, M.-A. Doucey, J.-F. Delaloye, T. Moh, G. Pandraud, L. Sarro, G. De Micheli and S. Carrara, "High Sensitive Detection in Tumor Extracts with SiNW-FET Biosensors," *IEEE Sensors 2014*, Valencia, Spain, 2014.
705. O. Zografos, L. Amarù, P.-E. Gaillardon and G. De Micheli. "Majority Logic Synthesis for Spin Wave Technology," *Euromicro Conference on Digital System Design 2014*, Verona, Italy, 2014.
706. C. Baj-Rossi, G. De Micheli and S. Carrara. "Electrochemical Biochip for Applications to Wireless and Batteryless Monitoring of Free-Moving Mice," *36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2014)*, Chicago, Illinois, USA, 2014.
707. F. Puppo, M.-A. Doucey, M. Di Ventra, G. De Micheli and S. Carrara. "Memristor-Based Devices for Sensing," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, 2014.

708. J. M. Ghaye, C. Succa, D. Demarchi, S. K. Muldu, P. Colpo, P. Silacci, G. Vergères, G. De Micheli and S. Carrara, “Quantitative Estimation of Biological Cell Surface Receptors by Segmenting Conventional Fluorescence Microscopy Images,” *2014 IEEE International Symposium on Circuits and Systems (ISCAS 2014)*, Melbourne, Australia, 2014.
709. P.-E. Gaillardon, L. Amarù and G. De Micheli. “Unlocking Controllable-Polarity Transistors Opportunities by Exclusive-OR and Majority Logic Synthesis,” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Tampa, Florida, 2014.
710. S. Rahimian Omam, Y. Leblebici and G. De Micheli. “Parallel vs. Serial Inter-plane communication using TSVs,” *5th IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, Santiago, Chile, 2014.
711. L. Amarù, P.-E. Gaillardon and G. De Micheli. “Majority-Inverter Graph: A Novel Data-Structure and Algorithms for Efficient Logic Optimization,” *51st Design Automation Conference (DAC)*, San Francisco, California, USA, 2014.
712. K. Kang, S. Lee, G. De Micheli and C.-M. Kyung. “Temperature-Aware Runtime Power Management for Chip-Multiprocessors with 3-D Stacked Cache,” *International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, California, USA, 2014.
713. P.-E. Gaillardon, L. Amarù, J. Zhang and G. De Micheli. “Advanced System on a Chip Design Based on Controllable-Polarity FETs,” *Design, Automation and Test in Europe Conference (DATE)*, Dresden, Germany, 2014.
714. L. Amarù, P.-E. Gaillardon and G. De Micheli. “An Efficient Manipulation Package for Biconditional Binary Decision Diagrams,” *Design, Automation and Test in Europe (DATE)*, Dresden, Germany, 2014.
715. L. Amarù, P.-E. Gaillardon, A. Burg and G. De Micheli. “Data Compression via Logic Synthesis,” *9th Asia and South Pacific Design Automation Conference (ASP-DAC 2014)*, Singapore, 2014.
716. I. P. Radu, O. Zografos, A. Vaysset, F. Ciubotaru, J. Yan, G. De Micheli et al.. “Spintronic majority gates”. *IEEE International Electron Devices Meeting (IEDM)*, 2015.
717. I. Tzouvadaki, F. Puppo, M.-A. Doucey, G. De Micheli and S. Carrara. “Modeling Memristive Biosensors”. *IEEE Sensors 2015*, Busan, South Korea, 2015.
718. F. Basilotta, S. Riario, F. Stradolini, I. Taurino and D. Demarchi, G. De Micheli and S. Carrara. “Wireless Monitoring in Intensive Care Units by a 3D-Printed System with Embedded Electronics”. *IEEE/CAS-EMB Biomedical Circuits and Systems Conference (BioCAS 2015)*, Atlanta, Georgia, USA, 2015.
719. C. Baj-Rossi, A. Cavallini, T. Rezzonico Jost, M. Proietti, F. Grassi, G. De Micheli and S. Carrara. “Bio-compatible Packagings for Fully Implantable Multi-Panel Devices for Remote Monitoring of Metabolism”. *Biomedical Circuits and Systems Conference (BiOCAS 2015)*, Atlanta, Georgia, USA, 2015.
720. G. Sanzo, I. Taurino, G. Favero, F. Mazzei, G. De Micheli and S. Carrara. “Highly Sensitive Electrode Materials Based on Pt Nanoflowers Grown on Pt Nanospheres for Biosensor Development”. *15th International IEEE Conference on Nanotechnology (NANO 2015)*, Rome, Italy, 2015.
721. B. Staar, M. Schirmer, C. Baj-Rossi, G. De Micheli, S. Carrara and E. Chicca. “A neural approach to drugs monitoring for personalized medicine”. *International Joint Conference on Neural Networks 2015 (IJCNN)*, Killarney, Ireland, 2015.
722. I. Tzouvadaki, N. Madaboosi, R. G. Soares, J.-P. Conde, G. De Micheli, and S. Carrara. “Bio-functionalization studies on Silicon Nanowire arrays with Anti-Prostate Specific Antigen Antibodies.” *IEEE PRIME 2015*, Glasgow, Scotland, UK, 2015.
723. N. Aliakbari, G. De Micheli and S. Carrara. “Optimized Electrochemical Detection of Anti-Cancer Drug by Carbon Nanotubes or Gold Nanoparticles.” *IEEE PRIME 2015*, Glasgow, Scotland, UK, 2015.
724. X. Tang, P.-E. Gaillardon and G. De Micheli. “Accurate Power Analysis for Near-Vt RRAM-based FPGA.” *25th International Conference on Field-programmable Logic and Applications (FPL)*, London, UK, 2015.
725. P.-E. Gaillardon, J. Zhang, M. De Marchi and G. De Micheli. “Towards Functionality-Enhanced Devices: Controlling the Modes of Operation in Three-Independent-Gate Transistors .” *10th IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Anchorage, Alaska, USA, 2015.
726. J. Zhang, P.-E. Gaillardon and G. De Micheli. “A Surface Potential and Current Model for Polarity-Controllable Silicon Nanowire FETs.” *45th European Solid-State Device Conference (ESSDERC)* Graz, Austria, 2015.
727. X. Tang, P.-E. Gaillardon and G. De Micheli. “FPGA-SPICE: A Simulation-based Power Estimation Framework for FPGAs.” *33rd IEEE International Conference on Computer Design (ICCD)*, New York, New York, USA, 2015.

728. O. Zografos, B. Sore, A. Vaysset, S. Cosemans, L. Amar, G. De Micheli et al. “Design and Benchmarking of Hybrid CMOS-Spin Wave Device Circuits Compared to 10nm CMOS.” *15th International IEEE Conference on Nanotechnology (NANO)*, Rome, Italy, 2015.
729. H. Ghasemzadeh, P.-E. Gaillardon, J. Zhang, G. De Micheli, E. Sanchez and Matteo Sonza Reorda. “On the Design of a Fault Tolerant Ripple-Carry Adder with Controllable-Polarity Transistors.” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, France, 2015.
730. A. Lotfi, D. Demarchi, F. Puppo, G. De Micheli, S. Carrara and M.A. Ducey. “Reliable Redundancy with Memristive-Biosensors to achieve Statistical Significance in Immunosensing.” *6th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Gallipoli, Italy, 2015.
731. G. De Micheli. “E-Health: From Sensors to Systems.” *Transducers 2015*, Anchorage, Alaska, 2015.
732. A. Ibrahim, A. Simalatsar, S. Skalistis, F. Angiolini, M. Arditi, J-P. Thiran and G. De Micheli. “Assessment of Image Quality vs. Computation Cost for Different Parameterizations of Ultrasound Imaging Pipelines”. *6th Workshop on Medical Cyber-Physical Systems*, Seattle, WA, USA, 2015.
733. W. Haaswijk, L. Amar, P.-E. Gaillardon and G. De Micheli. “NEM Relay Design with Biconditional Binary Decision Diagrams”. *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH '15)*, Boston, Massachusetts, USA, 2015.
734. L. Amarú, P.-E. Gaillardon, A. Mishchenko, M. Ciesielski and G. De Micheli. “Exploiting Circuit Duality to Speed Up SAT”. *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, France, 2015.
735. S. Miryala, V. Tenace, A. Calimera, E. Macii, M. Poncino, L. Amarù, P.E. Gaillardon and G. De Micheli, “Exploiting the Expressive Power of Graphene Reconfigurable Gates via Post-Synthesis Optimization”. *25th Great Lakes Symposium on VLSI (GLSVLSI)*, Pittsburgh, Pennsylvania, USA, 2015.
736. S. Rahimian Omam, X. Tang, P.-E. Gaillardon and G. De Micheli. “A Study on Buffer Distribution for RRAM-based FPGA Routing Structures”. *6th IEEE Latin American Symposium on Circuits and Systems (LASCAS 2015)*, Montevideo, Uruguay, 2015.
737. G. De Micheli, J. Bagherli, T. Collette, A. Domic, H. Symanzik, H. Yassaie, and M. Casale-Rossi “The Future of Electronics, Semiconductors, and Design in Europe.” *Design, Automation & Test in Europe (DATE 2015)*, Grenoble, France, 2015.
738. L. Amarú, P.-E. Gaillardon and G. De Micheli. “Boolean Logic Optimization in Majority-Inverter Graphs”. *Design Automation Conference (DAC)*, San Francisco, California, USA, 2015.
739. A. Chattopadhyay, A. Littarru, L. Amar, P.-E. Gaillardon and G. De Micheli. “Reversible Logic Synthesis via Biconditional Binary Decision Diagrams”. *IEEE International Symposium on Multiple-Valued Logic (ISMVL)*, Waterloo, Ontario, Canada, 2015.
740. S. Carrara, C. Baj-Rossi, S. S. Ghoreishizadeh, S. Riario, G. Surrel, F. Stardolini, C. Boero, G. De Micheli, E. Kilinc and C. Dehollain, “Full System for Translational Studies of Personalized Medicine with Free-Moving Mice”. *International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, 2015.
741. H. Ghasemzadeh, P.-E. Gaillardon and G. De Micheli. “Fault Modeling in Controllable Polarity Silicon Nanowire Circuits”. *Design, Automation & Test in Europe (DATE 2015)*, Grenoble, France, 2015.
742. P.-E. J. M. Gaillardon, X. Tang, J. Sandrini, M. Thammasack, S. Rahimian Omam, D. Sacchetto, Y. Leblebici and G. De Micheli, “A Ultra-Low-Power FPGA Based on Monolithically Integrated RRAMs”. *Design, Automation & Test in Europe (DATE 2015)*, Grenoble, France, 2015.
743. A. Ibrahim, P. Hager, F. Angiolini, M. Arditi, L. Benini and G. De Micheli, “Tackling the Bottleneck of Delay Tables in 3D Ultrasound Imaging”. *Design, Automation & Test in Europe (DATE 2015)*, Grenoble, France, 2015.
744. L. Amarú, A. Petkovska, P.-E. Gaillardon, D. Novo and P. Ienne et al. “Majority-Inverter Graph for FPGA Synthesis”. *19th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI 2015)*, Yilan, Taiwan, 2015.
745. J. Broc, P.-E. Gaillardon, L. Amar, J. J. Murillo, K. Palem and G. De Micheli, “A Fast Pruning Technique for Low-Power Inexact Circuit Design”. *6th IEEE Latin American Symposium on Circuits and Systems (LASCAS 2015)*, Montevideo, Uruguay, 2015.
746. P.-E. Gaillardon, L. Amar, G. Kim, X. Tang and G. De Micheli. “Towards More Efficient Logic Blocks by Exploiting Biconditional Expansion”. *23rd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2015)*, Monterey, California, USA, 2015.

747. L. Amarú, G. Hills, P.-E. Gaillardon, S. Mitra and G. De Micheli. "Multiple Independent Gate FETs: How Many Gates Do We Need?" *20th Asia and South Pacific Design Automation Conference (ASP-DAC 2015)*, Chiba/Tokyo, Japan, 2015.
748. G. De Micheli. "NANO-TERA.CH: Electronic Technology for Health Management", *9th Jordanian International Electrical and Electronics Engineering Conference (JIEEEEC 2015)*, Amman, Jordan, 2015.
749. A. C. Yzglyer, W. Simon, A. Ibrahim, F. Angiolini, M. Arditi, J.P. Thiran and G. De Micheli, "Dem: Efficient Delay and Apodization for on-FPGA 3D Ultrasound." *Conference on Design and Architectures for Signal and Image Processing (DASIP)*, Rennes, France, 2016.
750. A. C. Yzglyer, W. Simon, A. Ibrahim, F. Angiolini, M. Arditi, J.P. Thiran and G. De Micheli, "Single-FPGA 3D Ultrasound Beamformer." *26th International Conference on Field-Programmable Logic and Applications (FPL)*, Lausanne, Switzerland, 2016.
751. W. Simon, A. C. Yzglyer, A. Ibrahim, F. Angiolini, M. Arditi, J.P. Thiran and G. De Micheli, "Single-FPGA, Scalable, Low-Power, and High-Quality 3D Ultrasound Beamformer." *26th International Conference on Field-Programmable Logic and Applications (FPL)*, Lausanne, Switzerland, 2016.
752. A. Ibrahim, F. Angiolini, M. Arditi, J.-P. Thiran and G. De Micheli. "Apodization Scheme for Hardware-Efficient Beamformer." *12th Conference on PhD Research in Microelectronics and Electronics (PRIME)*, Lisbon, Portugal, 2016.
753. I. Tzouvadaki, X. Lu, G. De Micheli, S. Ingebrandt and S. Carrara. "Nano-fabricated memristive biosensors for biomedical applications with liquid and dried samples." *IEEE 38th Annual International Conference of the Engineering in Medicine and Biology Society (EMBC)*, Orlando, Florida, USA, 2016.
754. M. Soeken, P. Raiola, B. Sterin, B. Becker, G. De Micheli and M. Sauer "SAT-Based Combinational and Sequential Dependency Computation." *12th Haifa Verification Conference (HVC 2016)*, Haifa, Israel, 2016.
755. F. Stradolini, E. Lavalle, G. De Micheli, P. Motto Ros, D. Demarchi and S. Carrara, "Paradigm-Shifting Players for IoT: Smart-Watches for Intensive Care Monitoring." *6th International Conference on Wireless Mobile Communication and Healthcare (MobiHealth)*, Milan, Italy, 2016.
756. A. Petkovska, M. Soeken, G. De Micheli, P. Ienne and A. Mishchenko. "Fast Hierarchical NPN Classification." *International Conference on Field-Programmable Logic and Applications*, Lausanne, Switzerland, 2016.
757. M. Casale-Rossi, G. De Micheli, A. Domic, E. Macii, D. Rossi and J. Sawicki, "Panel: Looking Backwards and Forwards." *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Dresden, Germany, 2016.
758. A. Petkovska, A. Mishchenko, M. Soeken, G. De Micheli and R. K. Brayton et al. "Fast generation of lexicographic satisfiable assignments: enabling canonicity in SAT-based applications." *International Conference on Computer Aided Design (ICCAD)*, Austin, Texas, USA, 2016.
759. E. Testa, M. Soeken, O. Zografos, L. Amaru, P. Raghavan, R. Lauwereneis, P.E. Gaillardon and G. De Micheli, "Inversion optimization in majority-inverter graphs." *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Beijing, China, 2016.
760. M. Soeken, N. Abdessaied and G. De Micheli. "Enumeration of reversible functions and its application to circuit complexity." *8th Conference on Reversible Computation (RC)*, Bologna, Italy, Lecture Notes in Computer Science, 2016.
761. M. Soeken, A. Mishchenko, A. Petkovska, B. Sterin, P. Ienne, A. Mishchenko and G. De Micheli, "Heuristic NPN classification for large functions using AIGs and LEXSAT." *19th International Conference on Theory and Applications of Satisfiability Testing (SAT)*, Bordeaux, France, Lecture Notes in Computer Science, 2016.
762. I. Tzouvadaki, A. Vallero, F. Puppo, G. De Micheli and S. Carrara. "Resistance impact by long connections on electrical behavior of integrated Memristive Biosensors." *IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, Canada, 2016.
763. S. Ghoreishizadeh, P. Georgiu, S. Carrara and G. De Micheli. "An Integrated Platform for Differential Electrochemical and ISFET Sensing." *IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, Canada, 2016.
764. F. Stradolini, T. Elboshra, A. Biscontini, G. De Micheli and S. Carrara. "Simultaneous Monitoring of Anesthetics and Therapeutic Compounds with a Portable Multichannel Potentiostat." *IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, Canada, 2016.

765. K. Kang, S. Park, J.-B. Lee, L. Benini and G. De Micheli. "A Power-Efficient 3-D On-Chip Interconnect for Multi-Core Accelerators with Stacked L2 Cache. " *Design, Automation and Test in Europe (DATE)*, Dresden, Germany, 2016.
766. A. Chattopadhyay, L. Amaru, M. Soeken, P.-E. Gaillardon and G. De Micheli. "Notes on Majority Boolean Algebra. " *IEEE International Symposium on Multi-Valued Logic (ISMVL)*, Sapporo, Japan, International Symposium on Multiple-Valued Logic, 2016.
767. M. Soeken, S. Shirinzadeh, P.-E. Gaillardon, L. Amaru R. Drechsler and G. De Micheli, "An MIG-based Compiler for Programmable Logic-in-Memory Architectures. " *53rd Design Automation Conference (DAC)*, Austin, Texas, USA, , 2016.
768. L. Amaru, P.-E. Gaillardon and G. De Micheli. "Majority-based Synthesis for Nanotechnologies. " *21st Asia and South Pacific Design Automation Conference (ASP-DAC 2016)*, Macao SAR, China, 2016.
769. X. Tang, P.-E. Gaillardon and G. De Micheli. "A Full-Capacity Local Routing Architecture for FPGAs. " *24rd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2016)*, Monterey, California, USA, 2016.
770. P.-E. Gaillardon, L. Amaru, A. Siemon, E. Linn, R. Waser, A Chattopadhyay and Giovanni De Micheli, "The Programmable Logic-in-Memory (PLiM) Computer ," *Design, Automation & Test in Europe Conference (DATE)*, Dresden, Germany, 2016.
771. M. Soeken, L. Amaru P.-E. Gaillardon and G. De Micheli. "Optimizing Majority-Inverter Graphs with Functional Hashing," *Design, Automation & Test in Europe Conference (DATE)*, Dresden, Germany, 2016.
772. L. Amaru, P.-E. Gaillardon, R. Wille and G. De Micheli. "Exploiting Inherent Characteristic of Reversible Circuits for Faster Combinational Equivalence Checking. " *Design, Automation & Test in Europe Conference (DATE)* Dresden, Germany,2016.
773. I. Tzouvadaki, N. Aliakbarinodehi, G. De Micheli and S. Carrara. "Memristive Aptasensors for Theranostics", *International Conference on Memristive Materials, Devices and Systems*, Athens, Greece, 2017.
774. B. Donato, F. Stradolini, A. Tuoheti, F. Angiolini, D. Demarchi, G. De Micheli and S, Carrara. "Raspberry Pi Driven Flow-Injection System for Electrochemical Continuous Monitoring Platforms", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Turin, Italy, 2017.
775. F. Criscuolo, I. Taurino, T. Kili, S. Carrara and G. De Micheli. "An electrochemical sensor for quantitative analysis of Rhesus D antibodies in blood", *7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Vieste, Italy, 2017.
776. A. Ibrahim, D. Doy, C. Loureiro, E. Pignat, F. Angiolini, M. Arditi, J.-P. Thiran and G. De Micheli. "Inexpensive 1024-Channel 3D Telesonography System on FPGA", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Turin, Italy, 2017.
777. A. Ibrahim, W. Simon, D. Doy, E. Pignat, F. Angiolini, M. Arditi, J.-P. Thiran and G. De Micheli. "Single-FPGA complete 3D and 2D medical ultrasound imager", *2017 Conference on Design and Architectures for Signal and Image processing (DASIP)*, Dresden, Germany, 2017.
778. S. Naus, I. Tzouvadaki, P.-E. Gaillardon, A. Biscontini, G. De Micheli and S. Carrara. "An Efficient Electronic Measurement Interface for Memristive Biosensors", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, USA, 2017.
779. L. Amaru, M. Soeken, P. Vuillod, J. Luo, A. Mishchenko, P.-E. Gaillardon, J. Olson, R. Brayton and G. De Micheli, "Enabling exact delay synthesis", *36th IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Irvine, California, USA, 2017.
780. E. Testa, O. Zografos, M. Soeken, A. Vaysset and M. Manfrini, R. Lauwereins, G. De Micheli. "Inverter Propagation and Fan-Out Constraints for Beyond-CMOS Majority-Based Technologies", *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Bochum, Germany, 2017.
781. M. Soeken, M. Roetteler, N. Wiebe and G. De Micheli. "Hierarchical Reversible Logic Synthesis Using LUTs", *54th ACM/IEEE Design Automation Conference (DAC)*, Austin, Texas, USA, 2017.
782. M. Soeken, P.-E. Gaillardon and G. De Micheli. "RM3 based logic synthesis", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, USA, 2017.
783. Z. Chu, X. Tang, M. Soeken, A. Petkovska, G. Zgheib , L. Amar, Y. Xia, P. Ienne and G. De Micheli, P.-E. Gaillardon. "Improving Circuit Mapping Performance Through MIG-based Synthesis for Carry Chains", *Great Lakes Symposium on VLSI (GLVLSI)*, Banff, Alberta, Canada, 2017.

784. W. Haaswijk, E. Testa, M. Soeken and G. De Micheli. "Classifying Functions with Exact Synthesis" ,*IEEE 47th International Symposium on Multiple-Valued Logic (ISMVL)*, Novi Sad, Serbia, 2017.
785. F. Angiolini, A. Ibrahim, W. Simon, A. C. Yuzuguler, M. Arditi, J.-P. Thiran, G. De Micheli. "1024-Channel 3D Ultrasound Digital Beamformer in a Single 5W FPGA",*2017 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, EPFL, Lausanne, Switzerland, 2017.
786. X. Tang, G. De Micheli and P.-E. Gaillardon. "Optimization Opportunities in RRAM-based FPGA Architectures",*IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS)*, Bariloche, Argentina, 2017.
787. O. Zografos, A. De Meester, E. Testa, M. Soeken, P.-E. Gaillardon, G. De Micheli, L. Amar, P. Raghavan, F. Catthoor and R. Lauwereins. "Wave Pipelining for Majority-based Beyond-CMOS Technologies",*Design, Automation & Test in Europe (DATE)*, Lausanne, Switzerland, 2017.
788. M. Soeken, M. Roetteler, N. Wiebe and G. De Micheli. "Design Automation and Design Space Exploration for Quantum Computers",*Design, Automation & Test in Europe (DATE)*, Lausanne, Switzerland, 2017.
789. M. Soeken, G. De Micheli and A. Mishchenko. "Busy Mans Synthesis: Combinational Delay Optimization With SAT",*Design, Automation & Test in Europe (DATE)*, Lausanne, Switzerland, 2017.
790. S. Shirinzadeh, M. Soeken, P.-E. Gaillardon, G. De Micheli and R. Drechsler. "Endurance Management for Resistive Logic-In-Memory Computing Architectures",*Design, Automation & Test in Europe (DATE)*, Lausanne, Switzerland, 2017.
791. X. Tang, E. Giacomini, G. De Micheli and P.-E. Gaillardon. "Physical Design Considerations of One-level RRAM-based Routing Multiplexers",*International Symposium on Physical Design (ISPD)*, Portland, Oregon, USA, 2017.
792. L. Amaru, M. Soeken, W. Haaswijk, E. Testa, P. Vuillod, J. Luo, P.-E. Gaillardon, and G. De Micheli. "Multi-level Logic Benchmarks: An Exactness Study",*22nd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Chiba, Japan, 2017.
793. W. Haaswijk, M. Soeken, L. Amaru, P.-E. Gaillardon and G. De Micheli. "A Novel Basis for Logic Rewriting",*22nd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Chiba, Japan, 2017.
794. L. Amaru, M. Soeken, P. Vuillod, J. Luo, A. Mishchenko, J. Olson, R. Brayton and G. De Micheli. "Improvements to Boolean resynthesis",*Design, Automation and Test in Europe*, Dresden, Germany, pp. 755-790, 2018.
795. Z. Chu, M. Soeken, Y. Xia and G. De Micheli. "Functional decomposition using majority",*23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Korea, 2018.
796. G. Meuli, M. Soeken, M. Roetteler, N. Wiebe and G. De Micheli. "A best-fit mapping algorithm to facilitate ESOP-decomposition in Clifford+T quantum network synthesis",*23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 664-669, Jeju Island, Korea, 2018.
797. W. J. Haaswijk, L. Amaru, P. Vuillod, J. Luo, M. Soeken, G. De Micheli, "Integrated ESOP Refactoring for Industrial Designs" , *Proceedings of the 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. Bordeaux, France. December 2018.
798. F. Criscuolo, I. Taurino, S. Carrara, G. De Micheli, "A novel electrochemical sensor for non-invasive monitoring of lithium levels in mood disorders" , *Proceedings of the 40th International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. pp. 3825-3828, Honolulu, HI, USA. July 2018.
799. W.J. Haaswijk, E. Collins, B. Seguin, M. Soeken, F. Kaplan, S. Susstrunk, G. De Micheli, "Deep Learning for Logic Optimization Algorithms" , *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*. pp. 1-4., Florence, Italy. May 2018.
800. W. J. Haaswijk, A. Mishchenko, M. Soeken, G. De Micheli, "SAT Based Exact Synthesis using DAG Topology Families" , *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 1-6. San Francisco, CA, USA. June 2018.
801. G. Meuli, M. Soeken, G. De Micheli, "SAT-based CNOT, T Quantum Circuit Synthesis" , International Conference on Reversible Computation, *Reversible Computation*, pp. 175-188, Leicester, UK. August 2018.
802. M.I. Ny Hanitra, L. Lobello, F. Stradolini, A. Tuoheti, F. Criscuolo, T. Kilic, D. Demarchi, S. Carrara, G. De Micheli, "A Flexible Front-End for Wearable Electrochemical Sensing" , *IEEE International Symposium on Medical Measurements and Applications (MeMeA)*, pp. 1-6. Rome, Italy. June 2018.



803. G.V. Resta, Y. Balaji, D. Lin, I.P. Radu, F. Catthor, P.-E. Gaillardon, G. De Micheli, "Doping-free complementary inverter enabled by 2D WSe<sub>2</sub> electrostatically-doped reconfigurable transistors", *76th Device Research Conference (DRC)*, p. 1-2. Santa Barbara, CA, USA. June 2018.
804. G. V. Resta, J. R. Gonzalez, Y. Balaji, T. Agarwal, D. Lin, F. Catthor, I.P. Radu, G. De Micheli, P.-E. Gaillardon, "Towards high-performance polarity-controllable FETs with 2D materials", *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 637-641. Dresden, Germany. March 2018.
805. M. Soeken, W. J. Haaswijk, E. Testa, A. Mishchenko, L. Amaru, R. Brayton, G. De Micheli, "Practical Exact Synthesis", *Proceedings of the 2018 Design, Automation & Test In Europe Conference & Exhibition (DATE)*. pp. 309-314. 2018.
806. I. Tzouvadaki, A. Tuoheti, G. De Micheli, D. Demarchi, S. Carrara, "Portable Memristive Biosensing System as Effective Point-of-Care Device for Cancer Diagnostics", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, Florence, Italy. May 2018.
807. C. Yu, C.-C. Huang, G.-J. Nam, M. Choudhury, V.N. Kravets, A. Sullivan, M. Ciesielski, G. De Micheli, "End-to-End Industrial Study of Retiming", *IEEE Computer Society Annual Symposium on VLSI*. pp. 203-208, Hong Kong, China. July 2018.
808. C. Yu, H. Riener, F. Stradolini, G. De Micheli, "Generating Safety Guidance for Medical Injection with Three-Compartment Pharmacokinetics Model", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI18)*, IEEE Computer Society Annual Symposium on VLSI. pp. 299-304, Hong Kong, China. July 2018.
809. C. Yu, H. Xiao, G. De Micheli, "Developing Synthesis Flows without Human Knowledge", *Proceedings of the ACM/IEEE Design Automation Conference (DAC18)*, pp. 1-6, San Francisco, CA, USA. June 2018.
810. H. Riener, E. Testa, L. Amaru, M. Soeken, and G. De Micheli, "Size Optimization of MIGs with an Application to QCA and STMG Technologies", In *14th IEEE / ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Athens, Greece, 2018.
811. Z. Chu, W. Haaswijk, M. Soeken, Y. Xia, L. Wang, and G. De Micheli, "Exact Synthesis of Boolean Functions in Majority-of-Five Forms", in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019.
812. H. Riener, W. Haaswijk, A. Mishchenko, G. De Micheli, and M. Soeken, "On-the-y and DAG-aware: Rewriting Boolean Networks with Exact Synthesis" *DATE 2019* Firenze, Italy, March 2019.
813. G. Meuli, M. Soeken, M. Roetteler, N. Bjorner, G. De Micheli, "Reversible Pebbling Game for Quantum Memory Management", *DATE 2019*, Firenze, Italy, March 2019.
814. E. Testa, L. Amaru, M. Soeken, A. Mishchenko, P. Vuillod, J. Luo, C. Casares, P.-E. Gaillardon, G. De Micheli, "Scalable Boolean Methods in a Modern Synthesis Flow" *DATE 2019*, Firenze, Italy, March 2019.
815. H. Riener, E. Testa, W. Haaswijk, A. Mishchenko, L. Amar, G. De Micheli, and M. Soeken, "Scalable Generic Logic Synthesis: One Approach to Rule Them All" *DAC 2019*, Las Vegas, USA, June 2019.
816. E. Testa, M. Soeken, L. Amaru, G. De Micheli, "Reducing the Multiplicative Complexity in Logic Networks for Cryptography and Security Applications" *DAC 2019*, Las Vegas, USA, June 2019.
817. G. Meuli, M. Soeken, M. Roetteler, G. De Micheli, "Resource constrained oracle synthesis for quantum computers" *Quantum Physics and Logic (QPL)*, Orange CA, USA, June 1014, 2019.
818. K. Smith, M. Soeken, B. Schmitt, G. De Micheli, M. Thornton, "Using ZDDs in the mapping of quantum circuits" *Quantum Physics and Logic (QPL)*, Orange CA, USA, June 1014, 2019.
819. F. Criscuolo; M. Galfione; S. Carrara; G. De Micheli, "All-solid-state Reference Electrodes for analytical applications" *8th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Otranto, Italy, June 2019
820. G. Meuli, B. Schmitt, R. Ehlers, H. Riener, G. De Micheli, "Evaluating ESOP Optimization Methods in Quantum Compilation Flows" *Reversible Computing (RC)*, Lausanne, Switzerland, June 24-25, 2019.
821. I. Ny Hanitra, F. Criscuolo, S. Carrara, G. De Micheli, "Multi-Target Electrolyte Sensing Front-End for Wearable Physical Monitoring", *15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, Lausanne, Switzerland, July 2019
822. M. Imani, J. Morris, S. Bosch, H. Shu, G. De Micheli, T. Rosing, AdaptHD: Adaptive Efficient Training for Brain-Inspired Hyperdimensional Computing, *BioCAS*, Nara, Japan, October 17-19, 2019
823. F. Criscuolo, F. Cant, I. Taurino, S. Carrara, G. De Micheli, Flexible sweat sensors for non-invasive optimization of lithium dose in psychiatric disorders, *IEEE Sensors 2019*, Montreal, Canada, October 27-30, 2019.

824. M. Soeken, E. Testa and M. Miller, "A Hybrid Method for Spectral Translation Equivalent Boolean Functions", *Pacific Rim Conference on Communication Computers and Signal Processing*, 2019.
825. G. Meuli, M. Soeken, E. Campbell, M. Roetteler and G. De Micheli, The Role of Multiplicative Complexity in Compiling Low T-count Oracle Circuits, *ICCAD*, 2019.
826. E. Testa, M. Soeken, H. Riener, L. Amaru, G. De Micheli, A Logic Synthesis Toolbox for Reducing the Multiplicative Complexity in Logic Networks, *DATE 2020* Grenoble, France, March 2020.
827. E. Testa, S. Lubaba Noor, O. Zografos, M. Soeken, F. Catthoor, A. Naeemi, G. De Micheli, Multiplier Architectures: Challenges and Opportunities with Plasmonic-based Logic, *DATE 2020* Grenoble, France, March 2020.
828. L. Amaru, F. Marranghello, E. Testa, C. Casares, V. Possani, J. Luo, P. Vuillod, A. Mishchenko, G. De Micheli, "SAT-Sweeping Enhanced for Logic Synthesis", *DAC 2020* San Francisco, USA.
829. G. Meuli, M. Soeken, M. Roetteler, G. De Micheli, "Enumerating Optimal Quantum Circuits using Spectral Clasification" *ISCAS 2020* Seville, Spain, October 2020.
830. I. Ny Hanitra, D. Demarchi, S. Carrara, G. De Micheli, "Emulator Design and Generation of Synthetic Dataset in Multi-Ion Sensing", *ISCAS 2020* Seville, Spain, October 2020.
831. F. Mozafari, M. Soeken, H. Riener, G. De Micheli, "Automatic Uniform Quantum State Preparation Using Decision Diagrams", *ISMVL 2020* Miyazaki, Japan, November 2020.
832. B. Schmitt, M. Soeken, G. De Micheli, "Symbolic Algorithms for Token Swapping", *ISMVL 2020* Miyazaki, Japan, November 2020.
833. E. Testa, S-Y. Lee, H. Riener and G. De Micheli, "Algebraic and Boolean Optimization Methods for AQFP Superconducting Circuits", *ASPDAC*, Tokyo, Japan, 2021.
834. S. Rai, H. Riener, G. De Micheli and A. Kumar, "Preserving Self-Duality During Logic Synthesis for Emerging Reconfigurable Nanotechnologies", *DATE 2021* Grenoble, France, February 2021.
835. B. Schmitt, A. Javadi-Abhari and G. De Micheli, "Compilation flow for classically-defined quantum operations", *DATE 2021* Grenoble, France, February 2021.
836. B. Schmitt, F. Mozafari, G. Meuli, H. Riener and G. De Micheli, "From Boolean functions to quantum circuits: A scalable quantum compilation flow in C++", *DATE 2021* Grenoble, France, February 2021.
837. S-Y Lee, H. Riener and G. De Micheli, "Logic Resynthesis of Majority-Based Circuits by Top-Down Decomposition", *DDECS*, Vienna, April 2021.
838. D. Marakkalage, H. Riener and G. De Micheli, "Optiomizing Adiabatic Quantum Flux Parametron (AQFP) Circuits using Exact Database", *NanoArch*, 2021.
839. L. Amaru, V. Possani, E. Testa, F. Marranghello, C.Casares, J. Luo, P. Vuillod, A. Mishchenko and G. De Micheli, "LUT-Based Optimization For ASIC Design Flow", *Dersign Automation Conference*, San Francisco, CA, 2021.
840. H. Riener, S.-Y. Lee, A. Mishchenko and G.De Micheli "Boolean Rewriting Strikes Back: Reconvergence-Driven Windowing meets Resynthesis," *Proceedings ASPDAC*, January 2022.
841. F. Mozafari, Y. Yang and G.De Micheli "Efficient preparation of Cyclic Quantum States" *Proceedings ASPDAC*, January 2022.
842. A. Tempia Calvino, H. Riener, S.Rai A. Kumar and G. De Micheli "A Versatile Mapping Approach for Technology Mapping and Graph Optimization," *Proceedings ASPDAC*, January 2022.
843. G. Meuli, V. Possani, R. Singh, S.-Y. Lee, A. Tempia Calvino, D. Marakkalage, P. Vuillod, L. Amaru, S. Chase, J. Kawa and G. De Micheli, "Majority-based Design Flow for AQFP Superconducting Family", *DATE 2022*.
844. B. Schmitt and G. De Micheli, "tweedledum: A Compiler Companion for Quantum Computing", *DATE 2022*.
845. A. Costamagna and G. De Micheli, Logic Synthesis From Incomplete Specifications Using Disjoint Support Decomposition, *Prime*, Cagliari, 2022.
846. S.-Y. Lee, H. Riener and G. De Micheli, Beyond Local Optimality of Buffer and Splitter Insertion for AQFP Circuits, *DAC*, San Francisco, 2022.
847. A. Tempia Calvino and G. De Micheli, "Depth-Optimal Buffer and Splitter Insertion and Optimization in AQFP Circuits", *Proceedings of ASPDAC*, January 2023.

848. D. Sudara Marakkalage and G. De Micheli, "Fanout-Bounded Logic Synthesis for Emerging Technologies - A Top-Down Approach", *Proceedings of DATE*, March 2023.
849. M. Yu and G. De Micheli, "Generating Lower-Cost Garbled Circuits: Logic Synthesis Can Help," *HOST*, 2023.
850. R. Bairamkulov and G. De Micheli, "Compound Gates for Pipeline Depth Optimization in Single Flux Quantum Integrated Systems," *Proceedings of GVLIS*, 2023.
851. A. Tempia Calvino, Al. Mishchenko, H. Schmit, E. Mahintorabi, G. De Micheli, and X. Xu, "Improving Standard-Cell Design Flow using Factored Form Optimization," *DAC* 2023.
852. G. De Micheli, "Logic Synthesis for Emerging Technologies," *Proceedings ASICON*, Nanjing, 2023.
853. G. De Micheli, "Cyclical Progress in Design and Technology," *Proceedings ICTA*, Hefei, 2023.
854. A. Tempia Calvino and G. De Micheli, "Technology Mapping using Multi-output Library cells," *Proceedings ICCAD*, 2023.
855. M. Yu and G. De Micheli, "Striving for both quality and Speed: Logic Synthesis for Practical Garbled Circuits," *Proceedings ICCAD*, 2023.
856. R. Bairamkulov, Al. Tempia Calvino and G. De Micheli, "Synthesis of SFQ Circuits with Compound Gates," *Proceedings of VLSI-SOC*, Dubai, 2023.
857. A. Calvino and G. De Micheli, "Algebraic and Boolean Methods for SFQ Superconducting Circuits", *Proceedings ASPDAC*, Incheon, Korea, 2024.
858. A. Calvino, G. Radi and G. De Micheli, "In Medio Stat Virtus: Combining Boolean and Pattern Matching", *Proceedings ASPDAC*, Incheon, Korea, 2024.
859. R. Bairamkulov, A. Tempia Calvino and G. De Micheli, "Multiphase Clocking in Single-Flux Quantum Systems", *Proceedings ASPDAC*, Incheon, Korea, 2024.
860. C. Meng, H. Wang, Y. Mai, W. Qian, and G. De Micheli, "VACSEM: Verifying Average Errors in Approximate Circuits Using Simulation-Enhanced Model Counting", *DATE*, Valencia 2024.
861. A. Tempia Calvino G. De Micheli, "Scalable Logic Rewriting Using Dont Cares," *DATE*, Valencia 2024.
862. H. Wang, J. Cong and G. De Micheli, "Quantum State Preparation Using an Exact CNOT Synthesis Formulation," *DATE*, Valencia 2024.
863. D. Marakkalage, E. Testa, W. Lau Neto, A. Mishchenko, G. De Micheli and L. Amaru, "Scalable Sequential Optimization Under Observability Dont Cares", *DATE*, Valencia 2024.
864. R. Bairamkulov, M. Yu and G. De Micheli, "Unleashing the Power of T1-cells in SFQ Arithmetic Circuits", *DATE*, Valencia 2024.
865. R. Bairamkulov, S.-Y. Lee, A. Tempia-Calvino, D. Marakkalage, M. Yu and G. De Micheli, "Technology-Aware Logic Synthesis for Superconducting Electronics", *DATE*, Valencia 2024.
866. A. Costamagna, A. Mishchenko, S. Chatterjee and G. De Micheli, "An Enhanced Resubstitution Algorithm for Area-Oriented Logic Optimization", *ISCAS* Singapore 2024.
867. R. Bairamkulov, M. Yu and G. De Micheli, "Unleashing the Power of T1-cells in SFQ Arithmetic Circuits", *DAC*, San Francisco, 2024.
868. S.Y. Lee, A. Tempia Calvino, H. Riener and G. De Micheli, "Late Breaking Results: Majority-Inverter Graph Minimization by Design Space Exploration", *DAC*, San Francisco, 2024.
869. T. Koike-Akino, C. Meng, V. Cevher and G. De Micheli, "Hardware-Efficient Quantization for Green Custom Foundation Models", *ES-FoMo-II, International Conference on Machine Learning (ICML)*, Vienna, 2024
870. D. Marakkalage, M. Weber, S.-Y. Lee, R. Wille and G. De Micheli, "Technology Mapping for Beyond-CMOS Circuitry with Unconventional Cost Functions", *IEEE Nano*, Girona 2024.
871. M. Yu, S. Carpov, A. Tempia-Calvino and G. De Micheli, "On the synthesis of high-performance homomorphic Boolean Circuits", *Proceedings of WAHC: Workshop on Encrypted Computing & Applied Homomorphic Cryptography*, Salt Lake City, 2024.
872. C. Meng, M. Yu, W. Burleson, H. Wang and G. De Micheli, "Rarity-Reducing Logic Synthesis for Mitigating Hardware Trojan Threats", *Proceedings ICCAD*, Newark, NJ, 2024
873. A. Costamagna, A. Mishchenko, S. Chatterjee and G. De Micheli, "Symmetry-Based Synthesis For Interpretable Boolean Evaluation," *Proceedings of VLSI Design*, Bengaluru, India, 2025.

874. A. Costamagna, A. Tempia Calvino, A. Mishchenko and G. De Micheli, "Area-Oriented Optimization After Standard-Cell Mapping," *Proceedings of ASPDAC*, Tokyo, 2025.
875. M. Yu, A. Tempia Calvino, M. Soeken and G. De Micheli, "Back-end-aware Fault-tolerant Quantum Oracle Synthesis," *Proceedings of ASPDAC*, Tokyo, 2025.
876. C. Meng, W. Burleson, W. Qian and G. De Micheli, "Gradient Approximation of Approximate Multipliers for High-Accuracy Deep Neural Network Retraining," *Proceedings of DATE*, Lyon, 2025
877. A. Costamagna, X. Xu, G. De Micheli, D. Ruic, "Lazy Mans Resynthesis For Glitching-Aware Power Minimization", *Proceedings of DDECS*, Lyon, 2025
878. A. Costamagna, C. Meng and G. De Micheli, "SPFD-Based Delay Resynthesis", *Proceedings of SMCAD*, Istanbul, 2025

#### Conference Proceedings Abstracts (fully refereed)

879. C. Nardini, S. Cha, D. Wang, M. Diehn, M. Mayo, L. Benini, G. De Micheli, M. Kuo, "A Non-invasive Approach for Molecular Characterization of Glioblastoma Multiforme: MRI Correlation with cDNA Expression Profiles, *AANS - Proceedings of the 6th annual meeting of Neurological Surgeons*, San Francisco, 2004. ([www.ans.org](http://www.ans.org))
880. E. Ficarra, G. De Micheli, S. Yoon, L. Benini and E. Macii "Bioimaging and Functional Genomics," *pHealth*, Luzern, Switzerland, 2006.
881. D.S. Wand, S. Cha, C. Nardini, M. Diehn, B.K.Chan, L. Benini, G. De Micheli and M. Kuo, "A Method for Extracting Imaging Correlations with Alterations in Global Gene Expression." *RSNA - Proceedings of the Radiological Society of North America Conference*, Chicago, 2004. ([www.rsna.org](http://www.rsna.org))
882. A. Garg, A. Di Cara, M. Ibberson, G. Degueurce, I. Xenarios, G. De Micheli, and K. Mohanram, "Efficient method for generating minimal intervention sets in Gene Regulatory Networks," in *3rd Annual Joint Conference on Systems Biology, Regulatory Genomics, and Reverse Engineering Challenges*, 2010.
883. G. De Micheli. Integrated biosensing for diagnosis and therapy. *4th Annual World Congress of Industrial Biotechnology (ibio-2011)*, Dalian, China, 2011.
884. G. De Micheli, C. Boero, J. Olivo and S. Carrara, "Integrated biosensors for cell culture monitoring", *Congress on Molecular & Cell Biology*, Dalian, China, 2014.
885. G. De Micheli, W. You, N. Widmer and A. Simalatsar, "Drug concentration prediction and delivery", *Annual World Congress of Industrial Biotechnology*, Dalian, China, 2014.
886. P.-E. Gaillardon, L. Amarù, G. Kim, X. Tang and G. De Micheli. "Towards More Efficient Logic Blocks by Exploiting Biconditional Expansion". *23rd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2015)*, Monterey, California, USA, 2015.
887. X. Tang, P.-E. Gaillardon and G. De Micheli. "A Full-Capacity Local Routing Architecture for FPGAs". *24rd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2016)*, Monterey, California, USA, 2016.
888. G. De Micheli, "Design and Optimization of Quantum Electronic Circuits", *International Symposium on Physical Design (ISPD)*, Banff, virtual, April 2022
889. F. Mozafari, G. De Micheli, and Y. Yang, "Efficient Quantum State Preparation Using Decision Diagrams", *Quantum Techniques for Machine Learning*, Naples, 2022.
890. G. De Micheli, "Wearable Sweat-Sensing Mobile Device for Efficient Healthcare Monitoring," *Cluster Meeting of Gala Technology*, Osaka, 2023.

#### Other Publications (fully refereed and with limited distribution)

891. R. Brayton and G. De Micheli, "A Method for Minimizing Critical Timing of a Digital System," *IBM Technical Disclosure Bulletin*, Vol. 30, No. 2, July 1987, pp. 586-589.
892. G. De Micheli and A. Ruehli, "Switching-time of MOS Transistors in Presence of Inductive Effects," *IBM Technical Disclosure Bulletin*, Vol. 31, No. 8, January 1989, pp. 447-448.
893. G. De Micheli, "Synchronous Logic Synthesis," *International Workshop on Logic Synthesis*, Research Triangle Park, May 1989.

894. M. Damiani and G. De Micheli, "The Role of Don't Cares Conditions in Synchronous Circuit Optimization," *SASIMI '90, Proceedings of the Synthesis and Simulation Meeting and International Interchange*, Kyoto, Japan, October 1990, pp. 55-62.
895. D. Filo, D. Ku and G. De Micheli, "Optimizing Control by Delayed Execution of Operations," *International High-Level Synthesis Workshop*, Buelerhoehe, Germany, March 1991, pp. 118-125.
896. M. Damiani and G. De Micheli, "Derivation of Don't Care Conditions by Perturbation Analysis of Combinational Multiple-Level Logic Circuits," *International Logic Synthesis Workshop*, Raleigh, May 1991, Vol. 2, pp. 1-12.
897. A. Bedarida, S. Ercolani and G. De Micheli, "A New Technology Mapping Algorithm for the Design and Evaluation of Field-Programmable Gate Arrays," *ACM International Workshop on Field-Programmable Gate Arrays*, February 1992, pp.103-108.
898. G. De Micheli, "Synthesis of High-Performance Digital Circuits: Logic Transformations for Cycle-Time Reduction of Synchronous Circuits," *SASIMI '92, Proceedings of the Synthesis and Simulation Meeting and International Interchange*, Kobe, Japan, April 1992, pp. 133-142.
899. R. Gupta, C. Coelho and G. De Micheli, "Program Implementation Schemes for Hardware-Software Systems," *ACM Workshop on Hardware-Software Co-design*, October 1992. (Cross-listed as Journal No. 76.)
900. D. Ku, D. Filo, C. Coelho and G. De Micheli, "Interface Optimization for Concurrent Systems Under Timing Constraints using Interface Matching," *International High-Level Synthesis Workshop*, Dana Point, California, November 1992, pp. 202-213.
901. J. Fron, J. Yang, M. Damiani and G. De Micheli, "A Synthesis Framework Based on Trace and Automata Theory," *International Workshop on Logic Synthesis*, 5c-1, 5c-15, May 1993.
902. C. Coelho, D. Ku and G. De Micheli, "An Algebra for Modeling Concurrent Digital Systems," *TAU, ACM International Workshop on Timing Issues*, Malente (Germany), September 1993.
903. L. Benini and G. De Micheli, "Optimal Synthesis of Gated-Clocks for Low-Power Finite-state Machines," *International Logic Synthesis Workshop*, 1995.
904. L. Benini, M. Favalli and G. De Micheli, "Generalized Matching: a New Approach to Concurrent Logic Optimization and Library Binding," *International Logic Synthesis Workshop*, 1995.
905. L. Benini and G. De Micheli, "A Survey of Boolean Matching Techniques for Library Binding," *Proceedings of the Logic and Architecture Workshop*, Grenoble, 1995.
906. A. Bogliolo, L. Benini, D. Guan, D. Ku, and G. De Micheli "Open Distributed EDA Environments on the Web" *SASIMI '96, Proceedings of the Synthesis and Simulation Meeting and International Interchange*, Fukuoka, Japan, 1996, pp.47-56.
907. V. Bertacco, S. Minato, P. Verplaetse, L. Benini and G. De Micheli, "Decision Diagrams and Pass-Transistor Logic Synthesis", *International Logic Synthesis Workshop*, 1997.
908. L. Benini, G. De Micheli, E. Macii, M. Poncino, Q. Quer, D. Sciuto and C. Silvano, "On-going Research on Address Bus Encoding for Low-Power: a Status Report", *International Logic Synthesis Workshop*, 1997.
909. L. Benini, G. De Micheli, E. Macii and M. Poncino, "Telescopic Units: a New Paradigm for Performance Optimization of VLSI Design," *International Logic Synthesis Workshop*, 1997.
910. A. Bogliolo, L. Benini, G. De Micheli, B. Riccò, "Stima di potenza nella progettazione di circuiti integrati a basso consumo," *AEI Annual meeting*, pp. 137 - 142, Baveno, 1997 (in Italian).
911. L. Benini and G. De Micheli "Dynamic Power Management of Electronic Circuits and Systems," *SASIMI '97, Proceedings of the Synthesis and Simulation Meeting and International Interchange*, Osaka, Japan, 1996, pp. 3-10.
912. L. Benini, G. De Micheli, E. Macii, M. Poncino and R. Scarsi, "Integrating Logic-level Power Management Techniques," *SASIMI '97, Proceedings of the Synthesis and Simulation Meeting and International Interchange*, Osaka, Japan, 1996, pp. 59-65.
913. L. Séméria and G. De Micheli, "Encoding of Pointers for Hardware Synthesis," *Proceedings of the Logic and Architecture Workshop*, Grenoble, 1998.
914. M. Barocci, L. Benini, A. Bogliolo, B. Riccò and G. De Micheli, "Look-up Table Power Macro-models for Behavioral Library Components," *Proceedings Volta Memorial Conference*, Como, pp. 173-181, 1999.
915. L. Benini, A. Bogliolo, and G. De Micheli, "Dynamic Power Management for Electronic Systems," *Proceedings Volta Memorial Conference*, Como, pp. 23-31, 1999.

916. L. Séméria, K. Sato and G. De Micheli, "Memory Representation and Hardware Synthesis of C Code with Pointers and Complex Data Structures," *SASIMI '00, Proceedings of the Synthesis and Simulation Meeting and International Interchange*, Kyoto, Japan (2000), pp. 43-48.
917. Eui-Young Chung, L. Benini and G. De Micheli, "Energy Efficient Source Code Transformations based on Value Profiling," *Proceedings of the International Workshop on Compilers and Operating Systems for Low Power*, Philadelphia, October 2000.
918. E.Y. Chung, L. Benini, De Micheli, G. Luculli and M. Carilli, "Value-sensitive Automatic Code Specialization for Energy Reduction," *ST Journal of System Research*, Vol. 3, No. 1, pp. 29-48, 2002. (Cross-listed as Journals 121.)
919. W. Qadeer, T. Simunic, J. Ankorn, V. Krishnan and G. De Micheli, "Heterogeneous wireless network management," *PACS - Workshop on Power-Aware Computer Systems*, San Diego, December 2003.
920. N. Genko, D. Atienza and G. De Micheli, Emulation on FPGA: HW/SW Synergy for NoC Features Exploration, in G.R. Joubert, W.E. Nagel, F.J. Peters, O.Plata, P. Tirado, E. Zapata, Editors, *Parallel Computing: Current & Future Issues of High-End Computing*, *Proceedings of the International Conference ParCo*, 2005.
921. P. Meloni, S. Murali, S. Carta, M. Camplani, L. Raffo and G. De Micheli, "Routing Aware Switch Hardware Customization for Networks on Chips", *Nano-net*, September 2006.
922. D. Atienza, S. Murali, F. Angiolini, L. Benini, G. De Micheli, J. Mendias, and R. Hermida, "Diseo de redes en chip de proposito especifico con informacin de rutado fsico," *XVII Jornadas de Parelelismo*, 2006. (in Spanish).
923. H. Xu, V. F. Pavlidis, and G. De Micheli, "Process-induced skew variation for scaled 2-D and 3-D ICs," in *Proceedings of the 12th ACM/IEEE international workshop on System level interconnect prediction - SLIP '10*, (New York, New York, USA), pp. 17-24, ACM Press, 2010.
924. I. Hatirnaz, S. Badel, N. Pazos, Y. Leblebici, S. Murali, D. Atienza, and G. De Micheli, "Early Wire Characterization for Predictable Network-on-Chip Global Interconnects", *System Level Interconnect Prediction (SLIP)*. Workshop, 2007.
925. C. Seiculescu, S. Volos, N. Khosro Pour, B. Falsafi and G. De Micheli. CCNoC: On-Chip Interconnects for Cache-Coherent Manycore Server Chips. *Workshop on Energy-Efficient Design (WEED 2011)*, San Jose, California, USA, 2011.
926. I. Taurino, S. Carrara, M. Giorcelli, A. Tagliaferro and G. De Micheli. Comparing the enhanced sensing interfaces of differently oriented carbon nanotubes onto silicon for bio-chip applications. *4th International Workshop on Advances in Sensors and Interfaces (IWASI)*, Savelletri di Fasaro, Brindisi, Italy, 2011.
927. S. S. Ghoreishizadeh, C. Baj-Rossi, S. Carrara and G. De Micheli. Nano-Sensor and Circuit Design for Anti-Cancer Drug Detection. *IEEE/NIH 5th Life Science Systems and Applications Workshop*, Bethesda, Maryland, USA, 2011.
928. W. You, A. Simalatsar and G. De Micheli. "RANSAC-based Enhancement in Drug Concentration Prediction Using Support Vector Machine" *International Workshop on Innovative Simulation for Healthcare (IWISH)*, Vienna, Austria, 2012.
929. L. Amarù, P.-E. Gaillardon and G. De Micheli. "Majority Logic Representation and Satisfiability," *23rd International Workshop on Logic Synthesis (IWLS)*, San Francisco, California, USA, 2014.
930. L. Amarù, P.-E. Gaillardon and G. De Micheli. "The EPFL Combinational Benchmark Suite". *24th International Workshop on Logic & Synthesis (IWLS)*, Mountain View, California, USA, 2015.
931. E. Testa, M. Soeken, L. Amaru, P.-E. Gaillardon and G. De Micheli. "Inversion Minimization in Majority-Inverter Graphs." *25th International Workshop on Logic & Synthesis (IWLS)*, Austin, Texas, USA, 2016.
932. W. J. Haaswijk, M. Soeken, L. Amaru, P.-E. Gaillardon and G. De Micheli. "LUT Mapping and Optimization for Majority-Inverter Graphs." *25th International Workshop on Logic & Synthesis (IWLS)*, Austin, Texas, USA, 2016.
933. G. Meuli, M. Soeken, P.-E. Gaillardon and G. De Micheli. "A Compiler for Parallel and Resource-Constrained Programmable in-Memory Computing" *26th International Workshop on Logic & Synthesis (IWLS)*, Austin, Texas, USA, 2017.
934. E. Testa, M. Soeken, O. Zografos, F. Catthoor and G. De Micheli. "Exact Synthesis for Logic Synthesis Applications with Complex Constraints" *26th International Workshop on Logic & Synthesis (IWLS)*, Austin, Texas, USA, 2017.

935. H. Riener, E. Testa, W. Haaswijk, A. Mishchenko, L. Amaru, G. De Micheli, and M. Soeken, "Logic Optimization of Majority-Inverter Graphs", *Workshop MBMV*, Kaiserslautern, Germany, April 2019.
936. E. Testa, W. Haaswijk, M. Soeken, G. De Micheli: "The Complexity of Self-Dual Monotone 7-Input Functions" *28th International Workshop on Logic Synthesis (IWLS)*, Lausanne, Switzerland, June 21-23, 2019.
937. F. Mozafari, M. Soeken, G. De Micheli, "Automatic Preparation of Uniform Quantum States Utilizing Boolean Functions", *28th International Workshop on Logic Synthesis (IWLS)*, Lausanne, Switzerland, June 21-23, 2019.
938. D. S. Marakkalage, E. Testa, H. Riener, A. Mishchenko, M. Soeken, G. De Micheli, "Three-Input Gates for Logic Synthesis", *IWLS 2020*, San Francisco, USA, July 2020.
939. S.-Y. Lee, H. Riener, A. Mishchenko, R. Brayton, G. De Micheli, Simulation-Guided Boolean Resubstitution, *IWLS 2020*, San Francisco, USA, July 2020.
940. S. Rai, H. Riener, G. De Micheli, A. Kumar, XMG-based Logic Synthesis for Emerging Reconfigurable Nanotechnologies, *IWLS 2020*, San Francisco, USA, July 2020.
941. F. Mozafari, H. Riener, and G. De Micheli, "Uniform Quantum State Preparation: A Boolean Approach for Preparing Uniform Quantum States Efficiently and Precisely", In *International Workshop on Quantum Compilation (IWQC)*, Cambridge, UK, September 2020.
942. H. Riener, S.-Y. Lee, A. Mishchenko and G. De Micheli "Boolean Rewriting Strikes Back: Reconvergence-Driven Windowing and Resynthesis," *International Workshop on Logic Synthesis (IWLS) 2021*
943. S.-Y. Lee, H. Riener, and G. De Micheli "Irredundant Buffer and Splitter Insertion and Scheduling-Based Optimization for AQFP," *International Workshop on Logic Synthesis (IWLS) 2021* and ArXiv <http://arxiv.org/abs/2109.00291>
944. D. Marakkalage, H. Riener and G. De Micheli "Optimizing Adiabatic Quantum-Flux-Parametron (AQFP) Circuits using Exact Methods," *International Workshop on Logic Synthesis (IWLS) 2021*
945. A. Tempia Calvino, H. Riener, S. Rai and G. De Micheli "From Logic to Gates: A Versatile Mapping Approach to Restructure Logic," *International Workshop on Logic Synthesis (IWLS) 2021*
946. D. Marakkalage and G. De Micheli Fanout-Bounded Logic Synthesis for Emerging Technologies - A Top-Down Approach *International Workshop on Logic Synthesis (IWLS) 2022*.
947. A. Tempia Calvino and G. De Micheli, Depth-optimal Buffer and Splitter Insertion and Optimization in AQFP Circuits *International Workshop on Logic Synthesis (IWLS) 2022*.
948. S.-Y. Lee, H. Riener and G. De Micheli An Automated Testing and Debugging Toolkit for Gate-Level Logic Synthesis Applications *International Workshop on Logic Synthesis (IWLS) 2022*.
949. H. Wang, S.-Y. Lee and G. De Micheli A Cost-generic Resubstitution Algorithm with Customizable Cost Functions *International Workshop on Logic Synthesis (IWLS) 2022*.
950. S. Y. Lee, H. Riener and G. De Micheli, External don't cares in logic synthesis, *International workshop on Boolean Problems*, Bremen, 2022.
951. S.-Y. Lee, H. Riener and G. De Micheli, "Customizable On-the-fly Design Space Exploration for Logic Optimization of Emerging Technologies," *International Logic Synthesis Workshop (IWLS)*", Lausanne 2023.
952. A. Costamagna, A. Mishchenko and G. De Micheli, "The Combinational-Complexity Game For Symmetric Functions", *International Logic Synthesis Workshop (IWLS)*, Lausanne 2023.
953. A. Tempia Calvino and G. De Micheli, "Technology Mapping Using Multi-output Library Cells," *International Logic Synthesis Workshop (IWLS)*", Lausanne 2023.
954. D. Marakkalage, M. Walter, S.-Y. Lee, R. Wille and G. De Micheli, "Technology Mapping for Beyond-CMOS Circuitry with Unconventional Cost Functions," *International Logic Synthesis Workshop (IWLS)*, Lausanne 2023.
955. A. Mishchenko, R. Brayton, A. Tempia-Calvino, and G. De Micheli, "Boolean Decomposition Revisited," *International Logic Synthesis Workshop (IWLS)*, Lausanne 2023.
956. A. Tempia Calvino, A. Mishchenko, G. De Micheli and R. Brayton, "Practical Boolean Decomposition for Delay-driven LUT Mapping, IWLS 2024, Zurich.
957. A. Costamagna, A. Tempia Calvino, A. Mishchenko and G. De Micheli, "Area-Oriented Resubstitution For Networks of Look-Up Tables, IWLS 2024, Zurich.
958. A. Costamagna, A. Tempia Calvino, A. Mishchenko and G. De Micheli, "Post-Mapping Resubstitution For Area-Oriented Optimization, IWLS 2024, Zurich.

959. G. H. Wang, C. Meng and G. De Micheli, “Global Crossover: An Evolution Strategy for Logic Synthesis, IWLS 2024, Zurich.
960. E. Testa, D. Marakkalage, W. Quayle, S. Kundu, A. Kumar, D. Ghosh, D. De Micheli and L. Amaru, “Enabling Scalable Sequential Synthesis and Formal Verification in an Industrial Flow, IWLS 2024, Zurich.

#### Other Publications (technical reports)

961. G. De Micheli, “A SATAN Controlled High Voltage Distributor,” *Report NA4/37*, CERN-European Center for Nuclear Research, Geneva (CH), November 1978.
962. G. De Micheli, “Computer Aided Synthesis of PLA-based Systems,” *Ph.D. Dissertation*, University of California, Berkeley, 1983, and UCB/ERL Memo. No. M84/31.
963. D. Ku and G. De Micheli, “Hardware C: A Language For Hardware Description,” *CSL Report*, CSL-TR-88-362, 1988.
964. D. Ku and G. De Micheli, “Hardware C: A Language For Hardware Description (Version 2.0),” *CSL Report*, CSL-TR-90-419, 1990.
965. R. Gupta and G. De Micheli, “Vulcan: a System for High-Level Partitioning of Synchronous Digital Circuits,” *CSL Report*, CSL-TR-91-471, 1991.
966. M. Ligthart and G. De Micheli, “Automatic Test Pattern generation for Logic Synthesis Systems,” *Philips Research Palo Alto Report*, PRPA 9101, 1991.
967. R. Schutten, D. Ku and G. De Micheli, “ODE: A Design Environment for High-Level Synthesis,” *Philips Research Palo Alto Report*, PRPA 9102, 1991.
968. J. Yang and G. De Micheli, “Spectral Techniques for Technology Mapping,” *CSL Report*, CSL-TR-91-498, 1991.
969. R. Gupta and G. De Micheli, “System Synthesis via Hardware-Software Co-design,” *CSL Report*, TR-92-548, Stanford, 1992.
970. G. De Micheli, R. Otten and T. Vierhaus *Workshop on High-Level Synthesis Algorithms, Tools and Design*, GMD Studien Nr. 276, December 1995.
971. A. Bogliolo, L. Benini, G. De Micheli and B. Riccò, “PPP: A Gate-Level Power Simulator - A World Wide Web Application,” *CSL Report*, TR-96-691, Stanford, 1996.
972. V. Bertacco, S. Minato, P. Verplaetse, L. Benini and G. De Micheli “Decision Diagrams and Pass Transistor Logic Synthesis,” *CSL Report*, TR-97-748, Stanford, 1997.
973. V. Mooney and G. De Micheli “Hardware/Software Co-design of Run-time Schedulers for Real-Time Systems,” *CSL Report*, TR-97-739, Stanford, 1997.
974. G. De Micheli “Internet: Services and Opportunities in the 21st Century,” *Memento technique No. 11*, Conseil Scientifique, France Telecom, pp. 23-30.
975. C. Boero, S. Carrara and G. De Micheli, “Design and Optimization of a Lactate Amperometric Biosensor based on Lactate Oxidase and Multi Walled-Carbon Nanotubes,” *Nanotech*, Montreux, November 2008.
976. L. Amarù, A. Balatsoukas Stimming, P.-E. Gaillardon, A. Burg and G. De Micheli. “Restructuring of Arithmetic Circuits with Biconditional Binary Decision Diagrams,” University Booth at DATE 2014 (*Design, Automation & Test in Europe*), Dresden, Germany, 2014.
977. M. Soeken, H. Rienner, W. Haaswijk, E. Testa, B. Schmitt, G. Meuli, F. Mozafari, G. De Micheli, “The EPFL Logic Synthesis Libraries”, ArXiv <https://arxiv.org/abs/1805.05121>.
978. F. Mozafari, G. De Micheli, and Y. Yang, “Efficient deterministic preparation of quantum states using decision diagrams”, arXiv:2206.08588
979. M. Yu and G. De Micheli, “Expediting Homomorphic Computation via Multiplicative Complexity-aware Multiplicative Depth Minimization” URL: <https://eprint.iacr.org/2024/1015>

#### Patents

980. P.E. Gaillardon, X. Tang, G. Kim, G. De Micheli and E. Giacomini, “Resistive Random Access Memory based Multiplexers and Field Programmable Gate Arrays,” U.S. Patent No. 10’348’306 B2, 2018.



981. P.E. Gaillardon, L. Amaru and G. De Micheli, "Majority Logic Synthesis," U.S. Patent No. 10,394,988 B2, 2018.
982. L.Amaru, P.E. Gaillardon and G. De Micheli, "Boolean Logic Optimization in Majority Inverter Graphs," U.S. Patent No. 10,380,309 B2, 2018.
983. X.Tang, P.E. Gaillardon and G. De Micheli, "Pattern-based FPGA logic block and clustering algorithm," U.S. Patent No. 9,971,862 B2, 2018.
984. G.Amaru', P.E. Gaillardon and G. De Micheli, "Method for speeding up Boolean satisfiability," U.S. Patent No. 9,685,959 B2, 2017.
985. D. Sacchetto, S. Bobba, P.E. Gaillardon, Y. Leblebici, G. De Micheli and T. Demirci, 'Resistive switching element and use thereof," U.S. Patent No. 9412940 B2, 2016.
986. P.E.Gaillardon, X/ Tang and G.De Micheli, "High-performance low-power near-Vt resistive memory-based FPGA," US patent 9276573 B2, 2016.
987. G.De Micheli,Y. Leblebici, M. De Marchi and D. Sacchetto, "Ambipolar silicon nanowire field effect transistor," US patent 9252252 B2, 2016.
988. L.Amaru', P.E.Gaillardon and G.De Micheli, "Controllable-polarity FET based arithmetic and differential logic," US patent 9130568 B2, 2015.
989. F. Angiolini, D. Atienza and G. De Micheli, 'Method to manage the load of peripheral elements within a multicore system," US patent 7995599, 2011.
990. S. Murali, L. Benini and G. De Micheli, "Method to design network-on-chip (NOC)-based communication systems," US patent 8042087, 2009.
991. K. Sato, L. Semeria and G. De Micheli, "Resolution of Dynamic Memory Allocation/Deallocation and Pointers," US patent 6467075, 2002.
992. G. De Micheli, "Electronic alarm system", Chamber of Commerce of Milano No.986637," 1975, Italy.