A Fault-Tolerant Ripple-Carry Adder with Controllable-Polarity Transistors

HASSAN GHASEMZADEH MOHAMMADI, Ecole Polytechnique Fédérale de Lausanne (EPFL)
PIERRE-EMMANUEL GAILLARDON, University of Utah
JIAN ZHANG and GIOVANNI DE MICHELI, Ecole Polytechnique Fédérale de Lausanne (EPFL)
ERNESTO SANCHEZ and MATTEO SONZA REORDA, Politecnico di Torino

This article first explores the effects of faults on circuits implemented with controllable-polarity transistors. We propose a new fault model that suits the characteristics of these devices, and we report the results of a SPICE-based analysis of the effects of faults on the behavior of some basic gates implemented with them. Hence, we show that the considered devices are able to intrinsically tolerate a rather high number of faults. We finally exploit this property to build a robust and scalable adder whose area, performance, and leakage power characteristics are improved by 15%, 18%, and 12%, respectively, when compared to an equivalent FinFET solution at 22nm technology node.

CCS Concepts: • **Hardware → Fault tolerance**; **Emerging technologies**

Additional Key Words and Phrases: Nano-electronics, controllable-polarity transistors, fault tolerant adder

ACM Reference Format:
Hassan Ghasemzadeh Mohammadi, Pierre-Emmanuel Gaillardon, Jian Zhang, Giovanni De Micheli, Ernesto Sanchez, and Matteo Sonza Reorda. 2016. A fault-tolerant ripple-carry adder with controllable-polarity transistors. J. Emerg. Technol. Comput. Syst. 13, 2, Article 16 (November 2016), 13 pages.
DOI: http://dx.doi.org/10.1145/2988234

1. INTRODUCTION

In the recent years, many novel Field-Effect Transistor (FET) technologies have been proposed and evaluated in order to overcome the ultimate limits of conventional silicon-based Integrated Circuits (ICs). While most of them improve the structure and materials of FETs to boost their intrinsic performances, an alternative approach increases the functionality of the individual device for a constant area [Bernstein et al. 2010].

One of the most promising devices with enhanced functionalities is the Controllable-Polarity (CP) transistor. Exploiting a dual-gate structure, CP transistors can be electrostatically configured to be either n- or p-type [Heinzig et al. 2011; De Marchi et al. 2012]. The functionality of such a device is logically biconditional on both gate values and enables a compact realization of eXclusive OR (XOR)/ MAJority (MAJ)-based logic functions, which are not implementable in complementary metal-oxide-semiconductor (CMOS) in a compact form [Ben-Jamaa et al. 2011; Gaillardon et al. 2013]. CP devices

This work was partially supported by the ERC senior grant NanoSys ERC-2009-AdG-246810.
Authors' addresses: H. Ghasemzadeh Mohammadi, J. Zhang, and G. De Micheli, Integrated Systems Laboratory (LSI), EPFL, Building INF 341, Station 14, Lausanne 1015, Switzerland; P.-E. Gaillardon, University of Utah, MEB 2126, Electrical and Computer Engineering Department, MEB building, 50 S. Central Campus Dr., Salt Lake City, UT, 84112, USA; E. Sanchez and M. Sonza Reorda, Politecnico di Torino, Dip. Automatica e Informatica, corso Duca degli Abruzzi 24, I-10129 Torino, Italy.

DOI: http://dx.doi.org/10.1145/2988234

can be fabricated in many different technologies, from pure silicon [Heinzig et al. 2011; De Marchi et al. 2012; Appenzeller et al. 2006] to carbon electronics [Lin et al. 2005; Harada et al. 2010]. In particular, a top-down fabrication process showing full compatibility with industrial fabrication techniques has been employed in De Marchi et al. [2012] to demonstrate the feasibility of the approach. Basic logic gates exploiting the enhanced expressiveness of the technology have been demonstrated in De Marchi et al. [2014], making the practical usage of this technology even closer. In addition to showing interests in the realization of compact logic elements, emerging technologies with enhanced functionalities can also introduce novel opportunities in terms of fault tolerance.

In this article, we first propose a new transistor-level fault model that takes into account the specific characteristics of a generic CP device, extending the popular stuck-open/stuck-short fault model traditionally used at that level. While the analysis reported in Ghasemzadeh Mohammadi et al. [2015b] mainly aims at proposing fault models for end-of-manufacturing device testing, in this article we rather focus on faults that affect the behavior of the device when it is deployed in the field. Then, we analyze the behavior of circuits based on CP devices when permanent faults matching the proposed fault model are present, and identify the conditions for their detection/masking. Results show that a high number of faults are masked, thus making this new technology particularly interesting from a reliability point of view.

Performing this analysis at the transistor level allowed us to express the behavior of each gate when any of the possible faults affecting each of its transistors arise. We use this information to forecast the behavior of more complex circuits composed out of the above gates, thereby achieving the same precision than a transistor-level analysis but with a much lower computational complexity.

Based on the results of the previous analysis, we also propose in this artilce a fault-tolerant ripple-carry adder architecture exploiting XOR/MAJ logic gates built entirely with CP transistors. In order to guarantee a high degree of resiliency with respect to single and double permanent faults in every single stage, we combine the intrinsic resiliency of the CP-based circuits with the usage of the Triple Modular Redundancy (TMR) architecture. Moreover, the intrinsic fault tolerance of the gates implemented with the CP transistors makes the resulting TMR architecture not prone to faults affecting the voters. In this way, we can devise an architecture that is able to mask the effect of any single fault, including those affecting the voters, without resorting to more expensive solutions to harden them (e.g., Ban et al. [2010]). Finally, the specific architecture of the proposed TMR solution, where the 3 replica of the 1-bit adder have swapped inputs, guarantees a very high resiliency with respect to double faults: only less than 0.5% of them do produce a failure. Although faster solutions can be adopted to implement adders, for example, based on the Kogge-Stone architecture [Kogge et al. 1973] and its fault tolerant version [Ghosh et al. 2008], the TMR version of the ripple-carry adder still represents the reference to compare with, especially when the parallelism is limited and power is not a major issue (in the latter case, solutions based on reversible logic are often adopted [Mitra and Chowdhury 2012]).

Experimental validation shows that the full-adder architecture we propose is able to tolerate all possible single permanent faults and more than 99.5% of the double ones. In addition, it proves that the proposed solution provides a 15%, 18%, and 12% gain in area, performance, and leakage power with respect to similar architectures implemented in FinFET technology at 22nm technology node. Finally, the proposed architecture is significantly cheaper with respect to solutions based on hardening the circuit at the transistor level, such as those proposed in Anghel and Nicolaidis [2007], whose area is about four times the one of the unhardened circuit.

This article is organized as follows. Section 2 gives some background related to CP transistors. Section 3 introduces a new fault model suited to CP devices and analyzes

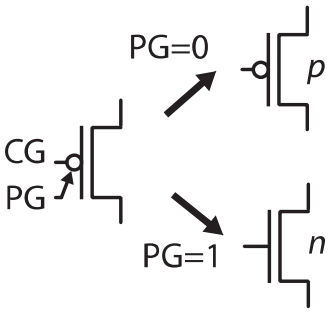

Fig. 1. CP transistor behavior.

the conditions for its detection/masking; a method allowing to easily analyze the fault tolerance of complex circuits out of the knowledge about the fault-free and faulty behavior of the composing gates is also presented. The method is first used to analyze the behavior of a 1-bit full adder when single permanent faults affect it. Section 4 proposes a fault tolerant architecture for a 1-bit adder that can be exploited to build cost-effective fault-tolerant ripple-carry adders and analyzes its fault-tolerant characteristics. Section 5 reports the results of a quantitative analysis of the characteristics of the proposed architecture. Finally, Section 6 draws some conclusions.

2. BACKGROUND

Transistors with CP are Double-Independent Gate (DIG) FETs having one gate controlling online the device polarity. Transistors with CP have been experimentally fabricated in several novel technologies, such as carbon nanotubes [Lin et al. 2005], graphene [Harada et al. 2010] and Silicon NanoWires (SiNWs) [Heinzig et al. 2011; De Marchi et al. 2012; Appenzeller et al. 2006].

In DIG devices, one gate electrode, denoted the Control Gate (CG), acts conventionally by turning on and off the device. The other electrode, denoted the Polarity Gate (PG) acts on the side regions of the device, dynamically switching the device polarity between n- (PG = 1) and p-type (PG = 0). The behavior of this device is illustrated in Figure 1.

Using CP devices, it is possible to build very compact arithmetic logic gates, such as XOR [Ben-Jamaa et al. 2011] and MAJ [Turkyilmaz et al. 2013]. For instance, a 2-input XOR gate requires only four transistors [Ben-Jamaa et al. 2011] instead of the eight required by the traditional full-swing static CMOS implementation [Rabaey et al. 2003]. This compactness can be leveraged in adder implementations, as reported in Figure 2, where we show a full adder composed of only eight CP transistors. This circuit exploits 3-input XOR and MAJ gates to implement the sum and the carry, respectively. Note that the proposed cells exploit a transmission-gate design. We will see in the following that this introduces a degree of redundancy at the gate level, which is beneficial from a robustness perspective. A self-checking ripple-carry adder architecture, exploiting this adder structure, is proposed in Turkyilmaz et al. [2013]. This architecture is far less expensive in terms of area than comparable CMOS architectures.

In this article, we make one step forward with respect to Turkyilmaz et al. [2013]. In addition, to exploit the reduced area cost offered by CP devices, we take into account their intrinsic capabilities in masking (i.e., tolerating) faults and use them to build a fault-tolerant adder.

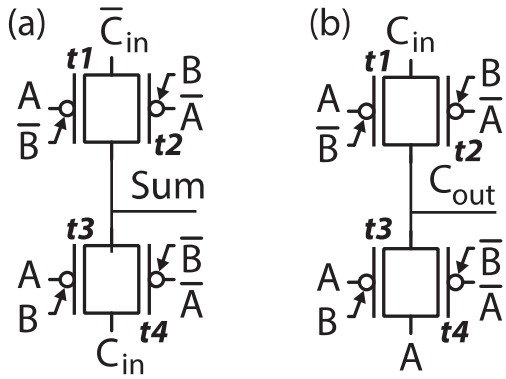

Fig. 2. Realization of a 1-bit full adder using CP transistors. (a) 3-input XOR – Sum = A⊕B⊕Cin, (b) 3-input MAJ – Cout = MAJ(A,B,Cin).

Table I. Manufacturing Steps of CP Transistors with Corresponding Possible Defects

	Manufacturing steps	Outcome	Source of defects	Possible defect
1	Nanowire patterning (using Bosch process)	Transistor channel	Line edge roughness, twin boundaries	Nanowire break
2	Oxidation	Dielectric formation	Deviation of oxide growing, voltage stress	Gate Oxide Short (GOS)
3	Deposition of polarity/control gates	Gates formation	Lithographic particles, line edge roughness	Bridge among terminals
4	Ni silicide annealing and metal layers depositions	Drain/Source Schottky contacts, interconnections	Slurry particles during metallization, void boundary interactions	Bridge among interconnects, floating gates

3. EVALUATING CP CIRCUIT ROBUSTNESS

3.1. Fault Model

The robustness evaluation of circuits based on CP devices cannot be performed by relying on usual fault models and tools, for example, working at the gate level [Bushnell and Agrawal 2000]. Indeed, when new technologies are introduced, it is common to envisage a lower-level approach, for example, resorting to transistor-level fault models [Hapke et al. 2014]. In such a case, the most common solution lies in inductive fault analysis of the device as well as layout-based defect map extraction for feasible fabrication shortcomings [Ghasemzadeh Mohammadi et al. 2015b].

The selection of an appropriate fault model to analysis fault tolerant architectures in a new technology such as CP transistors is a very important task because it is not clear a priori that the current CMOS fault models can capture all the manufacturing defects of this technology. We addressed this concern in our previous works [Ghasemzadeh Mohammadi et al. 2015a, 2015b] by investigating the fabrication defects that may happen during the fabrication of CP transistors and CP circuits. Table I summarizes the possible defects that may happen during the manufacturing CP transistors or during the formation of the logic cells. Among the listed defects, a group of defects (e.g., Gate Oxide Short) result in performance degradation. The other group, however, contains the defects (e.g., bridge faults between Polarity Gate (PG) and Drain/Source) that leads to functional failures. This later group of defects is captured in the proposed model.

In this work, we only consider the defects that completely change the functionality [Ghasemzadeh Mohammadi et al. 2015b], for example, change the polarity of a transistor from p-type to n-type. Defects affecting the performances but keeping the functionality untouched are out of the scope of this article. These defects can be modeled by generalizing bridge defects to the two gates composing our transistors [Ghasemzadeh Mohammadi et al. 2015b]. Therefore, we introduce a new fault model that generalizes the stuck-at model for the mentioned bridge defects. The new fault model is based on four possible defects affecting each transistor:

—Stuck-at-0 on CG (CG/0) and stuck-at-1 on CG (CG/1): These defects are similar to what happens in the current technology. Depending on the polarity of the transistor, such defects will lead to a Stuck-Open (SO) or Stuck-Short (SS) behavior of the device.
—Stuck-at-0 on PG (PG/0) and stuck-at-1 on PG (PG/1): These defects affect the polarity of the device. In their presence, the device will be either stuck-at-n or stuck-at-p, affecting the logic operation.

The new fault model extends the traditional transistor-level fault model, where the gate can be either stuck-at-0 or stuck-at-1 and takes into account the specific characteristics of CP transistors. Each of these defects corresponds to forcing to 0 or 1 the value of the corresponding CP transistor input signal. We denote this fault model as the CG/PG fault model.

3.2. CP Device Fabrication Technology

The CP devices (e.g., DG-SiNWFET [De Marchi et al. 2012] and TIG-SiNWFET [Zhang et al. 2014]) are fabricated in a top-down approach. Table I summarizes the fabrications process of the device along with the outcome of each step. The BOSCH etching process [De Marchi et al. 2012] is used to form the silicon nanowire pattern. The nanowire forms the channel of the transistor. In the next step, gate dielectric is formed through self-limiting oxidation, which leads to the gate oxide layer (5nm) around the channel. This step is followed by a conformal polysilicon deposition and patterning to realize the polarity gates around the nanowire. Finally, the control gate structure is self-aligned to polarity gates. As a result, a CP device is obtained (as shown in Figure 3) in which the control gate can be modulated independently from the polarity gate.

3.3. XOR/MAJ Gates Robustness

In order to evaluate the robustness of a circuit implemented with CP devices, we now evaluate the behavior of the basic logic primitives, when a CG/PG fault occurs in any of the transistors of the gate.

3.3.1. Methodology. The 3-input XOR and MAJ logic gates, shown in Figures 2(a) and 2(b), respectively, have been characterized using electrical simulations. Figure 4 summarizes the simulation setup that we used for fault analysis.

The logic gates are realized using SiNW-based CP transistors [De Marchi et al. 2012]. A simple table-based compact model of the device is used with HSPICE simulator. The model is extracted using TCAD simulations of a 22nm device, as shown in De Marchi et al. [2012]. In the simulation experiments, the Vdd value was fixed to 1.2V, which is in line with the technological results. The output of the gates is loaded with a fixed 1fF capacitance.

First, we identify the input voltage ranges associated to Boolean input 0 (VIL) and 1 (VIH), according to the definitions given in Rabaey et al. [2003]. Defining the input voltage boundaries will help us to identify a faulty gate behavior in presence of a transistor-level fault. We report the obtained points for the logic gates:

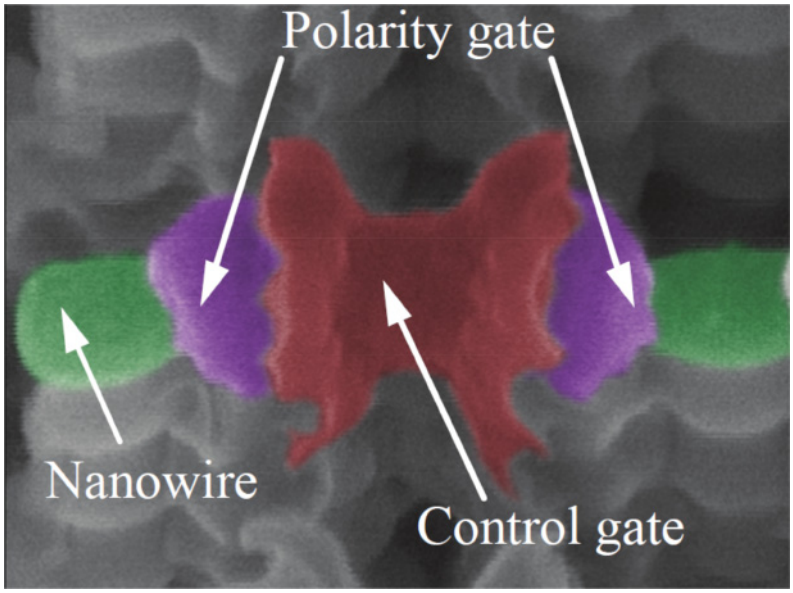

Fig. 3. Figure of a fabricated CP transistor [De Marchi et al. 2012]. The red, purple, and green colors highlight the control gate, polarity gate, and the nanowire, respectively.

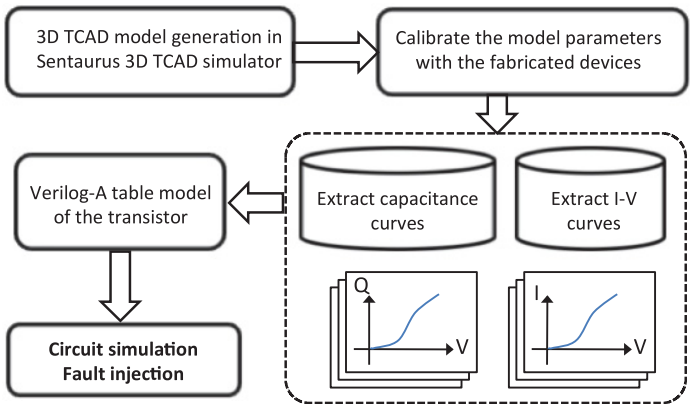

Fig. 4. Fault analysis methodology.

—VIH = 0.600V
—VIL = 0.540V.

Therefore, the two logic gates will correctly behave when the output voltages for Boolean output 0 (VOL) and 1 (VOH) are in the following ranges:

—0.600V < VOH < 1.2V
—0V < VOL < 0.540V.

The identified ranges are used to classify the output values of the different gates. Then, the behavior of the logic gates under all possible CG/PG faults is computed by using DC operating points analyses for all possible input conditions.

Table II. Output Voltage Values of the 3-Input XOR Gate

		t1				*t2*				*t3*				*t4*			
Input	**Fault-free**	CG/0	CG/1	PG/0	PG/1	CG/0	CG/1	PG/0	PG/1	CG/0	CG/1	PG/0	PG/1	CG/0	CG/1	PG/0	PG/1
000	0	0.32	0	0	0.27	0	0.27	0.32	0	0	0	0	0	0.14	0	0.13	0
001	1.2	0.83	1.2	1.2	**0.36**	1.2	**0.36**	0.83	1.2	1.2	1.1	1.2	1.1	1.2	1.2	1.2	1.2
010	1.2	1.2	1.1	1.2	1.1	1.2	1.2	1.2	1.2	0.83	1.2	1.2	**0.36**	1.2	**0.36**	0.83	1.2
011	0	0	0	0	0	0.14	0	0.13	0	0.32	0	0	0.27	0	0.27	0.32	0
100	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.2	1.1	1.2	**0.36**	0.83	1.2	0.83	1.2	1.2	**0.36**
101	0	0.14	0	0.13	0	0	0	0	0	0	0.27	0.32	0	0.32	0	0	0.27
110	0	0	0.27	0.32	0	0.32	0	0	0.27	0.14	0	0.13	0	0	0	0	0
111	1.2	1.2	**0.36**	0.83	1.2	0.83	1.2	1.2	**0.36**	1.2	1.2	1.2	1.2	1.2	1.1	1.2	1.1

Table III. Output Voltage Values of the 3-Input MAJ Gate

		t1				*t2*				*t3*				*t4*			
Input	**Fault-free**	CG/0	CG/1	PG/0	PG/1	CG/0	CG/1	PG/0	PG/1	CG/0	CG/1	PG/0	PG/1	CG/0	CG/1	PG/0	PG/1
000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
001	0	0.32	0	0	0.27	0	0.27	0.32	0	0	0	0	0	0.14	0	0.13	0
010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
011	1.2	1.2	1.1	1.2	1.1	1.2	1.2	1.2	1.2	0.83	1.2	1.2	**0.36**	1.2	**0.36**	0.83	1.2
100	0	0.14	0	0.13	0	0	0	0	0	0	0.27	0.32	0	0.32	0	0	0.27
101	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
110	1.2	1.2	**0.36**	0.83	1.2	0.83	1.2	1.2	**0.36**	1.2	1.2	1.2	1.2	1.2	1.1	1.2	1.1
111	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2

3.3.2. XOR/MAJ Gates Behavior under CG/PG Faults. Tables II and III report the simulated DC operating points of the 3-input XOR and MAJ gates, respectively, when the gates are fault-free and when each of the CG/PG faults are injected in the different transistors (t1 to t4). All possible input combinations are considered. The CG/PG fault injection induces different behaviors classified under three categories:

—*correct behavior* (highlighted in green) when a CG/PG fault is not excited by the applied input vector;
—*masked-fault behavior* (highlighted in light blue) when a CG/PG fault is excited and induces a reduction of the noise margin at the output of the gate but does not induce a faulty gate behavior, as the output voltage is still in the correct VOH and VOL range;
—*faulty behavior* (highlighted in red) when a CG/PG fault induces an incorrect value at the output of the gate.

Considering the 3-input XOR (Table II), the results indicate that 8 CG/PG faults out of 16 lead to a faulty gate behavior that is observable at the gate output for at least one input combination. The remaining 8 CG/PG faults are always masked. Moreover, the 8 detectable faults produce a faulty output when 4 out of 8 possible input values are applied (001, 010, 100, and 111). With the other 4-input combinations (000, 011, 101, and 110), the circuit always produces the correct output no matter the presence of a fault.

CP transistors have four different modes of operations: on n-type, off n-type, on p-type and off p-type. A CG/PG fault restricts the number of operations of the device but does not fully lock it in a unique mode. This property is unique to the class of CP

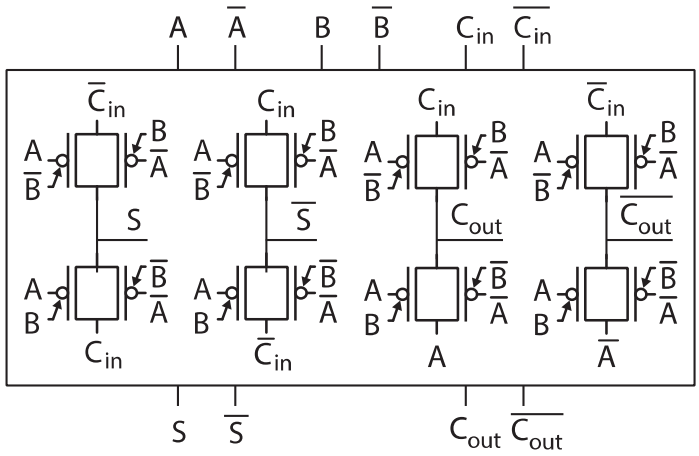

Fig. 5. 1-bit adder with generation of inverted sum and carry.

transistors and unachievable with standard transistors. This has a positive impact on the fault tolerance of the overall gate circuit. As an example, we can consider the PG/0 fault on t4 in the 3-input XOR under input values 000. Under fault-free conditions, the bottom transmission-gate is on, with t3 configured as p-type and t4 as n-type. Transistor t4 propagates properly the logic 0. However, when a PG/0 fault affects t4, t4 polarity switches to p-type. In this condition, the logic 0 cannot be fully propagated but is still transmitted with limited voltage degradation. Such degradation reduces the noise margin of the gate but does not induce a faulty behavior.

Similarly, for the 3-input MAJ (Table III), the results indicate that the number of faulty behaviors is very small: 12 faults out of 16 are always masked. Moreover, the remaining four faults do produce a difference in the output voltage only when two of the eight possible input combinations are applied (011 and 110). For the six remaining input combinations, the CG/PG faults never produce any output misbehavior.

3.4. Circuit-Level Analysis

Based on the results of the detailed transistor-level analysis presented so far, we can now describe the behavior of each possible logic gate for each possible input combination and for the four possible faults affecting each of the internal transistors. Therefore, we can build a detailed model of the fault-free and faulty behavior of each gate. Using these models, we can determine the fault-free and faulty behavior of any larger circuit composed of different gates working at the logic level, only. This allows us to ignore the details of the underlying transistor-level structure, without losing in accuracy. The approach we use in the remaining parts of this article is based on developing functional models for each gate (with suitable control signals to inject each possible fault), and combining them to extensively analyze the behavior of larger circuits.

As an example, let consider the 1-bit adder circuit represented in Figure 5 and consisting of two 3-input XOR gates for the sum generation and two 3-input MAJ gates for the carry generation. As compared to the simpler adder of Figure 2, this circuit generates both the sum and carry signals and their inverted versions in a unique logic level. This allows us to create ripple-carry adder structures and to implement the voting structures described in the next section without adding any inverters to drive the next stages. Note that, due to the transmission gates, buffers will be required every four stages in the resulting ripple-carry adder architecture.

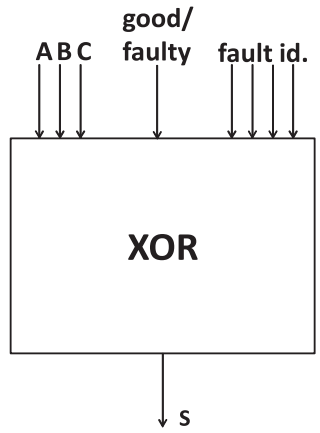

Fig. 6. Functional model supporting the simulation of the fault-free and faulty version of the 3-input XOR gate.

Table IV. Unmasked CG/PG 1-Bit Full Adder Faults

Circuit Inputs	XOR-S	XOR-nS	MAJ-C	MAJ-nC
000	0/16	2/16	0/16	0/16
001	2/16	0/16	0/16	2/16
010	2/16	0/16	0/16	0/16
011	0/16	2/16	2/16	0/16
100	2/16	0/16	0/16	2/16
101	0/16	2/16	0/16	0/16
110	0/16	2/16	2/16	0/16
111	2/16	0/16	0/16	0/16
TOTAL	**8**	**8**	**4**	**4**

In order to evaluate the behavior of the 1-bit adder in the presence of faults affecting its transistors, we first developed the good and faulty models for the 3-input XOR and 3-input MAJ gates, based on the results in Tables II and III. Figure 6 shows a symbolic representation of the model for the XOR gate, where we highlight the presence of control inputs to specify whether we want it to work in fault-free (or good) mode, or in faulty mode. In the latter case, the four inputs labeled as "*fault id*" allow us to select one out of the 16 possible faults affecting the 4 transistors in the gate. A similar model has been developed for the 3-input MAJ gate. By combining these models (that we implemented as a library of procedures in the C language), we could easily analyze the fault-free and faulty behavior of the 1-bit adder.

Table IV summarizes the fault simulation results for all the CG/PG single faults in the four gates of a 1-bit full adder. In particular, the table reports the number of faults producing a failure on the output of the adder for each possible input combination. It is possible to notice that considering all the possible circuit inputs, 40 out of 64 possible CG/PG faults are always masked, that is, never produce a difference on the outputs with respect to the fault-free circuit.

4. FAULT-TOLERANT RIPPLE-CARRY ADDER ARCHITECTURE

Knowing the behavior of the 3-input XOR and MAJ gates exploiting CP transistors, and using the approach we just described, we now investigate the possibility to implement a fault-tolerant ripple-carry adder architecture based on these primitives and on the

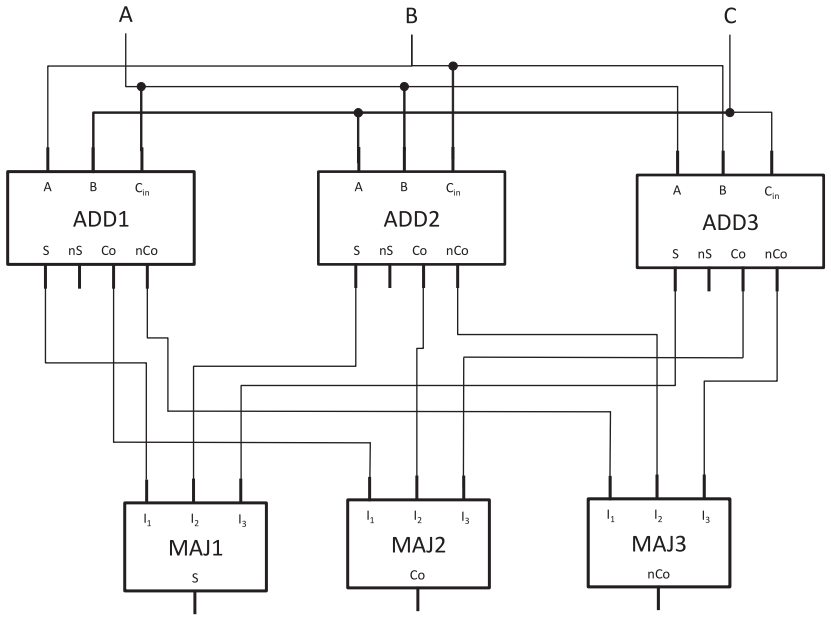

Fig. 7. Fault-tolerant 1-bit adder architecture.

results of the analysis on the behavior of the 1-bit adder of Figure 5, reported in Section 3.3.

In order to make the adder fault-tolerant with respect to possible faults and under the different input conditions, we first devised a fault-tolerant architecture for a 1-bit adder, shown in Figure 7, based on the Triple Module Redundancy (TMR) scheme.

In this architecture, each 1-bit adder is triplicated and voted. As a result, any single fault affecting a single adder can be tolerated and does not produce any failure on the data output bit or on the carry bits propagated to the following stages of the adder.

Thanks to the adoption of CP transistors, possible single faults affecting the voters do not produce any failure on the inputs. In fact, the majority voter has been shown (Table III) to never fail with the 000 and 111 input combinations; hence, the voter never fails when the three 1-bit adders are fault-free. This guarantees that the fault tolerant 1-bit adder never produces a faulty output in the presence of a single fault affecting either an adder or a voter.

Finally, in the proposed architecture, the inputs to each 1-bit adder replica, labeled from ADD1 to ADD3, are permuted. In this way, even if the same fault affects more than a single replica, this does not evolve into a common mode fault, and the circuit always behaves correctly. More in general, we performed an extensive experimental analysis aiming at understanding the number of double faults tolerated by the architecture, when different connections are adopted for the three adder replica. By hierarchically combining the functional models for the different modules and performing the exhaustive simulation of all possible input combinations, we could analyze the fault-tolerant 1-bit adder behavior when any double fault arises. Results reported in Table V show how many faults produce a failure on each output of the fault-tolerant 1-bit adder using three different configurations, which differ for the different way in which the three input signals A, B, and C are connected to the three replica. In particular, Table V shows that in the case of no input permutation (ABC (no permutation) row) the circuit masks a slightly lower number of double faults with respect to the situation, in which

Table V. Double Faults Producing Failures on the Outputs of the Fault-Tolerant 1-Bit Adder When Different Connections of the Inputs Are Adopted

	# of double faults producing a failure on			
Input connection	S	C	nC	Total
ABC (no permutation)	80	40	40	160
ABC CAB BAC	80	32	32	144
BCA ACB CBA	80	28	28	136

Table VI. Single and Double Fault Effects Analysis

	Faults	*Failures*	%
Single	256	0	0
Double	32,640	136	0,41

Table VII. Fault-Tolerant 1-Bit Adder Performances

20nm node	# Transistors	Area (μm^2)	Delay (ps)	Leakage Power (nW)
FinFET LSTP	108	5.89	371	23.84
NWFET	60	4.98	304	21.06
Gain	44%	15.5%	18.1%	11.6%

inputs are permutated, and that the connection BCA ACB CBA is the one masking the highest number of faults.

Table VI summarizes the key properties of the fault tolerant 1-bit adder, that is:

—single faults never produce any failure on the outputs of the fault tolerant 1-bit adder
—less than 0.5% of double faults produce failures.

Using the fault-tolerant 1-bit adder, one can easily build a fault-tolerant ripple-carry adder. In that case, the effects of any double fault that creates a failure on the C or nC output of its stage may possibly propagate to the following stage.

Finally, it is worth noting that the proposed architecture is also able to mask any transient fault affecting a single gate in any of the 1-bit adders.

5. QUANTITATIVE COMPARISON WITH CMOS

In order to provide the reader with some more details about the performance and characteristics of the proposed architecture, we first performed some experimental analysis, aimed at checking its behavior in the presence of single and double faults.

Results of this analysis (performed by combining at the gate level the results reported in the previous sections) confirmed that all single faults are masked, either by the characteristics of the CP gate implementation, or by the TMR architecture.

From the circuit-level performance perspective, we compared the proposed circuit implemented using SiNWFETs with its equivalent CMOS FinFET 20nm LSTP counterpart using electrical simulations. The load capacitance for the two circuits is set to 1fF. We consider the area, the worst-case delay and the leakage power. Note that dynamic power is not considered due to a lack of precision in the considered com-pact model. The circuit-level results are summarized in Table VII.

The proposed implementation requires 16 CP transistors for each 1-bit adder, plus 12 transistors for the 3 majority voters. Hence, 60 transistors are required for the proposed fault-tolerant 1-bit adder. By applying the same design principles with transmission-gate CMOS, we obtained 24 transistors for a 1-bit full adder. Note that we assume that the inputs are provided in a redundant form with $\bar{A}$, $\bar{B}$, and $\bar{C}_{in}$ available jointly with A, B and C_{in} for both the novel adder scheme and its standard CMOS counterpart. In the same way, it is possible to note that the reference structure also generates all the

inverted signals required to cascade the different adder stages. Smallest implementations can be identified for both CMOS and CP transistors if dedicated inverters are used to generate the inverted signals. Then, a TMR-based implementation in CMOS technology would require 3×24 transistors, plus the cost for the majority voter on the data output, accounting for 3×12 transistors. In total, 108 transistors would thus be required. Hence, the proposed solution requires 44% less transistors. When considering the area of the two adders, the proposed solution requires $4.98\mu m^2$ as compared to $5.89\mu m^2$ for its equivalent FinFET implementation. This leads to a gain of 15% in area. The gain is reduced compared to the simple transistor count, as CP transistors are bigger than FinFETs, due to the additional polarity terminals. The proposed solution is also significantly less expensive than the one proposed in Ban et al. [2010], which proposes a fault-tolerant architecture for the voter consisting of an XOR and a multiplexer.

Finally, the proposed solution can be easily used to build up an adder with whichever data parallelism n, whose total cost scales linearly with n. Since we demonstrated that single faults affecting one stage do not propagate to the following ones, the level of fault tolerance of the final adder is not affected by its parallelism.

From a performance perspective, the proposed implementation is shown to be faster with an 18% reduction of the worst-case delay. This is accounted to the reduced number of stacked transistors coming from the use of CP transistors. Finally, the leakage power is reduced by 12%, thanks to the good electrostatic control offered by the NWFETs.

6. CONCLUSIONS

CP transistors offer many advantages to implement arithmetic logic gates at a reduced implementation cost. Besides the implementation compactness, an important parameter to consider is the robustness with respect to possible faults. In this article, we performed such an analysis and showed that circuits based on CP transistors can tolerate a large number of faults. Thanks to this property, they can be used to build effective structures demonstrating large fault tolerance, in addition to area, power, and speed improvements. In particular, we showed that the SiNWFET implementation of a fault-tolerant 1-bit adder (that can be easily used to build an adder of any size) is 15% smaller, 18% faster, and 12% less power consuming than the corresponding CMOS solution. This module can be used to build a ripple-carry adder of any length able to tolerate any single permanent fault and more than 99% of the possible double faults in any of its stages.

REFERENCES

L. Anghel and M. Nicolaidis. 2007. Defects Tolerant Logic Gates for Unreliable Future Nanotechnologies. In *Proceedings of the 9th International Work Conference on Artificial Neural Networks (IWANN'07)*. 422–429.

J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha. 2006. Dual-gate silicon nanowire transistors with nickel silicide contacts. In *Proceedings of the International Electron Devices Meeting (IEDM'06)*. DOI:10.1109/IEDM.2006.346842

T. Ban and L. A. de Barros Naviner. 2010. A simple fault-tolerant digital voter circuit in TMR nanoarchitectures. In *Proceedings of the 8th IEEE International NEWCAS Conference (NEWCAS'10)*. 269–272. DOI:10.1109/NEWCAS.2010.5603933

M. H. Ben-Jamaa, K. Mohanram, and G. De Micheli. 2011. An efficient gate library for ambipolar CNTFET logic. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 30, 2 (2011). 242–245. DOI:10.1109/TCAD.2010.2085250

K. Bernstein, R. K. Cavin, W. Porod, A. Seabaugh, and J. Welser. 2010. Device and architecture outlook for beyond CMOS switches. *Proceedings of the IEEE* 98, 12 (Dec. 2010), 2169–2184. DOI:10.1109/JPROC.2010.2066530

M. L. Bushnell and V. D. Agrawal. 2000. *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Springer Science+Business Media New York.

M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli. 2012. Polarity control in double-gate gate-all-around vertically stacked silicon nanowire FETs. In *Proceedings of IEDM*. (Dec. 2012). DOI:10.1109/IEDM.2012.6479004

M. De Marchi, J. Zhang, S. Frache, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli. 2014. Configurable logic gates using polarity controlled silicon nanowire gate-all-around FETs. *IEEE Electron Device Letters* 35, 8 (Aug. 2014). 880–882. DOI:10.1109/LED.2014.2329919

P.-E. Gaillardon, L.G. Amaru, S. Bobba, M. De Marchi, D. Sacchetto, Y. Leblebici, and G. De Micheli. 2013. Vertically-stacked double-gate nanowire FETs with controllable polarity: from devices to regular ASICs. In *Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE'13)*. DOI:10.7873/DATE.2013.137

H. Ghasemzadeh Mohammadi, P.-E. Gaillardon, and G. De Micheli. 2015. Fault modeling in controllable polarity silicon nanowire circuits. In *Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE'15)*. 453–458.

H. Ghasemzadeh Mohammadi, P.-E. Gaillardon, and G. De Micheli. 2015. From defect analysis to gate-level fault modeling of controllable-polarity silicon nanowires. *IEEE Transactions on Nanotechnology*. 2015. DOI:10.1109/TNANO.2015.2482359

S. Ghosh, P. Ndai, and K. Roy. 2008. A novel low overhead fault tolerant Kogge-Stone adder using adaptive clocking. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE'08)*. 366–371. DOI:10.1145/1403375.1403462

F. Hapke, W. Redemund, A. Glowatz, J. Schloeffel, A. Fast, J. Rajski, M. Keim, M. Reese, and M. Hustava. 2014. Cell-aware test. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 33, 9 (Sep. 2014). 1396–1409. DOI:10.1109/TCAD.2014.2323216.

N. Harada, K. Yagi, S. Sato, and N. Yokoyama. 2010. A polarity-controllable graphene inverter. *Applied Physics Letters* 96 (2010). 12102. DOI:10.1063/1.3280042

A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber. 2011. Reconfigurable silicon nanowire transistors. *Nano Letters* 12 (2011), 119–124. DOI:10.1021/nl203094h

P. M. Kogge and H. S. Stone. 1973. A parallel algorithm for the efficient solution of a general class of recurrence equations. *IEEE Transactions on Computers* C-22, 8 (Aug. 1973), 786–793. DOI:10.1109/TC.1973.5009159

Y.-M. Lin, J. Appenzeller, J. Knoch, and P. Avouris. 2005. High-performance carbon nanotube field-effect transistor with tunable polarities. *IEEE Transactions on Nanotechnology* 4, 5 (Sep. 2005), 481–489. DOI:10.1109/TNANO.2005.851427

S. K. Mitra and A. R. Chowdhury. 2012. Minimum cost fault tolerant adder circuits in reversible logic synthesis. In *Proceedings of the 25th International Conference on VLSI Design (VLSID2012)*. 334–339. DOI:10.1109/VLSID.2012.93

J. Rabaey, A. Chandrakasan, and B. Nikolic. 2003. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall.

O. Turkyilmaz, F. Clermidy, L. G. Amaru, P.-E. Gaillardon, and G. De Micheli. 2013. Self-checking ripple-carry adder with Ambipolar Silicon NanoWire FET. In *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'13)*. 2127–2130. DOI:10.1109/ISCAS.2013.6572294

J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli. 2014. Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs. *IEEE Transactions on Circuits and Systems* 61, 2851–2861. DOI:10.1109/TCSI.2014.2333675

Received October 2015; revised June 2016; accepted August 2016