J Electroceram (2017) 39:137–142
DOI 10.1007/s10832-017-0077-y

Effect of O^{2-} migration in $Pt/HfO_2/Ti/Pt$ structure

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Received: 9 August 2016 / Accepted: 22 February 2017 / Published online: 1 April 2017

Abstract In this paper, we study the post-fabrication phenomenon of natural oxidation of the Ti layer observed in a $Pt/HfO_2/Ti/Pt$ *Resistive Random Access Memory* (OxRRAM) stack with no external influence. We identify that the resistance ratio decreases by 100× in a month time period due to the natural oxidation of the Ti layer in contact of the HfO_2 layer. We then propose two paths to control both the final properties of the device and the aging process. The first approach consists in carefully optimizing the thickness of the Ti layer to reduce the aging effect. However, the resistance ratio is proportional to the thickness of the layer, leading to an unwanted trade-off between device properties and aging effect. The second approach consists in adding a TiO_2 inter-layer, creating a $Pt/HfO_2/TiO_2/Ti/Pt$ OxRRAM stack that is more stable over time with similar resistive states. The obtained OxRRAM stack presents a resistance ratio in the order of 10^4 with no observable post-fabrication aging degradation.

Keywords Oxide-based memories · RRAMs · XPS · Aging

This work has been supported by the Swiss National Science Foundation under the project No. 200021-146600 and the University of Utah SEED grant 51900298.

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1 Introduction

When it comes to computing, memory is an essential component. Providing a processor with fast access to its data and instructions, the *Random Access Memory* (RAM) is a kind of memory that allows an equal access time to any data. Nowadays, RAM circuits used in computers, such as *Static RAM* (SRAM) and *Dynamic RAM* (DRAM), are mainly made of *Complementary Metal-Oxide-Semiconductor* (CMOS) transistors. They store the information in a volatile way, which means that the information is not maintained without power on. Recently, due to new materials developments, new classes of RAM memories appeared with promising properties, such as non-volatility at high speed [1]. Among all the emerging non-volatile memory technologies, *Oxide Resistive Random Access Memories* (OxRRAMs) have raised major expectations because of their non-volatility, high endurance [2], fast switching [3] and their simple easily-scalable structure [4], using mainly CMOS compatible materials. Therefore, it finds many applications such as data storage [5], reconfigurable logic [6] or neuromorphic applications [7].

The typical core structure of a OxRRAM is a *Metal-Insulator-Metal* (MIM) stack using *Transition Metal Oxides* (TMO) as insulator layer. When a voltage is applied, the OxRRAM cell switches between two states that can be interpreted as the two states of the binary code, a *Low Resistance State* (LRS) as a '1' or ON state and a *High Resistance State* (HRS) as a '0' or OFF state. The switch from HRS to LRS is called *'set'* and the change from LRS to HRS is called *'reset'*. Despite the mechanism behind the switching is still under debate, it is widely admitted that a *Conductive Filament* (CF) forms between the two metal electrodes during the set process thanks to oxygen vacancies (V_O) migration and redox processes under the application of an

electric field, and dissolves within the electrolyte during the reset process [8–10]. Among the many different possible material stacks, HfO_2-based OxRRAM shows promising properties of a high switching speed equivalent to SRAM [11, 12], high resistivity reducing the current consumption and high endurance. In OxRRAMs, the migration of O^{2-} ions induced by the application of an electric field on the device is at the origin of the switching effect. However, diffusion of O^{2-} ions in thin films of different nature does not only happen under the presence of external active excitation, but also under regular passive conditions that can create pronounced aging effects.

In this paper, we get a better understanding of the oxygen ions migration while no electric field is applied. We demonstrate and explain, using *X-ray Photoelectron Spectroscopy* (XPS), a phenomenon of post-fabrication aging due to a passive oxidation of the top electrode Ti metal. By inserting a TiO_2 barrier layer between the HfO_2 switching layer and the Ti top electrode, we have been able to not only improve the electrical properties, but also to stabilize the memory. The final memory presents a resistance ratio in the order of 10^4 with no observable post-fabrication aging phenomena.

The remainder of this paper is as follows. Section 2 introduces the device fabrication process flow and the electrical characterization setup. Then, Section 3 describes the switching mechanism of the fabricated device and studies the effect of passive oxidation of the top electrode layer. It further introduces different methods to tune the oxidation rate or fully eliminate the passive oxidation phenomenon.

2 Process development

2.1 Device fabrication methodology

The resistive memory structures under investigation are a stack of Pt/HfO_2/Ti/Pt with varying Ti thickness (10nm, 30nm and 100nm) and Pt/HfO_2/TiO_2/Ti/Pt. Each memory consists of two crossing lines of Pt of 10μm width creating a 100μm^2 OxRRAM with access pads of 200 × 200μm^2. On a 4" Si wafer, the bottom 100nm-thick lines and pads of Pt are deposited by sputtering from a Pt target with 1000W DC power. The bottom electrode is patterned by optical lithography using positive resist and dry etched by chlorine plasma. Then, a HfO_2 layer is deposited by *Atomic Layer Deposition* (ALD) at 200°C using TEMAH precursor and H_2O reactant, followed immediately by a TiO_2 ALD deposited layer at 200°C using $TiCl_4$ precursor and H_2O reactant in the case of the Pt/HfO_2/TiO_2/Ti/Pt stack. Then, a Ti layer is deposited by sputtering from a Ti target with 1000W DC power. The Ti layer thickness is verified using a profilometer. Measured thicknesses are 13nm ± 4nm, 31nm ± 4nm and 100nm ± 4nm for the theoretical 10nm, 30nm and 100nm samples. Subsequently, the top Pt electrodes are deposited with a similar recipe than for the bottom electrodes. Finally, both patterned top Pt and oxides layers are etched by dry etching using chlorine plasma. Figure 1 shows a *Transmission Electron Microscopy* (TEM) cross section picture of a Pt/HfO_2(10nm)/Ti(20nm)/Pt stack using the same deposition recipes than the devices used in this paper.

2.2 Electrical measurement setup

The devices are electrically connected with a Karl Suss PM8 manual probe station and tested with an Agilent B1500A device analyzer. The bottom electrode potential is fixed to ground and the voltage of the top electrode is swept with a 500mV.s^{-1} slew rate. As forming step, a dual-ramp voltage sweep from 0V to +5V is performed while applying a current compliance of 100μA . Then, cycles of reset-set operations are performed. The reset operation is a 0V to -2V single voltage sweep with no current limitation and the set operation is a 0V to +3V single voltage sweep with 100μA limitation. The HRS and LRS resistance values are extracted from the IV plots of a complete switching cycle at V_{read}=500mV and V_{read}=-500mV respectively. In the remaining of the paper, the memories are first stabilized by running 15 complete switching cycles prior to electrical measurements. The reported HRS and LRS are then averaged over 5 cycles to account for the intrinsic cycle-to-cycle variability of the OxRRAM devices.

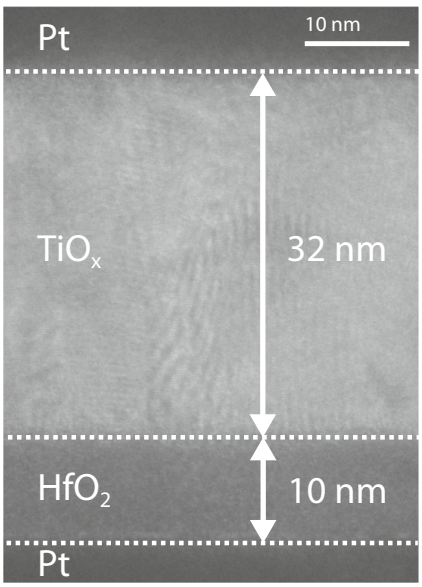

Fig. 1 TEM cross section picture of the Pt/HfO_2 (10nm)/Ti (30nm)/Pt stack. An additional Pt layer was used as capping layer for etching purpose of the cross section

3 Results and discussion

3.1 Switching mechanism and post-fabrication aging effect

We first observe, in Fig. 2, the I-V properties of a Pt/HfO_2 (10nm)/Ti (30nm)/Pt stack and illustrate the associated physical states explaining the formation of the *Conductive Filament* (CF). In this memory stack, the bottom Pt electrode serves as inert electrode while the Ti layer is used to create a sub-stoichiometric region in the HfO_2/Ti interface [13], introducing *Oxygen Vacancies* (V_O) and reducing the forming voltage. First, a forming procedure ① is performed by a 0V to 5V dual-ramp voltage sweep, with a slew rate of 500mV.s^{-1}. Starting from the pristine state (o) at 0V, the voltage increase generates and redistributes V_O and O^{2-} ions couples. More details about the formation and redistribution of Vo and O2- ions can be found in [14, 15].The O^{2-} ions are attracted to the positively charged Ti electrode, leaving oxygen vacancies in the structure and forming a Hf-rich conductive plug that leads to a non-linear decrease of the oxide resistivity (a). When reaching 4.5V, called $V_{Forming}$, the current sees a sudden increase due to the filament reaching the Pt electrode and changing the main conduction from tunnelling to ohmic point conduction (b). Note that the current is limited to 100μA by a current compliance to prevent any permanent damage of the cell. At this point, the memory is in a *Low Resistance State* (LRS) of 1.7kΩ on average. A reset procedure is then triggered ② by single sweeping the voltage from 0V to -1.5V. The negative sweep induces an opposite drift of the O^{2-} ions, that will recombine with the V_O (c) and break the filament when V_{Reset} reaches -1V (d). A second jump is happening at -1.4V and was demonstrated [16] to be due to multi filament formation in the oxide layer. There, a second filament bigger than the first one that broke at -1V is then broken. The memory is then in a *High Resistance State* (HRS) of 36MΩ on average. Note that reaching V_{Reset} imposes a large current due to the low LRS resistance value. Finally, a set procedure ③ is done by single sweeping the voltage from 0V to 2V and limiting the current to 100μA. The induced mechanism is similar to the forming step, except that it starts from an existing plug rather than from the pristine state, leading to a lower voltage needed for the switching to the LRS(e-f). At this point, the memory is in its working state where cycles, i.e. switching between HRS and LRS, can be done.

As discussed above, the migration of O^{2-} ions induced by the application of an electric field on the device is at the origin of the switching effect. However, diffusion of O^{2-} ions in thin films of different nature does not only happen under the presence of external active excitation, but also under regular passive conditions. Natural diffusion of O^{2-} is responsible of an exacerbated aging phenomenon, as studied in Fig. 3. Aging is defined as the natural drift of device parameters over time. In our case, we observe the evolution of HRS and LRS of the Pt/HfO_2 (10nm)/Ti (30nm)/Pt stack over two months after fabrication (Fig. 3(a)). Each

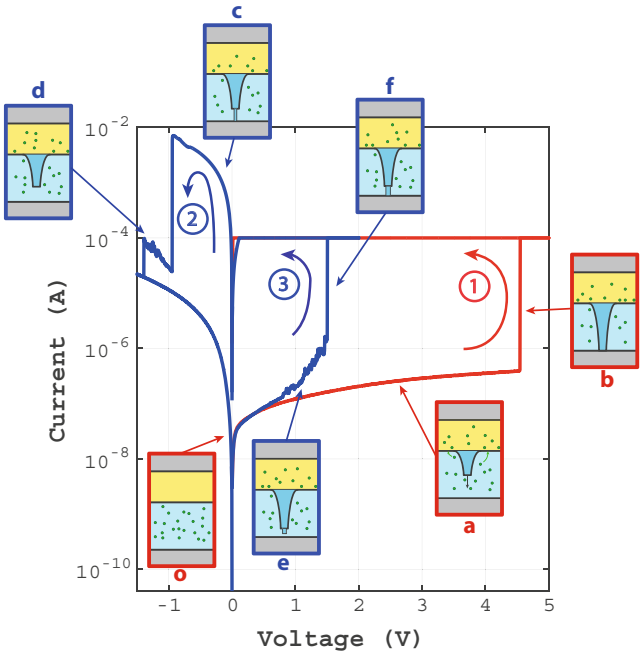

Fig. 2 Measured I-V characteristics of a Pt/HfO_2 (10nm)/Ti (30nm)/Pt cell and illustration of the associated switching mechanism. Red: forming step done with a single sweep from 0V to 5V. Blue: reset and set steps done with a single sweep respectively from 0V to -1.5V and from 0V to 2V

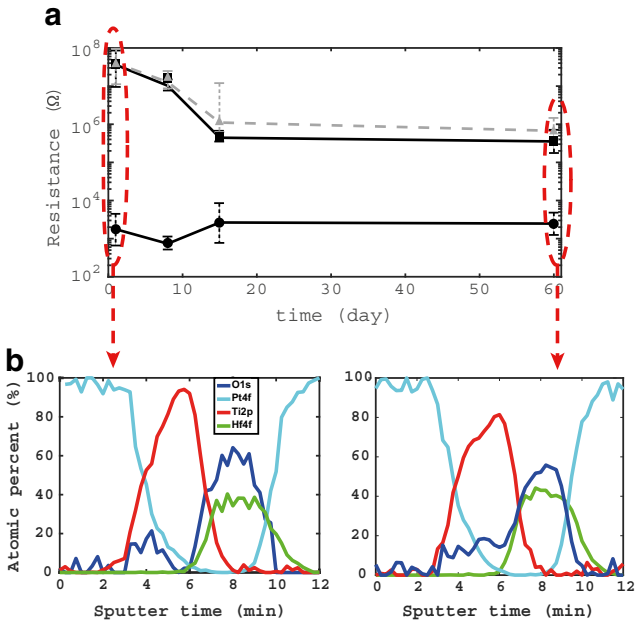

Fig. 3 Evolution over 2 months of the pristine state, HRS and LRS of the memory cell Pt/HfO_2(10nm)/Ti(30nm)/Pt with associated XPS depth profile analysis at day 1 and day 60. The resistance is measured as V/I where I is taken at 500mV. The triangles represents the pristine state, the squares the HRS, and the circles the LRS

measure was performed on 5 new cells from the same batch. For each cell, the HRS (triangle in Fig. 3(a)) and LRS (square in Fig. 3(a)) are reported. The lines correspond to the average HRS and LRS over the cells. After fabrication, the HRS/LRS ratio of 10^4 gradually decreases to 10^2 during the first two weeks. This originates from the natural redistribution of O^{2-} ions from the HfO_2 into the Ti layer at post-fabrication, as validated by the two *X-ray Photoelectron Spectroscopy* (XPS) analyses performed at day 1 and day 60 after fabrication (Fig. 3(b)). The ALD deposited HfO_2 layer is stoichiometric at day 1 with a 35 %/65 % Hf/O ratio and at day 60, a 10 % loss of oxygen ratio is observed in the HfO_2 while a 20 % increase of oxygen in the Ti-layer is observed. The redistribution of oxygen into the Ti layer is also visible in Fig. 1, where the TiO_x layer formed in contact with the HfO_2 layer appears darker. The final HRS obtained at day 60 mainly corresponds to the resistance of the HfO_2 layer and is then lower than day 1 due to the reduction of the stoichiometry of the oxide leading to a lower quality oxide, i.e. less insulating. Note that the oxidized Ti layer is essentially conductive since it contains about 80 % of Ti according to the XPS analysis. The final LRS, which corresponds to the resistance of the CF and the Ti layer, increased due to the slight oxidation of the Ti layer coming from the redistribution of the O^{2-} ions.

3.2 Effect of Ti layer thickness and tuning of the oxidation rate

The natural drift of O^{2-} ions and the resulting oxidation of the interfacial Ti layer has strong impact on the device properties. In this section, we study the impact of the Ti layer thickness.

Two additional devices were fabricated with a Ti layer thickness of 10nm and 100nm respectively. The different voltages (set, reset and forming) involve of these devices do not significantly change compared to the 30nm device. The thickness of the Ti layer has an impact on the amount of O^{2-} ions it can capture. Figure 4 plots the evolution of the HRS and LRS for the three different devices (10nm, 30nm and 100nm) over 60 days after the end of the device fabrication. The 10nm layer (symbols in black) shows a good stability and the average resistance after 60 days is similar to the average resistance after fabrication. Indeed, the layer is expected to be fully oxidized and no changes should occur afterwards. Our reference 30nm Ti layer device (symbols in blue) changed during the first 15 days after fabrication and remained stable after that, reaching a lower HRS than the 10nm Ti layer device. As already explained, this is due to the reduction of the oxygen ratio in the switching layer. The 100nm Ti layer device (symbols in red) slowly stabilizes over time close to its initial value. This can be accounted to the ability of a thicker Ti layer to capture more oxygen

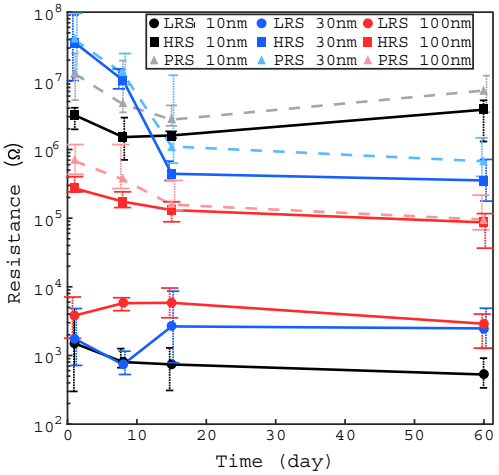

Fig. 4 Post-fabrication *Low Resistance State* (LRS), *High Resistance State* (HRS) and *Pristine Resistance State* (PRS) aging comparison of devices with different Ti layer thickness (Black = 10nm, blue = 30nm and red = 100nm)

from the HfO_2, further reducing the resistance of the resistive switching layer. The final LRS is close between devices because the equivalent resistance of the device in this state corresponds to the resistance of the conductive filament, which is very low for all devices, and the resistance of the formed mostly-conductive TiO_x layer that is directly proportional to the thickness of the material. The device with a 10nm Ti layer leads to the lowest resistance, reaching an average of 400Ω, while a device with a 100nm Ti layer reaches an average LRS of $3k\Omega$. Similarly, the final HRS obtained is the sum of the resistance of the remaining plug, the resistance of HfO_2 and the resistance of the Ti_x layer. The TiO_x layer resistance being in the order of $k\Omega$ and the plug being conductive, the main resistance comes from the HfO_2. Adding more defect to this layer, the 100nm Ti layer device becomes less resistive than the 30nm which, for the same reason, is less resistive than the 10nm.

As a conclusion, we saw that we can both mitigate the aging phenomenon and tune the final HRS/LRS ratio with the thickness of Ti layer. Both thin (10nm) and thick (100nm) Ti layers led to stable properties. The different devices reached a ratio of the order of 10 for 100nm of Ti, 100 for 30nm and a ratio of the order of 5.10^4 for a 10nm Ti layer.

3.3 Introduction of an ALD-deposited oxygen barrier layer

Another solution to alleviate the aging problem is the introduction of an oxygen scavenging layer. We now focus here on a Pt/HfO_2 (10nm)/TiO_2 (5nm)/Ti (10nm)/Pt stack. The TiO_2 layer was deposited by ALD in order to have a good quality oxide and stabilize the diffusion of the O^{2-} ions

in the Ti layer. This stack shows good electrical properties with on average a LRS of 200Ω, a HRS of 5MΩ, a $V_{Forming}$ of 7.5V, a V_{Reset} of -1.2V and a V_{Set} of 2V (Fig. 5). The pristine resistance state increased from $10^7\Omega$ without the TiO_2 layer to $10^9\Omega$. Indeed, a thicker oxide layer was obtained, formed by the stack of the 5nm TiO_2 and the 10nm HfO_2. Also, the introduction of the atomically perfect TiO_2 layer reduces the ability to capture the O^{2-} ions from the HfO_2 layer. On the one hand, the substoichiometric region is reduced compared to the Ti layer used in the previous section, thereby increasing the forming ① and set ③ voltages. On the other hand, the reset process with this new stack became different from previously and two distinct phases can now be distinguished. The first part of the reset process ②a happens after -0.5V with a progressive increase of the resistance, while the second phase ②b starts after -1V with an abrupt increase of the resistance. This phenomenon was reported to be due to the low conductance of the conductive filament during the LRS [16, 17]. In the progressive reset region, the filament is becoming thinner in the region between -0.5V and -1V until becoming a single channel quantum wire at the point of the abrupt increase of the resistance. The filament finally breaks and the OxRRAM resistance becomes high.

Figure 6 shows that the OxRRAM stack has a very stable resistance states over 40 days after fabrication compared to the previous Pt/HfO_2/Ti/Pt stack. Comparing the final resistance states of the two different stacks, adding the TiO_2 layer gives a similar HRS than the 10nm Ti layer device with 5MΩ, the main noticeable difference appears from a lower LRS with 100Ω compared to the 400Ω attributed to a larger current overshoot at forming/set caused by higher forming/set voltages. The endurance of the final device has been tested and showed 5000 stable cycles before the HRS/LRS ratio starts to degrade.

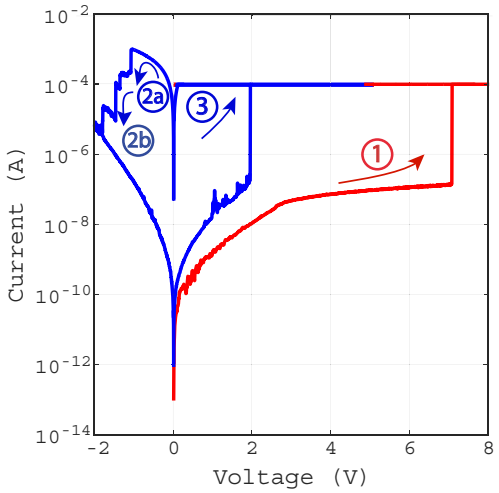

Fig. 5 Measured I-V plot of Pt/HfO_2 (10nm)/TiO_2 (5nm)/Ti (10nm)/Pt cell. First, the forming step is performed (*in red*) followed by the reset and set steps (*in blue*)

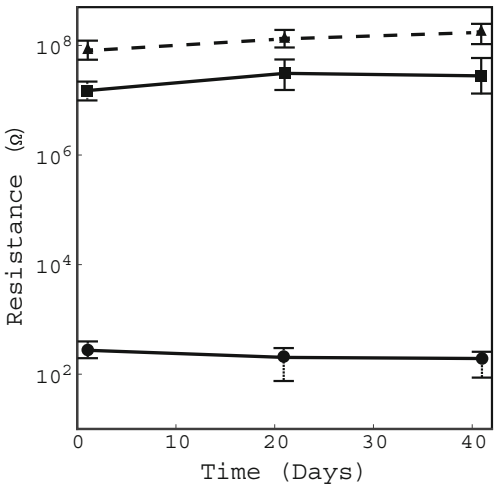

Fig. 6 Evolution over 2 months of its PRS (triangles), HRS (squares) and LRS (circles) of the Pt/HfO_2 (10nm)/TiO_2 (5nm)/Ti (10nm)/Pt stack

4 Conclusion

In this paper, we demonstrated an effect of fast aging of HfO_2/Ti - based OxRRAM stacks due to a O^{2-} ions migration in the Ti layer happening with no external active excitation. By changing the Ti layer thickness, we then showed that the time of oxidation and the final resistance states can be controlled. However, the aging phenomenon is usually undesirable for regular memory applications. To mitigate this issue, a TiO_2 layer was added and devices with no pronounced post-fabrication aging as well as good properties were fabricated.

Acknowledgements The authors would like to acknowledge Pierre Mettraux for his help on XPS analysis, as well as the CMi (EPFL) and Nanofab (UofU) staffs for the help in cleanroom.

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