Co-Design of ReRAM Passive Crossbar Arrays Integrated in 180 nm CMOS Technology

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***Abstract*—This work presents the co-integration of resistive random access memory crossbars within a 180 nm Read-Write CMOS chip. TaO_x-based ReRAMs have been fabricated and characterized with materials and process steps compatible with the CMOS Back-End-of-the-Line. Two different strategies, consisting in insertion of an Al_2O_3 tunnel barrier layer and the design of a dedicated CMOS read circuit, have been developed in order to increase the cell high-to-low resistance ratio of a factor of 1000 and to reduce the sneak-path current effects by one order of magnitude. The ReRAM cells have been integrated directly on a standard CMOS foundry chip, enabling low cost ReRAM-CMOS integration. The integrated memories show a set and reset voltages of -1 and 1.3 V, respectively. The measured operating voltages are compatible for low-voltage applications.**

***Index Terms*—Heterogeneous integration, passive crossbar array, post-processing, read-write circuit, resistive ramdom access memories (ReRAMs).**

I. Introduction

RESISTIVE switching devices are a class of two terminal devices in which a resistance change is driven by an electrically induced effect. Within this category, Resistive Ramdom Access Memories (ReRAMs) are the devices in which the resistance change involves redox mechanisms [1]. These devices typically consist of a fairly simple structure made of a Metal–Insulator–Metal (MIM) stack and show an hysteretic resistance behavior that can be leveraged in non-volatile memory applications. The cell resistance can indeed switch from a Low Resistance State (LRS) and a High Resistance State (HRS), which can be associated to *0* and *1* bit levels. The progress achieved over the last few years made ReRAMs an interesting candidate for the next-generation non-volatile memory solutions [2] and for new application such as enhanced logic circuits [3] and neuromorphic architectures [4]. The key characteristics that make ReRAMs a potential competitor for the NAND Flash technology are a simple structure, a high scalability [5], a low voltage operation [6], a fast operating speed [7], and a high endurance [8].

In addition to that, high performance ReRAM cells have been demonstrated with CMOS compatible materials [6] and low thermal budget processes, making it possible to integrate the technology in the CMOS Back-End-of-Line (BEoL). Few examples of such materials are TiN, used in CMOS technology as a barrier layer for the metal lines, HfO_x, used as high-κ dielectric for the CMOS gate oxide and TaO_x, also employed as an high-κ dielectric. Past demonstrations of ReRAM-CMOS integration mainly came from CMOS foundries and were performed at wafer level [9]. The main problems with this approach are a very low accessibility (just few fabs have hybrid ReRAM-CMOS processes) and a high fabrication cost, because it requires a dedicated CMOS foundry.

Embedded ReRAMs are classically arranged in 1T1R or passive 1R crossbar configurations. In the 1T1R topology [10], each ReRAM cell is in series with a selector transistor, which can optimally control the current flowing into the memory device. In a passive crossbar configuration [11], the top and bottom electrodes are directly connected to the bit and word line of the memory array. In this case, the desired cell is selected by activating the bit and word lines corresponding to the selected ReRAM cell. The first configuration has the advantage of a better electrical control over the memory devices, while the latter presents a much smaller feature size ($4F^2$, where F is the lithography critical dimension) and the possibility for 3D integration.

Although the crossbar configuration is desirable for the above mentioned reasons, it has the inherent disadvantage of the presence of sneak-paths current. The sneak-paths current originates from the leakage current of unselected devices in the LRS. This unwanted current, proportional to the applied voltages and the size of the array, can compromise the read operation. Among the possible ways to target this problem, it is possible to mention the insertion of proper selector devices [12], the use of special device configurations, like complementary switching ReRAMs [13], and the design of dedicated read and write circuits [14].

In this paper, we present a co-design strategy for ReRAM passive crossbar arrays involving both device fabrication and

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CMOS design. We propose two different methods to improve the characteristics of passive ReRAM arrays. First, we show a technological solution consisting in an embedded Al_2O_3 layer to improve the HRS to LRS ratio. The Al_2O_3 layer acts as a secondary switching layer resulting in an increase of the HRS. The measurements of the ReRAM devices with an embedded Al_2O_3 layer reports a three orders of magnitude improvement of the HRS/LRS at -0.5 V. Second, we present a CMOS read circuit optimized for crossbar implementation based on the in-house developed ReRAM technology. The designed circuits minimizes the sneak-path current reducing the voltage drop of unselected cells by compensating the CMOS technology mismatches. The circuit shows a sneak-path current reduction of more than one order of magnitude. In addition, we demonstrate a ReRAM-CMOS embedding method based on BEoL chip-level integration. The advantage of this integration method, if compared to the classical wafer-based ones, is contained cost, a fast prototyping capability and the possibility of embedding CMOS circuit for current compliance to obtain a reliable electrical characterization during the development of the material stack. For our investigation, we use commercial 180 nm CMOS technology because of its low cost and its maturity. We demonstrate ReRAM cells fabricated directly on the BEoL of a standard CMOS foundry chip working with a set and reset voltages of -1 and 1.3 V, respectively. The measured working voltages are compatible with the selected CMOS technology and suitable for low-voltage applications. This study extends our previous work [15] and [16] by considering a novel electrical characterization methodology enabling to overcome the forming current peaks (Section II-D). This procedure improves the electrical characteristics of the memory, even for 1R configurations. Moreover, we present a device-based solution to increase the HRS to LRS ratio (Section III-A). Furthermore, we give a more detailed analysis for the integration approach including scalability considerations and additional structural analysis (Section IV-B).

The remainder of the paper is organized as follows. In Section II, the fabrication and characterization of TaO_x-based memories with fully CMOS compatible materials and processes are described. In Section III, a device add-on and a dedicated read circuit are presented to improve the crossbar array characteristics. In Section IV, a method for ReRAM-CMOS integration and the associated electrical results obtained for the co-integrated memory cells are presented. Finally, the conclusion of the paper is given in Section V.

II. ReRAM Fabrication and Characterization

This section introduces the fabricated ReRAM devices (Section II-A) and describes their fabrication process flow (Section II-B), material analysis (Section II-C), electrical characterization (Section II-D) and modeling (Section II-D).

A. Introduction

With the objective of integrating ReRAM memories in the BEoL of CMOS chips, we developed a ReRAM technology targeting CMOS compatible materials, low thermal process budget and electrical characteristics compatible with CMOS transistors. TiN has been selected as electrode material for its thermal stability and its extended use in CMOS technology, while TaO_x has been chosen for its endurance and data retention capability [8]. The devices mentioned hereafter are fabricated in a single cross point configuration on standard 4 inch wafers. The main purpose of this technology exploration is the development of the layer structure and evaluating the switching characteristics. The micrograph of the fabricated devices is reported in Fig. 1. The devices consist of a resistive switching oxide (not visible in the micrograph) interposed between the Bottom Electrode (BE) and the Top Electrode (TE). The switching phenomena take place in the area located inside the VIA, where the switching oxide is in contact with the BE and the TE. The BE and the TE are connected to pads for probe station testing.

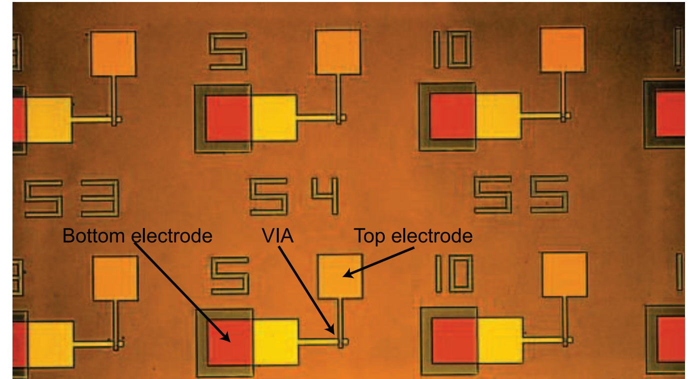


Fig. 1. Micrograph of the fabricated TaO_x-based cells. Each device is composed by VIA, top electrode, bottom electrode. The VIA, of diameter of 1, 2, 3, 5, and 10 μm, is located at the intersection of the top and bottom electrode.

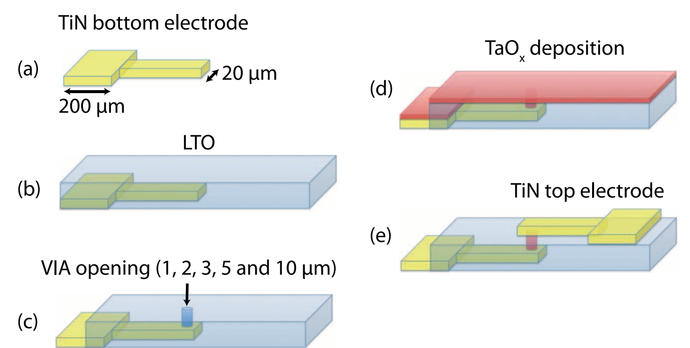


Fig. 2. Single cross-point ReRAM process flow: (a) TiN BE sputtering and RIE; (b) LTO deposition; (c) LTO BHF wet etching; (d) TaO_x sputtering; (e) TiN TE sputtering and RIE.

B. Device Process Flow

The fabrication process flow for the stand-alone ReRAM devices is shown in Fig. 2. First, a 200 nm TiN layer is deposited by room temperature reactive magnetron sputtering on a Si wafer passivated with 1 μm of SiO_2. The layer is then etched by a Cl-based Reactive Ion Etching (RIE) to create the bottom electrode [Fig. 2(a)]. Subsequently, a Low Temperature Oxide (LTO) SiO_x passivation layer is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) at 425 °C [Fig. 2(b)]. The 100-nm-thick LTO layer is then etched by BHF wet etching to open the VIAs and the BE contact pad. The VIAs determine the device diameter and have the diameter of 1, 2, 3, 5, and 10 μm [Fig. 2(c)]. The TaO_x deposition is achieved

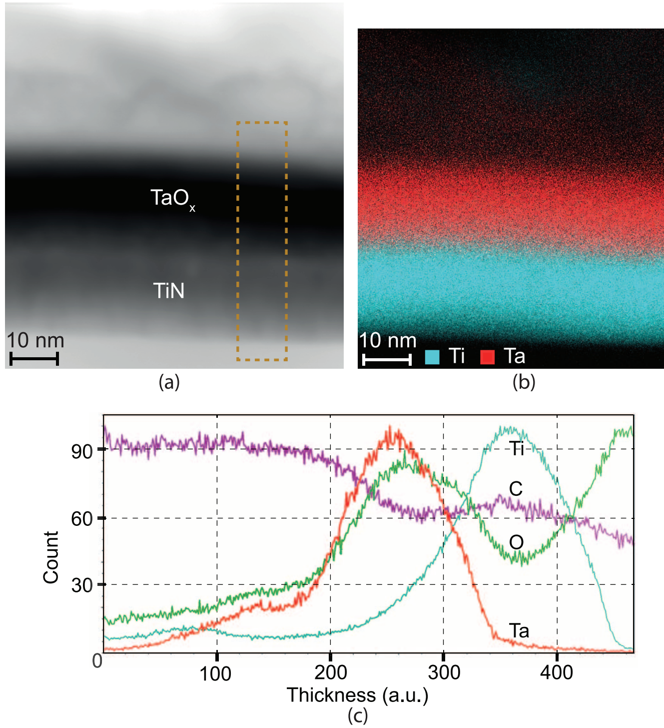


Fig. 3. Material analysis for the TiN-TaO_2 material stack showing (a) TEM micrograph, (b) EDX analysis for the Ti and Ta atoms, and (c) line profile. The line profile has been obtained along the line scan shown in (a). The TaO_2 layer has been deposited by reactive sputtering from a Ta_2O_5 target at 1000 W, 15 sccm Ar, and 3 sccm O.

by magnetron sputtering from a TaO_x target with increasing RF power in a O_2/Ar atmosphere [Fig. 2(d)]. The resistive switching layer is finally capped by a sputtered TiN TE that is etched by Cl-based RIE [Fig. 2(e)]. The device diameters were chosen to be in the μm range because in the targeted technology the minimal linewidth for the BEoL top metal line is 1.2 μm. If a higher cell density is needed, the presented process flow can be easily adapted in order to enable a further miniaturization of the fabricated devices.

C. *Material Characterization*

Material characterization was carried out to develop and characterize the sputtering recipe for the TaO_x switching layer. We optimized the oxygen flow, the deposition time and the RF power to target Ta_2O_5 and TaO_2 stoichiometries. Fig. 3 shows an example of a TEM-EDX analysis for a TaO_2 deposited layer deposited by reactive sputtering from a Ta_2O_5 target at 1000 W, 15 sccm Ar, and 3 sccm O. The samples used for the material analysis were prepared by a blanket deposition of TiN and TaO_x on a 1 μm SiO_2 passivated Si wafer performed with the same sputtering conditions as the ReRAM device films. Table I summarizes the obtained TaO_x stoichiometries for different deposition conditions. The analysis, obtained by AES and EDX depth profiling, shows Ta and O percentages close to the desired ones (the desired concentrations are 30% Ta and 70% O for Ta_2O_5, 33% Ta and 67% O for TaO_2).

TABLE I
TaO_x COMPOSITIONS

Recipe	Deposition condition	Element	Percentage
Ta_2O_5	Ta_2O_5 target, 1000 W	Ta	28.6%
	15 sccm Ar, 3 sccm O, room T°	O	71.4%
TaO_2	Ta_2O_5 target, 1000 W	Ta	35%
	15 sccm Ar, room T°	O	65%

D. *Electrical Characterization*

In this subsection, we presents the measurement setup, the test methodology, the forming procedure and the electrical characteristics of the fabricated devices.

1) Test Setup and Forming Methodology: The fabricated TaO_x-based ReRAMs have been electrically characterized with an automatic electrical characterization setup. The setup consist of an HP 4155b parameter analyzer and a Cascade Summit motorized probe station, controlled by GPIB interface through a gateway by a dedicated Matlab program.

Typically, ReRAM devices require an initial stress step known as forming process in order to exhibit memory characteristics. During that process, the applied electrical stress is intended to increase the concentration of defects in the resistive oxide, thus enabling conductive filament formation. It is therefore imperative to precisely control the current during forming, especially in passive elements, so as to avoid catastrophic dielectric breakdown.

For passive ReRAM devices, the parameter analyzer current compliance can be used to limit the maximum current running through the device. Nevertheless, the forming process characteristic response times are below the μs range, resulting in a time window much smaller than the characteristic response time of the parameter analyzer. As a consequence, in a passive element setup, it becomes practically impossible to completely suppress the current overshoot phenomena occurring during forming.

For our technology, we measured a current overshoot in the order of 1.2 mA for a compliance value of 500 μA set in the parameter analyzer and a rather slow response time of the parameter analyzer (70 μs) compared with the nature of the forming dynamics. These measurements were obtained monitoring the voltage drop over a 50 Ω resistor in series with the tested ReRAM.

Current overshoot is associated with excessive stress in the devices resulting in lower HRS/LRS resistance ratio and smaller device lifetimes. It can moreover increase power consumption as it results in higher reset current values. It is indeed reported that the current required for the reset is close to the one used during forming [17].

The current overshoot peak depends primarily on the cell forming voltage but can be limited by acting on the current compliance setting, the range but also hold and integration times of the parameter analyzer.

In order to reduce the overshoot peak, we used a two-step forming procedure. First, "forming" operation is performed with a large resistor in series to the ReRAM. The resistor, with a value in between the ReRAM pristine resistance value (GΩ) and the LRS (kΩ), is used to avoid an abrupt resistance change and to reach the current compliance smoothly in a linear way, instead of exponentially like during the forming process. Before

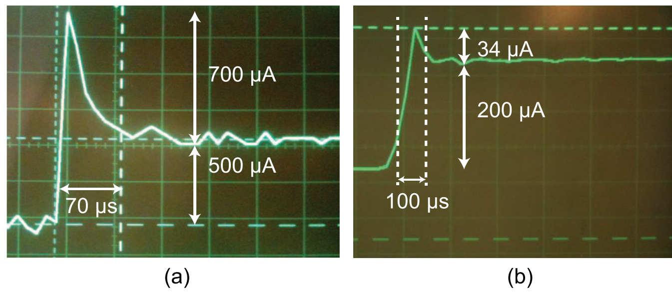


Fig. 4. Oscilloscope data of a 50 Ω resistor in series to TiN/TaO_2 (25 nm)/TiN ReRAM cell during the forming operation: (a) shows a forming operation using the parameter analyzer current compliance, which is reached just after 70 μ s and with a peak current is 1.2 mA (compliance current of 500 μA); (b) shows the forming result after a second forming operation. A very small current overshoot of 34 μA for a 200 μA compliance is reported.

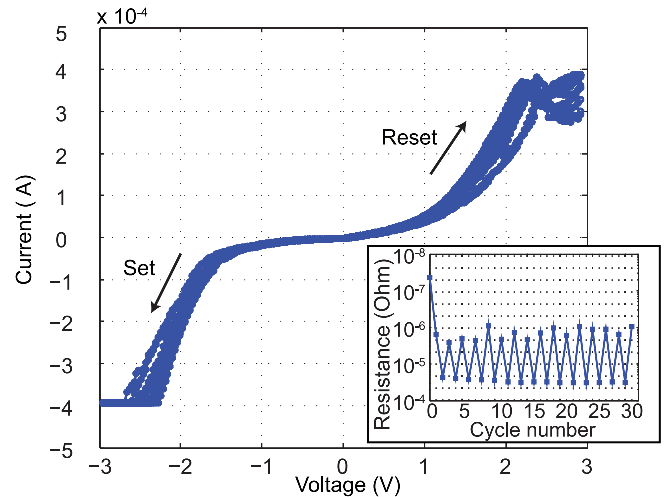


Fig. 5. Electrical results for the TiN/TaO_2(25 nm)/TiN. The forming operation was performed at 200 μA with a 100 kΩ series resistance. The cell has been cycled from 3 V, 400 μA and −3 V, 400 μA. Inset shows the result of the read operation, performed at 0.1 V. The memory shows a LRS of 20 kΩ and a HRS of 600 kΩ.

the forming process, a large part of the voltage drops directly on the memory cell, while, after the forming process starts, the series resistor absorbs the voltage drop avoiding reaching the current compliance set on the parameter analyzer. This first "forming" is a soft memory breakdown: the resistance of the memory is unchanged after this operation. The voltage drop on the memory cell is not large enough to trigger a complete forming process and the current values are sufficiently low, allowing to limit Joule heating effects in the device.

The result on the ReRAM cell of this first forming can be seen if a second forming is applied with a classical setup (no resistor in series and current compliance applied with a parameter analyzer). The forming voltage is largely reduced and, because of that, the current overshoot drops by two orders of magnitude.

2) Forming Process Results: Fig. 4 reports the oscilloscope data for a standard forming (a) and for a forming performed following the above mentioned procedure (b). In the latter case, we obtained an overshoot value 17% larger than the compliance current limit, while with a standard forming we can have a peak which is 140% larger than the nominal one. This elaborate forming procedure enables a better control of the current delivered to the stand-alone memory devices, greatly improving the device yield and the switching properties. This procedure has been applied in order to avoid the response time limitations of the parameter analyzer, a procedure not needed in the case of RERAM devices integrated in CMOS. Indeed, in this last case, the transistor would have direct control over the device, acting to directly limit the current.

3) Set/Reset Cycles: DC I-V tests have been performed on the fabricated TaO_x-based ReRAMs. After the forming operation, carried out by monitoring the absence of current overshoots and using a two-step forming operation with a 100 kΩ resistor, the memory sweep has been obtained by applying a DC voltage ramp to the ReRAM cell. The forming voltages were 10 V, 3.3 V, and 2.2 V for 25 nm TaO_2, 5 nm Ta_2O_5 and 3 nm Ta_2O_5, respectively. A typical I-V curve for the 25 nm TaO_2 is shown in Fig. 5. The 2 μm TiN/TaO_2 (25 nm)/TiN was first formed with a 100 μA compliance. Then, the cell was cycled from 0 to 3 V with a current compliance of 400 μA and from 0 to −3 V with a current compliance of 400 μA. The measured resistance values, shown in the Fig. 5 inset, are 20 kΩ for the LRS and 600 kΩ for the HRS. The resistance has been measured at 0.1 V by linear interpolation of the I-V curve. The device set and reset voltages are −1.7 V and 2.3 V, respectively. It is interesting to notice that, due to the proposed forming process, the current needed for the reset process is equal to the set current. This is an indicator of the absence of current overshoots during the set process.

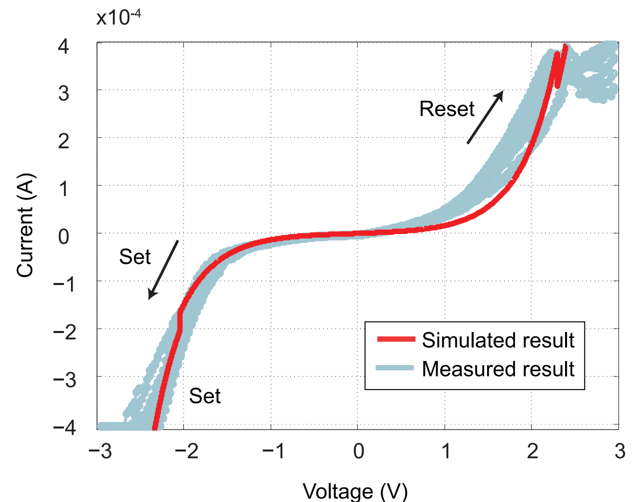


Fig. 6. I-V curve measurement for the fabricated TiN/TaO_2(25 nm)/TiN ReRAM cells and Verilog-A model.

E. Device Modeling

We used a Verilog-A compact model developed and released by Stanford University [18] to model our ReRAMs. A model that describes the behavior of the fabricated cells can be used to have a projection of the effects of technology variations (i.e., TaO_x thickness) and test conditions and for a partial verification of the physical principles behind the ReRAM cell switching. Fig. 6 shows a comparison between the electrical results obtained for the 2 μm TiN/TaO_2 (25 nm)/TiN ReRAM presented

TABLE II
FITTING PARAMETERS

Parameter name	Value	Unit	Description
t_{ox}	20.55	nm	Oxide thickness
g_{max}	455	pm	Maximum gap value
g_{min}	430	pm	Maximum gap value
g_0	125	pm	Gap scaling factor
V_0	413.9	mV	Voltage scaling factor
v_0	19	nm/ns	Escape velocity
I_0	91.3	µA	Current scaling factor
β	0.8	1	Gamma scaling factor
γ_0	16.2	1	Gamma initial value
δ_{g0}	20	mm	Random variations parameter
F_{min}	1.6	GV/m	Minimum field for gap enhancement

before and the modeled electrical behavior of the cell. The measured I-V relation shows a linear current-voltage dependency in the LRS, which is classically interpreted as a ohmic conduction mechanism associated to the conduction through the filament. In the HRS, the current and voltage are linked by an exponential I-V relation. The HRS conduction mechanism is usually identified by different phenomena, i.e., trap-assisted tunneling, Poole-Frenkel emission, Fowler-Nordheim tunneling and direct tunneling [18]. The used model embeds the mentioned mechanisms through the equations

$$I(g, V) = I_0 e^{-g/g_0} \sinh\left(\frac{V}{V_0}\right) \quad (1)$$

$$\frac{dg}{dt} = v_0 e^{-E_a/kT} \sinh\left(\frac{q\alpha\gamma V}{t_{ox} kT}\right) \quad (2)$$

where g is the gap between the tip of the filament end and the opposite electrode, v_0 is velocity containing the attempt to escape frequency of the oxygen ions to overcome the activation energy barrier, E_a is the activation energy for vacancy generation, a is the hopping site distance, γ an enhancement factor (related to the polarizability of the material and to the non-uniform potential distribution) and t_{ox} is the switching material thickness. The enhancement factor γ is calculated by the equation

$$\gamma = \gamma_0 - \beta\left(\frac{g}{10^{-9}}\right)^3. \quad (3)$$

Equation (1), defining the current as an exponential function of the voltage and the gap, describes both the linear and the exponential regimes of the ReRAM resistances. The simulation results, shown in Fig. 6 together with the measured result, fit well the electrical characteristic of the device, corroborating the hypothesis that the HRS I-V behavior is related to tunneling-based phenomena. The fitting parameters used in the model are summarized in Table II. The Verilog-A model simulation is limited to −2.5 V because the cell current attains the compliance value. In the simulation test bench there is no current limiter component, so the maximum current flowing through the cell is limited by controlling the applied voltage. This is possible in a simulation environment because of the deterministic behavior of the model, while it is not suitable for electrical tests of real components due to the set voltage variations. Furthermore, it is not possible to exactly simulate the cell behavior during the reset process. This is due to the stochastic nature of the reset, which is caused by the random probability associated to the filament breakdown phenomena.

III. PASSIVE CROSSBAR ARRAYS SOLUTIONS

In this section, two solutions for improving the characteristics of ReRAM passive arrays are presented. First, in Section III-A, we propose a technological method to increase the difference between the HRS and the LRS. Then, in Section III-B, we present a circuit solution to address the sneak-path current path problem.

A. Resistance Ratio Improvement

This subsection, first gives an overview of the limitations caused by the variations in ReRAMs on the read margin. Second, we show the effects of the insertion of an Al_2O_3 over the HRS/LRS ratio. Finally, we present an analysis and a discussion of the obtained electrical measurements.

1) Overview: Stochastic variation of the memory states is intrinsic to oxide ReRAM technology, both during SET, reset, and read operations. In oxide based ReRAM, it is directly linked to the oxygen vacancy movement as a result of the high local electric field and self heating mechanisms. Moreover, it is particularly evident in the HRS where the filament breakdown process is dominant. In that regime, small variations of the tunneling gap results in significant HRS variations as indicated by their exponential interdependence [20]. LRS is generally less prone to noise fluctuations as the formed filament exhibits ohmic conduction characteristics and is typically associated with large current values, rendering the effect of noise less significant. Added to that, the architectural configuration and the parasitics of the circuit reduce the memory read margin by a significant amount [21]. It is therefore of paramount importance to ensure a safe read both during LRS and even more so while in the HRS state.

One way to achieve this is to increase the ratio between the HRS and LRS which would result in a safer read in both states even in very low voltage. Increasing the read margin can not only result in a reliable read operation, but also decrease the complexity of the read circuit required. In this section we focus on this aspect, from a technological point of view.

2) Al_2O_3 Tunnel Layer: In order to increase the HRS to LRS ratio, we experimented with the insertion of an Al_2O_3 layer between the switching oxide and the chemically reactive BE. The objective was the increase of the HRS by inserting a tunnel barrier in series with the ReRAM. We fabricated TiN/HfO_x/Pt and TiN/Al_2O_3/HfO_x/Pt memory cells based on the process flow shown in Section II-B. The 10-nm HfO_x and the 2-nm Al_2O_3 depositions are achieved by Atomic Layer Deposition (ALD) at 200 °C from TMA and TEMAH precursors, respectively. The Pt electrode was deposited by room temperature sputtering and etched by RIE with a Cl_2-Ar based chemistry.

DC I-V test were performed on the fabricated ReRAMs. Tests comparison between the electrical characteristics of TiN/HfO_x(10 nm)/Pt and TiN/Al_2O_3(2 nm)/HfO_x(10 nm)/Pt memory cells is shown in Fig. 7.

The results show a HRS of 10 MΩ and a LRS of 1.5 kΩ for the TiN/Al_2O_3/HfO_x/Pt cells, and a HRS of 25 kΩ and a LRS of 6 kΩ for the TiN/HfO_x/Pt cells. The HRS to LRS ratio improved by three orders of magnitude factor for the cells with the Al_2O_3 layer at −0.5 V. The main drawbacks related to the Al_2O_3 layer insertion are a larger voltage operation and the lowering of the low resistance state. The set voltage increased from

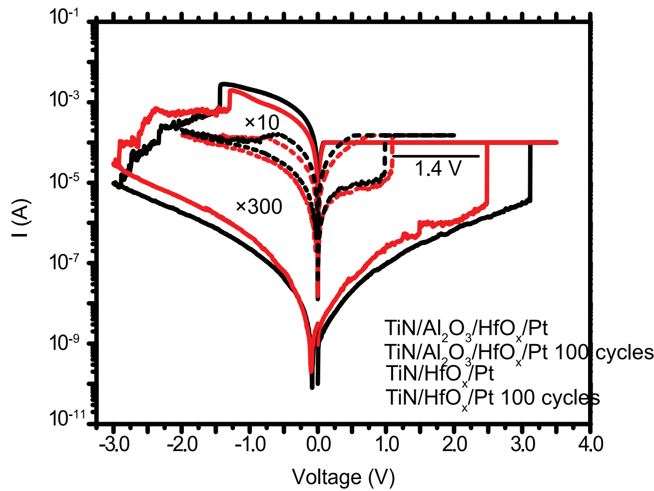


Fig. 7. Electrical measurements comparison between TiN/HfO_x/Pt and TiN/Al_2O_3/HfO_x/Pt memory cells. The insertion of the Al_2O_3 layer improves the HRS to LRS ratio by a three order of magnitude factor, while increasing the Set and Reset voltages by 1.4 V and 0.8 V, respectively.

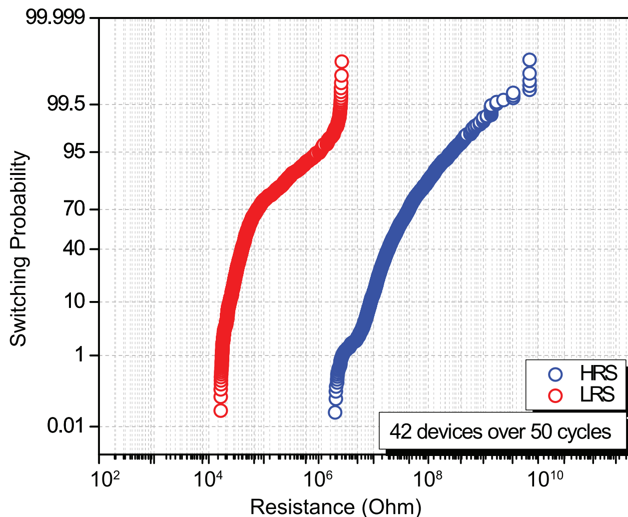


Fig. 8. Switching probability for the TiN/Al_2O_3/HfO_x/Pt memories. The data are extracted from 42 devices over 50 cycles of operation.

1 V to 2.5 V and the reset voltage from −0.7 V to −1.5 V, while the LRS decreased from 6 kΩ to 1.5 kΩ. Moreover, the insertion of the Al_2O_3 layer changed the forming voltage from 6.7 V to 9.1 V. Furthermore, the switching resistance variation is higher for the TiN/Al_2O_3/HfO_x/Pt memories. Fig. 8 shows the switching probability for the memory with the Al_2O_3 layer. The 70% switch probability for the LRS varies from 10^4 Ω to 10^5 Ω, while the HRS one varies from 10^6 Ω to 10^8 Ω. The results for the TiN/HfO_x/Pt memory (not shown in the figure), show a LRS variation from 1 kΩ to 10 kΩ, and a HRS variation from 108 kΩ to 120 kΩ. The data have been obtained from 42 devices cycled 50 times each, and the resistances have been obtained by a read operation at +0.1 V (which is why the resistance numbers are slightly different compared to the ones reported for Fig. 7). It is interesting to notice that the LRS curve of Fig. 8 could be interpreted as the superimposition of two normal distributions. The last part of the curve is caused by the devices stacked at the HRS.

Two solutions to address these effects are the modulation of the Al_2O_3 thickness to reduce the operating voltage and the design of specific circuit solutions, like the one presented in Section III-B, to address the lower LRS, and the associated crossbar array leakage currents.

3) Results Analysis and Discussion: The main differences between the curves of Fig. 7 can be explained by the participation of the Al_2O_3 layer in the ReRAM cell switching. This hypothesis is supported by the results shown in the literature for single layer Al_2O_3 ReRAMs. These cells show indeed a highly resistive HRS, a high forming voltage and an abrupt reset characteristic [22]. Consistent results for hybrid resistive switching layers have also been demonstrated in [23]. Zhang *et al.* show how the forming voltage of TiO_x-Al_2O_3-based memories are related to the film thicknesses and how the TiO_x thickness influences the stack resistance values.

It is then conceivable that the Al_2O_3 is switching as well as the HfO_x layer. It is important to point out that the cells are tested with different parameters in order to improve their performances.

The bilayer stack can safely support a larger range of voltage whereas a HfO_x layer in the order of 10 nm suffers from catastrophic breakdown in the range of 3 V/−3 V, resulting in permanent dielectric damage, a lower resistance ratio and endurance. A further consideration can be made about the difference between the very first memory cycle and the subsequent ones in the Al_2O_3 memory. It can be noted indeed that the set voltage reduces from 3.3 V (for the first cycle) to 2.5 V. This effect can be explained by the stabilization of the conductive filaments in the Al_2O_3 layer. This stabilization is caused by the creation of permanent defects, by the cell heating effects resulting from the cell set-reset switching and by lower current overshoots in the set phase, which results from a lower set voltage. It is possible to notice indeed that the first reset-set cycle requires more power than the subsequent ones. These phenomena are more visible in the Al_2O_3 cell because of the higher energy field required for the creation of oxygen vacancies. These set variations also results in a higher spread in the resistance distribution.

We already stated that the addition of the Al_2O_3 layer influence the switching characteristic of the ReRAM cell in participating to the switching phenomena, and that the resulting I-V curve of the HfO_x-Al_2O_3 bilayer shows switching characteristics typical for Al_2O_3 memories. Moreover, Al_2O_3, when coupled to the typical ReRAM oxides (e.g., HfO_x, TiO_x, TaO_x, etc.) to create an heterojunction, creates a potential barrier because of it large bandgap. As a first approximation, the Al_2O_3 layer can be conceived as a tunnel barrier that inhibit the device current when the cell is in the HRS. These reasons, combined by the fact that also TiO_x-Al_2O_3 memories show Al_2O_3-like switching characteristics, suggest that the insertion of an Al_2O_3 layer could be use to improve the resistance ratio of other memory oxide materials, such as TaO_x.

A last consideration should be made on the influence of the Al_2O_3 layer on the ReRAM switching characteristic. If the Al_2O_3 layer effects on the HRS resistance could be approximated as a barrier, as it has been suggested before, a modulation of the Al_2O_3 thickness would result in a change

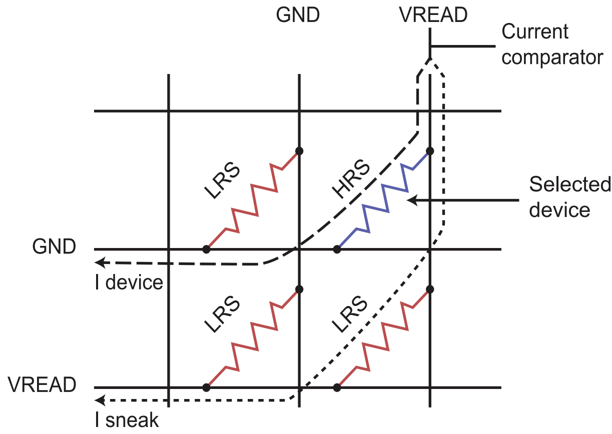


Fig. 9. Schematic representation of the sneak-path current. The total current has two components: one is the current flowing through the selected device, in blue in the figure, and one resulting from the unselected memory components in a LRS.

in the tunneling probability, and so a change in the HRS. Full study of the tunneling phenomena and its dependence from the material characteristics is out of the scope of this paper.

B. Sneak-Path Current Solutions

In this subsection, we first introduce the sneak-path current phenomena. Second, we present a read circuit designed to reduce the sneak-path currents by compensating the CMOS mismatches. We finally presents the results of the designed circuit.

1) Sneak-Path Current Introduction: The sneak-path current is intrinsically related to the passive crossbar array configuration. This phenomenon arises from unwanted current paths generated by unselected cells in a LRS and from a low-resistance value HRS. Fig. 9 shows a schematic representation of the sneak-path current problem. In the example, the current resulting from a read operation performed on the device in the HRS, reported in blue in Fig. 9, is composed by two elements. The first one is the desired output current and results from the voltage drop on the selected device, while the second term is the sneak-path current. If the magnitude of this second term is comparable or larger than the one flowing through the selected device, the circuit periphery may be led to an incorrect interpretation of the addressed bit. The sneak-path current is dependent on the memory array size and on the resistance configuration of the cells. This leakage current is the major limitation for the fabrication of large passive crossbar arrays. This limitation is even more severe in case we consider in this analysis the CMOS technology variations.

In order to limit the sneak-path current, we designed a read circuit that forces the potential drop across the unselected devices to a value close to zero. This is obtained applying the same voltage value at the device electrodes and compensating the technological mismatches with a calibration circuit.

2) Circuit Description: We designed the Read/Write circuit reported in Fig. 10. The system includes a digital controller, a reference voltage generator and the row and column drivers and address decoders shown in Fig. 11. The two blocks are used both for the read and write operation of the memory arrays by appropriately selecting the transistor switches.

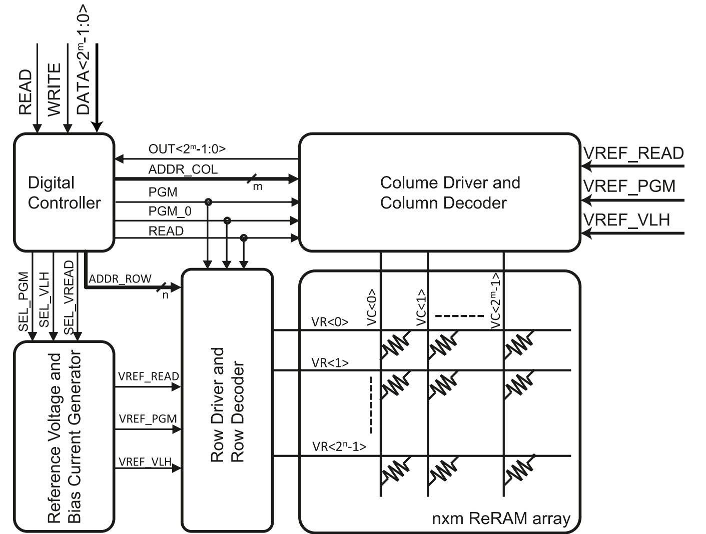
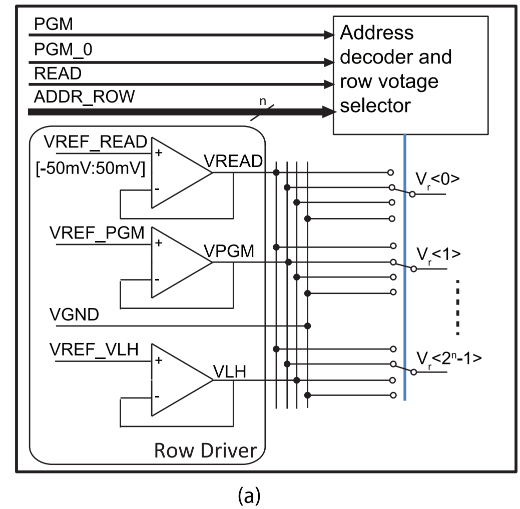


Fig. 10. Read/Write circuit block diagram. The system is composed by row and column drivers, a digital controller and a reference voltage generator.



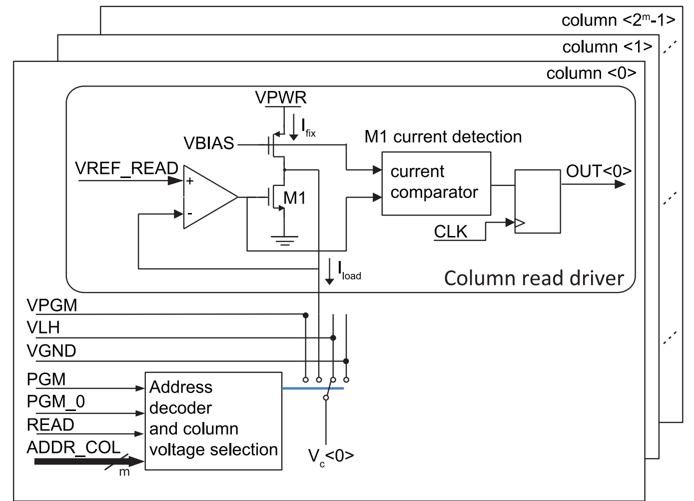


Fig. 11. Schematic representation of (a) the row driver and (b) the column driver.

During the read operation, the applied voltage scheme is similar to the one schematized in Fig. 9. The only difference lies in the resulting voltage VREAD for the rows and columns, which will be different due to the CMOS mismatches. In the following section, we refer with $\mathrm{VREAD_{row}}$ to the VREAD voltage resulting on the rows, and with $\mathrm{VREAD_{column}}$ to VREAD voltage resulting on the columns. In details, the row driver of Fig. 11(a) sets the unselected cells to the $\mathrm{VREAD_{row}}$ voltage level, while the selected cell's row is pulled down to GND. When the voltage $\mathrm{VREAD_{column}}$ is set by the column driver of the selected ReRAM, a current can flow through the selected device. This current will be equal to the voltage drop across the cell ($\mathrm{VREAD_{column}}$) divided by the stored resistance value. The load current $\mathrm{I}_{\mathrm{load},i}$ sensed for the selected device's i column is equal to $\mathrm{VREAD_{column}}$/R just if $\mathrm{I}_{\mathrm{load},i}$ does not have any sneak-path current contributions. In an ideal case, indeed, the unselected devices of the i column do not undergo any voltage drop as $\mathrm{VREAD_{row}}$ and $\mathrm{VREAD_{column}}$ equal. In this scenario, the device logic state can be easily evaluated by setting the current comparator to the value $VREF_{\mathrm{READ}}/(2 \times R_{LRS})$.

The circuit can be configured for reading a single ReRAM device or a complete row. In order to read a complete row, all the column drivers are set to $\mathrm{VREAD_{column}}$ while, as in the previous example, the selected row is pulled to GND and the unselected ones are forced to $\mathrm{VREAD_{row}}$. The resistance state evaluation of the selected ReRAMs is carried out by the current comparators of the column drivers as shown in Fig. 11(b).

Different considerations must be taken into account if we include the effects of the ReRAM resistance variability and the layout mismatches. In particular, the effect of this second term may lead to discrepancies between the differential amplifiers of the row and column drivers, resulting in a difference between $\mathrm{VREAD_{row}}$ and $\mathrm{VREAD_{column}}$. In this case, the current $\mathrm{I}_{\mathrm{load},i}$ can be described by the equation

$$I_{\mathrm{load},i} = \sum_{k=1}^{n} \frac{\Delta V_k}{R_k} \tag{4}$$

where n is the number of rows of the array and ΔV_k is the voltage drop for the k device that is connected to the column i. The maximum value for $\mathrm{I}_{\mathrm{load},i}$ is obtained when all the unselected cells are in a LRS state and the selected device is in the HRS

$$I_{\mathrm{load,max}} = (n-1)\frac{VREAD_{col,i} - VREAD_{\mathrm{row}}}{R_{LRS}} + \frac{VREAD_{col,i}}{R_i} \tag{5}$$

where R_i is the resistance value of the selected ReRAM and R_{LRS} is the LRS value. The aforesaid device resistances configuration corresponds to the maximum influence of the sneak-path current path on the current $\mathrm{I}_{\mathrm{load},i}$. This influence leads to an inaccurate result of the read operation when the load total current becomes higher than the reference one. The limit value for $\mathrm{I_{load}}$ can be then expressed as

$$I_{\mathrm{load},i} < I_{ref} \tag{6}$$

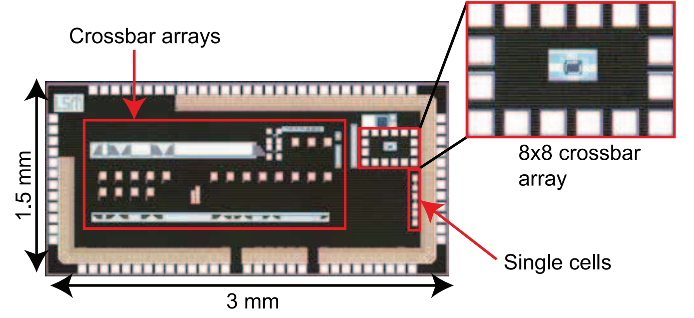


Fig. 12. Chip micrograph. Systems includes different size of ReRAM arrays (up to 128 × 8), a read/write circuitry and single cell test areas.

$$(n-1)\frac{VREAD_{col,i} - VREAD_{\mathrm{row}}}{R_{LRS}} + \frac{VREAD_{col,i}}{R_{HRS}} < \frac{VREAD_{col,i}}{2 \times R_{LRS}} \tag{7}$$

that can be simplified, neglecting the second term as $HRS \gg LRS$, into

$$n < \frac{1.5VREAD_{col,i} - VREAD_{\mathrm{row}}}{VREAD_{col,i} - VREAD_{\mathrm{row}}}. \tag{8}$$

Equation (8) shows that the maximum size of the ReRAM crossbar array is then not only limited by the HRS over LRS ratio (the term simplified in (7)), but also from the layout mismatches. To reduce its effect on the sneak-path current path problem, we introduced an offset calibration circuit that modifies the $\mathrm{VREF_{read}}$ reference voltage in the differential amplifier in Fig. 11(a). The $\mathrm{VREAD_{row}}$ can be modified in a ± 50 mV range according to the difference between $\mathrm{VREAD_{row}}$ and $\mathrm{VREAD_{column}}$ obtained from a differential pair voltage comparator.

3) Results: The previously described read circuit has been implemented together, with a write circuitry, in a commercial 180 nm CMOS technology. The micrograph of the chip is reported in Fig. 12. The chip, designed to enable a CMOS-ReRAM BEoL co-integration (further described in Section IV-B), contains different crossbar arrays, with size up to 128×8, and different test structures directly accessible through the pads for technology calibration. In the chip, the CMOS read and write circuitry is laying underneath the BEoL area designated for the crossbar arrays. For this test chip, the array column size has been limited to 8, while the row size goes up to 128. During the write operation of a whole row, the write currents resulting from each column sums up and flows through the row driver. A limited column size allows to limit the maximum row current and to reduce the sizing of the row driver transistors. The selected configuration is, at least for some extent, arbitrary. Other organizations could have been used such as a 32×32 array subdivided in four banks of 32 8-bit words.

The effects of the read circuit on the sneak-path current reduction has been validated by post-layout simulation. For the analysis we have chosen ReRAM values compatible with the ReRAM electrical results shown in Fig. 5. The values used for the analysis were 10 kΩ for the LRS and 100 kΩ for the HRS, with a 10% additional resistance variability from those nominal

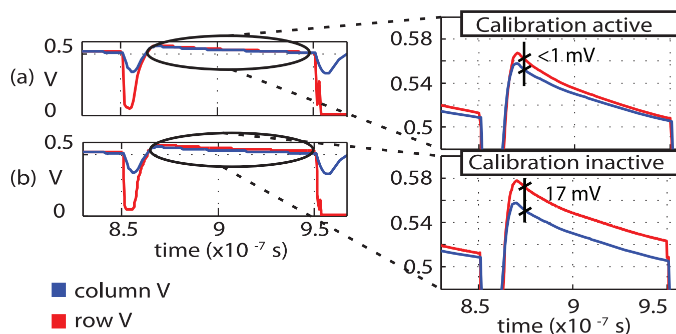


Fig. 13. Postlayout simulation of the voltage drop across an unselected ReRAM cell (a) with and (b) without the calibration circuit during the read operation. Voltage difference between the column (blue) and row (red) voltages, directly proportional to the cell sneak-path current, is reduced by more than one order of magnitude when the calibration circuit is active.

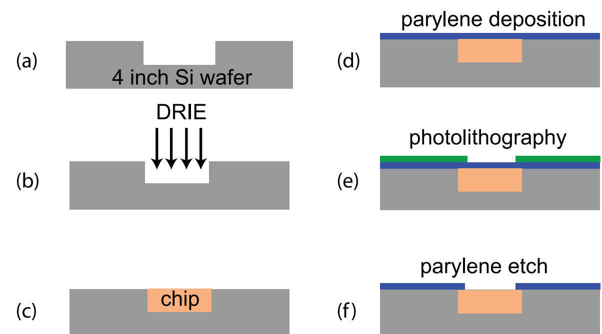


Fig. 14. Process flow representation for the carrier wafer fabrication: (a) Si substrate; (b) Si DRIE; (c) Chip mounting; (d) Parylene deposition; (e) Photolithography; (f) Parylene RIE.

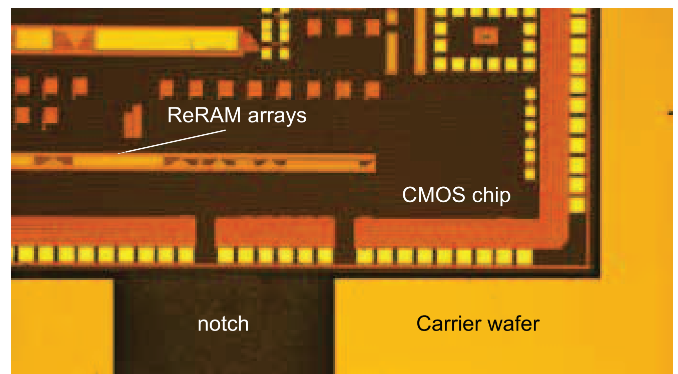


Fig. 15. Micrograph of the carrier wafer with embedded the CMOS chip. Visible notch is used to facilitate the chip release.

values in order to compensate eventual resistance fluctuations. The read voltage used in the simulation is VREAD $= 500$ mV. Fig. 13 shows the effect of the read calibration circuit during the read operation. In the figure, the voltage levels are shown across an unselected cell of the crossbar array, being the blue and red lines the column and row voltages at the ReRAM electrodes. Fig. 13(a) and (b) shows the same read operation with and without the offset calibration circuit, respectively. It can be noted that the calibration circuit reduces drastically the voltage drop across the unselected cell, resulting in a smaller sneak-path current generated from the unselected device. The voltage drop change indeed from 17 mV to less than 1 mV. On a general basis, a reduction of the leakage across unselected cells can play a relevant role in improving the read operation reliability, reducing the power consumed through the leak current paths and allowing a larger array size.

IV. Heterogeneous Integration of ReRAM on CMOS Chip

In this section, a method to integrate ReRAM on the BEoL of fully finished 180 nm CMOS foundry chip is presented. The ability of achieving chip level ReRAM co-integration is a key factor in order to lower fabrication costs and to speed up the prototyping ability. The main challenges of this methodology, rather than working at wafer level, are the chip handling and the lithography steps. The solution adopted to overcome these difficulties, described in Section IV-A, is the embedding of the CMOS chip in a carrier wafer. A wafer carrier helps indeed with the chip handling, enabling the use of machines that are designed to operate with standard Si wafers, and helps the lithography process, permitting the use of standard Cr-glass masks. Subsequently to the chip embedding, the die is processed to integrate the ReRAM memories on the CMOS chip. The integration approach is based on standard features present in commercial CMOS technologies. The integration fabrication flow and the electrical results for the embedded ReRAMs are described in Section IV-B.

A. Die Embedding

The developed process flow to create the carrier wafer is summarized in Fig. 14. The carrier wafer has been fabricated starting from a standard 4-in Si wafer [Fig. 14(a)]. After a lithography step to delimit the area where the chip will be located, a Si Deep Reactive Ion Etching (DRIE) based on a standard Bosh process with SF_6 and C_4F_8 and corresponding to the chip height has been performed [Fig. 14(b)]. A crucial point to improve the lithography resolution is avoiding any high mismatch between the Si wafer and the chip. The chip is then placed in the created Si pocket, which is designed to compensate the chip dicing tolerances and with a notch to facilitate the chip release [Fig. 14(c)]. The next step is the chip sealing, which is performed at room temperature by a parylene deposition [Fig. 14(d)]. This step has both a mechanical function, keeping the chip in the notch, and a masking function, protecting the chip from the following processes. Finally, a lithography step [Fig. 14(e)] and an anisotropic parylene etch by O_2 RIE [Fig. 14(f)] open the chip region for the subsequent process steps. Fig. 15 shows an optical image of a chip inserted in a carrier wafer, right after the parylene deposition.

B. MMC-Based Integration

In this section, we discuss an integration approach that has been used to integrate ReRAMs in standard CMOS foundry chip. The employed technique is based on a feature called Metal to Metal Capacitor (MMC), which is commonly used in standard CMOS technology to create small embedded capacitor. A scanning electron micrograph of a MMC structure is reported in Fig. 16. The MMC layer, in blue in the picture, is electrically connected to the *Metal 6* (M6) by means of internal via,

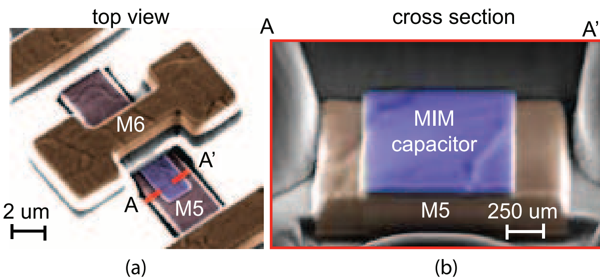


Fig. 16. (a) Scanning electron micrograph of the MMC capacitor and (b) FIB-SEM cross section.

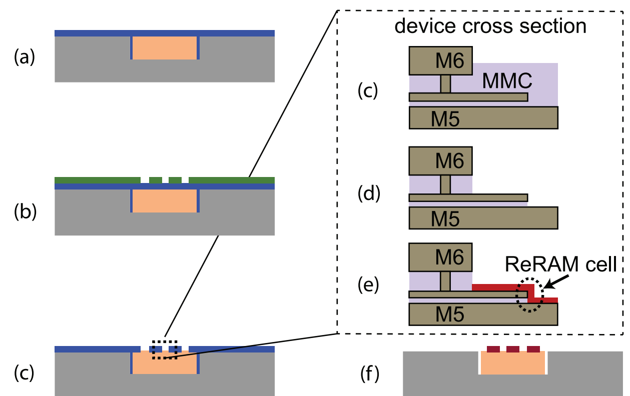


Fig. 17. Process flow representation for ReRAM post-processing: (a) Parylene layer coating; (b) Photolithography; (c) Parylene RIE; (d) Passivation BHF; (e) TaO_x sputtering; (f) Parylene lift off.

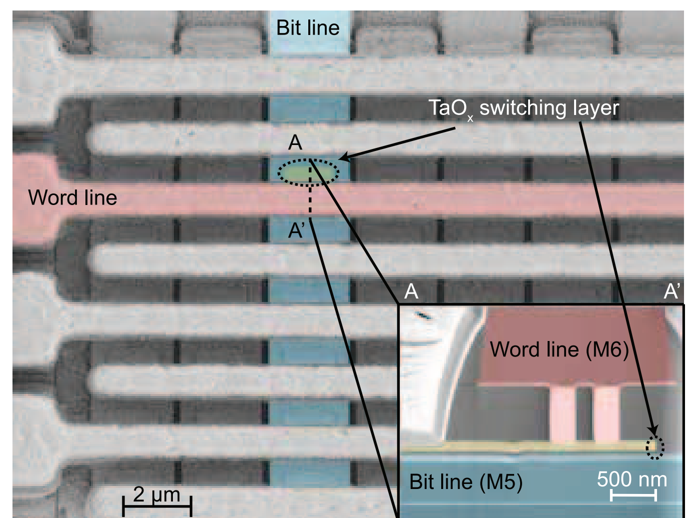


Fig. 18. Scanning electron micrograph of an 8 Bit line-8 Word line crossbar array with Word and Bit lines in M6 and M5. Inset shows a TEM cross section of the memory cross point. One of the ReRAM cells is highlighted in yellow.

and insulated from the *Metal 5* (M5) by a 50-nm-thick dielectric layer. The structure acts as a capacitor with the MMC layer and M5 being the top and bottom electrode, respectively. In the following subsections, we present the integration process flow, the electrical results and a discussion of the influence of the capacitor in the cell switching.

1) Integration Process Flow: The process flow for the ReRAM integration is reported in Fig. 17. First, the area-of-interest on the chip must be opened from the protective parylene layer [Fig. 17(a)], which will be used both as etchant protective layer and as a lift off sacrificial layer. A lithography step [Fig. 17(b)] and a O_2 RIE step [Fig. 17(c)] to etch the parylene layer are performed to open the chip area in which the ReRAM crossbars will be created. The chip passivation is then etched by a BHF solution [Fig. 17(d)] to access metal 5 (M5) and the MMC layer. Afterwards, the TaO_x switching layer is deposited by a room temperature reactive sputtering [Fig. 17(e)]. The parylene layer is then lifted off [Fig. 17(f)] to access the chip pads and to remove the unwanted deposited TaO_x.

The advantage of the proposed integration method is the absence of high-resolution lithography steps during the chip post-processing, reducing the total lithography steps and process cost. The cell dimension is indeed defined by the size of the MMC capacitor. The MMC layer has been designed in a way that, from a top view prospective, it is not completely overlapping with the M6. It is then possible to deposit the resistive switching material over the the MMC layer and M5. The deposited switching oxide covers the structure and connects the MMC layer and M5, which becomes the TE and the BE of the memory cell, respectively. The cell switching area is located at the structure edge, and the oxide conductive filaments are formed parallel to the structure sidewall. It is important to underline that the materials of the memory stack are the same as the ones used to fabricate the single cell memory cells presented in Section II. In the selected technology, the MMC layer is composed by TiN and M5 is an aluminum line coated by TiN, which acts as a barrier layer. The TaO_x layer is deposited under the same conditions of the above mentioned devices.

A further advantage of the absence of high resolution lithography steps is the possibility to scale the process to smaller technology nodes. Because the ReRAM cell is created just by the deposition of the switching oxide, the limiting factor is the sputtering conformality. Deposition techniques with a better conformality and control of the layer thickness, such as ALD, would enable the fabrication of highly scaled devices. A second point for the process scaling is the presence of TiN at lower CMOS technology nodes, as the described integration method relies on TiN as BE and TE materials. TiN is used as a barrier layer not only for Al interconnection technologies (such as the 180 nm CMOS technology described here), but also for many of the Cu-based ones (sub-180 nm CMOS technology nodes). Refractory metals or their nitrides, such as TiN, are used to prevent the Cu rapid diffusion in many materials used as inter-metal dielectrics and the drifts of Cu ions in these materials under the influence of electric fields [25].

Fig. 18 shows a combination of a SEM image and a TEM image (inset) of a ReRAM passive crossbar. Highlighted in the image, it is possible to recognize in red the Word line (M6), in blue the Bit line (M5, which corresponds to the bottom electrode of the ReRAM cell) and, in yellow, the MMC layer. From the inset, it is possible to notice that the MMC layer, which is the top electrode of the memory cell, is electrically connected to the M6. Fig. 19 shows a TEM-EDX cross section closeup of the MMC-M5 interface after the TaO_x deposition. It is possible to recognize the elements composing the $TiN/TaO_x/TiN$ memory stack.

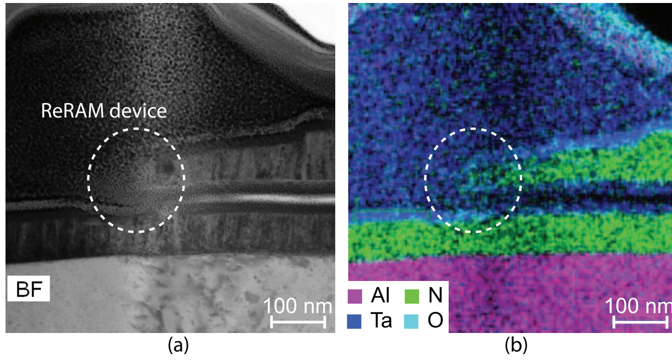


Fig. 19. Transmission electron micrograph of the MMC-M5 interface. (a) Bright field image and (b) EDX elemental analysis.

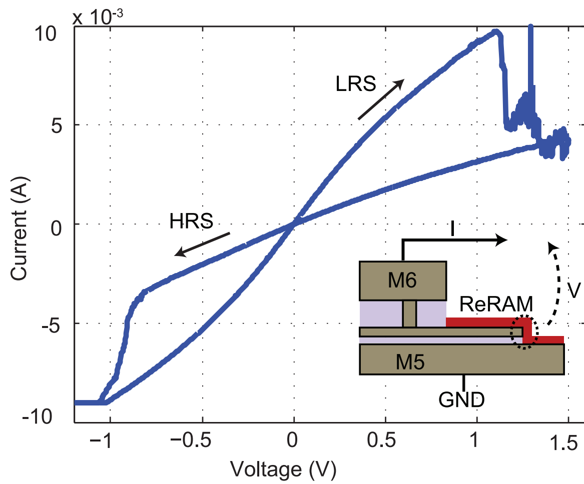


Fig. 20. Electrical results for the TiN/TaO_2/TiN ReRAM integrated cell. Set voltage is −1 V, Reset voltage is 1.3 V. The operating voltages are compatible for low-voltage applications.

2) Electrical Results: The ReRAM cells integrated in the BEoL of the CMOS chip have been electrically characterized. The test setup is the same as the one used for the single cross-point cells presented in Section II-D. The measurement results, obtained from single cross point cells directly accessible by the metal pads, are reported in Fig. 20. The ReRAM cell shows a LRS of 80 Ω, a HRS of 320 Ω and set and reset voltages of −1 V and 1.3 V, respectively. The operating voltages makes the cell suitable for low voltage applications.

The electrical behavior of the MMC-based ReRAMs, if compared to the single cross point cells, presents some differences. First, the integrated memories show forming-free characteristics. Indeed, during the first read operation, performed at low voltage and with no current compliance, the cells are already in the LRS. This could be caused by the fact that the TaO_x film is not embedded in a protective layer, so during the process steps following the oxide deposition it may have been reduced, and by the shape of the MMC structure. The MMC structure from the top prospective shows a square shape whose angles act a field enhanced structure lowering the electric field required for the cell switching. A second major difference lies in the resistance levels. The integrated cell shows a LRS of 80 Ω and HRS of 320 Ω. This difference is explained by the fact that the cell pristine resistance is a LRS. Because the TaO_x layer in its earliest resistance state presents a high-current leakage, it is difficult to obtain a proper reset. Furthermore, the reset operation, for the same reasons described before, requires a relatively high current flowing into the device, which can create the current spike phenomena visible in Fig. 20. These events are characterized by a stochastic nature, they are indeed not reproducible for subsequent write cycles, and, according to the literature, are caused by the high current and electric field effect on the oxygen vacancy-based filament [24].

3) Capacitor Influence: A final consideration can be made on the influence of the MMC capacitor on the ReRAMs switch characteristic. The capacitance has a value of 3.6 fF and it is electrically connected in parallel to the ReRAM cell. The resulting RC time constant is less than 1 ps, making it negligible if compared with the time scale of the observed phenomena. This time is indeed much faster than the voltage ramp time step used for the I-V sweep measurement and faster than any reported value for the ReRAM switching time. Furthermore, there was no need for a forming operation, which is the procedure that is the most sensitive to the current overshoots created by the line parasitics and by the setup, and the set operation was limited by the parasitic resistances in series with the ReRAM cell, so there was not an abrupt resistance change when reaching the current compliance. Moreover, this device configuration is not different from the VIA-based cell showed in Section II. In that case, the capacitance created by the electrode surface was also in parallel with the ReRAM cell, and in that case the analytically calculated capacitance value is around 100 times larger than the MMC one. Because of these considerations we can conclude that the influence of the MMC capacitor on the electrical characteristics of the ReRAM cell are negligible.

V. CONCLUSION

First, TiN/TaO_x/TiN-based memories have been fabricated and characterized, targeting CMOS compatibility and low-voltage operations. Second, based on the obtained electrical results, we designed a CMOS read circuit dedicated to passive crossbar array implementations. The read circuit allowed the reduction of the unselected cell voltage drop, and therefore the sneak-path current, by more than one order of magnitude. Then, we present a technology solution based on Al_2O_3 layer to improve the HRS to LRS ratio of a factor of three orders of magnitude. Finally, we demonstrated a low cost technique for heterogeneous integration of ReRAM devices in the BEoL of fully processed 180 nm CMOS chip. We applied the presented integration scheme to fabricate standalone memories and achieved ReRAM-CMOS post-processing integration. The measured integrated ReRAMs show characteristics with a SET voltage and RESET voltage of −1 V and 1.3 V, respectively.

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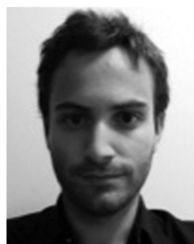

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