Computationally Efficient Multiple-Independent-Gate Device Model

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Abstract—Nanowire field effect transistors (FETs) with multiple independent gates around a silicon channel feature ultimate gate control, and are regarded as promising candidates for next-generation transistors. Being inherently more complex than the conventional gate-all-around nanowire FETs, they require longer simulation time, especially with numerical simulations. We present a new model, enabling the efficient computation of voltages and current in modular semiconductor structures with an arbitrary number of independent gate regions. Its validity extends on gate-all-around MOSFETs, FinFETs, and gateless channels. It exploits existing models for conventional devices and builds results on top of these. Being completely general, the method is independent from the models used to describe each region, a charge-based model in our case. Applied to a multiindependent-gate nanowire FET structure, extensive comparison of the proposed method with results from physics-based TCAD Atlas software and with numerical exact results show very good agreement with relative errors of less than 1.8% for potentials and less than 4% for currents, under a broad variations of physical parameters as well as biasing conditions. Interpreted language implementation shows a performance advantage in excess of one order of magnitude with respect to standard optimized numerical methods, still providing excellent accuracy, and making it suitable for implementation in circuit simulators.

Index Terms—Charge-based compact model, gate-all-around, multiple independent gate devices, silicon nanowire FETs.

Fig. 1. General structure of a device with multiple sections and two examples of application: (a) Cascade of N GAA MOSFETs: current and voltages are related the gate voltages and V_{DS}; (b) Structure of a GAA Vertically Stacked Silicon Nanowire FET where different structures in (a) are connected in parallel between metallic contacts and biased by three different gate potentials; (c) Schematic representation of a GAA Silicon Nanowire array: nanowires on the top layer bias the transistors on the bottom one: resulting current flows through the sections.

I. INTRODUCTION

MULTIGATE *Transistors*, e.g., gate-all-around (GAA) *Metal Oxide Semiconductor Field Effect Transistors* (MOSFETs), double-gate MOSFETs, FinFETs, have been thoroughly investigated in recent years primarily because of their

high electrostatic control over the channel and their high immunity to *Short Channel Effects* (SCE) [1]. To pursue these highly sought-after electrical characteristics and to achieve an even greater immunity to SCE, researchers are considering *Nanowire Field Effect Transistors* (NWFETs) with *Multiple Independent Gates* (MIG). In addition to the good electrostatic properties, MIG structures enable innovative semiconductor structures like double-gate and *Gate-All-Around* vertically-stacked Silicon NWFETs, which are regarded as the evolution of FinFETs due to their improved control [3]. The unique feature of these devices is their capability of being polarized electrostatically through a terminal, called the Polarity Gate (PG), (see Fig. 1(b)) which allows the users to dynamically select between the n- and p-type characteristics. The ambipolar behavior of these devices, traditionally suppressed by processing steps [2], [3]), is of high interest for logic design. Vertically-stacked silicon NWFETs were first employed to build a reconfigurable logic cell [4], and later used to define a static XOR intensive logic family [5] with improved compactness compared to standard CMOS transistors.

Similarly, interest is growing for new nanowire transistors where numerous nanowire FETs are connected in parallel between drain and source in nanoarray disposition [6], [7].

In particular, nanowire arrays (see Fig. 1(c)) [8]–[10] are organized in matrices [11], which allow the creation of active

nanodevices (diodes and FETs) in their crosspoints [12]. These structures combine high compactness with good performances and, therefore, are extremely promising in terms of parallel computation capabilities. NanoASICs designs indeed have been indicated as a valid way to reach denser designs with better fabric exploitation and efficient cascading of circuits with respect to general-purpose programmable fabrics [13]–[15]. Narayanan *et al.* [16], [17] proposed these structures for an optimal deployment of massively parallel architectures in specific applications, like cellular neural networks or image processors.

Due to their promising circuit impacts, designers are in need for analytical descriptions of MIG performances. Recent literature presents several compact models [1], [18]–[24] able to describe the electrical behavior of multi-gate transistors. Nevertheless, analyzing and verifying the behavior of circuits based on a large number devices of this kind is still hardly doable due to the computation complexity and the lack of a proper support of the gate independence in the existing models [6].

This work aims to meet the need of compact models for MIG devices, by building the proposed model on-top of the vast body of knowledge developed for multi-gate devices. The study of a MIG is performed by viewing it as a series of MG devices. Our method consists of estimating the charge densities and voltages at the interface between the different sections with successive approximations. Models, available in literature are used to describe the internal behavior of the different sections.

The proposed methodology (i) is capable to describe structures with MIG devices in series. Potentials and current inside the structure are computed with few algorithmic steps; (ii) is based on existing multi-gate single-device compact models to describe each section separately. This modularity also makes it suitable for analysis in circuit simulators; and (iii) is completely general and independent from the compact models chosen for a given section and from the number and topology of devices.

Choosing [25] as charge-based model, we apply the proposed methodology to MIG structures, composed of two and three sections, and show its accuracy and computation efficiency. Experimental validation is performed by applying the method to a multi-independent-gate nanowire FET structure. The method is proved to validly describe devices with channel lengths larger than 50 nm and radius larger than 5 nm. In this geometrical parameter range, drift-diffusion transport is dominant. Comparisons of the proposed approach are done with respect to an exact numerical solution and to data from software TCAD Atlas, and reveal a good agreement. Worst case relative errors lower than 4% and 10% have been found for potentials and current, respectively. It is also computationally efficient: times of hundreds of microseconds (in an interpreted language) shown to be necessary for current computations with respect to hundreds of milliseconds necessary for exact numerical solutions implemented in highly optimized code. Furthermore, the computation time is linearly increasing with the number of cascaded devices, and maintains a very good accuracy (3%).

The paper is organized as follows. Section II presents background of the work. Section III presents an overall description of the device structure considered by the proposed methodology. Section IV describes the method itself and analyzes the associated physical expressions. Section V extends the method to more particular structures and includes a model for quantum-mechanical and SCE while Section VI compares the results with data from a commercial TCAD simulator and comments on the computational time. Finally, Section VII concludes the paper.

II. BACKGROUND

This section deals with the structure of multiple-independent-gate field effect transistors and some possible realizations, as well as with compact models for multi-gate devices, which are exploited in the present work.

A. Multiple-Independent-Gate Field Effect Transistors

In Fig. 1(a), an idealized version of the general structure of a MIG device with N sections is shown. Such a device consists of two pillars, namely the source and drain contacts, and a variable number of sections in between. In the figure, the sections, labeled S_1 to S_N, are all-gated channels. The space between gates can also be considered as a section. The support for this kind of section is provided in Section V-B. Two specific examples of application using MIG FETs are given in Fig. 1(b) and (c).

In Fig. 1(b), a GAA vertically stacked silicon nanowire FET is shown. Such transistor structure shows promises from a circuit perspective. In fact, by exploiting dynamic polarity control, reconfigurable logic gates [27] can be implemented with these devices. Fundamental logic circuits have also been demonstrated in [28]. This device can be seen as different MIG structures connected in parallel. Should the distance between gated sections be relevant, those parts could be modeled more correctly as gateless sections, that can be treated as well by the proposed methodology.

In Fig. 1(c), a schematic representation of a GAA silicon nanowire array is shown. This kind of structure, declined in different architectures [29], [30], seems of particular interest for massively parallel architectures [6]. Nanowires on the top layer bias the transistors on the bottom one: resulting current flows through the sections. In this case too, there can be sequences of gated and gateless sections. This necessity is even more relevant in this case because of the fabric properties themselves.

B. Multi-Gate Device Models

In this work, we rely on existing models for MG devices to describe the different sections of MIGs.

The models in [18] and [19] are two interesting descriptions of DG MOSFETS which derive expressions for mobile charge densities and current along the channel in long-channel devices. In [19], a description of SCE in subthreshold region, including *Drain Induced Barrier Lowering* (DIBL), sub-threshold swing and mobility degradation[1], enters into the expressions of charge and current. SCE are also a subject of [20] while quantum effects (carrier quantization) are treated and included in the models presented in [21]–[24]. Given the structural similarities between DG MOSFET and FinFET, several models for the latter are directly derived from the models for the former (if the top gate is sufficiently high to neglect the edge effects).
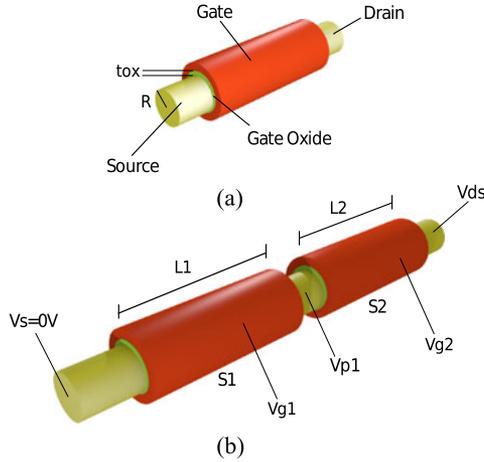
Fig. 2.   GAA Single-Gate MOSFET and a two-section structure.

In particular, Tang *et al.* [37] exploits the results of [18] to derive a model for FinFETs including drain saturation voltage and quantum-mechanical effects (QME). However, Smit *et al.* [32] describes a PSP-based compact model for FinFETs which, taking advantage of the similarities of its hierarchical structure with PSP model, is particularly suitable for circuit simulations.

Compact models for gate-all-around MOSFETs, reported in [33] and [34], present expressions for charge and current including fitting parameters to increase accuracy. The study of SCE in GAA MOSFETs in [35] lead to analytical expressions for threshold voltage, subthreshold swing and channel length modulation. Another model presented in [25] has the main advantage of being easily adapted and applied to double-gate MOSFETs and FinFETs. Its validity extends to devices with channel lengths larger than 50 nm in the regime of drift-diffusion transport. This model was used as the basis for the implementation of the methodology presented in what follows, for each of the sections, and endowed with a semi-empirical description of quantum-mechanical and SCE.

III. Structure Definition and Objectives

To apply the proposed methodology, the device is divided into a series of slices (S_i) for which an electrical model is available. The overall structure is thus decomposed into a series of sections and the study is brought back to the analysis of simpler parts. In the case of Fig. 1(a), for example, a single slice is represented by a single-gate GAA MOSFET (see Fig. 2(a)). The constitutive sections don't need to be identical or to share the same parameters (they can lack a gate or differ in length). In Section V, we will show, as an illustrative case, how to modify the procedure when gateless sections are present and the silicon channel of the device is uniformly doped.

In the proposed method, the electrical behavior of the single slice (hereinafter section) is supposed to be known and expressed through a model. This allows the current flowing in it to be calculated with a formula which, for GAA MOSFETs, has the form:

$$I_{DS} = \mu \frac{2\pi R}{L} \int_0^{V_{DS}} Q(V)\, dV \qquad (1)$$

Algorithm 1 Procedure for two sections

1: **procedure**
2:      Estimate Q_{s2} with $Q_{s2,in}$ ▷ from (11)
3:      Calculate V_{p1} ▷ from (12)
4:      **repeat**
5:          Calculate Q_{d1} ▷ from (13)
6:          Calculate I_{DS1} ▷ from (15)
7:          Calculate Q_{s2} ▷ from (16)
8:          Calculate V_{p1} ▷ from (17)
9:      **until** $\|V_{p1} - V_{p1@previousiteration}\| < \epsilon$
10:     **return** V_{p1}, I_{DS1}
11: **end procedure**

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where μ is the mobility of carriers, L is the length of the section, R its radius, $Q(V)$ and V the density charge and the potential along the channel, respectively. Between the drain and source terminals, a potential V_{DS} is applied. The drain current of any single section S_i is then function only of the charge densities at its source and drain ends and can be thus computed independently provided that the potentials V_{Di} and V_{Si} are known.

For the entire structure of Fig. 1, the objective is to analyze the voltages and current along the device with no constraint on its parameters: the lengths of the sections L_1, L_2, L_3, the applied voltages to the gates V_{g1}, V_{g2}, V_{g3}, the radius of the nanowire R and the oxide thickness t_{ox}.

The following hypothesis are necessary: no voltage drop occurs across the contacts between two adjacent sections S_i, S_{i+1}; the current flowing in each section is the same ($I_{DS_i} = I_{DS_{i+1}}$). The fundamental ideas behind the proposed methodology will be outlined in the following section.

IV. The Core of the Multi-Gate Device Model

This section presents the method for calculating the voltages and currents along a structure constituted by only two physical sections in order to show the main steps in a simple case.

A. Generalities

Algorithm 1 presents the steps to follow for the analysis of a two-section structure when the charge model in [25] is adopted to describe each section. This scheme is in principle almost independent of the employed charge-based model. A different choice of model would imply slight modifications in the overall method, basically requiring to solve the equations (for current, charge, etc.) outlined in Section IV-C for the new expressions. The considered two-section device is depicted in Fig. 2(b). Its electrical behavior is exhaustively described by V_s and V_d, the potentials at its source and drain terminals, V_{p1} the potential at the interface between the sections, I_{DS_i} the current along the section S_i and Q_{si}, Q_{di} the charge densities at source and drain, respectively. The method consists of estimating the charge densities in the structure and then of calculating the potentials and currents with successive approximations. A traditional approach in determining charge and current would proceed by reducing the number of variables in the equations. However, the strongly non-linear equations to solve do not usually admit closed-form solutions and require numerical solutions. Here, we introduce a

procedure that allows us to accurately estimate the potential V_{p1} after few mathematical steps, that will provide the basis to the calculation of the current. All the steps are discussed in details in the following section.

B. Discussion About Convergence

The introduced relaxation method allows us to compute the solution of a non-linear system starting from an initial estimate. Its value is then gradually refined by applying repeatedly an operator until the method converges to a sufficient accuracy. In our case, we refine the value of the intermediate potential V_{p1}. The refinement process can be described, such that an operator $\hat{O}$ is applied to V_{p1} at step m in order to obtain its value at step $m + 1$:

$$V_{p1}(m + 1) = \hat{O}V_{p1}(m) \tag{2}$$

This procedure is iterated until the solution is sufficiently accurate, or equivalently until the error between two successive approximations becomes smaller then an arbitrary threshold ϵ:

$$Err(m) := \|V_{p1}(m + 1) - V_{p1}(m)\| < \epsilon \tag{3}$$

This condition can be rewritten in terms of the operator $\hat{O}$, as:

$$
\begin{aligned}
Err(m) &= \|\hat{O}V_{p1}(m) - V_{p1}(m)\| = \|(\hat{O} - \mathbf{1})V_{p1}(m)\| \\
&= \|(\hat{O} - \mathbf{1})\hat{O}V_{p1}(m - 1)\| \\
&= \|\hat{O}(\hat{O} - \mathbf{1})V_{p1}(m - 1) + \hat{K}V_{p1}(m - 1)\| \\
&\le \|\hat{O}\|Err(m - 1) + \|\hat{K}\|\|V_{p1}(m - 1)\|
\end{aligned}
\tag{4}
$$

In (4), we expressed the error at step m as a function of the error at the preceding step and we introduced the non-linear operator $\hat{K} := [\hat{O}, \hat{O} - \mathbf{1}]$ defined as the commutator of the two operators in brackets, with $\mathbf{1}$ is the identity operator. At this point, a formal analysis would be required to validate the convergence of the error. However, such formal proof is difficult due to the strong non-linearity of the operators involved, as highlighted in the following sections. Moreover, the nature itself of the operator $\hat{O}$ depends on several physical parameters (channel lengths, gate voltages, . . .) which can vary over a large physical domain, thus making the analytical treatment difficult. Hence, a general proof for the gradual reduction of the error will not be proposed here. We resort, instead, to present a heuristic reasoning which justifies the convergence of the approach. In the considered device structure, the currents flowing through the different sections are the same, namely $I_{DS1}(V_{p1}(m)) = I_{DS2}(V_{p1}(m))$. According to the device physics, the two currents are continuous functions of V_{p1}, respectively, monotonically increasing and decreasing. The value of $V_{p1}(m + 1)$ is computed by evaluating one of the members of the equation and solving the resulting expression for a new value of V_{p1}. If the value of V_{p1} used as an estimate is larger than its exact solution, then the next value $V_{p1}(m + 1)$ will be smaller than the exact solution since only a smaller potential allow the same current to flow through the devices. The same consideration holds if the estimate of V_{p1} is larger than the exact solution. Thus, the sequence of values of V_{p1} are alternatively larger and smaller with respect to the exact

value V_{p0}. If the initial difference between the initial guess and the exact solution is not too large, the method will converge to the exact solution in most cases. For the initial value adopted in the paper, convergence has been verified by extensive simulation for a large variety of parameters' choice. In case of missed convergence, a different initial guess can be used.

C. Closed Form Expressions Derivation

The introduced procedure requires to solve closed form expression a certain number of times. This number depends on the accuracy to be met: for greater accuracy, a better estimate of Q_{s2} is required. Results will show that this number is usually very small and dependent on the number of sections. In what follows, the equation for the potential has been written for intrinsic channel. In Section V-C, the derivation for a doped channel will be shown.

According to the hypothesis that the current flowing in each section is the same, we start by imposing the condition $I_{DS1} = I_{DS2}$. By referring to the formula for the current from the model in [25], this is equivalent to

$$
\begin{aligned}
&\mu \frac{2\pi R}{L_1} \left[2\frac{kT}{q}(Q_{s1} - Q_{d1}) + \frac{Q_{s1}^2 - Q_{d1}^2}{2C_{OX}} \right. \\
&\left. + \frac{kT}{q}Q_0 \log\left[\frac{Q_{d1} + Q_0}{Q_{S1} + Q_0}\right] \right] \\
&= \mu \frac{2\pi R}{L_2} \left[2\frac{kT}{q}(Q_{s2} - Q_{d2}) + \frac{Q_{s2}^2 - Q_{d2}^2}{2C_{OX}} \right. \\
&\left. + \frac{kT}{q}Q_0 \log\left[\frac{Q_{d2} + Q_0}{Q_{S2} + Q_0}\right] \right]
\end{aligned}
\tag{5}
$$

where kT/q (henceforth, V_{th}) is the volt-equivalent of temperature, where Boltzmann's constant k must be in units of J/K and the temperature T is in units of K. The unit of charge q is $1.6022 \times 10^{-19}C$. Q_0 is a constant with the dimension of a charge, whom value is $(4\epsilon_{S_i}/R) \times (kT/q)$, and C_{OX} is the oxide capacitance of a cylindrical capacitor given by $\epsilon_{OX}/(R\log(1 + t_{ox}/R))$. Q_{di} and Q_{si} relate to the potentials at the source and drain ends by the charge-control equation (6), where $V = V_{si}$ and $V = V_{di}$ for the two cases Q_{di} and Q_{si} respectively:

$$
\begin{aligned}
&V_{GSi} - \Delta\varphi - V - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) = \frac{Q}{C_{OX}} \\
&+ \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q + Q_0}{Q_0}\right)
\end{aligned}
\tag{6}
$$

where $\Delta\varphi$ is the difference between gate metal and silicon working functions. No analytical solution for the charge densities and V_{p1} can be found from (5) and (6). However, we can actually realize that, in our problem, we have:

$$V_{s1} < V_{d1} \equiv V_{p1} \tag{7}$$

$$V_{s2} \equiv V_{p1} < V_{DS} \tag{8}$$

These inequalities express the fact that, assuming that the potential on the source of the structure is zero ($V_{s1} = 0V$) and

that a positive voltage V_{DS} is imposed to the whole structure (a negative V_{DS} does not imply modifications due to the symmetry), a positive voltage drop occurs on each of the two inner regions between their drain and source terminals. This is to say that the drain potential is larger than the source potential on both inner devices. These considerations made, the monotonic trend of charge with voltage revealed by (6) yields consequently:

$$Q_{d1} < Q_{s1} \tag{9}$$

$$Q_{d2} < Q_{s2} \tag{10}$$

As a first approximation, we can neglect Q_{d1} and Q_{d2} in (5) in order to find an initial estimation of Q_{s2} and solve the resulting equation (11). We stress here that this is only an initial estimate for the charge densities at the drain contacts, which will be corrected by successive iterations of the procedure. The obtained approximate initial value of Q_{s2} is called $Q_{s2,\mathrm{in}}$:

$$\frac{1}{2C_{OX}L_2}Q_{s2,in}^2 + \frac{2V_{th}}{L_2}Q_{s2,in}$$
$$-\frac{Q_{s1}^2}{2C_{OX}L_1} - \frac{2V_{th}Q_{s1}}{L_1} = 0 \tag{11}$$

With the obtention of $Q_{s2,\mathrm{in}}$, V_{p1} is easily found by directly solving the charge-control equation (6) as:

$$V_{G2} - \Delta\varphi - V_{p1} - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) = \frac{Q_{s2,\mathrm{in}}}{C_{\mathrm{OX}}}$$
$$+ \frac{kT}{q}\log\left(\frac{Q_{s2,\mathrm{in}}}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q_{s2,\mathrm{in}} + Q_0}{Q_0}\right) \tag{12}$$

This value of V_{p1} is, however, only a rough estimate whose accuracy needs to be improved. We proceed then and compute Q_{d1} through

$$Q_{d1} = C_{OX}\left(-\frac{2C_{\mathrm{OX}}V_{\mathrm{th}}^2}{Q_0} + \sqrt{\left(\frac{2C_{\mathrm{OX}}V_{\mathrm{th}}^2}{Q_0}\right)^2 + B}\right) \tag{13}$$

$$B = 4V_{\mathrm{th}}^2\log^2\left(1 + \exp\left(\frac{V_{\mathrm{GS1}} - V_T + \Delta V_T - V_{p1}}{2V_{\mathrm{th}}}\right)\right) \tag{14}$$

These relations, taken from [26], give reasonably accurate solutions to (6). The parameters non explicit here, such as V_T, ΔV_T or V_0, can be found in [26]. In particular, V_T corresponds to the threshold voltage and plays a crucial role in describing the quantum mechanical and SCE in the device, as it will be described in the next section. From Q_{d1}, the current I_{DS1} in the first section is given by

$$I_{\mathrm{DS1}} = \mu\frac{2\pi R}{L_1}\left[2\frac{kT}{q}(Q_{s1} - Q_{d1}) + \frac{Q_{s1}^2 - Q_{d1}^2}{2C_{\mathrm{OX}}}\right.$$
$$\left. + \frac{kT}{q}Q_0\log\left[\frac{Q_{d1} + Q_0}{Q_{s1} + Q_0}\right]\right] \tag{15}$$

The current must be equal in the two sections. Imposing again the condition (5), we now get a new equation for Q_{s2}

$$\frac{1}{2C_{\mathrm{OX}}}Q_{s2}^2 + 2V_{\mathrm{th}}Q_{s2} - \frac{I_{\mathrm{ds1}}L_2}{2\pi\mu R}\frac{Q_{s1}^2}{2C_{\mathrm{OX}}L_1} - 2V_{\mathrm{th}}Q_{d2}$$
$$-\frac{Q_{d2}^2}{2C_{\mathrm{OX}}} + V_{\mathrm{th}}Q_0\log\left(\frac{Q_{d2}^2 + Q_0}{Q_{s2,\mathrm{in}} + Q_0}\right) = 0 \tag{16}$$

Finally, a more accurate estimate of V_{p1} can be found by substituting this new value in

$$V_p = V_{G2} - \Delta\varphi - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) - \frac{Q_{s2}}{C_{\mathrm{ox}}}$$
$$-\frac{kT}{q}\log\left(\frac{Q_{S2}}{Q_0}\right) - \frac{kT}{q}\log\left(\frac{Q_{s2} + Q_0}{Q_0}\right). \tag{17}$$

The introduced procedure allows us to describe voltages and currents in a structure consisting of two different sections by means of a limited number of computational steps. It does not require numerical solutions of nonlinear equations, which usually represent a consequent overhead on the computational efficiency and time requirements. A fundamental feature of the proposed method is its iterative nature. Steps can be repeated in sequence in order to meet the accuracy requirements (see Algorithm 1). Yet, good accuracy of data after only one iteration (1IT) has been verified for two-sections devices (two iterations are necessary for three-sections). This will be shown in next sections.

D. QME and SCE

When the dimensions of the sections enter the nanometer range ($<10\,\mathrm{nm}$), QME start affecting the behavior of the device. Consequently, the charge density should be computed taking into account the quantum potential confinement inside the channel. Following [36] and [37], this effect produces a bandgap opening which can be described with a semi-empirical shift of the threshold voltage V_T in the compact model on which our procedure relies. The change of V_T is:

$$\Delta V_{T(\mathrm{QME})} = \frac{\Delta E_{\mathrm{qm}}}{q}$$

where ΔE_{qm} is the shift of the conduction band due to potential confinement. Its actual expression depends on the geometry of the sections and on the assumption made on the shape of the confining potential.

Analogously, SCE and DIBL are modeled with an extra shift in the threshold voltage given by:

$$\Delta V_T = -2\gamma_{\mathrm{SCE}}(V_{\mathrm{To}} - V) + \gamma_{\mathrm{DIBL}}V_{\mathrm{ds}}$$

where V_{To} is the long-channel threshold voltage while the parameters γ_{SCE} and γ_{DIBL} are determined trough extrapolation from simulation results.

V. GENERALIZATIONS OF THE METHOD TO MORE COMPLEX STRUCTURES

The method illustrated in the preceding section can be extended to more complex structures. Indeed, our method presents

Fig. 3. N-section Structure.

Algorithm 2 Procedure for three sections

1: **procedure**
2:     Estimate Q_{s2} and Q_{s3} with $Q_{s2,\text{in}}$ and $Q_{s3,\text{in}}$
3:   ▷ from (18)
4:     **repeat**
5:         Calculate Q_{d1} and Q_{d2} ▷ from (13)
6:         Calculate $I_{\text{DS}1}$, $I_{\text{DS}2}$ and $I_{\text{DS}3}$ ▷ from (20)
7:         Calculate Q_{s2} and Q_{s3} ▷ from (21)
8:         Calculate V_{p1} and V_{p2} ▷ from (22)
9:     **until** Accuracy not met
10:     **return** $V_{p1}, V_{p2}, I_{\text{DS}1}$
11: **end procedure**

Fig. 4. Structure with a gateless section.

features which make it useful to describe a wide variety of problems. The most important is its independence on the model adopted for describing each section. In the following, we describe how to modify it, while maintaining the same model in each section, when the number of connected devices is arbitrary (see section A), when devices without gate contact are considered (see section B) and when doped-channel sections are present in the structure (see section C). The whole procedure will be illustrated and schematized. Finally, some considerations are made about the possibility of adapting the method also to devices with different geometry with respect to GAA MOSFETs (subject. D).

A. Arbitrary Number of Gates

The method enables an efficient description of structures with an arbitrary number of gates as illustrated in Fig. 3. By referring to the model proposed in [25], the extension of the algorithm proposed to this general case is almost straightforward (see Algorithm 2). By supposing that the current flowing in each of the n devices is the same, we impose that for $i = 2, \ldots, n$:

$$I_{\text{DS}i} = I_{\text{DS}1}.$$

The choice of current $I_{\text{DS}1}$ in the above equation is arbitrary and any other current in the device could be adopted. Under the initial assumption $Q_{\text{di}} << Q_{\text{si}}$, this leads to the following equation to a first estimate $Q_{\text{si,in}}$ of Q_{si}:

$$\frac{1}{2C_{\text{OX}}L_i}Q_{\text{si,in}}^2 + \frac{2V_{\text{th}}}{L_i}Q_{\text{si,in}} - \frac{Q_{s1}^2}{2C_{\text{OX}}L_1} - \frac{2V_{\text{th}}Q_{s1}}{L_1} = 0. \tag{18}$$

The voltages at the interface of adjacent sections V_{pi} can then be described with the charge-control equation:

$$V_{Gi} - \Delta\varphi - V_{\text{pi}} - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right)$$
$$= \frac{Q_{\text{si,in}}}{C_{\text{OX}}} + \frac{kT}{q}\log\left(\frac{Q_{\text{si,in}}}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q_{\text{si,in}} + Q_0}{Q_0}\right). \tag{19}$$

The charge densities at the drain, instead, are given by (13) and (14). The current comes from:

$$I_{\text{DS}i} = \mu\frac{2\pi R}{L_i}\left[2\frac{kT}{q}(Q_{\text{si}} - Q_{\text{di}}) + \frac{Q_{\text{si}}^2 - Q_{\text{di}}^2}{2C_{\text{OX}}}\right.$$
$$\left. + \frac{kT}{q}Q_0\log\left[\frac{Q_{\text{di}} + Q_0}{Q_{\text{si}} + Q_0}\right]\right] \tag{20}$$

with $i = 1, .., n-1$. Given the currents, the charge densities at source ends Q_{si} and the values for V_{pi} are obtained from the following equations, respectively:

$$\frac{1}{2C_{\text{OX}}}Q_{\text{si}}^2 + 2V_{\text{th}}Q_{\text{si}} - \frac{I_{\text{DS}1}L_i}{2\pi\mu R}\frac{Q_{s1}^2}{2C_{\text{OX}}L_1} - 2V_{\text{th}}Q_{\text{di}}$$
$$- \frac{Q_{\text{di}}^2}{2C_{\text{OX}}} + V_{\text{th}}Q_0\log\left(\frac{Q_{\text{di}}^2 + Q_0}{Q_{\text{si,in}} + Q_0}\right) = 0 \tag{21}$$

$$V_{\text{pi}} = V_{G(i+1)} - \Delta\varphi - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) - \frac{Q_{s(i+1)}}{C_{\text{ox}}}$$
$$- \frac{kT}{q}\log\left(\frac{Q_{S(i+1)}}{Q_0}\right) - \frac{kT}{q}\log\left(\frac{Q_{s(i+1)} + Q_0}{Q_0}\right). \tag{22}$$

The aforementioned procedure is summarized in Algorithm 2, for an illustrative number of sections equal to three. Starting from an estimate of Q_{s2} and Q_{s3}, the procedure iterates four closed form calculations to attain voltage (V_{p1}, V_{p2}) and current (I_{ds}) results.

B. Gateless Sections

As stated in Section II-A, not all parts of complex devices are gated. Fig. 4 shows an example of a structure where an inner section is not wrapped with a gate. The problem of determining

Algorithm 3 Procedure for structures with gateless sections

1: **procedure**
2:     Estimate Q_{s2} with $Q_{s2,\text{in}}$ ▷ from (11)
3:     Calculate V_{p2} ▷ from (22)
4:     **repeat**
5:         Calculate Q_{d2} ▷ from (13)
6:         Calculate I_{DS2} ▷ from (20)
7:         Calculate V_{p1} ▷ from (23)
8:         Calculate Q_{d1} ▷ from (13)
9:         Calculate I_{DS1} and Q_{s2} ▷ from (20) and (16)
10:         Calculate V_{p2} ▷ from (22)
11:     **until** Accuracy not met
12:     **return** $V_{p1}, V_{p2}, I_{\text{DS1}}$
13: **end procedure**

the potential along the structure and the resulting current can be addressed easily through the method already discussed with only slight modifications. Let us define the parameters related to a gateless section: L_R the length of the section, N_D its doping level and R its radius. No control is actually exerted externally on the charge density along the gateless section. In the context of Fig. 4, where the inner part is gateless, this leads to a simple resistive behavior of the slice:

$$V_{p1} = V_{p2} - RI_{\text{DS2}} \tag{23}$$

where the resistance of the channel is related to the channel length and doping level by:

$$R = \rho \frac{L_R}{A} = \frac{1}{q\mu N_D} \frac{L_R}{2\pi R^2} \tag{24}$$

where A is the section of the channel, L_R its length and ρ the channel resistivity. By introduction of this new equation into the previous methodology, one gets a simple algorithm to derive potentials V_{p1}, V_{p2} and current I_{DS}. Algorithm 3 describes schematically the whole iterative process, that is again very close to the one presented in Section IV-C for a two-sections structure. The main difference between the two is given by (23) which is now adopted to compute V_{p1} instead of (22).

C. Doped Channel Sections

We now adapt the general procedure to doped channel sections. The structure is formally identical to the one shown in Fig. 3 and the change in doping level can be described in the charge-model of a single section. By referring to the model in [25], it suffices to reanalyze the entire procedure leading to the final formulas for current and charge densities along the channel and to modify the inputs of the problem. The main difference which arises in the model's deduction is a new solution of the Poisson equation for the potential in a perpendicular direction to the channel length. If N_A is defined to be the channel doping (all the remaining quantities do not vary), the solution becomes, after a few approximations not reproduced here for the sake of brevity:

$$\psi(r) = -\delta \frac{N_A}{4n_i} \frac{kT}{q} R^2 + \delta \frac{N_A}{4n_i} \frac{kT}{q} r^2 + V$$

$$+ \frac{kT}{q} \log\left(\frac{-8B}{\delta(1 + Br^2)^2}\right). \tag{25}$$

This is the first step to move forward a charge-control equation. By imposing the appropriate boundary condition at the channel-oxide interface [25], one finally arrives to (26) relating the charge density to the potential along the channel:

$$V_{\text{GS}} - \Delta\varphi - V - \frac{kT}{q} \log\left(\frac{8e^{\alpha/(V_t C_{\text{ox}})}}{\delta \frac{N_A}{n_i} R^2}\right)$$

$$= \frac{Q - \alpha}{C_{\text{OX}}} + \frac{kT}{q} \log\left(\frac{Q - \alpha}{Q_0}\right) + \frac{kT}{q} \log\left(\frac{Q - \alpha + Q_0}{Q_0}\right) \tag{26}$$

where the only new quantity is $\alpha = \varepsilon_{Si} \frac{N_A}{2n_i} \frac{kT}{q} R$, a parameter related to the device structure and obviously to its channel doping. By noticing the numerous similarities between this formula and (6), it is possible to apply slight substitutions to (26) in order to fall back on the one previously discussed. The change of variables to be accomplished is:

$$Q \leftarrow Q^* = Q - \alpha \tag{27}$$

$$\delta \leftarrow \delta^* = \frac{e^{\alpha/(C_{\text{ox}} V_t)}}{N_A/n_i}. \tag{28}$$

This small changes make it easy and effortless to include such a modification in the general frame of the method for the solution of structures with doped channels.

D. Sections With Different Geometry

The proposed method also applies to problems where devices with a different geometry are involved. Again, this is performed by substituting the employed models in the different sections. An interesting case is the cascade of FinFETs, where the models from [18] and [37] can be effortlessly adopted in applying the methodology discussed here, thanks to their evident similarities with [25] for GAA MOSFETs.

VI. VERIFICATION AND RESULTS

This section focuses on techniques and procedures used to implement and verify the results of the proposed methodology. Tests were performed for devices of growing complexity (see Sections VI-B and VI-C) and under different biasing conditions (see Section VI-D).

A. Methodology

This methodology was developed in MATLAB [38], mainly because the focus of the work, at an early stage, was accuracy and scalability and MATLAB language allows rapid prototyping. The structure considered in the experiments is shown in Fig. 3. Most of the results shown are for two and three section devices, but data are provided from experiments up to nine sections. The method was validated through an extensive experimental comparison of results with the exact numerical solution and with the output from a physics-based software. Specifically,
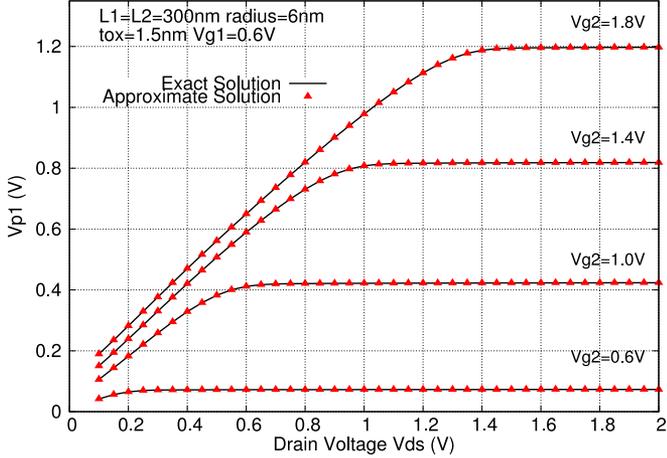
Fig. 5. Comparison of the exact solution of V_{p1} with data from the model in a two-section structure for different values of V_{g2}; in the inset a zoom of the region with low V_{ds} is shown.

Fig. 6. Comparison of the exact solution of V_{p1} with data from the model in a two-section structure for different values of L_2; region with low V_{ds} is shown in a larger scale in the right box of the figure.

we have computed the potential at the interface between different sections in various multiple-gate structures as a function of the applied voltages and structural parameters. Data were then compared with two set of results calculated by TCAD software Atlas including the computation of QME [39]. The first set was obtained numerically for the entire structure, while the second one considers the values obtained just for potentials (V_{p1}, V_{p2}) from the numerical simulation. This approach was chosen to better assess the validity of the algorithm that estimates potentials into the structure and the relative importance of this step into the overall procedure. Simulations in Atlas were performed under the assumption of a Boltzmann distribution for carriers in the silicon channel and of highly doped contacts ($10^{23}\,\mathrm{cm}^{-3}$). The latter condition guarantees a small voltage drop across the contacts themselves. Complex structures analyzed present sections with channel radius between 5 and 10 nm while their oxide thickness is 1.5 nm. QME, and in particular the potential confinement, which are expected to play a role in the device characteristics in this range of geometrical parameters, are taken into account as described in section IV-D. Analogously, the SCE, DIBL, sub-threshold swing and mobility degradation are consistently modeled in the charge-model adopted of each section. The channel lengths of simulated devices range from 60 nm to 300 nm. These dimensions of channel length are, instead, sufficiently high for ballistic transport not to take place and for coherent transport not to become evident. Hence, diffusive regime of transport is assumed.

B. Two-Section Structure

Fig. 5 shows the potential V_{p1} in a two-section device for different values of gate voltage V_{g2} with varying drain-source voltage. Each section is 300 nm long, has radius $R = 6$ nm and oxide thickness $t_{\mathrm{ox}} = 1.5$ nm. The gate voltage applied to the first section is $V_{g1} = 0.6$ V. The graph reveals that our numerical procedure, after only 1IT step, gives accurate outputs if compared with the exact numerical solution. Indeed, maximum relative errors of 1.6% are obtained after 1IT. Thus, for a two-section structure, only 1IT is actually sufficient to get accurate
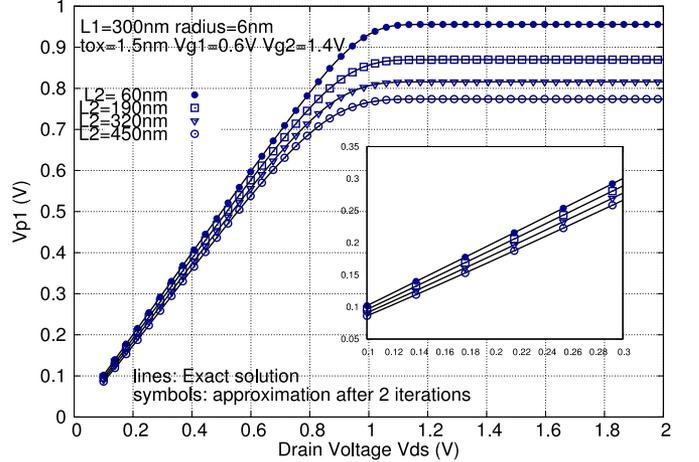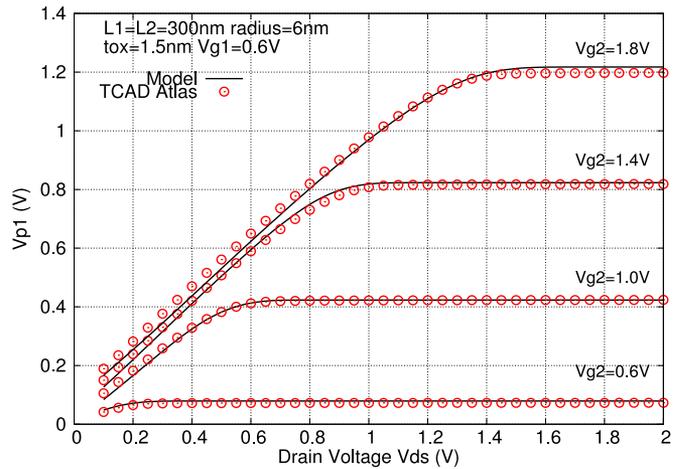
Fig. 7. Comparison of the exact solution of V_{p1} with output from TCAD Atlas: two-section structure for different values of V_{g2}.

results. This is also true if we let other parameters vary in the same structure, such as in Fig. 6 where the length of section L_2 is varied between 60 nm and 450 nm while L_1 is kept at $L_1 = 300$ nm. We compared also the results with the simulation data from TCAD Atlas.

Figs. 7 and 8 present the data from the simulator corresponding to the plots of Figs. 5 and 6, respectively. Coherence of values is observable. Worst relative errors of a few percent are obtained for relatively large V_{DS} polarization combined with shorter channel. For longer channels, relative errors well below 1% are obtained over the full biasing range.

C. Three-Section Structure

While augmenting the complexity of the structure by cascading more sections, the method preserves its validity and accuracy. This is shown for a three-section device in Fig. 9, where the potentials at the interface between the two sections are represented as a function of the total voltage applied. Data
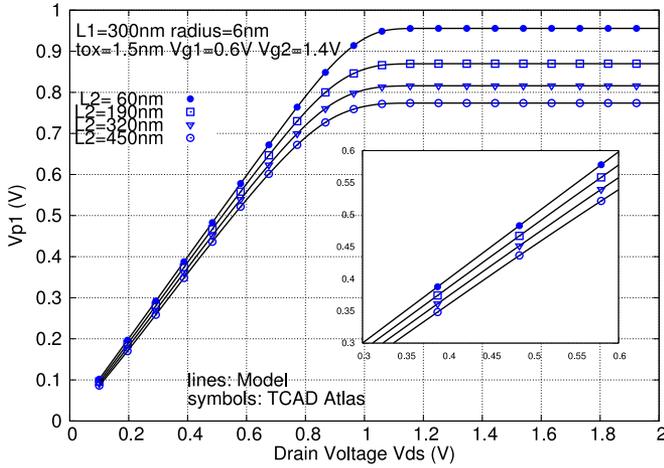
Fig. 8.   Comparison of the exact solution of V_{p1} with output from TCAD Atlas in a two-section structure for different values of L_2.
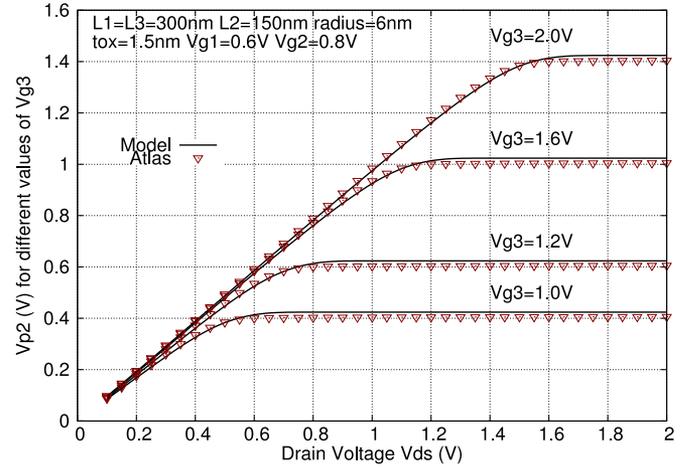
Fig. 10.   Comparison of the exact solution of V_{p2} with data from TCAD Atlas in a three-section structure for different values of V_{g3}.
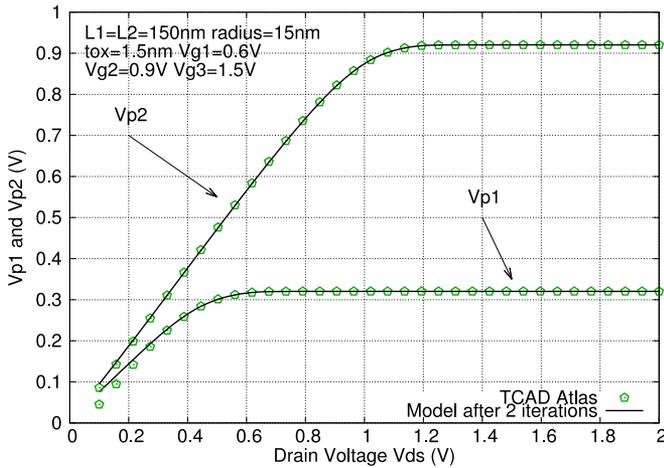
Fig. 9.   Comparison of the exact solution of V_{p1} and V_{p2} with data from the method in a three-section structure.
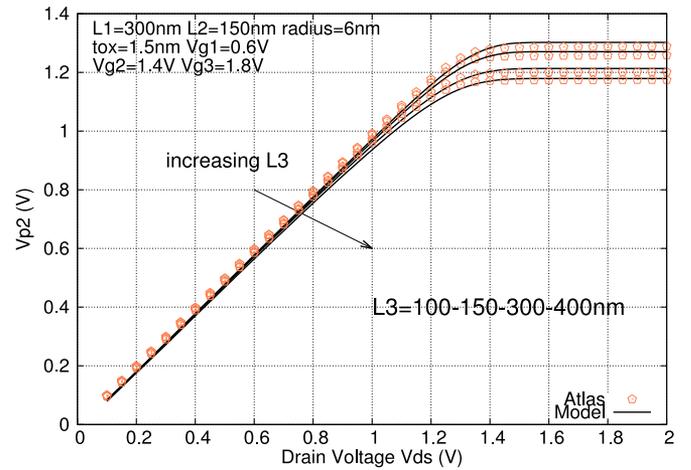
Fig. 11.   Comparison of the exact solution of V_{p2} with data from TCAD Atlas in a three-section structure for different values of L_3.

were obtained by iterating just twice the proposed method. This led to a discrepancy in results from numerical simulations that tops to a few tenth of percent across the full range of potentials considered. A direct comparison was also made with Atlas simulation outputs. Fig. 10 plots the values of V_{p2} for different V_{g3} in a structure of three sections with $L_1 = L_3 = 300$ nm, $L_2 = 150$ nm, $R = 6$ nm, $V_{g1} = 0.6$ V and $V_{g2} = 0.8$ V. Data largely agree with simulation results, with relative errors of few percent over the full biasing range (V_{g2} from 1 to 2 V), showing little sensitivity of the methodology to variations in V_{g2}.

In Fig. 11, the potential V_{p2} with varying $V_{\rm DS}$ for different values of L_3 are shown. Data from Atlas stand close to the numerical model adopted also for high voltages.

From the values of potentials obtained, the current has been estimated. Fig. 12 shows the current flowing in a three-section structure when V_{g1} and V_{g3} are kept fixed while V_{g2} is varied. Comparison with data from Atlas in linear and logarithmic scale shows good accuracy over the whole range of applied voltages. More precisely, the figure reveals how the operating region of the
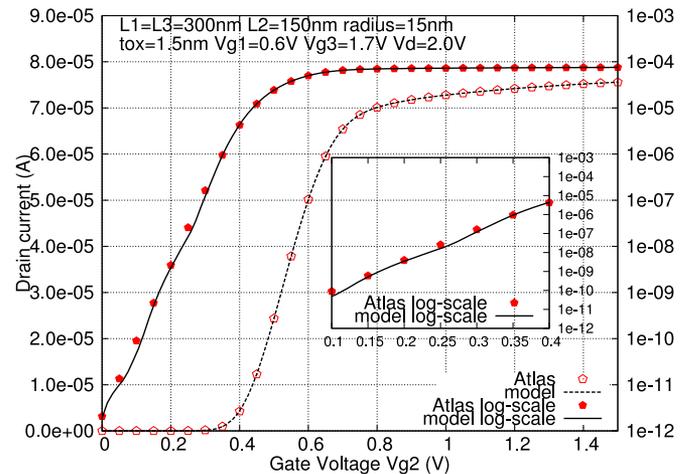
Fig. 12.   Current $I_{\rm DS}$ in a three-section structure where $V_{g1} = V_{g3}$ for different values of V_{g2}. Dotted line: current from the model in linear scale; solid line: current from the model in logarithmic scale. Points represent data from simulator Atlas in linear and logarithmic scale.
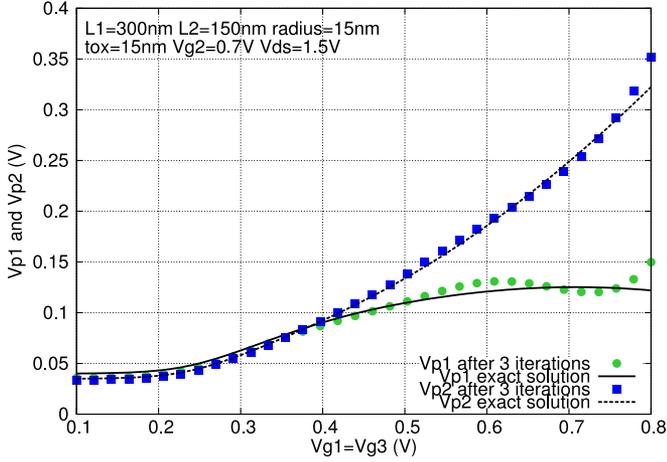
Fig. 13.   Comparison of values of V_{p1} and V_{p2} obtained from the method after three iterations with exact results in a triple structure with $V_{g1} = V_{g3}$, $V_{g2} = 0.7$ V.

Fig. 15.   Relative errors on I_{DS} in a three-section structure where $V_{g1} = V_{g3}$ for two different values of V_{g2}.

Fig. 14.   Comparison of values of V_{p1} and V_{p2} obtained from the model after three iterations with exact results in a triple structure with $V_{g1} = V_{g3}$, $V_{g2} = 1.2$ V.
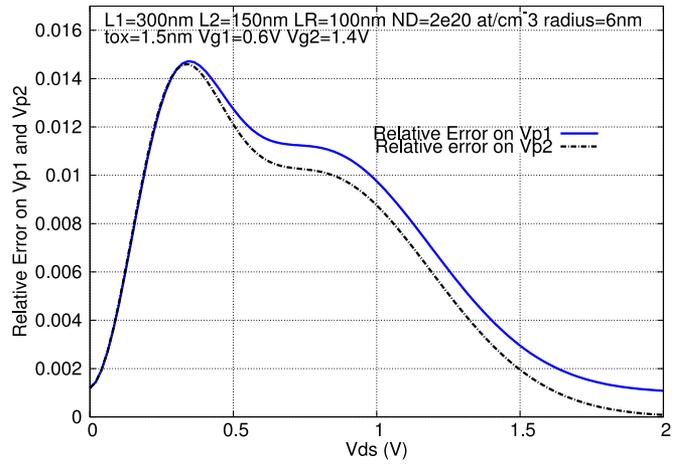
Fig. 16.   Relative errors on V_{p1} and V_{p2} in a three-section structure with a gateless section with parameters $N_D = 2 \cdot 10^{20} \text{cm}^{-3}$, $L_R = 100$ nm.

central section changes when the gate voltage applied is varied. For small values of V_{g2}, the section operates in subthreshold region since its gate voltage is lower than V_{g1}, thus limiting the overall current flowing into the device. When V_{g2} is increased over $V_{g1} = 0.6$ V, the section exits the subthreshold region and enters saturation: then the current continues to increase but with a lower growing rate.

D. Three-Section Structure With Fixed Gate Voltages at Extremes

Structures with three sections are often used to realize double-gate devices by fixing the same potential on the two lateral gates [28], thereby leading to the condition $V_{g1} = V_{g3}$. Figs. 13 and 14 show how V_{p1} and V_{p2} vary with V_{DS} when V_{g2} is kept constant and $V_{g1} = V_{g3}$. Exact numerical data and method output are represented. Using the obtained values for V_{p1} and V_{p2}, the current flowing in the series of the sections has been subsequently evaluated and compared with numerical exact. In Fig. 15, a plot of relative errors on current value is shown. In the worst case, the strongly non-linear error tops at 4%.

E. Gateless Section Structure

Finally, we present an example of data obtained for a structure with gateless section. Fig. 16 shows the relative errors of V_{p1} and V_{p2} as a function of V_{DS} with respect to the exact values of potential. A maximum error of 1.8% is obtained. This section is required to correctly model the region of multi-gate devices with uniform doping level, as detailed in Section II-A. Relative error tops for very low V_{DS}, with 0.1% at $V_{DS} = 1$ V.

F. Computation Times

A final discussion is worth doing on the timing efficiency of our model. The experiments have been performed on MIG devices made of up to nine sections under different biasing conditions, reported for each test. Some results are worth pointing out for test cases that are particularly significant. For a three section structure, relative errors on I_{DS} of less than 4% are shown in Fig. 15. From a timing perspective, current evaluation for the mentioned cases required less than 0.2 ms in an interpreted language, with given drain and gate voltages. These times result one order of magnitude shorter than computation times necessary
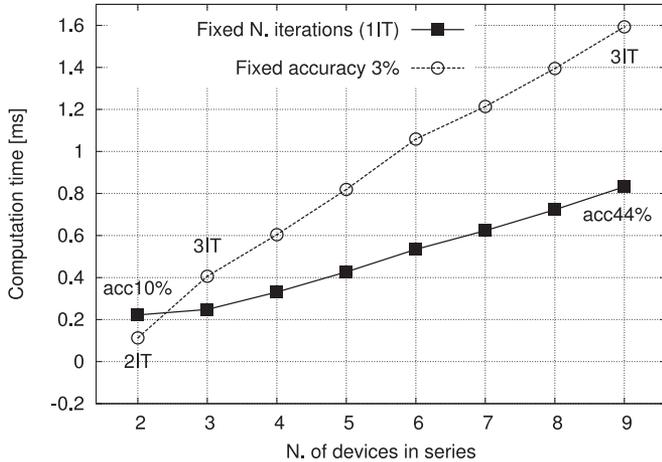
Fig. 17.   Computation times (in seconds) required to solve complex structures with different number of devices: with fixed number of iterations of our model (squares) and with the minimum number of iterations required to get an accuracy of 3% on potentials (circles).

for a numerical solution where tenths of milliseconds are necessary. The method is, therefore, computationally efficient.

Fig. 17 shows CPU times necessary to solve potentials and currents in structures with a variable number of devices under a single bias condition. Both curves reveal a linear trend with the number of devices connected. We kept the number of iterations (1IT) of the model constant along the bottom curve (squares) obtaining an overall proportionality of time and number of sections, but a variable accuracy (between acc10% to more than acc40% in the worst case). In the other case, we adopted a variable number of iterations in order to get a particular level of accuracy (acc3%). 1IT was necessary for a two-section structure, and three iterations for all the others (3IT). Still the trend remains linear and the computation times approximately doubles. Similar iterations performed using a spice engine (Eldo) required more than one order of magnitude in time. Clearly, this is not affordable in a context where thousand of devices are to be simulated in the same time.

G. Discussions

Overall, our results indicate that the proposed methodology suits the need for versatile, accurate and scalable modeling of MIG devices. Tests were performed by varying the structural aspects of devices as well as the biasing conditions (see Figs. 5–11) over large ranges of parameters (e.g., 50 to 400 nm for section length, 0 to 2 V for potentials). Versatility was also demonstrated by simulating structures made of up to nine sections, each section potentially differing from its neighborhood in different respects (length, diameter, etc.), as previously described. Efficiency was shown both in terms of computation time required and in scalability, due to the linear dependence of computation time on the number of sections, irrespectively of the targeted accuracy (see Fig. 17). In addition, note that the measured performance is underestimated, because an interpreted language has been used to implement equations to speed up development and to focus on accuracy rather than focusing on performances. Further work will be required to implement

the methodology in optimized compiled code, to attain a fair comparison with standard numerical simulators.

According to the performed analyses, and in particular those in Fig. 16, we conclude that relative errors on potentials are always below 2% in the measurement range. Results for current show analogous behavior, with only slightly degraded performance (4% maximum relative error) for a three sections structure.

Therefore, it follows that the proposed methodology is well suited to be applied in circuit simulators where efficiency and scalability are key enabling features.

VII. Conclusion

In this paper, we presented a new iteration-based analytical model suitable to analyze complex semiconductor structures with several cascaded devices. Based on the computation of charge densities and potentials along the structure, it presents a high degree of versatility: we illustrated its application to a series of two or more GAA MOSFETs. Nevertheless, no constraint actually holds on the topology and features of the sections in the structure. FinFETs-based structures can easily be analyzed through the methodology presented only with the modification of the analytical expressions for charge and currents in each section. Besides, generalizations of the method have been discussed and the inclusion of gate-less sections with description of QME and SCE has been presented.

The method has an iterative nature, although only few numerical steps are necessary to compute potentials and currents in the structure. Computational efficiency of the method is a key feature. In particular, accuracy of 3% in potentials can be obtained for up to nine sections in linear time, after just two or 3IT, without nonlinear equations to be solved numerically.

Verification has been demonstrated through extensive simulation on devices with channel lengths ranging from 50 to 450 nm and radius larger than 1 nm. The comparison of the data obtained with our model to results from commercial physics-based software reveals a good agreement. Similarly, relative errors top at 1.8% on potentials and about 4% on currents with respect to exact numerical solutions. The method is also timing efficient leading to accurate values of potentials in a shorter amount of time than a numerical method would require. Computation times of one order of magnitude shorter have been found, still maintaining the aforementioned accuracy and linear proportionality with the number of devices.

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