# On the Design of a Fault Tolerant Ripple-Carry Adder with Controllable-Polarity Transistors

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*Abstract*— **This paper first explores the effects of faults on circuits implemented with controllable-polarity transistors. We propose a new fault model that suits the characteristics of these devices, and report the results of a SPICE-based analysis of the effects of faults on the behavior of some basic gates implemented with them. Hence, we show that the considered devices are able to intrinsically tolerate a rather high number of faults. We finally exploit this property to build a robust and scalable adder whose area, performance and leakage power characteristics are improved by 15%, 18% and 12%, respectively, when compared to an equivalent FinFET solution at 22-nm technology node.**

***Keywords—Controllable-polarity Transistors, Fault model, Fault-tolerant adder***

## I. Introduction

In the recent years, many novel *Field-Effect Transistor* (FET) technologies have been proposed and evaluated in order to overcome the ultimate limits of conventional silicon-based *Integrated Circuits* (ICs). While most of them improve the structure and materials of FETs to boost their intrinsic performances, an alternative approach increases the functionality of the individual device for a constant area [1].

One of the most promising devices with enhanced functionalities is the controllable-polarity transistor. Exploiting a *dual-gate* structure, controllable-polarity transistors can be electrostatically configured to be either *n*- or *p*-type [2][3]. The functionality of such a device is logically biconditional on both gate values and enables a compact realization of XOR/MAJ-based logic functions, which are not implementable in CMOS in a compact form [4][5]. Controllable-polarity devices can be fabricated in many different technologies, from pure silicon [2][3][6] to carbon electronics [7][8]. In particular, a top-down fabrication process showing full compatibility with industrial fabrication techniques has been employed in [3] to demonstrate the feasibility of the approach. Basic logic gates exploiting the enhanced expressiveness of the technology has been demonstrated in [9], making the practical usage of this technology even closer. In addition to showing interests in the realization of compact logic elements, emerging technologies with enhanced functionalities can also introduce novel opportunities in terms of fault tolerance.

In this paper, we first perform an analysis on the effects of possible permanent faults affecting a generic controllable-polarity device and studied in details in [10]. In order to take into account the specific characteristics of the controllable-polarity devices, this analysis has to be performed at the transistor level. We propose a new fault model that takes into account the specific characteristics of these devices, extending the popular stuck-open/stuck-short fault model traditionally used at that level. Then, we analyze the behavior of circuits based on controllable-polarity devices when permanent device faults are present, and identify the conditions for their detection/masking. Results show that a high number of faults are masked, thus making this new technology particularly interesting from a reliability point of view.

Performing this analysis at the transistor level allowed us to express the behavior of each gate when any of the possible faults affecting each of its transistor arise. We use this information to forecast the behavior of more complex circuits composed out of the above gates, thereby achieving the same precision than a transistor level analysis but with a much lower computational complexity.

Based on the results of the previous analysis, we also propose in this paper a fault-tolerant ripple-carry adder architecture exploiting XOR/MAJ logic gates built entirely with controllable-polarity transistors. In order to guarantee a high degree of resiliency with respect to single and double permanent faults in every single stage, we combine the intrinsic resiliency of the controllable-polarity-based circuits with the usage of the *Triple Modular Redundancy* (TMR) architecture. Although faster solutions are often adopted to implement adders, e.g., based on the Kogge-Stone architecture [11] and its fault tolerant version [12], the TMR version of the ripple-carry adder still represents the reference to compare with, especially when the parallelism is limited and power is not a major issue (in the latter case, solutions based on reversible logic are often adopted [13]).

Experimental validation shows that the full-adder architecture we propose is able to tolerate all possible single faults and a very high percentage of the double ones. In addition, it proves that the proposed solution provides a 15%, 18% and 12% gain in area, performance and leakage power with respect to similar architectures implemented in FinFET technology at 22-nm technology node. Finally, the proposed architecture is significantly cheaper with respect to solutions based on hardening the circuit at the transistor level, such as those proposed in [14], whose area overhead 4× the unhardened circuit.

This paper is organized as follows. Section II gives some background related to controllable-polarity transistors. Section III introduces a new fault model suited to controllable-polarity devices and analyzes the conditions for its detection/masking. Section IV proposes a fault tolerant architecture for a 1-bit adder that can be exploited to build cost-effective fault-tolerant adders. Section V reports the results of a quantitative analysis of the characteristics of the proposed architecture. Finally, Section VI draws some conclusions.

## II. BACKGROUND

Transistors with controllable polarity are *Double-Independent Gate* (DIG) FETs having one gate controlling on-line the device polarity. Transistors with controllable polarity have been experimentally fabricated in several novel technologies, such as carbon nanotubes [7], graphene [8] and *Silicon NanoWires* (SiNWs) [2][3][6].

In DIG devices, one gate electrode, denoted the *Control Gate* (CG), acts conventionally by turning *on* and *off* the device. The other electrode, denoted the *Polarity Gate* (PG) acts on the side regions of the device, dynamically switching the device polarity between *n*-type (PG=1) and *p*-type (PG=0). The behavior of this device is illustrated in Fig. 1.

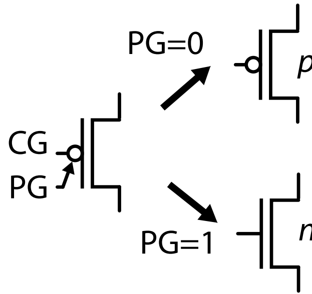


Fig. 1. Controllable-polarity transistor behavior.

Using controllable-polarity devices, it is possible to build very compact arithmetic logic gates, such as *eXclusive OR* (XOR) [4] and *MAJority* (MAJ) [15]. For instance, a 2-input XOR gate requires only 4 transistors [4] instead of the 8 required by the traditional full-swing static CMOS implementation [16]. This compactness can be leveraged in adder implementations, as reported in Fig. 2, where we show a full adder composed of only 8 controllable polarity transistors. This circuit exploits 3-input XOR and MAJ gates to implement the sum and the carry, respectively. Note that the proposed cells exploit a transmission-gate design. We will see, in the following, that this introduces a degree of redundancy at the gate level, that is beneficial from a robustness perspective. A self-checking ripple-carry adder architecture, exploiting this adder structure, is proposed in [15]. This architecture is far less expensive in terms of area than comparable CMOS architectures.

In this paper, we make one step forward with respect to [15]. In addition to exploit the reduced area cost offered by controllable-polarity devices, we take into account their intrinsic capabilities in masking, i.e., tolerating, faults and use them to build a fault-tolerant adder.

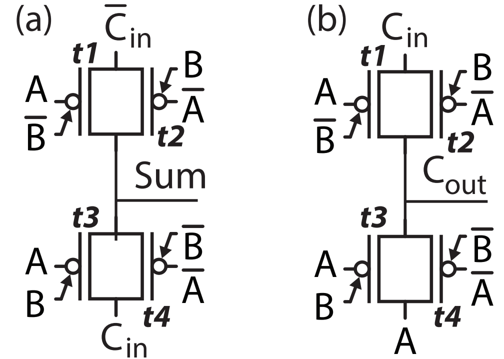


Fig. 2. Realization of 1-bit full adder using controllable-polarity transistors. (a) 3-input XOR – $Sum=A\oplus B\oplus C_{in}$, (b) 3-input MAJ – $C_{out}=MAJ(A,B,C_{in})$.

## III. EVALUATING CONTROLLABLE-POLARITY CIRCUIT ROBUSTNESS

In this section, we introduce a new fault-model suited to controllable-polarity transistors, study the robustness of operations for XOR and MAJ logic gates exploiting controllable-polarity transistors, and extend the results of this analysis to circuits composed of different gates.

### *A. Fault Model*

The robustness evaluation of circuits based on controllable-polarity devices cannot be performed by relying on usual fault models and tools, e.g., working at the gate level [17]. Indeed, when new technologies are introduced, it is common to envisage a lower-level approach, e.g., resorting to transistor-level fault models [18]. In such a case, the most common solution lies in inductive fault analysis of the device as well as layout-based defect map extraction for feasible fabrication shortcomings [10].

In this work, we only consider the defects that completely change the functionality [10], e.g., change the polarity of a transistor from *p*-type to *n*-type. Defects affecting the performances but keeping the functionality untouched are out of the scope of this paper. These defects can be modeled by generalizing bridge defects to the two gates composing our transistors [10]. Therefore, we introduce a new fault model that generalizes the *stuck-at* model for the mentioned bridge defects:

- *stuck-at-0* on CG (CG/0), *stuck-at-1* on CG (CG/1)

This defect is similar to what happens in the current technology. Depending on the polarity of the transistor, such defect will lead to a *Stuck-Open* (SO) or *Stuck-Short* (SS) behavior of the device.

- *stuck-at-0* on PG (PG/0), *stuck-at-1* on PG (PG/1):

This defect affects the polarity of the device. The device will

be either *stuck-at-n* or *stuck-at-p*, affecting the logic operation.

The new fault model straightforwardly extends the traditional transistor-level fault model, where the gate can be either stuck-at-0 or stuck-at-1, and takes into account the specific characteristics of controllable polarity transistors. Each of these faults corresponds to forcing to 0 or 1 the value of the corresponding controllable-polarity transistor input signal. We denote this fault model as *CG/PG fault model*.

### B. XOR/MAJ Gates Robustness

In order to evaluate the robustness of a circuit implemented with controllable-polarity devices, we need to evaluate the behavior of the basic logic primitives, when a CG/PG fault occurs in any of the transistors of the gate.

#### 1) Methodology

The 3-input XOR and MAJ logic gates, shown in Fig. 2-a and Fig. 2-b, respectively, have been characterized using electrical simulations. Fig. 3 summarizes the simulation setup that we used for fault analysis.

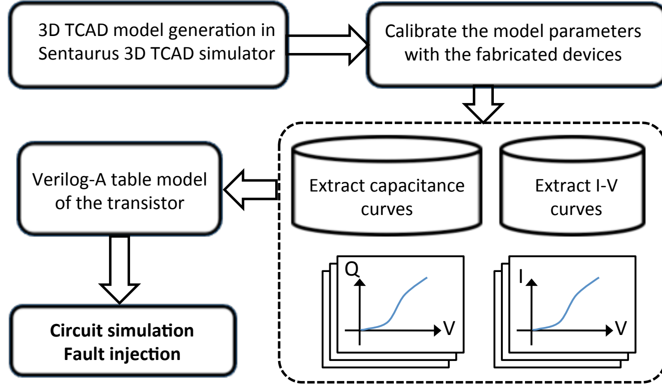


Fig. 3. Fault Analysis Methodology.

The logic gates are realized using SiNW-based controllable-polarity transistors [3]. A simple table-based compact model of the device is used with HSPICE simulator. The model is extracted using TCAD simulations of a 22-nm device, as shown in [3]. In the simulation experiments, the $V_{dd}$ value was fixed to 1.2V, which is in line with the technological results. The output of the gates is loaded with a fixed 1fF capacitance.

First, we identify the input voltage ranges associated to Boolean input *0* ($V_{IL}$) and *1* ($V_{IH}$), according to the definitions given in [16]. Defining the input voltage boundaries will help us to identify a faulty gate behavior in presence of a transistor-level fault. We report the obtained points for the logic gates:

- $V_{IH} = 0.600V$
- $V_{IL} = 0.540V$.

Therefore, the two logic gates will correctly behave when the output voltages for Boolean output *0* ($V_{OL}$) and *1* ($V_{OH}$) are in the following ranges:

- $0.600V < V_{OH} < 1.2V$
- $0V < V_{OL} < 0.540V$.

The identified ranges are used to classify the output values of the different gates. Then, the behavior of the logic gates under all possible CG/PG faults is computed by using DC operating points analyses for all possible input conditions.

#### 2) XOR/MAJ Gates Behavior under CG/PG Faults

Tables I and II report the simulated DC operating points of the 3-input XOR and MAJ gates, respectively, when the gates are fault-free and when each of the CG/PG faults are injected in the different transistors (*t1* to *t4*). The CG/PG fault injection induces different behaviors classified under three categories:

- correct behavior (highlighted in green) when a CG/PG fault is not excited by the applied input vector;
- masked-fault behavior (highlighted in blue) when a CG/PG fault is excited and induces a reduction of the noise margin at the output of the gate, but does not induce a faulty gate behavior as the output voltage is still in the correct $V_{OH}$ and $V_{OL}$ range;
- faulty behavior (highlighted in red) when a CG/PG fault induces an incorrect value at the output of the gate.

Considering the 3-input XOR (Table I), the results indicate that 8 CG/PG faults out of 16 lead to a faulty gate behavior that is observable at the gate output for at least one input combination. The remaining 8 CG/PG faults are always masked. Moreover, the 8 detectable faults produce a faulty output when 4 out of 8 possible input values are applied (*001*, *010*, *100*, and *111*). With the other 4 input combinations (*000*, *011*, *101*, and *110*), the circuit always produces the correct output no matter the presence of a fault.

Controllable-polarity transistors have 4 different modes of operations: *on* *n*-type, *off* *n*-type, *on* *p*-type and *off* *p*-type. A CG/PG fault restricts the number of operations of the device but does not fully lock it in a unique mode. This property is unique to the class of controllable-polarity transistors and unachievable with standard transistors. This has a positive impact on the fault tolerance of the overall gate circuit. As an example, we can consider the PG/0 fault on *t4* in the 3-input XOR under input values *000*. Under fault-free conditions, the bottom transmission-gate is *on*, with *t3* configured as *p*-type and *t4* as *n*-type. *t4* propagates properly the logic *0*. However, when a PG/0 fault affects *t4*, *t4* polarity switches to *p*-type. In this condition, the logic *0* cannot be fully propagated, but is still transmitted with limited voltage degradation. Such degradation reduces the noise margin of the gate, but does not induce a faulty behavior.

Similarly, for the 3-input MAJ (Table II), the results indicate that the number of faulty behaviors is very small: 12 faults out of 16 are always masked. Moreover, the 4 faulty conditions do produce a difference in the output voltage only when 2 of the 8 possible input combinations are applied (*011* and *110*). For the 6 remaining input combinations, the CG/PG faults never produce any output misbehavior.

TABLE I. OUTPUT VOLTAGE VALUES OF THE 3-INPUT XOR GATE.

| | | *t1* | | | | *t2* | | | | *t3* | | | | *t4* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input** | **Fault-free** | CG/0 | CG/1 | PG/0 | PG/1 | CG/0 | CG/1 | PG/0 | PG/1 | CG/0 | CG/1 | PG/0 | PG/1 | CG/0 | CG/1 | PG/0 | PG/1 |
| 000 | 0 | 0.32 | 0 | 0 | 0.27 | 0 | 0.27 | 0.32 | 0 | 0 | 0 | 0 | 0 | 0.14 | 0 | 0.13 | 0 |
| 001 | 1.2 | 0.83 | 1.2 | 1.2 | **0.36** | 1.2 | **0.36** | 0.83 | 1.2 | 1.2 | 1.1 | 1.2 | 1.1 | 1.2 | 1.2 | 1.2 | 1.2 |
| 010 | 1.2 | 1.2 | 1.1 | 1.2 | 1.1 | 1.2 | 1.2 | 1.2 | 1.2 | 0.83 | 1.2 | 1.2 | **0.36** | 1.2 | **0.36** | 0.83 | 1.2 |
| 011 | 0 | 0 | 0 | 0 | 0 | 0.14 | 0 | 0.13 | 0 | 0.32 | 0 | 0 | 0.27 | 0 | 0.27 | 0.32 | 0 |
| 100 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.1 | 1.2 | 1.1 | 1.2 | **0.36** | 0.83 | 1.2 | 0.83 | 1.2 | 1.2 | **0.36** |
| 101 | 0 | 0.14 | 0 | 0.13 | 0 | 0 | 0 | 0 | 0 | 0 | 0.27 | 0.32 | 0 | 0.32 | 0 | 0 | 0.27 |
| 110 | 0 | 0 | 0.27 | 0.32 | 0 | 0.32 | 0 | 0 | 0.27 | 0.14 | 0 | 0.13 | 0 | 0 | 0 | 0 | 0 |
| 111 | 1.2 | 1.2 | **0.36** | 0.83 | 1.2 | 0.83 | 1.2 | 1.2 | **0.36** | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.1 | 1.2 | 1.1 |

TABLE II. OUTPUT VOLTAGE VALUES OF THE 3-INPUT MAJ GATE.

| | | *t1* | | | | *t2* | | | | *t3* | | | | *t4* | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input** | **Fault-free** | CG/0 | CG/1 | PG/0 | PG/1 | CG/0 | CG/1 | PG/0 | PG/1 | CG/0 | CG/1 | PG/0 | PG/1 | CG/0 | CG/1 | PG/0 | PG/1 |
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 001 | 0 | 0.32 | 0 | 0 | 0.27 | 0 | 0.27 | 0.32 | 0 | 0 | 0 | 0 | 0 | 0.14 | 0 | 0.13 | 0 |
| 010 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 011 | 1.2 | 1.2 | 1.1 | 1.2 | 1.1 | 1.2 | 1.2 | 1.2 | 1.2 | 0.83 | 1.2 | 1.2 | **0.36** | 1.2 | **0.36** | 0.83 | 1.2 |
| 100 | 0 | 0.14 | 0 | 0.13 | 0 | 0 | 0 | 0 | 0 | 0 | 0.27 | 0.32 | 0 | 0.32 | 0 | 0 | 0.27 |
| 101 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| 110 | 1.2 | 1.2 | **0.36** | 0.83 | 1.2 | 0.83 | 1.2 | 1.2 | **0.36** | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.1 | 1.2 | 1.1 |
| 111 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |

### C. *Circuit-level Analysis*

Based on the results of the detailed transistor-level analysis presented so far, we can describe the behavior of each possible logic gate for each possible input combination and for each possible fault affecting each of the internal transistors. Therefore, we build a detailed model of the fault-free and faulty behavior of each gate. Using these models, we then determine the fault-free and faulty behavior of a larger circuit composed of different gates working at the logic level. This allows us to ignore the details of the underlying transistor-level structure, without loosing in accuracy. As a matter of facts, the approach we use in the remaining parts of this paper is based on developing VHDL models for each gate (with suitable control signals to inject each possible fault), and combining them to extensively analyze the behavior of larger circuits.

## IV. FAULT-TOLERANT RIPPLE-CARRY ADDER ARCHITECTURE

Knowing the behavior of the 3-input XOR and MAJ gates exploiting controllable-polarity transistors, and using the approach we just described, we now investigate the possibility to implement a fault-tolerant ripple-carry adder architecture based on these primitives.

We consider the 1-bit adder circuit represented in Fig. 4 and consisting of two 3-input XOR gates for the sum generation and two 3-input MAJ gates for the carry generation. As compared to the simpler adder of Fig. 2, this circuit generates both the sum and carry signals and their inverted versions in a unique logic level. This allows us to create ripple-carry adder structures without adding any inverters to drive the next stage. Note that the inverted sum is used for realizing a fault-tolerant version of the adder as described later and that, due to the transmission gates, buffers will be required every 4 stages.

Using the approach described in Section III.C, we first created a logic model of the proposed adder in VHDL combining the models of each composing gate, and used it to gather simulation results for every one of the proposed faults during an exhaustive simulation. Results (not reported here in details for sake of conciseness) show that most of the possible CG/PG faults (40 out of 64) are masked in this structure.

In order to make the adder fault-tolerant with respect to all the possible faults and under all the input conditions, we propose a *Triple Module Redundancy* (TMR)-based 1-bit adder architecture, shown in Fig. 5. Note that, in this figure, the inverted input and internal signals are not represented for the sake of visibility. The key characteristics of the proposed fault tolerant adder are:

- Each 1-bit adder of Fig. 4 is triplicated and voted. In this way, any single fault affecting a single adder can be tolerated and does not propagate to the following stages of the adder.
- The inputs to each replica, labeled from 1 to 3, are permuted. In this way, even if the same fault affects more than a single replica, this does not evolve into a common mode fault, and the circuit behaves correctly.
- Each of the 3 output signals, i.e., the sum and the carry signals (regular and complemented to cascade further stages)

is voted. Since the majority voter has been shown in the previous section to never fail with the *000* and *111* input combinations, the voter never fails when the three 1-bit adders are fault-free. This guarantees that the 1-bit adder never produces a faulty output in the presence of a single fault affecting an adder or a voter.

- Given the above properties, one can easily build a ripple-carry adder out of the proposed 1-bit adder, knowing that fault effects cannot propagate from one stage to another.

The proposed architecture provides significant benefits in terms of fault tolerance. Thanks to triplication, it can mask any single fault in the three 1-bit adders and in the voter, which is never stimulated with an input value able to excite a fault inside it, unless another fault exists in an adder. Clearly, faults on the inputs A and B of the single cell of the full adder cannot be tolerated (unless they are in turn triplicated).
Thanks to the input permutation and to the robustness of the 1-bit adder, less than 1% of the possible 4,032 (64 × 63) double faults affecting a couple of replicas produce a faulty behavior.

Moreover, based on the previous analysis we can state that only 192 faults can produce a failure out of the set of 6,912 (144 × 48) double faults composed of one fault in an adder, and another in a voter.

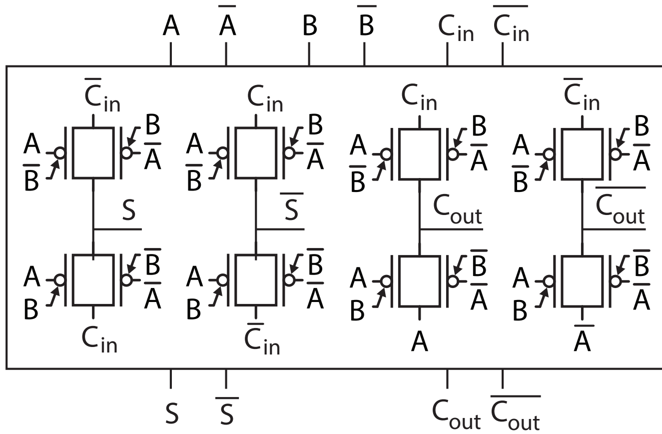


Fig. 4. 1-bit adder with generation of inverted sum and carry.

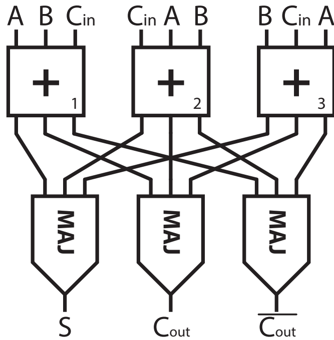


Fig. 5. Fault tolerant 1-bit adder exploiting TMR and MAJ voters. Inverted signals are not represented for the sake of visibility.

## V. QUANTITATIVE ANALYSIS

In order to provide the reader with some more details about the performance and characteristics of the proposed architecture, we first performed some experimental analysis, aimed at checking its behavior in the presence of single and double faults.

Results of this analysis (performed by combining at the gate level the results reported in the previous Sections) confirmed that all single faults are masked, either by the characteristics of the controllable-polarity gate implementation, or by the TMR architecture.

From the circuit-level performance perspective, we compared the proposed circuit implemented using SiNWFETs with its equivalent CMOS FinFET 20-nm LSTP counterpart using electrical simulations. The load capacitance for the two circuits is set to 1fF. We consider the area, the worst-case delay and the leakage power. Note that dynamic power is not considered due to a lack of precision in the considered compact model. The circuit-level results are summarized in Table III.

TABLE III. FAULT-TOLERANT 1-BIT ADDER PERFORMANCES

| **20-nm node** | **# Transistors** | **Area ($\mu m^2$)** | **Delay (ps)** | **Leakage Power (nW)** |
|---|---|---|---|---|
| FinFET LSTP | 108 | 5.89 | 371 | 23.84 |
| SiNWFET | 60 | 4.98 | 304 | 21.06 |
| **Gain** | 44% | 15.5% | 18.1% | 11.6% |

The proposed implementation requires 16 controllable-polarity transistors for each 1-bit adder, plus 12 transistors for the 3 majority voters. Hence, 60 transistors are required for the proposed fault-tolerant 1-bit adder. By applying the same design principles with transmission-gate CMOS, we obtained 24 transistors for a 1-bit full adder. Note that the reference structure also generates all the inverted signals required to cascade the different adder stages. Smallest implementations can be identified for both CMOS and controllable-polarity transistors if dedicated inverters are used to generate the inverted signals. Then, a TMR-based implementation in CMOS technology would require 3 × 24 transistors, plus the cost for the majority voter on the data output, accounting for 3 × 12 transistors. In total, 108 transistors would thus be required. Hence, the proposed solution requires 44% less transistors. When considering the area of the two adders, the proposed solution requires 4.98μm² as compared to 5.89μm² for its equivalent FinFET implementation. This leads to a gain of 15% in area. The gain is reduced compared to the simple transistor count, as controllable-polarity transistors are bigger than FinFETs, due to the additional polarity terminals. The proposed solution is also significantly less expensive than the one proposed in [19], which proposes a fault-tolerant architecture for the voter consisting of an XOR and a multiplexer.

Finally, the proposed solution can be easily used to build up an adder with whichever data parallelism *n*, whose total cost scales linearly with *n*. Since we demonstrated that single faults affecting one stage do not propagate to the following ones, the level of fault tolerance of the final adder is not affected by its parallelism.

From a performance perspective, the proposed implementation is shown to be faster with a 18% reduction of the worst case delay. This is accounted to the reduced number of stacked transistors coming from the use of controllable polarity transistors. Finally, the leakage power is reduced by 12%, thanks to the good electrostatic control offered by the SiNWFETs.

## VI. CONCLUSIONS

Controllable-polarity transistors offer many advantages to implement arithmetic logic gates at a reduced implementation cost. Besides the implementation compactness, an important parameter to consider is the robustness with respect to possible faults. In this paper, we performed such an analysis and showed that circuits based on controllable-polarity transistors can tolerate a large number of faults. Thanks to this property, they can be used to build effective structures demonstrating large fault tolerance, in addition to area, power and speed improvements. In particular, we showed that the SiNWFET implementation of a fault tolerant 1-bit adder (that can be easily used to build an adder of any size) is 15% smaller, 18% faster, and 12% less power consuming than the corresponding CMOS solution. This module can be used to build a ripple-carry adder of any length able to tolerate any single permanent fault and most of the possible double faults in any of its stages.

## ACKNOWLEDGMENTS

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