Novel Readout Circuit for Memristive Biosensors in Cancer Detection

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Abstract—We present a novel circuit for the automated and quick characterization of an array of experimental memristive nanowires that are functionalized as biosensors. Successfully functionalized nanowires will express the concentration of target molecules by hysteretic gaps of the zero crossing of their memristive I/V characteristics as the voltage across them is swept up and down. The width of the voltage gap is directly proportional to the target molecule concentration. The characterization circuit sorts out faulty, i.e. non-conducting nanowires in the array, and performs an analog to digital conversion of the voltage gap to assess successful functionalization of the others, and thus significantly reduces the time for functional testing. Many of the test parameters are configurable: the speed and range of the voltage sweep and the resolution of the measurements. An initial prototype 2x2 array of the circuit has been layed out in 0.35μm CMOS technology within an area of 0.429 mm^2 and has been thoroughly characterized in simulation, has been layed out, and is ready for fabrication.

Index Terms—Memristive, bio-sensor, fully pinched current detection, femto amps, sub-hertz triangular voltage source, cancer detection

I. INTRODUCTION

In recent years, silicon nanowires (SiNWs) have widely been investigated as highly sensitive biological and chemical sensors [1], [2]. Typically the currently developed SiNW biosensors require measurement with a probe station to monitor the conductance changes between source and drain electrodes induced by recognition event between target molecules and the surface-bound receptors. We have very recently introduced a completely novel approach based on the memristive effect in SiNWs [3], [4], [5], and have demonstrated great potentials for the ultra-high sensitive detection of biomarkers in air [6]. This method is based on charge effects of biomolecules on the so called voltage gap. The voltage gap is defined as the voltage difference calculated between the forward and backward zero crossing points of the $I_{ds} - V_{ds}$ curves. The corresponding sensing protocol requires the use of a probe station too, this time employed for the acquisition of the hysteretic $I_{ds} - V_{ds}$ characteristics on memrisitve devices. The probe station is, however, big, expensive, time-consuming and only applicable for single sensor measurement at one time, which hinders the development of miniaturized device for simultaneous-multiplexed detection of biomarkers. In this paper we describe a readout circuit that interfaces to an array of memristive SiNWs, does a functionality check for them,

extract the voltage gap for each sensor, and provides an error margin value for every individual sensor. Post layout simulations are also presented. This novel readout architecture is optimized for voltage-gap based sensing to achieve the ultra-high resolution detection (in the order of femto Mole (fM)) and the very low-current measurements on memrisitve devices. It will thus provide a fast and easy readout interface for the detection of multiple cancer markers.

II. BACKGROUND

A. Memristive Sensor Fabrication

Memristive SiNWs with NiSi Schottky-barrier junctions are obtained through a top-down fabrication process on a p-type Silicon-On-Insulator (SOI) wafer. The nanowires are patterned by Electron-Beam Lithography and a dedicated Deep Reactive Ion Etching (DRIE) process. Antibodies are bound to the SiNW surface using glycidoxypropyltrimethoxysilane (GPTS) chemistry. Ethanolamine is used as blocking agents for the remaining active GPTS-derived groups. A further blocking step is performed with 3% gelatin from cold water fish skin. More details on the fabrication protocol can be found in [4], [5].

B. Voltage-gap Based Sensing

Sensing experiments are done in direct current (DC) regime with drain-source V_{ds} being swept in the range -3 V to +3 V, with voltage step of 50mV. The backgate is fixed at $V_{bg} = 0$ V. $I_{ds} - V_{ds}$ characteristics are acquired in air, at room temperature, and 55% of relative humidity. For testing the device, the sample is removed from solution, gently dried under N_2 flow, inserted in the characterization tool and measured in dry conditions. The fabricated SiNWs feature a memristive effect that matches well with memristor theory [5]. Data demonstrates that the pinched hysteresis loop of the semi-logarithmic curve acquired from bare devices (Fig. 1a, solid line) is lost upon bio-functionalization of the device as effect of the antibody net charge contribution on the channel. The created electric field induces a voltage gap effect appearing as the voltage difference between the current minima for backward and forward regimes (Fig. 1a, dotted line). This phenomenon has been measured with very good repeatability in most of the tested devices, and can thus be used
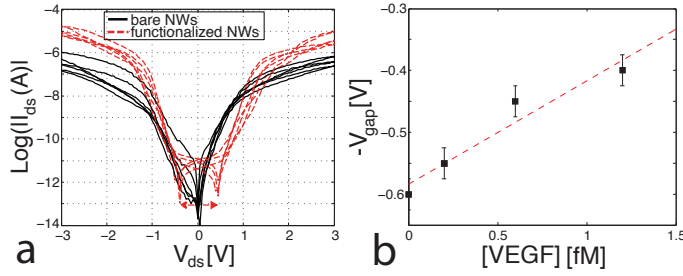
Fig. 1. a) Semi-logarithmic $I_{ds} - V_{ds}$ curves acquired on bare (solid line), and functionalized (dotted line) memristive sensors, showing the effect of biomolecules on the voltage gap. The good reproducibility of this phenomenon is demonstrated by the overlapping characteristics acquired from 4 different devices before and after the surface modification. b) Calibration curve for one memristive sensor used to detect VEGF molecules.

to detect biomolecules. Fig. 1b shows the occurring femto-molar detection of VEGF antigen: the voltage gap decreases as function of increasing uptaken VEGF molecules. The result has been confirmed also in the detection of rabbit antigen molecules [4] and pH sensing [7].

III. CIRCUIT REQUIREMENTS

The above description of the process of current zero crossing detection leads to a set of requirements that can be summarized as follows:

1) The voltage across the nanowire should be swept from a negative voltage to a positive voltage and vice versa in a sub-hertz frequency.
2) The voltage gap corresponding to the difference between the voltages where the current zero crossings occur should be extracted. Current values vary between tens of uA and 0A.
3) In case of multiple zero crossings while sweeping in one direction, they should be logged and reported since they contribute to the accuracy of the measurement.
4) Defects easily introduced with fabrication processes and non-homogeneous functionalization of the nanowire may cause the SiNWs to break down or stop conducting in the right manner. A functionality check checking for a minimal current at maximum voltage for the nanowire should be thus performed in order to prevent any mistake in the voltage gap calculation.

These tests should be applied for an array of sensors at the same time. In this paper, we are presenting the solution for one system implementation, which is scalable to any number of sensors. A 2x2 array of the circuit has been laid-out and will be sent to production shortly.

IV. CIRCUIT DESCRIPTION

The circuit is designed to extract the voltage gap by identifying the voltages across the nanowire when the current switches direction. One node of the nanowire, *SENS_P*, is kept at *Vref*, 2.5V in 5V technology, by using negative feedback via A1, as shown in figure 2, while the other node, *SENS_N*, is controlled by a voltage ramp sub-circuit linearly sweeping between a *VL* and *VH* where 2.5V is the mid voltage. Typically *VL* is 0V,

and *VH* is 5V, and the voltage sweep across the nanowire is from -2.5V to +2.5V. Now we need only sample *Vsweep* when the zero crossings occur.

A. Zero crossing detector

Transistors $Q2$ and $Q1$ are source connected between *VDD* and *GND* and have the gate in common. The current flows either from *VDD* via $Q2$, through *SENS_P* to *SENS_N* and down to *GND* via $Q4$, or from *VDD* via $Q3$ through *SENS_N* to *SENS_P* and down to *GND* via $Q2$. Between $Q1$ and $Q2$, only one is ON and conducting at any moment, and typically both are OFF at the moment when the current switches direction. That translates to *VGS* of both transistors, defined as *Vctrl-Vref*, being positive when $Q2$ is ON, negative when $Q1$ is ON, and equal to zero when the current through the nanowire changes its direction. Notice that this configuration allows $Q1$ and $Q2$ to be in the subthreshold region while conducting small currents. So, we define the current zero crossing as the voltage for which *Vctrl* is equal to *Vref*. With the help of a comparator having *Vref* and *Vctrl* as inputs, we can get a *CROSS* signal that has a rising/falling edge whenever the current switches direction. This is the signal we use in the digital part.
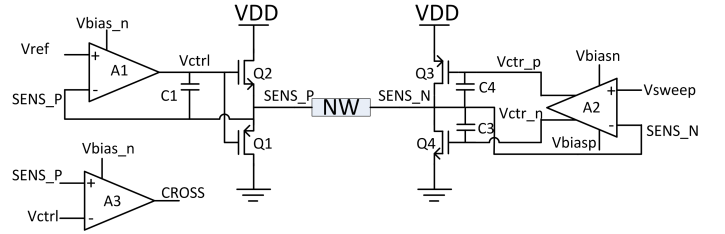

Fig. 2. Circuit solution per one sensor

B. Voltage ramp generator

The voltage ramp sub-circuit is made of a current mirror structure where the PMOS gate voltage *Vbramp* is controlled from off-chip as it appears in Fig. 3. Increasing *Vbramp* decreases the current through M3 and M4 which leads to a longer time constant charging/discharging C5, i.e. a smaller frequency for triangular signal *Vsweep*, and vice versa. The *Vsweep* signal varies between *VL* and *VH* through the use of the complementary input comparator A6 shown in Fig. 5(d) by generating the *Reset* and *Set_int* signals. These two signal are used in Fig. 3(b) to generate the control signals for the transmission gate, *CH* and *DCH*, reflecting the charging and the discharging phases of C5. These two signals are also passed to the digital part.

Long channel transistors are used for M1-M4 to reduce the channel length modulation. By doing that, the charging and the discharging periods only differ within 1%. The charging/discharging time is linear as long as *VL* and *VH* have sufficient headroom from *GND* and *VDD*. By setting *VL* to 100mV, and *VH* to 4.9V, the highest voltage deviation from linearity is within 1.6% from the linear value.

C. Device fault detector

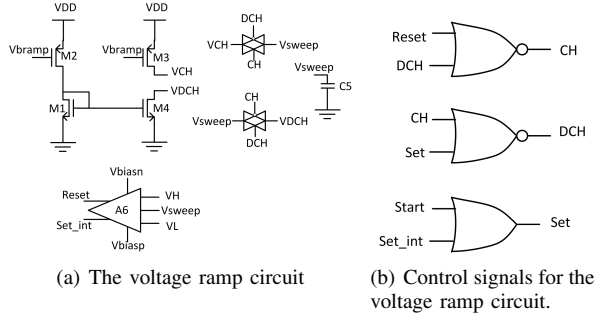The functionality check for faulty nanowires is depicted in Fig. 4(a). The idea is to check for the amount of current

(a) The voltage ramp circuit

(b) Control signals for the voltage ramp circuit.

Fig. 3. Configurable voltage ramp circuit shared by all sensors.

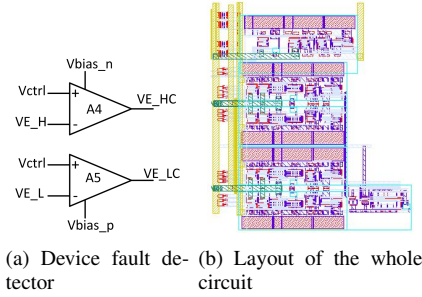
(a) Device fault detector

(b) Layout of the whole circuit

Fig. 4. Functionality check circuit and the layout of the analog parts of the whole circuit for the four sensors.

through the nanowire when *Vsweep* is at *VH* and at *VL*, and make sure that it is above a specific value (in nAs). This current will go through $Q1$ or $Q2$, setting *Vctrl* for a specific value (*VE_H* in case of $Q2$ conducting and *VE_L* in case of $Q1$ conducting), corresponding to the current we are after. So, if we compare *Vctrl* and *VE_L* at the beginning of the charge period, where the current goes through $Q2$, and find that *Vctrl* is smaller than *VE_L*, then the nanowire is not conducting the expected amount of current which is a sign of a faulty nanowire. The same applies for *VE_H* at the beginning of the discharge period. Signals *VE_HC* and *VE_LC* are also forwarded to the digital domain.

The schematics of the opamps (excluding bias generation) are shown in Fig. 5.

The layout of the analog parts is presented in Fig. 4(b).

D. Digital processing

The digital part receives the following input signals: *CH*, *DCH*, *CROSS*, *VE_HC* and *VE_LC*. This is depicted in Fig. 6, where *VE_HC* is removed for brefity. The signals evolve as follows:

1) *DCH* goes high, a global counter, *GC*, starts from 0. *VE_HC* is checked also in case it is low, meaning the nanowire is damaged and a flag is set.
2) *VE_LC* switches high and will be checked when *DCH* goes low, and in case *VE_LC* is low, the nanowire is faulty and a flag is set.
3) *CROSS* goes high, *GC* value is saved into register t1. If *CROSS* switches again, nt1 times, while *DCH* is high, the *GC* value for last crossing is saved into register t1f.
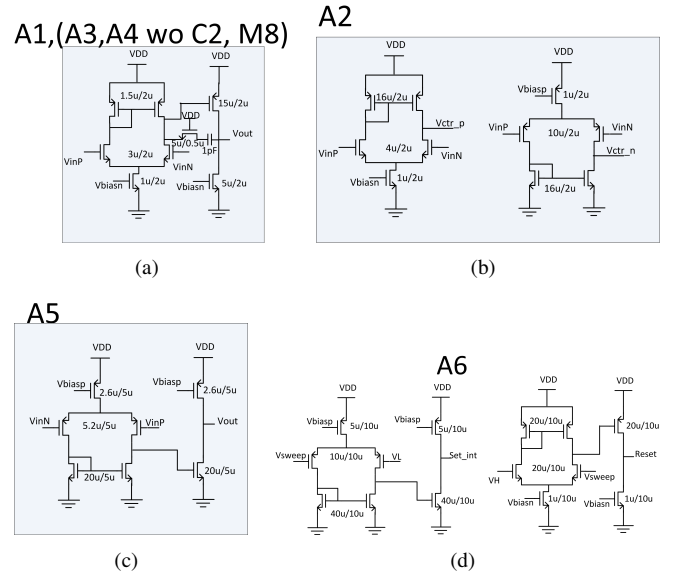4) *DCH* goes low, the functionality check on *VE_LC* is done as described above.

A1,(A3,A4 wo C2, M8)

A2

A5

A6

(a)

(b)

(c)

(d)

Fig. 5. Schematics of the used OpAmps.

5) *CROSS* goes low, the *GC* value is saved into register t2. If *CROSS* switches again, nt2 times, while *DCH* is low, the *GC* value for the last crossing is saved into register t2f.
6) *VE_LC* goes low, i.e *Vctrl* is lower than the *VE_L* limit.
7) *DCH* goes high again, the test period is finished. the *GC* value is saved to t_total.

The voltage gap is defined now as:

$$|t\_total - t1 - t2| \times \frac{2(VH - VL)}{t\_total} \qquad (1)$$

Other outputs, that are read out in the end of the test, are the number of crossings happening in one phase (charge or discharge), and how far the first crossing was from the last crossing according to these two formulae:

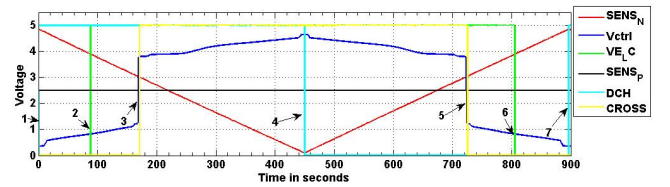$$(t1f - t1) \times \frac{2(VH - VL)}{t\_total} \ldots (t2f - t2) \times \frac{2(VH - VL)}{t\_total} \qquad (2)$$

Fig. 6. Basic signals arriving from the analog domain.

V. SIMULATIONS AND RESULTS

A. Simulations settings

The analog sub-circuits are implemented with 5V (thick gate oxide) transistors to handle a 5V sweeping range. Post-layout simulations are reported here. The nanowire is substituted by a current source implementing a I/V look-up table obtained from prior manual characterizations of nano wires.

Vbramp is set at 3.91V, *VL* to 100mV, *VH* to 4.9V, *VE_H* to 4V, and *VE_L* to 800mV. This configuration will run the test for 896 secs and will check for device failure for currents

below 2nA. The digital circuit is implemented in VHDL and simulated with a clock frequency of 1Hz, but has not yet been synthesized and is thus not included in the layout.

B. Results

We ran simulations and post-layout simulations using many lookup tables that were extracted from different nanowires at different stages while testing in the Lab. Figure 7 shows the current going through the nanowire (W=100nm and L=1μm) for one particular test run after the antigen uptake. The blue curve is the logarithmic plot of the absolute value of the current when sweeping the voltage from +2.5V to -2.5V, while the red one is for sweeping the voltage from -2.5V to +2.5V. The *CROSS* signals are what the circuit produces. Notice the hysteresis effect that the antigen has on the current behavior. The current changes all the way from 15.4μA to 0A where 14.3 fA is the last detectable value. This is almost 10^9 range difference which the circuit is able to react correctly to.
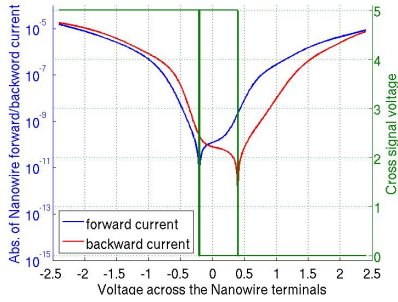

Fig. 7. Current minimum and *CROSS* signal.

C. Analysis

We start by presenting the equations relating the test duration, resolution and digital clock frequency with the circuit parameters:

$$Test\_duration = \frac{2(VH - VL)}{\frac{\Delta V}{\Delta t}} \quad (3a)$$

$$resolution = \frac{\frac{\Delta V}{\Delta t}}{freq} \quad (3b)$$

$$global\_counter\_bit\_width = \lceil \log_2(\frac{2(VH - VL)}{resolution}) \rceil \quad (3c)$$

where $\frac{\Delta V}{\Delta t}$ is the rate of change of *Vsweep* and is controlled by *Vbramp*, and in this simulation it is 10.7mV/sec.

As can be seen from Eq. 3a, the test duration is inversely proportional to the speed of the *Vsweep* signal, and from Eq. 3b, to achieve better resolution, either increase the frequency of the digital clock, or decrease the speed of the *Vsweep* signal, and this will come with the cost of longer testing time, and higher number of bits for the counter and consequently the registers for t1 and t2 as shown in Eq. 3c.

The voltage gap produced by measured currents in the lab for one particular device has been 0.6V, while the one produced by the cross signal when simulating this device is 0.605V. This difference is due to the delay between the current crossing zero, and *Vctrl* reacting to that and crossing *SENS_P*. It is caused by C1 which is used to stabilize the negative feedback loop. This delay depends also on the slope of the zero crossing.

If the transition is very slow/flat, this delay will grow bigger, and vice versa. The delay translates to voltage since *SENS_N* is changing linearly with time.

Another source of error is the difference in time between the rising edge of the clock and the edge transition of the *CROSS* signal. With 1Hz frequency, each transition of the *CROSS* signal can lead to a 10.7mV offset in the worst case. This double to 21.4mV offset in the voltage gap. The delay due to C1 can reduce this error if it makes the *CROSS* closer to the clock rising edge, but will increase the error, if it pushes the *CROSS* signal beyond the clock rising edge.

VI. Conclusion

In this paper, we presented a novel circuit that interfaces to memristive biosensor arrays used in cancer marker sensing. The analog parts that detect zero crossing currents have been implemented in 0.35μm AMS technology and sent for fabrication. We presented equations describing the relationship between different parameters. We reported post layout simulations where the current ranged from μAs to fAs and the circuit was able to extract a 600mV voltage gap with 5mV error. The circuit will enable automated characterization of arrays of nanowires (2×2 on the initial prototype) within few minutes where previous manual testing required few hours for single SiNW sensors as described in II. The proposed readout architecture, integrated with the digital part on a single chip, can also be scaled up to interface to a larger number of sensors, thus enabling fast and accurate multiplexed measurements for cancer marker detection. The ultimate goal shall of course be to add the nanowires onto the same AMS 0.35μ CMOS substrate as the circuits. The exact postprocessing steps for this have yet to be investigated.

VII. Acknowledgment

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