Unlocking Controllable-Polarity Transistors Opportunities by Exclusive-OR and Majority Logic Synthesis

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Abstract—**For more than four decades, *Complementary Metal-Oxide-Semiconductor* (CMOS) *Field Effect Transistors* (FETs) have been the baseline technology for implementing digital computation systems. CMOS transistors natively implement *Not-AND* (NAND)- and *Not-OR* (NOR)-based logic operators. Nowadays, we observe a trend towards devices with an increased set of logic capabilities, i.e., with the ability to realize in a compact way specific logic operators as compared to the standard CMOS. In particular, controllable-polarity devices enable a native and compact realization of *eXclusive-OR* (XOR)- and *MAJority* (MAJ)- logic functions, and open a large panel of opportunities for future high-performance computing systems. However, main current logic synthesis tools exploit algorithms using NAND/NOR representations that are not able to fully exploit the capabilities of novel XOR- and MAJ-oriented technologies. In this paper, we review some recent work that aims at providing novel logic synthesis techniques that natively assess the logic capabilities of XOR- and MAJ-operators.**

Keywords—Nanowire transistors; polarity control; logic synthesis; exclusive or (XOR); majority (MAJ)

I. Introduction

The increasingly higher level of integration reached by *Field Effect Transistors* (FETs) has been allowing, for more than four decades, the semiconductor industry to design computation systems with exponential capabilities. Silicon-based *Metal-Oxide-Semiconductor Field-Effect Transistors* (MOSFETs) form the elementary blocks for present electronics. In the digital domain, a MOS transistor behaves as a two-terminal binary switch driven by a single input signal. Such behavior makes them efficient in implementing *Not-AND* (NAND)- and *Not-OR* (NOR)-based logic operations.

Nevertheless, as the semiconductor industry is approaching the ultimate limits of conventional MOSFETs, researchers are focusing their effort to identify possible approaches that will enable the continuation of Moore's scaling laws. *Fin-based Transistors* (FinFETs) are successfully replacing planar CMOS transistors at the 22-nm technology node [1]. Following the trend to one-dimensional (1-D) structures, advanced structures, such as *Silicon NanoWires* FETs (SiNWFETs) [2] or *Carbon Nanotubes* FETs (CNFETs) [3] are promising candidates to push the device performances. 1-D structures exhibit a superior electrostatic control that can bring both performances [2] and novel functionalities, such as the dynamic control of the device polarity [4]. Transistors with controllable polarity are *Double-Independent Gate* (DIG) FETs having one gate controlling on-line the device polarity. Transistors with controllable polarity have been experimentally fabricated in several novel technologies, such as carbon nanotubes [5] and *Silicon NanoWires* (SiNWs) [4,6]. The on-line configuration of DIG FETs polarity is typically enabled by the regulation of Schottky barriers on source/drain junctions through the additional gate.

Transistors with controllable polarity intrinsically act as comparators and thus enable the realization of *eXclusive-OR* (XOR) and *MAJority* (MAJ) operators with the same complexity than AND/OR operators. To take advantage of this opportunity at circuit level, XOR and MAJ primitives should be efficiently manipulated during the design of a circuit.

Nowadays, virtually all digital integrated circuits are realized using logic synthesis techniques [7], whose performances depend on the manipulated logic representations. Many logic representation forms are inspired by the underlying functionality of contemporary digital circuits. Designed to support MOS technologies, original logic synthesis techniques, which are the basis for current commercial tools, exploit algorithms using NAND/NOR representations and miss the possibility to unlock the full expressive capabilities of the novel class of controllable-polarity FETs.

This paper aims at surveying some recent work on novel logic synthesis techniques that natively assess the logic capabilities of XOR- and MAJ-operators. We will focus on two promising logic representations: *Biconditional Binary Decision Diagram* (BBDD), which uses a comparator as its core logic expansion, and *Majority-Inverter Graph* (MIG), which extends standard *And-Or-Inverter Graph* and supports a powerful algebra.

The remainder of the paper is organized as follows. In Section II, we devise on the opportunities brought by controllable-polarity devices. In Section III, we review and discuss the basis of BBDDs, while, in Section IV, we focus on MIGs. In Section IV, we conclude the paper.

II. Towards the Native Implementation of Arithmetic Operators

In this section, we discuss the opportunities of controllable-polarity devices in light of arithmetic operators.

A. Transistors with Controllable Polarity

Advanced nanoscale device technologies often exploits Schottky barriers at their source and drain contacts. While decreasing the access resistances, they also lead to an ambipolar phenomena, coming from the conduction of both holes and electrons Its effect is reinforced today by the trend towards the use of intrinsic transistor channels at the 22-nm node and below. This phenomenon is typically a limitation for design and technologists try to suppress it through additional processing steps.

However, it is possible to control this phenomenon in order to enrich the capabilities of the elementary transistors by creating double-independent-gate structures.

Typically, in such device, one gate electrode, called *Control Gate* (CG) acts conventionally by turning *on* and *off* the device. The other electrode, called *Polarity Gate* (PG), acts on the side regions of the device, in proximity of the *Source/Drain* (S/D) Schottky junctions, switching the device polarity dynamically between *n*- and *p*-type, as illustrated in Fig. 1-a.

This elementary property defines a new class of emerging devices that inherently implement a two-input comparator rather than a simple switch. These innovative devices come in many different technologies, such as silicon nanowires [4,6], carbon nanotubes [5], graphene [8] and nanorelays [9]. In the first three approaches, the basic element is a double-gate controllable-polarity transistor. It enables online configuration of the device polarity (*n* or *p*) by adjusting the voltage at the second gate. Consequently, in such a double-gate transistor, the *on*/*off*

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state is biconditional on both gates values. The basic element in the last approach [9] is instead a six-terminals nanorelays. It can implement complex switching functions by controlling the voltages at the different terminals. Following to its geometry and physics, the final electric way connection in the nanorelay is biconditional on the terminal values [9]. Even though they are based on different technologies, all the devices in [4,5,8,9] have the same common logic abstraction, depicted by Fig. 1-b.

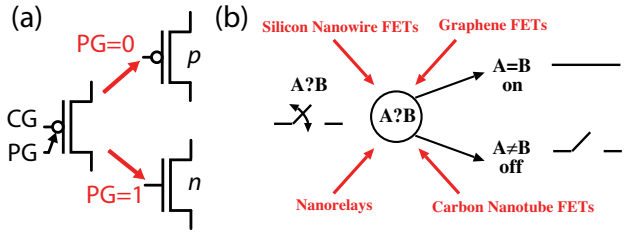

Fig. 1. Transistor with polarity control behavior illustration (a) and common logic abstraction (b).

B. Logic Operations with Higher Expressive Power

Digital circuits using these transistors can exploit both gates as inputs, thereby enabling the design of compact cells that implement XOR more efficiently than in CMOS. Indeed, the devices are logic biconditional on their two-gate polarities, and embed intrinsically an XOR characteristic. This unique feature is used to a full-swing 2-input XOR gate, reported in Fig.2-a, with only 4 transistors while the traditional full-swing static CMOS implementation uses 8 transistors [10]. Similarly, a 4-transistor 3-input majority logic gate is reported in Fig.2-b. This gate returns the logic value assumed by more than 2 inputs. In static CMOS, the same gate has 10 devices in place of 4 here [10].

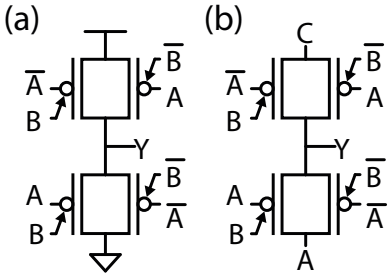

Fig. 2. 2-input XOR (b) and 3-input MAJ (c) gates.

Thanks to their improved expressive power, transistors with controllable polarity enable compact realizations for XOR- and MAJ-dominated circuits, that can be largely found in arithmetic systems. Unfortunately, traditional design methodologies are not always able to identify these primitives, thereby missing interesting design perspectives. In the following, we review two techniques developed to natively assess the performances of controllable-polarity devices.

III. Biconditional Binary Decision Diagrams

In this section, we report on a novel decision diagram able to natively abstract the functionality of controllable-polarity devices.

A. Generalities

As described before, many emerging devices can act as comparators. Therefore, we may try to naturally harness such logic functionality with a novel logic representation. We report on *Biconditional Binary Decision Diagrams* (BBDDs) that are a class of BDDs based on the biconditional expansion of two variables [11]. The biconditional expansion is defined as:

$$f(x,y,\ldots,z) = (x \oplus y).f(\bar{y},y,\ldots,z) + (\overline{x \oplus y}).f(y,y,\ldots,z)$$

and naturally model the comparator behavior of a controllable-polarity device. Such decomposition embeds the XOR functionality and makes the diagrams that exploit its functionality remarkably compact for arithmetic operations. A decision diagram node relying on the biconditional expansion is given in Fig. 3. Each non-terminal node in a BBDD has a branching condition biconditional on two variables. We call these two variables *Primary Variable* (PV) and the *Secondary Variable* (SV).

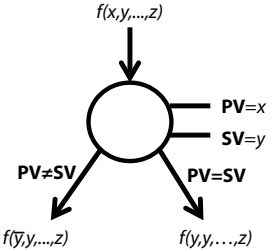

Fig. 3: BBDD *non-terminal* node [11].

B. Elementary Properties of BBDDs

BBDDs exhibit interesting properties for *Electronic Design Automation* (EDA). We report in this section on the canonicity property and some interesting theoretical bounds.

1) Canonicity

Many decision diagrams are a must in modern EDA tasks, such as logic synthesis or verification, because of their canonicity, i.e., the uniqueness of the structure for a given logic function. BBDDs are canonical under some order and reduction conditions. To correctly order a BBDD, one can impose a variable order for PVs and follow the *Chain Variable Order* (CVO) rule given in [11] to assign variables on the SVs. For convenience, the CVO, given an order $\pi = (\pi_0, \pi_1, \ldots, \pi_{n-1})$ of the inputs, is reported as the following:

$$\begin{cases} PV_i = \pi_i \\ SV_i = \pi_{i+1} \end{cases} with\ i = 0,1,\ldots,n-2; \begin{cases} PV_{n-1} = \pi_{n-1} \\ SV_{n-1} = 1 \end{cases}$$

From an ordered BBDD, it is possible to apply a set of transformations to reduce the number of nodes used by the diagram. Therefore, a reduced BBDD follows the following rules:

R1) It contains no two nodes, root of isomorphic subgraphs.
R2) It contains no nodes with identical children.
R3) It contains no empty levels.
R4) Subgraphs representing single variable functions degenerates into a single BDD driven by a traditional Shannon's expansion.

A BBDD ordered by the CVO and reduced according to these rules has been shown to be canonical in [11].

2) Theoretical Bounds

Intrinsically embedding the XOR primitive, BBDDs have been shown remarkably compact for some arithmetic functions. In [11], theoretical bounds have been drawn for adders and majority functions. While the demonstration is not reported here for the sake of simplicity, we would like to point out that a n-bit binary adder function has $3n+1$ nodes as compared to $5n+2$ nodes for standard BDDs [12]. This leads to a gain of about 40% nodes compared to state-of-the-art DDs. Similar results are also reachable for n-bit majority (n odd) functions.

C. Interest for Controllable-Polarity Devices

Well supported by an efficient manipulation package [13], BBDDs can efficiently exploit the properties of controllable-polarity devices at the logic synthesis level. Indeed, they are able to identify portions of circuits that require arithmetic operators more often than traditional methodologies.

Furthermore, one can note that there exists a one-to-one correspondence between BBDD nodes and controllable-polarity devices, as

illustrated in Fig. 4. It then becomes interesting to consider *One-Pass logic Synthesis* (OPS) techniques to build on-the-fly novel gate structures that embed the XOR operation.

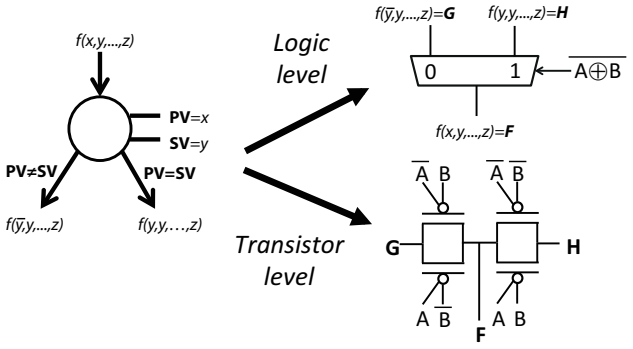

Fig. 4: Direct correspondance between a BBDD node and its realizations at both logic and transistor levels [11].

IV. MIG: Majority-Inverter Graphs

In this section, we report on a technique that exploits majority operator as a core logic representation. Therefore, we expect to leverage the performances of controllable-polarity devices that efficiently implement a majority primitive.

A. MIG Logic Representation

With the objective of extending the capabilities of standard NAND/NOR representations towards both arithmetic and control logic, we present *Majority-Inverter Graph* (MIG). An MIG is a logic network comprised of only 3-input majority primitives. MIG is a universal representation form that includes *And-Or-Inverter Graph* (AOIG), as proven in [14] and illustrated in Fig. 5.

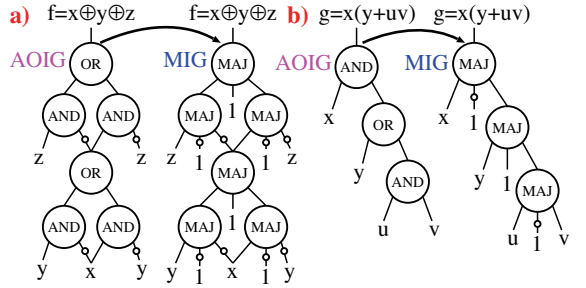

Fig. 5: Examples of MIG representations for $f=x\oplus y\oplus z$ (a) and $f=x(y+uv)$ (b) derived from their optimal AOIG representations [11].

In principle, MIGs can be manipulated using traditional AND/OR techniques. However, the potential of MIGs goes beyond standard AOIGs and, in order to unlock their full expressive power, a new Boolean algebra, natively supporting the majority/inverter functionality was introduced. The novel Boolean algebra is defined over the set $(\mathbb{B},M,',0,1)$, where M is the majority operator of three variables and $'$ is the complementation operator. The following set of five primitive transformation rules is an axiomatic system for $(\mathbb{B},M,',0,1)$ that enables an efficient manipulation of MIGs:

1- Commutativity: $M(x, y, z) = M(y, x, z) = M(z, y, x)$
2- Majority: $if(x = y), M(x, y, z) = x = y; if(x = y'), M(x, y, z) = z$
3- Associativity: $M(x, u, M(y, u, z)) = M(z, u, M(y, u, x))$
4- Distributivity: $M(x, y, M(u, v, z)) = M(M(x, y, u), M(x, y, v), z)$
5- Inverter Propagation: $M'(x, y, z) = M(x', y', z')$

B. Opportunities for Controllable-Polarity Devices

Thanks to the presented axiomatic system, applying simple transformations on an MIG, representing a Boolean function, ultimately consists of its transformation into a different MIG, with better figures of merit in terms of area (size), delay (depth), and power (switching activity). In [14], the application to logic synthesis produced competitive results, as compared to elaborated state-of-the-art techniques, thanks to the expressive power of MIGs and their associated algebra. Indeed, there exist logic circuits, for which traditional optimization reaches its limits while the proposed methodology can optimize further. In particular, MIGs open the opportunity for efficient synthesis of datapath circuits, where majority logic is dominant, and we can therefore envisage many advantageous use of MIG for controllable-polarity devices synthesis.

V. Conclusion

In this paper, we comment on a novel and promising class of semiconductor devices that exhibit an enhanced functionality. In particular, devices with a dynamic control of the polarity have been recently demonstrated. These devices act naturally as a comparator and present many compelling interests for realizing arithmetic circuits based on XOR and MAJ operators. Unfortunately, current logic synthesis techniques do not support well these operators and many advantages of controllable-polarity devices are lost during automated design. We then reviewed two interesting body of work that aim at fully unlocking these opportunities: *Biconditional Binary Decision Diagram* (BBDD), which uses a comparator as its core logic expansion, and *Majority-Inverter Graph* (MIG), which extends standard *And-Or-Inverter Graph* and supports a powerful algebra.

Acknowledgments

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