

Novel Grid-based Power Routing Scheme for Regular Controllable-Polarity FET Arrangements

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Abstract—Polarity-controllable transistors have emerged in the last few years as an adequate successor of current CMOS FinFETs. Due to the additional polarity terminal, novel physical design techniques are required. We present a novel grid-based power routing scheme able to mitigate the polarity terminal impact. The logic cells are organized in regular arrangements and easily configured using the novel power routing scheme. The impact of the placement and routing techniques used is gauged in terms of routing metal distribution, speed and area performance. Benchmark circuits are synthesized, placed and routed using commercial tools and performances are extracted. Post place and route results show 28% faster circuits compared to 22nm FinFET regular layout-based designs.

I. INTRODUCTION

The performance and power consumption limits of modern *Complementary Metal Oxide Semiconductor* (CMOS) devices are projected to be reached within this decade [1]. This motivates the study of new emerging devices that can complement and even replace current CMOS. One of the most promising candidates to replace standard CMOS devices is the *Silicon Nanowire Field Effect Transistor* (SiNWFET), that shows great electrostatic channel control and consequently superior scalability properties [2]. Furthermore, the addition of a second gate terminal of SiNWFETs enables the control of the intrinsic ambipolar conduction (otherwise considered a parasitic effect on standard technologies), giving to the device the ability to be on-line configured as a *n*- or *p*-type device. The controllable polarity gives them an advantage in terms of compact implementation of binate functions [3].

The added freedom of controllable polarity comes at a cost of adding an extra terminal to each device. This terminal, mostly called *Polarity Gate* (PG), has to be considered from a physical design perspective since it may affect the routing complexity of the gates and of the design in general. To mitigate this effect, regular organization of devices, referred to hereafter as *tiles*, reduce the number of terminal to route by sharing them at the active layer [4]. Tiles are subsequently configured by routing logic signals and power lines to their different terminals.

Implementing gates with polarity-controllable devices carries the advantage of the absence of segregated pull-up and pull-down networks. Since, both types of conduction are implemented by the same device, the flexibility of logic designing is increased. However, this comes again at a cost of sparse power/ground connectivity of the transistor nodes. Consequently, the standard power distribution scheme (i.e.,

alternating stripes of V_{DD} and GND) cannot be easily defined, as compared to standard cell methodology.

In this paper, we present a new power distribution scheme, where power supplies are distributed to basic gates through a regular mesh arrangement. This approach was first presented in [5]. Here, we propose a complete study of its impact on the metal distribution and performance of designs using SiNWFETs compared to standard approaches. We investigate how the use of an extra metal layer for power routing affects the the actual interconnection routing of designs. We benchmark the performance in terms of critical delay, area and routing complexity. We investigate various cases of benchmarks and we show that SiNWFET implementation has no impact on the routing of the design. Also, we show that using the proposed power routing scheme, SiNWFETs can lead to designs $\sim 28\%$ faster, compared to 22nm FinFET regular layout-based designs.

The remainder of this paper is organized as follows. In Section II, we present the state-of-the-art in physical design of SiNWFETs. In Section III, we present the configurations done in cell level and their impact in various parameters, compared to a regular layout FinFET cell library. Design-level results and comparisons in terms of performance, area and routing metal distribution are shown in Section IV followed by conclusions in Section V.

II. BACKGROUND AND MOTIVATION

First reported in [6], Silicon Nanowire FETs are *Double-Gate* (DG) *Gate-All-Around* (GAA) devices formed by a vertical stack of Si nanowires that act as channels connecting two pillars (the source and drain terminals). As shown in Fig. 1, the transistor has two gates: the *Control Gate* (CG), which turns the device *on* and *off* and the *Polarity Gate* (PG) that tunes the conduction of the channel from *n*- to *p*-type and vice-versa. For a complete discussion of the device fabrication and physics, we refer the reader to [7].

SiNWFET devices present a particular interest in terms of logic and circuit design. The enhanced functionality given by the PG enables a bi-conditional control of the *on/off* state of the device. This bi-conditionality is fully leveraged in implementing binate logic functions. In particular, a 2-input XOR gate reduces to only 4 transistors with this technology [3], open in new opportunities for arithmetic logic.

To leverage this compactness at the system level, it is required to mitigate the impact of the 4th terminal from a

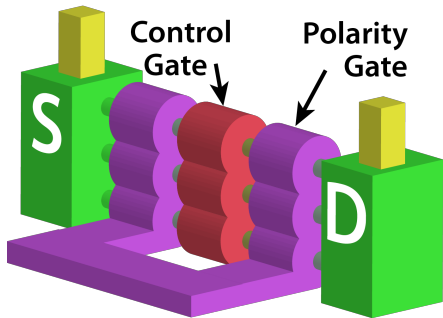


Fig. 1: Conceptual drawing of the SiNWFET and the associated device symbol. Source/Drain pillars (green) support a vertical stack of nanowires. The nanowires are surrounded by GAA Polarity Gate (violet) and Control Gate (red) [7].

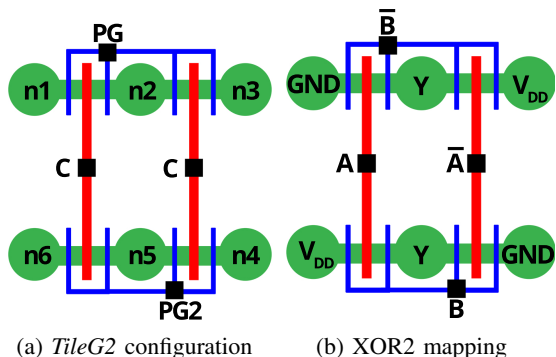


Fig. 2: Representation of the *TileG2* configuration consisting of 4 SiNWFETs and an example showing a XOR2 implementation.

physical design perspective. A regular approach, called *Sea-of-Tiles* (SoT) [4] arranges the devices in simple blocks that physically share a part of their terminals. While many different structures can be derived, we focus this work on the basic *TileG2* [4], depicted in Fig. 2a. It consists of 4 SiNWFETs paired according to their PG and CG. Fig. 2b presents an example configuration of the *TileG2* to a 2-input XOR gate.

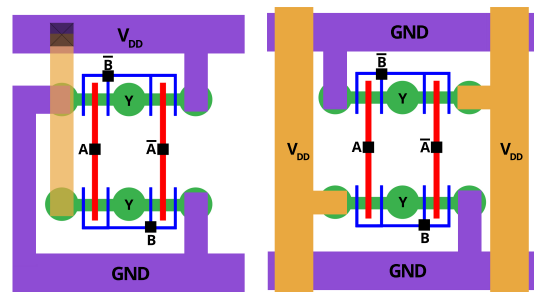
III. GATE-LEVEL IMPACT OF POWER ROUTING SCHEMES

In this section, we first introduce a two-metal layers routing scheme and then study its impact as compared to a regular layout FinFET approach.

A. Grid-based Power Routing Scheme

The configuration of a tile requires many terminals to be polarized at fixed biases. Therefore, the mapping of logic functions on regular tiles comes at a cost of an increasing complexity of power distribution, because the nodes connected to power signals have no localized distribution among the tiles. The irregularity of power signals connections becomes even more significant when a gate implementation requires multiple tiles to be interconnected. Approaching the power distribution of tile-based gates with the standard power routing schemes of horizontal rails on the same metal layer will induce an

unwanted gate-internal routing complexity as illustrated in Fig. 3a. An alternative power routing scheme is then proposed and shown in Fig. 3b. Such a scheme was first sketched in [5]. This power routing distributes one of the power signals (here V_{DD}) with vertical rails of metal2, in order to decongest the local routing interconnections of fixed polarity biases. As in standard power routing approach, the power rails are shared among neighboring tiles.



(a) Power routing used with standard cell libraries. (b) Grid-based power routing scheme.

Fig. 3: Standard (a) and grid-based (b) power routing schemes. Metal1 is represented in purple and metal2 in orange. The use of an extra layer of metal (metal2) reduces the routing complexity of regular tile implementations.

Thanks to the immediate access of the internal nodes to the power rails, the configuration of both unate and binate functions can be achieved without variations of complexity. However, relieving the routing complexity on the internal gate level may lead to increasing complexity on the design routing level. Indeed, using an extra metal layer for power routing means that we decrease the amount of metal2 that can be used for routing between gates. The gate-level and design-level study presented in the following section, show how the the power routing scheme choices affect the performance of the designs.

B. Tile Configurations

In order to test the impact the power routing scheme, we created two kinds of tile configurations suited to each scheme. These two configurations are named SiNWFET1 and SiNWFET2. SiNWFET1 consists of a *TileG2* placed between two horizontal metal1 rails that serve as power/ground pins. This configuration implements the standard horizontal power routing.

SiNWFET2 is again using a *TileG2* configuration but with the alternative power routing, where a vertical metal2 pin exists on the side of each tile to connect one of power signals. Furthermore, an auxiliary horizontal metal1 line is placed on the upper side of the tile, used to propagate the metal1 power signal on both sides (upper/lower) of all tiles to ensure the regular connectivity dictated by the grid-based power distribution network.

Both tile configurations were sized in order to allow enough routing space (for all metal layers) through the gates. More specifically, the gap between the two ‘rows’ of transistors in

each tile is enough to let 3 horizontal metal lines go through it. Also the whole tile structures are placed in appropriate coordinates so that enough space is left between two adjacent tiles for metal2 lines to be passed through.

Comparing the two configurations, SiNWFET2 is larger on both dimensions (15% wider and 20% taller), since it involves more fixed metal routes for power routing. These two tile configurations are used to create two SiNWFET libraries respectively, where all gates/cells are implemented using the *TileG2* approach.

C. Library Experimental Comparison

This part presents the methodology and results of comparing the cell libraries created using the aforementioned tile configurations and regular layout 22nm FinFET library.

1) *Methodology*: In order to fairly judge the routability and performance of the SiNWFET libraries, we created a FinFET 22nm library whose cells are implemented using regular layout techniques [8]. The two SiNWFET libraries differ in the power distribution network. Hereafter, the FinFET library is called plainly ‘CMOS22’ and the two tile-based libraries SiNWFET1 and SiNWFET2 according to their tile configuration.

All three libraries were generated using a custom tool that utilizes the output mappings of a SoT mapping tool [9]. Running this tool recursively for all cell mappings of the library ultimately creates the complete set of cell descriptions.

2) *Results*: The most important comparison, in order to quantify the differences among these three libraries is to analyze the distribution of the area of an average cell (single or multi-tile). Initially, we note that unate gates are smaller with standard CMOS. Indeed, a simple inverter cell occupies $0.8064\mu\text{m}^2$ in the CMOS22 library while, in the SiNWFET2 library, it occupies $1.3968\mu\text{m}^2$. However, binate gates take advantage of SiNWFET compactness. For instance, XOR2 cell occupies $3.2256\mu\text{m}^2$ in CMOS22 but $2.7936\mu\text{m}^2$ in SiNWFET2. Fig. 4 presents the average area breakdown of logic cells belonging to the different libraries. The area of a tile can be categorized into four domains, I/O pin, power/ground (PG) pin, actual routing (considered as obstruction zone - OBS) and free space. Note that the distributions of each library are normalized with their respective tile size.

As we can see, the FinFET approach leaves on average 53% of the cell’s area free and limits the intra-cell routing to a very small percentage. The other half of the area is covered by pins (either I/O or power pins). This approach maximizes the connectivity of each cell and enables a better optimization in the P&R stage. Comparing the FinFET library to the first SiNWFET library (with standard power routing) the free (routable) area is decreased in half and the intra-cell routing’s area is more than four times larger. This is a direct representation of the gate-level routing complexity when using tile configurations with standard power routing.

However, the impact of SiNWFETs in terms of routability is improved when we consider the alternative power routed library, where the free space is increased almost to 50%. This makes SiNWFET2 library to be on average more routable than

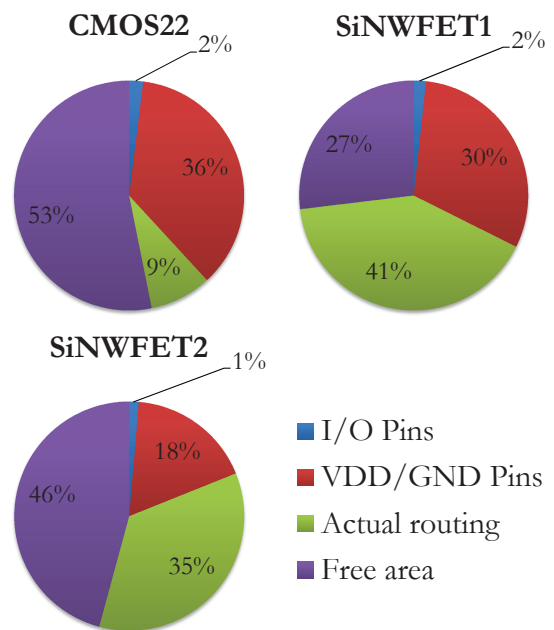


Fig. 4: Average area distribution of the created cell libraries.

SiNWFET1. This is a useful observation, highlighting the fact that the proposed power routing, not only decongests internal cell routing but also leaves more routable space for the P&R phase.

IV. DESIGN-LEVEL ANALYSIS

This section evaluates the impact of the novel routing scheme from a system-level perspective.

A. Methodology

We implemented benchmark circuits from their verilog description up to the physical level. Synthesis is done by *Synopsis Design Compiler*® using a reduced library of standard cells (NOT, NAND, NOR, XOR and DFF). The libraries are generated using 22nm design rules. Performances of the different gates are obtained by electrical simulations. The compact model for FinFET devices is taken from [10], while a custom model for the SiNWFETs is derived from the experimental measurements taken from [7].

Placement and routing steps (P&R) are done using *SOC Encounter*®. Traditional P&R tools are mostly optimized for standard cell with standard power routing methodology. In order to accommodate with the grid-based power routing we edited the operation of the special router, employed for power net connections. The performance of the approach is tested using combinational arithmetic benchmarks. More specifically, we employed mostly XOR-rich designs in order to exploit the binate compactness of controllable-polarity FET-based gates. We implemented a two-operand 64-bit multiplier, a three-operand 16-bit multiplier-accumulator (MAC) and a Mastrovito multiplier (used to solve to irreducible polynomial 17th degree), generated using [11]. The performance of these designs is evaluated in terms of routing metal distribution,

critical path delay and total core area. Due to the lack of accurate power models of SiNWFETs, power and corner simulations are not considered in this study.

B. Results

Performance results are extracted from post P&R reports. We comment them by first looking at routing metal distribution and then at performance analysis.

1) *Routing Metal Distribution*: Since we showed in the previous section that the tile-based cell library (SiNWFET2) is similar in terms of routability to the regular layout cell library, we now investigate the impact of the tile configuration on the distribution of interconnecting routing metal layers. Fig. 5 shows the metal distribution average for all designs. Note that only the routing area is considered in this plot. Hence, metal1 and metal2 look artificially underused as they mainly serve for the power distribution network.

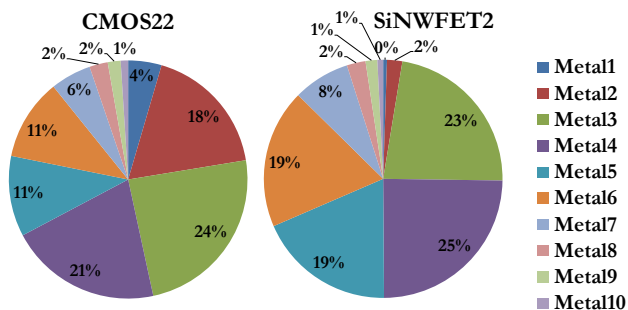


Fig. 5: Average routing metal distribution of the benchmarks implemented with the regular layout and the tile-based cell libraries.

We observe a shift of the routing metals by one layer. The shift affects only the metal layers until metal6. This demonstrates a rather local impact. In addition, the proposed power distribution scheme increases the use of these layers by only 4.2% on average that is negligible in terms of routability. Hence, we conclude that the use of the grid-based power routing scheme has no critical impact on the design-level routability. Furthermore, since the grid-based power routing introduces a denser mesh of power connections, no specific impact is expected on the electrical properties of the power distribution network.

2) *Performance Analysis*: As seen previously, the grid-based routing scheme doesn't impact the metal usage repartition. Hence, we now investigate the impact of the tile configurations on the general performance of the benchmarks. Table I presents the speed and area results of the three benchmarks normalized to the respective performance of the FinFET-implemented designs.

Considering the benchmark with a big binate ratio, i.e., with a large amount of binate gates, we observe a 26% of improvement in speed with only a 17% of area increase trade-off. This trade-off is caused by the fact that the unate gates implemented by SiNWFET are larger than their FinFET

TABLE I: Comparative performance of the benchmarks implemented with SiNWFET2 library respectively to the FinFET library.

	Binate Ratio	speed-up (%)	area+ (%)
mult64	0.431	18.441	30.133
mac316	0.464	27.978	25.767
mastrovito	1.107	26.221	17.120

counterparts, because the grid-based power routing scheme is not as compact as the standard one. The reported performance could largely improve by using specific synthesis tools that promote binate gates in circuits [12].

V. CONCLUSIONS

In this work, a novel grid-based power routing scheme able to deal with controllable-polarity devices is presented, along with a study on its impact on the performance of various designs. Through benchmarking, we show that the designs using the grid-based power routing do not get impacted from the routing metal distribution perspective compared to regular layout 22nm FinFET designs. It is also shown that it leads to excellent performance in terms of speed with a small trade-off of core area when used to implement XOR-rich designs. The grid-based power routing scheme implemented simplifies the tile cell creation and helps reaching up to 28% faster XOR-rich designs.

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