

Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-All-Around FETs

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Abstract—This letter demonstrates the first fabricated four-transistor logic gates using polarity-configurable, gate-all-around silicon nanowire transistors. This technology enhances conventional CMOS functionality by adding the degree of freedom of dynamic polarity control *n*- or *p*-type. In addition, devices are fabricated with low, uniform doping profiles, reducing constraints at scaled technology nodes. We demonstrate through measurements and simulations how this technology can be applied to fabricate logic gates with fewer resources than CMOS. In particular, full-swing output XOR and NAND logic gates are demonstrated using the same physical four-transistor circuit.

Index Terms—Ambipolar transistor, double-gate, dual-gate, gate-all-around (GAA), polarity control, silicon nanowire (SiNW), post-CMOS, top-down fabrication, XOR logic gate.

I. INTRODUCTION

THE increasing pressure to overcome conventional MOSFET physical limitations, such as short channel effects and high variability, has stimulated the engineering of a number of advanced device geometries and materials. Among these novel devices are FD-SOIs, FinFETs, Graphene, Nanowires and Carbon Nanotube based FETs, featuring quasi two- and one-dimensional channel geometries for better electrostatics. Whereas many of these innovations only focus on developing high-performance devices, the creation of a roadmap to predict in-circuit performance and large scale integration for these technologies is highly desirable [1]–[3]. Moreover, new functionalities can be exploited at scaled technology nodes. In particular, all these devices can be built to exhibit electrostatic polarity control (*n*- or *p*-type) [4], [5].

Hence, we developed silicon nanowire configurable devices (SiNWFETs), shown in Fig. 1(a–b), that can change polarity (*n*- or *p*-type) during operation by setting a polarity gate electrode (PG) bias. We chose SiNWFETs as these devices combine an efficient *gate-all-around* (GAA) geometry [6], [7]

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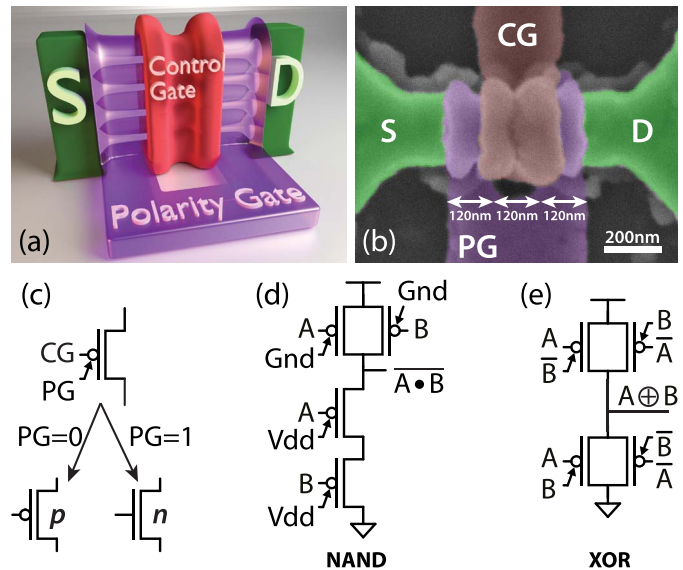


Fig. 1. 3-D conceptual view (a) of the complete device showing S/D pillars supporting a nanowire stack (green), the GAA PG (violet), and central CG (red). (b) SEM micrograph with false colors of a fabricated device. (c) Circuit symbol and (d)–(e) circuit schematics of NAND and XOR logic gates.

with the use of uniform low doping of the nanowire channel, thus reducing short channel effects and variability as no sharp doping profiles are required.

In this letter, we show measurement results of fabricated four-transistor (4T) configurable logic gates built with polarity controlled SiNWFET devices, in NAND and XOR configurations. In order to further investigate device performance, we also present TCAD simulations we performed at device and circuit level, showing simulations of NAND and XOR logic gates.

II. FABRICATION AND MEASUREMENTS

The devices comprise a vertical stack of four ~ 30 nm diameter nanowires, covered by three 120 nm long gate regions, as depicted in Fig. 1(b). A 8 nm thick gate oxide was used in this early process in order to reduce the risk of gate leakage. Details on the fabrication steps are described elsewhere [4]. Fig. 2(a) shows a SEM micrograph overlay of the 4T fabricated circuit. Large pads are used to land the measurement probes.

Thanks to dynamic polarity control, a single physical circuit with fixed polysilicon lines, consisting of 4 identical

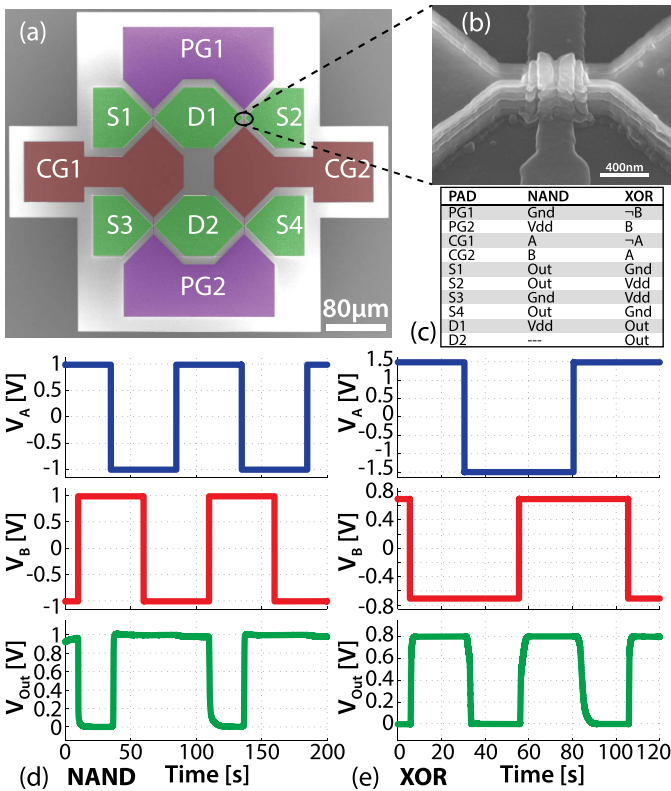


Fig. 2. Four-transistor NAND and XOR circuit measurements. (a) SEM micrograph overlay of the 10-probe measurement setup. The false colors follow the convention of Fig. 1. (b) SEM zoom-in on one of the four devices. (c) Configuration table for the fabricated tile to obtain NAND or XOR functionality. (d)–(e) time-domain measurement results for NAND and XOR configurations.

transistors, can be configured to implement various logic functions including NAND, XOR [Fig. 2(c)], NOR and minority gate (a Full Adder requiring only 8 transistors) [3] by only changing its back-end metal connections. Note that the fabricated devices do not require the use of doping wells, thus reducing constraints at layout design level.

In Fig. 2(d–e), we show measurements for the NAND and XOR configurations. We observe correct output values and full swing output voltages, demonstrating the applicability of this approach.

Measurement of the output response of the tile in the NAND configuration (circuit in Fig. 1(d)) for all the A and B input combinations shows that the output is at logic 1 (1 V) only when A and B are both at logic 0. This result demonstrates a correct NAND logic behavior. Similarly, the output of the tile configured in the XOR configuration [Fig. 1(e)] is at logic level 1 (0.8 V) only when the inputs signals are different ($A = 0, B = 1$ or $A = 1, B = 0$), justifying a correct XOR behavior. For both configurations, the output response shows full swing output voltage levels from logic state 0 (0 V) to 1 (1 V for NAND and 0.8 V for XOR). A batch of more than 20 different 4T tiles was characterized, all correctly calculating the output function. Note that, in order to obtain fully cascadable logic gates, only positive voltages would be required as inputs of the CG and PG electrodes. As previously considered in [4], this would require tuning of process parameters to obtain the desired CG and PG thresholds. Nonetheless, neither exotic materials nor advanced techniques such as strain technology

were added to the presented structure. However, these improvements are indeed applicable to the analyzed structures, giving a range of opportunities for device tuning.

Moreover, note that the DG device geometry imposes a difference in input/output capacitances for PG and CG structures, with the PG being more capacitive as it covers a longer channel length. As shown in Section III-B, this translates into two different intrinsic delays for a transistor. The PG capacitance becomes relevant only when the PG is fed by a logic input and not pre-set to a fixed bias voltage, i.e., in the case of binate (e.g., XOR) functions. However, since an XOR/XNOR function is symmetric to its inputs, this effect can be minimized by feeding all PGs by signals on non-critical delay paths and with the lowest switching activity of the two. Moreover, in our implementation, contrarily to standard CMOS, no transistor series are found in the PUN and PDN of XOR logic gates. Thus, all transistors can be sized to the minimum technology size, directly leading to an overall reduction in transistor sizing and gate capacitance compared to standard CMOS. For a complete review on design opportunities regarding scalability and resource utilization compared to CMOS, we refer the reader to our previous work on circuit architectures with the presented technology [3].

III. PERFORMANCE INVESTIGATION THROUGH SIMULATIONS

In order to better evaluate device properties and expected performance in large scale circuit applications, we performed device and mixed-mode simulations using 3-D Sentaurus TCAD software.

A. Simulation Setup

The simulated transistor dimensions are the same as for the fabricated case, with three 120 nm GAA regions separated by 15 nm gaps but isolated by an optimized 1 nm equivalent gate oxide thickness. The nanowire channel is uniformly lowly p -doped ($1 \times 10^{15} \text{ cm}^{-3}$), and source and drain are defined as nickel silicide metal contacts (NiSi) at the nanowire extremities, at a distance of 5 nm from the polarity gate edges. As described in [4], the NiSi work function was set at 4.43 eV, consistently with performed measurements and providing optimal symmetry between n - and p -type operation in the simulated device characteristics.

B. Device Transfer Characteristics

Fig. 3 shows simulated $I_d V_{cg}$ (a) and $I_d V_{pg}$ (b) characteristics of the considered devices. In the case of $I_d V_{pg}$, the side regions of the channel are polarized to a p -type equivalent electrostatic doping by the high (1.5 V) PG bias. Note that the two gate structures (PG and CG) act sequentially on the carrier injection from source/drain (S/D), with the PG bias first setting the maximum current flowing through the channel, and the CG bias conventionally switching *on/off* the device. Thus, for increasing V_{cg} , current saturation is observed in Fig. 3(a) when all the carriers entering the channel at either the source or drain regions are also allowed to flow through the CG region. Nonetheless, at high V_{ds} biases (> 2.5 V) and low PG biases (< 1.5 V), strong leakage is observed in the channel. This is mainly due to the thinning of the Schottky barrier at the drain, that allows holes to flow through the channel without being stopped by the CG barrier, resulting in a strong

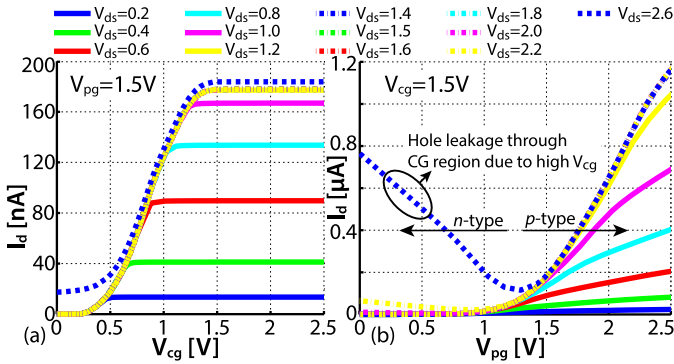


Fig. 3. Simulated $I_d V_g$ plots at different V_{ds} . (a) $I_d V_{cg}$ characteristics and (b) $I_d V_{pg}$ characteristics. Due to the asymmetry in geometry, different threshold voltages are expected in the two characteristics.

ambipolar behavior. In terms of circuit performance, the two gate structures have different influences on the channel, both in terms of geometry (length) and influence on the Schottky barriers. This directly translates into different fingerprints (see Fig. 3) for the two $I_d V_g$ characteristics, with the $V_{T,pg}$ threshold being significantly higher (~ 1.4 V) than the $V_{T,cg}$ threshold (~ 0.5 V). As shown in the next section for the XOR logic gate, therefore, differences in output delays are observed between the cases of the CG or PG input transitions.

C. Logic Gate Simulation

In order to predict dynamic performance of the measured circuits, we performed mixed mode circuit simulations of 4T logic gates. Note that, due to the geometry of this device, stray capacitances between the CG and PG gate electrodes will influence performance when driven by the output of another gate. Therefore, we first performed capacitance simulations using 3D Sentaurus TCAD software, obtaining CG to PG capacitances in the range of $[2 \times 10^{-16}, 7 \times 10^{-16}]$ F for wire diameters between 30 nm and 80 nm and a gate-to-gate polysilicon contact distance of 10 nm. Thus, Fig. 4(a) shows the output of a NAND logic gate (circuit in Fig. 1(d)) for output load capacitances in the range $[10^{-16}, 5 \times 10^{-15}]$ F. Calculated delays at 50% V_{dd} for $C_L = 10^{-16}$ F are 31 ns and 9.7 ns for falling and rising transition, respectively. In this case, all transistors are pre-polarized by setting fixed biases to the PGs (V_{dd} for n -type and Gnd for p -type). Thus, differences in delays are mainly due to the presence of a 2-transistor series in the *pull-down* network as in standard CMOS design. In Fig. 4(b), the output of a XOR logic gate is shown for all input configurations and for the same C_L range as for the NAND gate. Significantly lower delays at 50% V_{dd} for $C_L = 10^{-16}$ F are obtained compared to the NAND case, with delays of 2.8 ns for the falling output transition (triggered by switching of the CG biases) and 11 ns for the rising output transition (triggered by a switching of the PG biases). In this case, we attribute the delay difference to the asymmetry in $I_d V_g$ fingerprints between the PG and CG inputs (Fig. 3). Furthermore, the XOR circuit exhibits an interesting feature due to the presence of two transistors switching at the same time both in its *pull-up* and *pull-down* networks. Specifically, at any time, one transistor is correctly polarized (i.e., $p(n)$ -type in the *pull-up(down)* network), conventionally driving the output. The other transistor, ($n(p)$ -type, respectively), will also turn *on* at the beginning of the transition, effectively boosting output switching. Only later, this transistor will see a

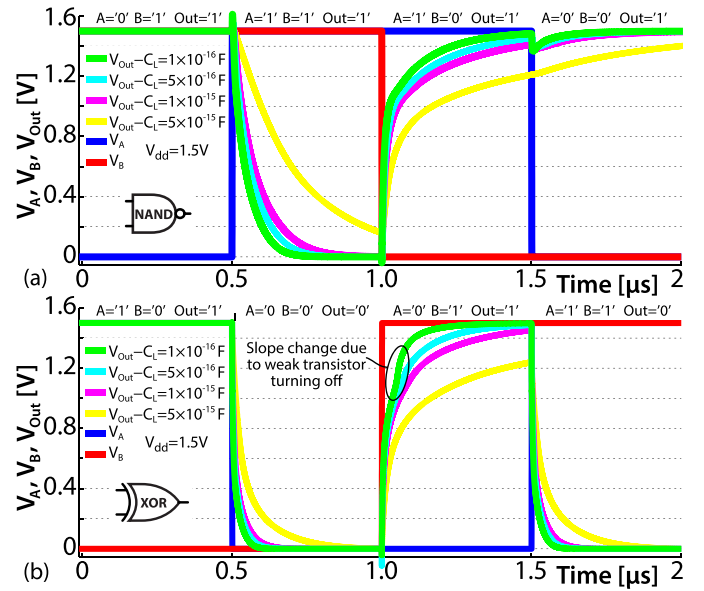


Fig. 4. Transient simulation for the 4-transistor (a) NAND and (b) XOR logic gates with 1 ns input rise/fall times.

decreasing V_{pg-s} while V_{out} rises, and will turn *off* before the end of the transition. Nonetheless, a faster response is observed at the gate output. This can be seen in Fig. 4(b), where a slope change can be observed when the output approaches its final bias voltage. As a consequence, the simulated XOR is about $3 \times$ faster than the NAND, further demonstrating the advantage of this technology over CMOS in implementing complex functions.

IV. CONCLUSION

Devices for the post-CMOS era have to integrate new degrees of freedom which can relax constraints at the physical and design levels. In this work, we evaluated SiNWFET devices and integrated circuits combining an efficient GAA channel geometry and the added degree of freedom of polarity control without requiring wells nor sharp doping profiles. With this technology, we presented a further step in the roadmap to large scale integration. We measured and simulated 4T circuits using this technology, showing full swing output operation of NAND and XOR fabricated circuits by configuring the same physical tile.

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