

Efficient Arithmetic Logic Gates Using Double-Gate Silicon Nanowire FETs

Luca Amarú, Pierre-Emmanuel Gaillardon, Giovanni De Micheli
Integrated Systems Laboratory (LSI), EPFL, Switzerland.

Abstract— *Silicon NanoWire* (SiNW) based *Field Effect Transistors* (FETs) are promising candidates to extend Moore’s law in the coming years. Recently, *Double-Gate* (DG) SiNWFETs have been demonstrated to allow on-line configurability of *n*-type and *p*-type device polarity through the second gate. Such feature enables novel compact realizations for XOR- and MAJ-based logic gates that are intensively used in arithmetic applications. In this paper, we present a complete design framework of DG-SiNWFETs technology for arithmetic logic. We characterize and validate compact arithmetic logic gates (XOR, MAJ, FA) using circuit level simulations. SiNW-based controllable polarity transistors at 22-nm technology node, first characterized at the physical level with Synopsys Sentaurus, enable a full-adder implementation about 3.8x faster than its CMOS FinFET 22-nm counterpart, according to HSPICE circuit simulations. Then, we study the application of these arithmetic gates in the automated synthesis of datapath circuits which are dominated by arithmetic operations. Experimental results show that datapath circuits synthesized in DG-SiNWFETs 22-nm technology are about 1.5x faster than in CMOS FinFET 22-nm technology while having practically the same area occupation.

I. INTRODUCTION

Arithmetic logic is critical in most of today’s *Integrated Circuits* (ICs). Indeed, arithmetic operations are the basis of datapaths that form the reasoning core of logic applications in silicon. *EXclusive-OR* (XOR) and *MAJority* (MAJ) logic functions are extensively used in arithmetic circuits, consequently their physical realization is of paramount importance to achieve efficient datapath cores in ICs. Novel *Double-Gate* (DG) transistors with on-line controllable polarity present the opportunity to implement XOR- and MAJ-based logic gates with low physical resources. Controllable polarity behavior is a desirable feature of DG devices fabricated in carbon nanotubes [1], graphene [2] and *Silicon NanoWires* (SiNWs) [3]. Among such technologies, SiNWs are a promising platform for controllable polarity transistors thanks to their high electrostatic control [3] and fabrication process compatible with the current semiconductor industry.

In this paper, we design efficient arithmetic logic gates with DG-SiNWFETs. Such gates are characterized and validated using circuit-level simulations. Considering the full-adder circuit, characterization results show that the realization in DG-SiNWFET 22-nm technology is about 3.8x faster than in CMOS FinFET 22-nm. Then, we study the application of such arithmetic gates in the design and synthesis of datapaths. For this purpose, we employ a novel synthesis flow that natively supports the logic expressive power of DG-SiNWFETs. Experimental results show that datapaths designed by the proposed

approach at 22-nm technology node, have the same area and at the same time 32.4% smaller delay with respect to their corresponding CMOS FinFET realizations.

The remainder of this paper is organized as follows. Section II introduces DG-SiNWFETs. In Section III, arithmetic logic gates are designed and characterized at circuit level. Section IV describes experimental results for datapath circuits designed and synthesized in DG-SiNWFETs 22-nm technology. The paper is concluded in Section V.

II. DOUBLE-GATE CONTROLLABLE POLARITY SiNWFETs

Double-gate controllable polarity SiNWFETs are transistors whose device polarity is configurable via the second gate. The on-line configuration of *n*- or *p*-type polarity in DG-SiNWFETs is depicted by Fig. 1(a). The *Control Gate* (CG) acts as in standard unipolar FETs, while the *Polarity Gate* (PG) controls the device polarity. A sketch of the vertically stacked SiNWs implementation of controllable polarity FETs is provided in Fig. 1(b). The PG is formed by two external gates, connected together, located near to the *Source/Drain* (S/D) contacts. In this configuration, the PGs tune the Schottky barriers at the S/D junctions choosing the channel carriers type. The CG is the central gate, and directly modulates the amount of carriers flowing into the channel. We refer the interested reader to [3] for more details about the physics of DG-SiNWFETs.

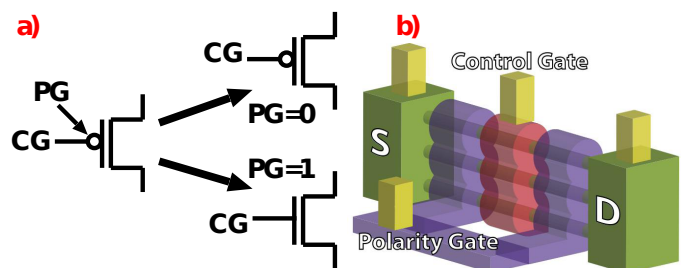


Fig. 1. On-line polarity control (a) ambipolar vertically stacked SiNWFET conceptual structure (b).

Vertically stacked SiNWs have a CMOS compatible fabrication process that can be easily integrated by the current semiconductor industry. With DG-SiNWFETs, the process complexity related to chemical doping is avoided thanks to the electrical device configurability. In addition, DG-SiNWFETs

enable a high I_{on}/I_{off} ratio [3] and also efficient regular layout opportunities [6].

III. EFFICIENT ARITHMETIC LOGIC GATES

Traditional unipolar FETs can implement an inverter with a single device [8]. However, with novel DG-SiNWFETs the 2-input XOR function is realized in a single device [3], enabling compact implementation opportunities for arithmetic and XOR-intensive logic. In the rest of this section, we discuss the design of complex arithmetic logic with controllable polarity transistors.

A. XOR-based Logic

The opportunity to have compact XOR-based logic gates with controllable polarity transistors was first exploited in [7]. In particular, the XOR-2 gate from [7] is reported in Fig. 2(a). Note that the equivalent CMOS realization employs 2x more devices [8]. The transmission-gate configuration in Fig. 2(a) permits to have always a full-voltage swing path between signal output and the power rails while embedding the XNOR logical connective. Extending the logic design style from static to pass-transistor, the XOR-3 realization introduced in [9] is obtained and depicted by Fig. 2(b).

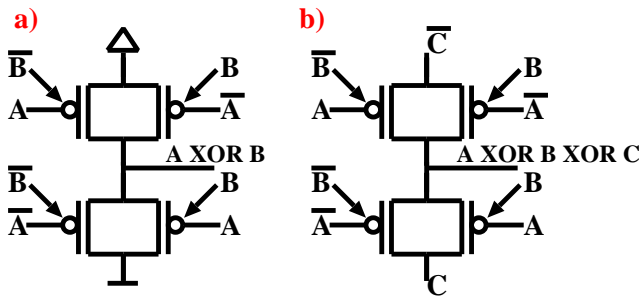


Fig. 2. Static XOR-2 gate (a) Transmission-gate XOR-3 gate (b).

B. MAJ/MUX-based Logic

Devices with controllable polarity enable not only efficient XOR-intensive logic but also compact logic gates based on the majority voting operation. In [4], a 4-transistor 3-input majority logic gate is proposed and reported here in Fig. 3(a).

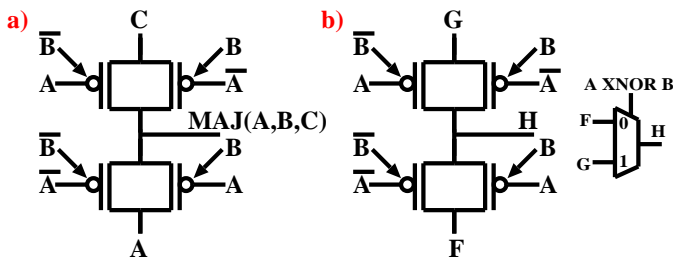


Fig. 3. MAJ-3 logic gate in transmission-gate style (a) MUX driven by a XNOR in transmission-gate style (b).

Note that in static CMOS, the same gate has 10 devices in place of 4 [8]. The 4 controllable polarity FETs configuration used in the previous logic gates can be generalized in

the MUX-like structure depicted by Fig. 3(b). Its functionality corresponds to a multiplexer driven by a XNOR signal, namely $A \oplus B$, selecting between two external signal G and F . With different assignments of G and F it is possible to reproduce MAJ ($G=C, F=A$), XOR-3 ($G=\bar{C}, F=C$) and XOR-2 ($G=1, F=0$) logic gates. Therefore, the MUX-XNOR gate can be seen as a generalized arithmetic gate.

C. Full-adder

The full-adder is a widely used arithmetic circuit that supports the addition of two binary numbers. It is represented by the following 3-input 2-output logic function: $Sum = A \oplus B \oplus C$ and $C_{out} = \text{MAJ}(A, B, C)$. Controllable polarity transistors offer an advantageous implementation for both the Sum and C_{out} functions, therefore, the full-adder is competitively realized with 8 devices, input inverters apart, as depicted by Fig. 4. The corresponding static (transmission-gate) CMOS version has 28 (14) transistors [8].

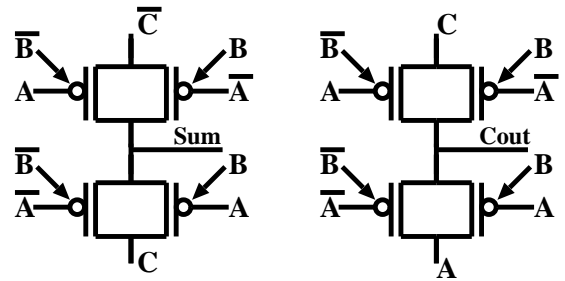


Fig. 4. Full-adder with 8 controllable polarity devices.

D. Characterization and Validation

The presented logic gates are characterized and validated using circuit-level simulations. Controllable polarity devices are vertically-stacked DG-SiNWFETs at 22-nm technology node. The transistors are characterized using Synopsys Sentaurus and the obtained results are employed to create a simple table model. Then, this model is embedded in the HSPICE circuit simulator. Simulated waveforms for the MAJ-3 ambipolar gate (Fig. 3(a)) are shown in Fig. 5. The power supply voltage is set to 0.9 V according to the 22-nm technology node typical working point.

For the sake of comparison, XOR-2 and full-adder logic gates are simulated also in CMOS HP FinFET 22 nm technology using the model available from [10]. The electrical models of FinFETs and DG-SiNWFETs are calibrated to reach the same on-current target in order to provide a fair comparative study. Simulation results are presented in Table I. For DG-SiNWFET technology, only result for the MUX-XNOR gate are presented since the other gates can be seen as its special case configurations (and duplication in the case of the full-adder). In the proposed study, gate-level interconnects are not considered during simulations. Note that the inherent increase of wiring complexity with DG-SiNWFETs can be handled by physical design [6].

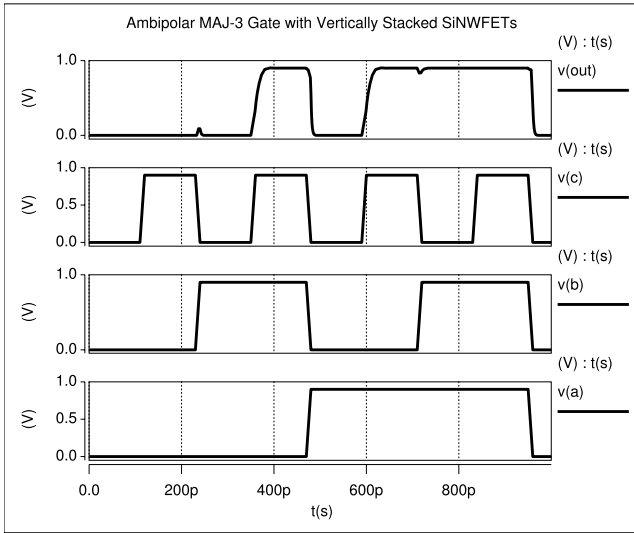


Fig. 5. Simulation waveforms for the MAJ-3 gate with double-gate controllable polarity SiNWFETs.

TABLE I
HSPICE SIMULATIONS FOR ARITHMETIC GATES

Technology	Logic Gate	Load Capacitance	Delay 50%	Area
SiNWFET 22nm	MUX-XNOR	0.5 fF	15.02 ps	0.45 μm^2
FinFET 22nm	XOR-2	0.5 fF	18.11 ps	0.42 μm^2
FinFET 22nm	Full-Adder	0.5 fF	57.62 ps	0.85 μm^2

The area of the 4-transistor DG-SiNWFET configuration is 0.45 μm^2 and its worst case delay, under a load of 0.5 fF, is 15.02 ps. In FinFET technology, the area of a XOR-2 gate is slightly lower than in DG-SiNWFET technology, 0.42 μm^2 , but its worst case delay is larger, about 18.11 ps. Indeed, the area of a single DG-SiNWFET device is larger than its FinFET counterpart, at the same technology node, due to the presence of extra gates for the electrical polarity control. In the case of the full-adder, again the area of CMOS FinFET and DG-SiNWFET is comparable, 0.85 μm^2 and 0.90 μm^2 respectively, but DG-SiNWFET technology is faster achieving a speed-up factor of about 3.8x with respect to CMOS FinFET.

IV. DATAPATH SYNTHESIS OPPORTUNITY

Datapath circuits are rich in XOR and MAJORITY functions. The compact implementations of XOR and MAJ operators with ambipolar SiNWFETs bear a promise for superior datapaths realizations. However, conventional logic synthesis tools are not adequate to fully harness the advantage led by the controllable polarity feature in arithmetic logic, missing some optimization opportunities. In this section, we first introduce the application of a novel synthesis methodology [5] to natively support the XOR and MAJ operators that are very efficient with controllable polarity transistors. Then, we present and compare experimental results for the synthesis of datapath circuits in DG-SiNWFET and FinFET technologies.

A. BDS-MAJ

BDS-MAJ [5] is a decomposition system based on binary decision diagrams and supports integrated MUX, XOR, AND, OR and MAJ logic decompositions. The logic decomposition features provided by BDS-MAJ represent an effective alternative to synthesize datapath circuits when compared to standard optimization techniques. Indeed, considering datapath circuits, traditional optimization methods are very efficient for AND/OR operations while they may be not satisfactory for XOR and MAJ functions. BDS-MAJ instead has an extended efficiency for MUX, XOR, AND, OR and MAJ logic structures. In Fig. 6, the main steps of BDS-MAJ are shown. First,

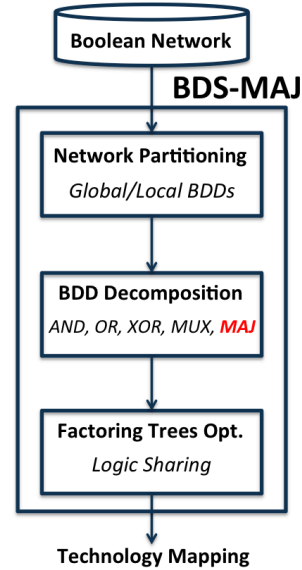


Fig. 6. BDS-MAJ synthesis flow targeting datapath circuits.

a network partitioning phase decomposes the initial logic circuits in local BDDs when a single monolithic BDD is too large to be manipulated. Then, the core BDD decomposition engine generates a logic circuit (made of factoring trees) consisting only of AND, OR, XOR, MUX and MAJ nodes. Finally, logic sharing between factoring trees is detected to further optimize the logic circuit. After the BDS-MAJ decomposition, a technology mapping approach based on Boolean matching can complete the synthesis flow and preserve the highlighted XOR and MAJ functions intensively used in datapaths.

B. Experimental Results

We present hereafter the results for DG-SiNWFETs employed in the automated synthesis of datapath circuits. We provide a comparison with CMOS FinFET implementations.

1) *Methods*: BDS-MAJ is employed to synthesize datapaths in DG-SiNWFET technology in a traditional *optimization-mapping* flow. To this end, a simple arithmetic standard cell library consisting of FULL-ADDER, MAJ-3, XOR-2, XNOR-2, XOR-3, NAND-2, NOR-2 and INV logic gates is characterized for DG-SiNWFET 22-nm technology and also for CMOS FinFET 22-nm technology. Technology mapping after

TABLE II
DATAPATH SYNTHESIS, AMBIPOLAR SiNWFETS vs. CMOS FinFET, 22NM TECHNOLOGY NODE

Benchmark	Ambipolar SiNWFET									CMOS FinFET		
	BDS-MAJ			BDS-PGA			ABC			ABC		
	Area	Gate count	Delay	Area	Gate count	Delay	Area	Gate count	Delay	Area	Gate count	Delay
	μm^2	G.C.	ns	μm^2	G.C.	ns	μm^2	G.C.	ns	μm^2	G.C.	ns
MCNC Benchmarks												
alu2	37.89	180	0.26	60.53	287	0.28	95.85	469	0.33	66.50	503	0.41
C6288	415.59	1272	0.70	434.62	1409	0.80	428.79	1443	0.79	355.18	1350	1.08
C1355	65.11	186	0.18	67.71	197	0.20	69.08	204	0.19	60.69	213	0.29
dalu	169.22	838	0.24	372.36	1748	0.35	362.97	1711	0.33	171.36	1292	0.44
apex6	144.43	720	0.18	165.73	812	0.21	160.22	790	0.20	100.73	733	0.26
vda	112.21	569	0.20	168.74	837	0.18	218.79	1068	0.18	133.56	1035	0.20
f51m	18.47	77	0.11	19.89	86	0.13	33.24	160	0.14	26.18	199	0.17
misex3	272.36	1349	0.26	373.34	1840	0.24	355.41	1759	0.24	225.12	1753	0.28
seq	457.39	2275	0.25	794.10	3831	0.21	790.57	3841	0.20	488.32	3678	0.26
bigkey	686.10	3585	0.19	827.44	4116	0.21	845.40	4230	0.18	713.79	5692	0.22
Average	237.87	1105.10	0.25	328.44	1516.30	0.28	336.05	1567.50	0.28	234.14	1644.80	0.37

BDS-MAJ logic optimization is performed in two steps. First, MAJ, XOR and XNOR nodes are directly assigned to logic cells in order to preserve such highlighted functions, otherwise potentially hidden by standard technology mappers. Then, the rest of the logic circuit is mapped using ABC [13] mapper. BDS-MAJ synthesis flow is compared to academic ABC [13], BDS [11] (BDD-based decomposition without majority logic) academic synthesis tools. CMOS benchmarks are synthesized by ABC. Defaults and options for ABC and BDS flows are:

- ABC: ABC *resyn2* optimization script and ABC mapper.
- BDS: BDS logic optimization and ABC mapper.

The logic circuit benchmarks employed are arithmetic circuits taken from the MCNC suite.

2) *Results*: Table II summarizes experimental results for datapath synthesis in DG-SiNWFET and CMOS FinFET 22nm technologies. Using DG-SiNWFETs, the average area of datapath circuits synthesized by BDS-MAJ is $237.87 \mu\text{m}^2$. BDS and ABC synthesis flows produce circuits that are 27.5% and 29.2% bigger, respectively. In CMOS FinFET technology, the area is practically the same as for circuits synthesized by BDS-MAJ with DG-SiNWFETs. Considering the delay, the advantage of DG-SiNWFET technology with respect to CMOS becomes evident. DG-SiNWFET datapaths synthesized by BDS-MAJ have on average a delay of 0.25 ns while the CMOS versions are 48% slower.

3) *Discussion*: Arithmetic logic gates based on controllable polarity transistors are more compact than their traditional CMOS counterparts. When employed in the synthesis of datapath circuits, compact arithmetic logic gates enable the opportunity to have faster realization of arithmetic operations that are the basis of silicon computation. To fully exploit this potential, we employed a novel synthesis methodology, BDS-MAJ, to natively highlight the efficient implementation of arithmetic gates with controllable polarity devices. As a result, the datapath circuits synthesized in DG-SiNWFET technology are on average 32.4% faster than in CMOS FinFET while having practically the same area requirement.

V. CONCLUSIONS

We presented in this paper the efficient realization of arithmetic functions with controllable polarity DG-SiNWFETs. We characterized and validated, through circuit-level simulations, arithmetic logic gates based on DG-SiNWFETs. Such gates are employed later in the synthesis of datapath circuits that are dominated by arithmetic operations. To fully harness the potential of DG-SiNWFETs during logic synthesis, we adapted a novel synthesis flow that natively supports the logic expressive power of controllable polarity devices. Experimental results show that datapath circuits in DG-SiNWFET 22-nm technology are on average 32.4% faster than in CMOS FinFET 22-nm technology while requiring practically the same area occupation. This result opens up the opportunity to have fast and efficient SiNW-based integrated circuits where arithmetic operations are a critical design element.

REFERENCES

- [1] Y. Lin *et al.*, *High-Performance Carbon Nanotube Field-Effect Transistor with Tunable Polarities*, IEEE Trans. Nanotech., 4(5): 481-489, 2005.
- [2] N. Harada *et al.*, *A polarity-controllable graphene inverter*, Applied Physics Letters, 96(1): 012102 - 012102-3, 2010.
- [3] M. De Marchi *et al.*, *Polarity control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs*, Proc. IEDM, 2012.
- [4] L. Amaru, P.-E. Gaillardon, G. De Micheli, *Biconditional BDD: A Novel Canonical Representation Form Targeting the Synthesis of XOR-rich Circuits*, Proc. DATE 2013.
- [5] L. Amaru, P.-E. Gaillardon, G. De Micheli, *BDS-MAJ: A BDD-based Logic Synthesis Tool Exploiting Majority Logic Decomposition*, Proc. DAC 2013.
- [6] S. Bobba *et al.*, *Physical synthesis onto a Sea-of-Tiles with double-gate silicon nanowire transistors*, Proc. DAC, pp. 42-47, 2012.
- [7] M.H. Ben-Jamaa, K. Mohanram and G. De Micheli, *An Efficient Gate Library for Ambipolar CNTFET Logic*, IEEE Trans. CAD, vol. 30, pp.242-255, Feb. 2011.
- [8] J.M. Rabaey *et al.*, *Digital Integrated Circuits*, Prentice Hall, 2003
- [9] A. Zukoski, X. Yang and K. Mohanram, *Universal logic modules based on DG carbon nanotube transistors*, Proc. DAC, pp.884-889, 2011.
- [10] PTM models available online <http://ptm.asu.edu/>.
- [11] C. Yang and M. Ciesielski, *BDS: A BDD-Based Logic Optimization System*, IEEE Trans. CAD, vol. 21, pp. 866-876, July 2002.
- [12] N. Vemuri, P. Kalla and R. Tessier, *BDD-based Logic Synthesis for LUT-based FPGAs*, ACM Trans. TODAES, Vol.7, pp. 501-525, Oct. 2002.
- [13] ABC Logic Synthesis Tool [Online]. Available: <http://www.eecs.berkeley.edu/alanmi/abc/>