Vertically-Stacked Double-Gate Nanowire FETs with Controllable Polarity: From Devices to Regular ASICs

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Abstract—*Vertically stacked nanowire FETs* **(NWFETs) with gate-all-around structure are the natural and most advanced extension of FinFETs. At advanced technology nodes, many devices exhibit ambipolar behavior, i.e., the device shows *n*- and *p*-type characteristics simultaneously. In this paper, we show that, by engineering of the contacts and by constructing independent double-gate structures, the device polarity can be electrostatically programmed to be either *n*- or *p*-type. Such a device enables a compact realization of XOR-based logic functions at the cost of a denser interconnect. To mitigate the added area/routing overhead caused by the additional gate , an approach for designing an efficient regular layout, called *Sea-of-Tiles* is presented. Then, specific logic synthesis techniques, supporting the higher expressive power provided by this technology, are introduced and used to showcase the performance of the controllable-polarity NWFETs circuits in comparison with traditional CMOS circuits.**

Keywords—Nanowire transistors; controllable polarity; regular fabrics; XOR logic synthesis

I. INTRODUCTION

As the semiconductor industry is approaching the ultimate limits of conventional silicon-based *Integrated Circuits* (IC), researchers are focusing their effort to identify possible approaches that will enable the continuation of Moore's scaling laws.

FinFET transistors are successfully replacing planar CMOS transistors at the 22nm technology node [1]. Following the trend to one-dimensional (1-D) structures, *vertically-stacked Silicon NanoWires Field Effect Transistors* (SiNWFETs) are a promising extension to the tri-gate FinFETs [2]. Indeed, by splitting the 2-D thin film channel in a collection of 1-D structures, the device exhibits superior performance. The *Gate-All-Around* (GAA) structure improves the electrostatic control of the channel and leads to a higher *Ion/Ioff* ratio and reduced leakage current [3].

At advanced technology nodes, more and more devices are affected by Schottky contacts at the source and drain interfaces. Hence, devices face an ambipolar behavior, i.e., that the device exhibits *n*- and *p*-type characteristics simultaneously. While technologists target to suppress the ambipolar behavior of the devices through additional process steps, new design methodologies [4,5] showed that it is of high interest to control the ambipolar phenomenon through programmable polarity devices.

By engineering of the source and drain contacts and by constructing independent double-gate structures, the device polarity can be electrostatically programmed to be either *n*- or *p*-type. The functionality of such a device is logical biconditional on both gate values and enables a compressed realization of XOR-based logic functions, which are not implementable in CMOS in a compact form [5].

While such devices were already demonstrated using silicon [6,7] and carbon electronics [8,9], they suffered from the lack of maturity of the bottom-up fabrication processes. In this work, the ambipolar behavior of the SiNWFET is controlled by realizing a *Double-Gate* SiNWFET (DG-SiNWFET), built using a top-down fabrication flow [10]. The presence of an extra gate, called the *Polarity Gate* (PG), for each and every transistor, increases the routing complexity of the basic standard gates. Hence, special regular layout techniques to mitigate the additional gate impact are required.

Regularity is one of the key features to increase the yield of integrated circuits at advanced technology nodes [11], while keeping the routing complexity under control. We describe here a regular array of elementary logic blocks, called *Sea-of-Tiles* (SoT). This structure was presented as an optimal layout fabric for ambipolar SiNWFET [12]. Thanks to a novel symbolic layout methodology, a desired logic function can be mapped onto an array of logic tiles, thereby enabling the automatic placement of digital circuits onto a SoT organization.

DG-NWFETs can efficiently realize either NAND/NOR or XOR/XNOR logic operators. However, the efficiency of the current heuristic methods for logic synthesis is heavily dependent on the targeted circuit type, producing near-optimal results either for NAND/NOR- or XOR/XNOR-dominated circuits. Addressing these limitations and by taking advantage of the high expressive nature of transistors with controllable polarity, a novel logic synthesis methodology, *MIXSyn*, was introduced in [13].

This paper aims at surveying the main results associated with DG-SiNWFETs from technology to physical design and logic synthesis. In addition, we provide a benchmarking study which aims at evaluating the interest of the technology and the associated methodologies with regards to advanced baseline CMOS. We show that, thanks to its higher logic expressive power, controllable-polarity NWFET technology leads to, on average, 13.9% smaller and 29.5% faster circuits than in FinFET CMOS technology at 22nm technology node.

The remainder of the paper is organized as follows. In Section 2, we present our DG-SiNWFET technology and its opportunities at circuit-level. In Section 3, we introduce the interests of regular arrangements to mitigate the impact of the additional gate, and summarize the associated physical design methodologies. In

Section 4, *MIXSyn* logic synthesis flow is detailed and used, in Section 5, to benchmark the performances of the DG-SiNWFET technology at the system-level.

II. VERTICALLY-STACKED DOUBLE GATE NANOWIRES FETS: TECHNOLOGY OVERVIEW AND CIRCUIT OPPORTUNITIES

In this section, we introduce the technology of Si-NWFETs and the associated design opportunities.

A. Transistors with Controllable Polarity

Ambipolar conduction is observable in several nanoscale FET devices (45nm node and below), including silicon [14], carbon nanotube [15] and graphene [16]. Specifically, the trend towards the use of intrinsic transistor channels at the 22nm node and below, makes this phenomenon a potential limitation in circuit design. Whereas ambipolarity is often suppressed by processing steps, we exploit this feature to our advantage.

Transistors with controllable polarity are *Double-Independent Gate* (DIG) *Field Effect Transistors* (FETs) having one gate controlling on-line the device polarity (Fig. 4a). Transistors with controllable polarity have been experimentally fabricated in several novel technologies, such as carbon nanotubes [8], graphene [9] and *Silicon NanoWires* (SiNWs) [6,7]. The on-line configuration of DIG ambipolar FETs polarity is enabled by the regulation of Schottky barriers on source/drain junctions through the additional gate.

In this paper, we use a top-down fabricated, vertically-stacked SiNW FET, featuring two *Gate-All-Around* (GAA) electrodes (Fig. 1). Vertically-stacked GAA SiNWs represent a natural evolution of FinFET structures, providing the best electrostatic control over the channel and consequently superior scalability properties [10].
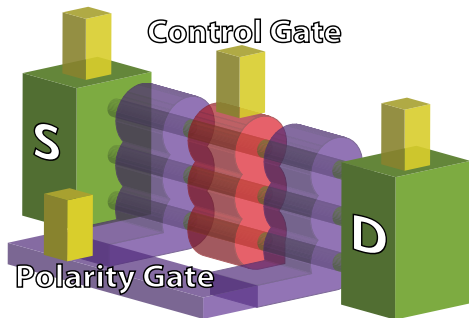

Fig. 1. 3D sketch of the SiNWFETs featuring 2 independent gates.

In our device, one gate electrode, the *Control Gate* (CG) acts conventionally by turning *on* and *off* the device. The other electrode, the *Polarity Gate* (PG), acts on the side regions of the device, in proximity of the *Source/Drain* (S/D) Schottky junctions, switching the device polarity dynamically between *n*- and *p*-type (Fig. 2). The applied voltage range is comparable to the voltage range applied to the CG. The input and output voltage levels are compatible, resulting in directly-cascadable logic gates.

B. Logic Operations with Higher Expressive Power

Digital circuits using these transistors can exploit both gates as inputs, thereby enabling the design of compact cells that implement XOR more efficiently than in CMOS. Indeed, SiNWFETs are logic biconditional on their two-gate polarities, and embed intrinsically an XOR characteristics. Fig. 3 presents a pseudo-logic XOR gate. The device in the *pull-down* network is

polarized by means of the PG. In the case of the *n*-type polarization, the characteristic of a pseudo-logic inverter is obtained (green). In the *p*-type polarization, a buffer is obtained (blue). As shown in the inset truth table, overall an XOR function can be implemented by a single transistor.
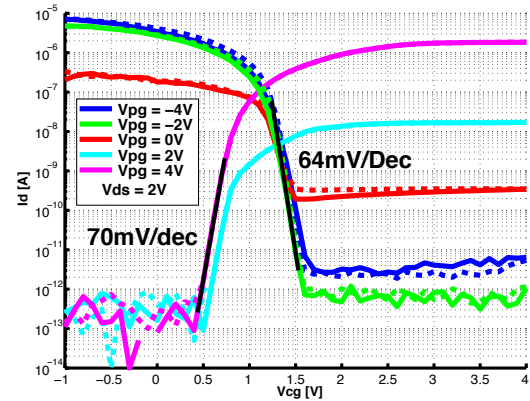

Fig. 2. I_{DS}-V_{CG} logarithmic plot of a measured device for serveral V_{PG} voltages. Curves extracted at V_{DS}=2V [10].
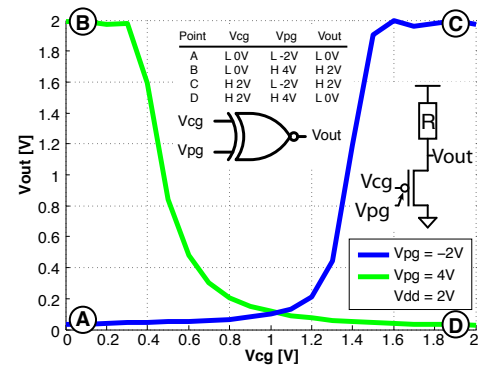

Fig. 3. Pseudo-logic XOR characteristic obtained using a single SiNWFET with controllable polarity [10].

The unique feature of this device of being polarized electrostatically was first employed to build a reconfigurable logic cell [4], and later used to define a static XOR-intensive logic family [5]. In particular, a full-swing XNOR-2 gate was proposed. The XNOR implementation, reported in Fig.4b, requires 4 transistors while the traditional full-swing static CMOS implementation uses 8 transistors [17].
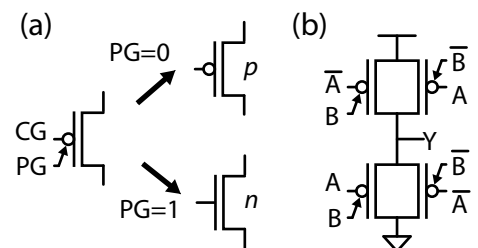

Fig. 4. Polarity control in nanowire transistors (a) and XOR-2 gate (b) [17].

Thanks to their improved expressive power, transistors with controllable polarity intrinsically embed the XOR logical connective, therefore enabling compact realizations for XOR/XNOR-dominated circuits. In the following, we will present

a device arrangement that complies with the increase in routing requirements and introduce an XOR-intensive logic synthesis tool.

III. Sea-Of-Tiles: How to Deal with the Routing Congestion

Regular layout fabrics have the advantage of higher yield as they maximize layout manufacturability. In this section, we sketch a novel architecture, called *sea-of-tiles* (SoTs), in which an array of logic tiles are uniformly spread across the chip. Then, we summarize a novel layout methodology that takes advantage of the proposed enhanced functionality transistors in a compact way [12].

A. Towards a Regular Gate Arrangement

Layout regularity is one of the key features required to increase the yield of ICs at advanced technology nodes [11]. Hence, design styles based on regular layout fabrics are promising techniques to increase the manufacturing yield of NWFETs. Various regular fabrics have been proposed throughout the evolution of the semiconductor industry, with some recent approaches explained in [11, 18, 19]. In gate-array fabric style, a sea of prefabricated transistors is customized to obtain a desired logic gate. The customization of generic gate arrays comes at a large area cost as well as routing overhead, thereby increasing the performance gap between ASICs and gate arrays. However, strict design rules, at 22nm technology node and beyond, has led to ASIC cell layouts with arrays of gates with a constant gate pitch, which resemble a sea-of-gates layout style. In this work, we define a regular logic *tile* that has an array of prefabricated transistor-pairs grouped together. A desired logic can be mapped onto a fabric of logic tiles, a Sea-of-Tiles, in a way reminiscent of pre-characterized gate arrays (Fig. 5).
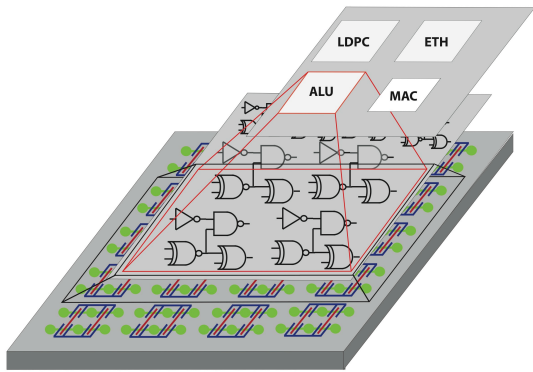
Fig. 5. Conceptual representation of a regular *sea-of-tiles*. Tiles are configured to realize logic functions that are part of a complex system such as a processor

B. Layout Techniques

To enable the compact implementation of functions with the proposed transistors, we report a novel symbolic-layout technique, *dumbell-stick diagrams*, based on which we present a layout technique to design complex gates [12].

1) Dumbell-Stick diagram

Similar to the CMOS stick diagrams, *dumbell-stick diagrams* are proposed for double-gate devices with controllable polarity for designing compact layouts by minimizing the cell routing complexity. Fig. 6a shows the dumbell-stick diagram and how it is inspired from the physical shape of the device. The suspended silicon nanowires between the source and drain contacts form the basic dumbell. The control gate and the polarity gate constitute the sticks. From this representation, we introduce the notion of

transistor grouping and transistor pairing. Transistor pairing (Fig. 6b) helps in aligning the control gates of the complementary transistors in the pull-up and pull-down networks, whereas with transistor grouping (Fig. 6c) polarity gates of adjacent transistors are connected together. A logic tile is defined as an array of transistor pairs, which are grouped together. By grouping the polarity gates of the adjacent transistors we can reduce the number of *input* pins to the connected fabric, tile. A *Tile*, consisting of two transistor-pairs grouped together is depicted in Fig. 6d.
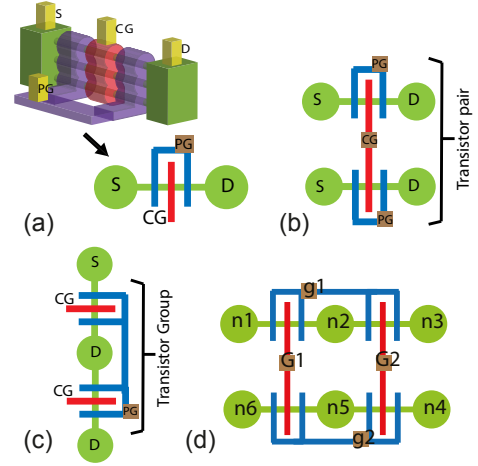
Fig. 6. Dumbell-stick diagram (a), transistor pairing (b), transitor grouping (c) and logic *Tile* (d).

2) Layout Technique for Simple Unate Logic Gates

Unate logic functions (e.g. NAND, NOR, AOI …) with controllable-polarity devices are obtained by biasing the PGs of the *Pull-Up-Network* (PUN) and *Pull-Down-Network* (PDN) to Gnd and V_{DD} respectively. Hence, all the transistors in the PUN (and PDN) can be grouped together (i.e., PGs of the stacked transistors are connected together), thereby forming one PG for each PUN and PDN. After biasing the PGs, CMOS layout style with transistors aligned according to the Euler paths can be employed [20]. The transistors are placed in two parallel rows where all transistors in the PUN are in one row while all the transistors in the PDN are in the other. The main objective is to place transistors in such a way that the gate signals are aligned and drain/source regions of adjacent transistors are abutted. Fig. 7a shows an example of a 2-input NAND gate with the PGs biased to either Gnd or V_{DD}. Fig. 7b shows its equivalent dumbell-stick diagram.
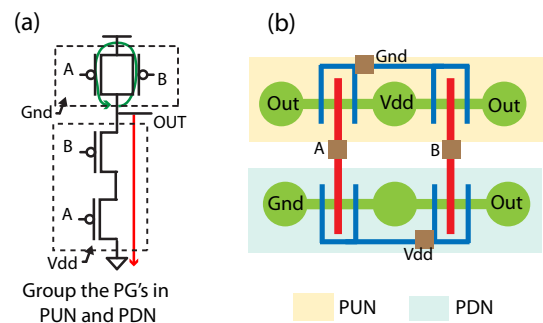
Fig. 7. Schematic of a static NAND-2 gate (a) and its equivalent Dumbell-Stick diagram (b).

3) Layout Technique for Simple Binate Logic Gates

In the case of binate functions (such as the XOR-2 gate), the polarity gates in the PUN (and PDN) cannot be grouped. Since the adjacent transistors cannot be grouped, extra routing effort is needed to connect similar polarity gates together. An efficient implementation is shown in Fig. 8, where similar polarity gates are grouped together. From the dumbell-stick diagram, we can observe that the PUN and PDN are placed next to each other, which is possible with DG-SiNWFET technology as the transistors are field controlled to make them *p*-type or *n*-type. Several novel circuit designs and architectures have been proposed which leverage upon embedded XOR functionality of double-gate NWFET [5, 21, 22]. In the proposed circuits, 2-input XOR/XNOR gates form the main building block of logic cells and are surrounded by traditional NAND/NOR constructions. Generation of complex layout patterns is fully described in [12].
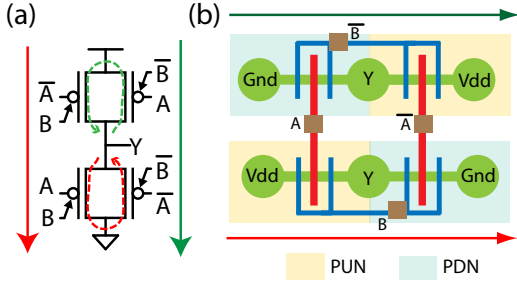

Fig. 8. Schematic of a static XOR-2 gate [5] (a) and its equivalent Dumbell-Stick diagram (b).

4) Layout Technique for Sequential Elements

We apply the layout techniques presented in the previous sections to sequential elements. Though sequential elements design does not generally leverage double gate feature of controllable-polarity transistors, they can still be efficiently mapped onto a set of tile. Indeed, sequential elements often embed transmission gates that can be grouped together. Fig. 9 illustrates a D Flip-Flop (DFF) mapped onto an array of tiles. In this implementation, we can observe that the two transmission gates in the master (slave) stage are physically mapped onto $Tile_1$ ($Tile_3$), efficiently compacting the overall mapping of the circuit. The inverters in the master, slave and output stages of the DFF are mapped onto $Tile_2$, $Tile_4$ and $Tile_5$ respectively. Inverting stage of the clock signal is not depicted.
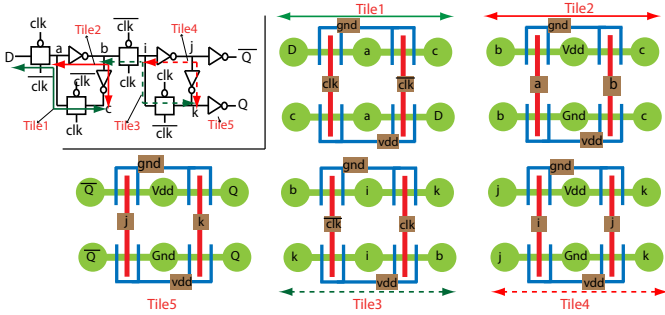

Fig. 9. D Flip-Flop mapped on a regular set of tiles.

IV. MIXED XOR-AND/OR-ORIENTED LOGIC SYNTHESIS

In this section, we summarize a synthesis system that exploits both XOR and AND/OR logic operators [13] and we showcase its use for automated logic synthesis targeting controllable-polarity transistor-based circuits.

A. Mixed Synthesis Motivation

Transistors with controllable polarity intrinsically embed the XOR logical connective and thus enable the realization of XOR operator with the same complexity than AND/OR operators. To take advantage of this opportunity at circuit level, both XOR and AND/OR networks should be manipulated during logic synthesis. Traditional logic synthesis methods [23, 24, 25], which are the basis for current commercial tools, employ techniques using AND/OR representations and produce near-optimal results for AND/OR-dominated logic circuits. An alternative synthesis approach is proposed in [26], where *Binary Decision Diagrams* (BDDs) are used in a practical tool, named BDS, to fully represent, manipulate and decompose logic functions. Thanks to the advantageous BDD-based XOR-decomposition techniques, BDS efficiently synthesize XOR-intensive circuits. In order to fully harness the logic expressive power of controllable-polarity transistors, we combined XOR-decomposition techniques [26] with traditional optimization methods [25] in a novel synthesis methodology, named *MIXSyn* [13].

B. MIXSyn Tool

MIXSyn is an area-oriented logic synthesis methodology with novel hybrid logic optimization and library-free technology mapping methods. Hybrid logic optimization consists of two steps to identify and selectively manipulate AND/OR and XOR operations in the logic circuit. In this paper, we propose a custom standard-cell library mapping technique to substitute the original library-free method in *MIXSyn* [13]. In this way, we extend the capability of *MIXSyn* to produce area-delay efficient results with corresponding accurate delay estimation. The flavor and an example of logic optimization and technology mapping are given in the following subsections.

1) Hybrid 2-step Logic Optimization Algorithm

The hybrid logic optimization method employed in *MIXSyn* is a two-step process, that allows us to efficiently minimize both AND/OR and XOR operations in the logic circuit. To introduce the concept of a mixed logic optimization, we report a simple example of hybrid logic optimization and compare it with standard AND/OR and XOR optimization methods alone.

The objective function *f* in this example has the following *Sum-Of-Products* form: $f = ab+bc+ab+ca$. A single step XOR-optimization can reduce the objective function to $f = bc+(a\oplus b)+ca$. Instead, a single step AND/OR-optimization can factor *c* and obtain $f = ab+a'b'+c.(a+b)$. However, a hybrid optimization method can further minimize the objective function as shown in Fig. 10. A first XOR-optimization phase extracts the node $x = (a\odot b)$ (Step a). After this, the extracted *x* node is separated from the original function and treated as a new primary input (Step b). The resulting Boolean network comprises *a*, *b*, *c* and *x* as primary inputs. Since the function *x* has a common set of input variables with the split network, it is possible to specify the *Controllability Don't Care* (CDC) set containing the input combinations that never occur, $CDC_{in}(x,a,b)=\{101,110,011,000\}$. Exploiting this information, the Boolean network can be further minimized by an AND/OR-optimization step in $f = x+c$ (Step d). Finally, the previously separated *x* node is merged with such optimized network (Step e), achieving $f=(a\odot b)+c$.
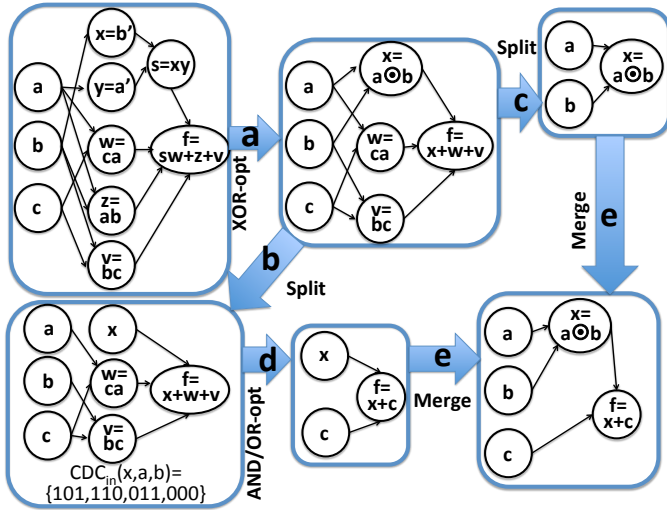
Fig. 10. Hybrid Logic Optimization example for $f = ab+bc+ab+ca$.

In order to give the flavor of the hybrid optimization procedure in *MIXSyn* [13], a simplified flowgraph is depicted in Fig. 11 and briefly commented hereafter. In the first step, XOR/XNOR operations are extracted from the input Boolean network and detached in a separate auxiliary network. Then, the remaining logic circuit is processed by an AND/OR optimization method taking into account intermediate *Don't Care* conditions. Finally, the auxiliary network with XOR/XNOR is reattached to form the entire optimized Boolean network. We refer the interested reader to [13] for a detailed explanation of the hybrid optimization procedure.
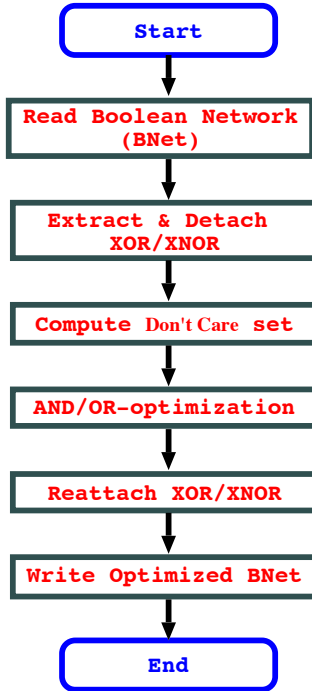

Fig. 11. Hybrid Logic Optimization flowchart.

2) Modified Technology Mapping

Technology mapping, in this paper, is based on a simple standard cell library consisting of NAND-2, NOR-2, XOR-2,

XNOR-2 and INV logic gates. We split the mapping task in two phases. First, XOR-2 and XNOR-2 nodes extracted during hybrid logic optimization are directly assigned to their corresponding logic cells. Indeed, such functions are potentially hidden by traditional mapping algorithms while our aim is to exploit their efficient implementation in ambipolar technology. Finally, the rest of the logic circuit is mapped using standard techniques [25].

V. System-level Performance Evaluation

In this section, we present experimental results for the *MIXSyn* methodology. We compare it with ABC and BDS academic synthesis tools fed with the same standard cell library based on controllable polarity transistors. Finally, we evaluate the advantage of the synthesized circuits with respect to traditional CMOS technology.

A. Methodology

Our proposed methods are implemented in C language. Interaction with external optimization tools is done via Perl scripts. In the mixed logic optimization phase, AND/OR-optimization is performed with ABC [25] while XOR-optimization is done by BDS-pga [26]. The current *MIXSyn* implementation does not include the CDC computation described in the previous section, as ABC does not properly support extensive *don't care* set [27]. The standard cell library consisting of NAND-2, NOR-2, XOR-2, XNOR-2 and INV logic cells is characterized for vertically stacked SiNWFETs and also for CMOS FinFET for the sake of comparison. In controllable-polarity technology, the library cells are designed using layout techniques introduced in Section III. The technology node considered is 22nm for both technologies and the power supply voltage is V_{dd}=0.9 V. Defaults and options for the reference flows are:

- ABC: ABC *resyn2* optimization script and ABC mapper.

- BDS: BDS logic optimization and ABC mapper.

The circuit benchmarks are taken from the MCNC suite.

B. Results and Discussion

Area, gate count and delay results for the considered synthesis flows are reported in Table I. *MIXSyn* is the best synthesis flow for controllable-polarity technology achieving an average (area/gate-count/delay) reduction of (11.2/10.7/3.9)% with respect to BDS flow and (6.3/6.8/0.7)% compared to ABC. *MIXSyn* takes advantage of the tunable polarity opportunity producing circuits in SiNWFET technology that are, on average, 13.9% smaller and 29.5% faster than in FinFET CMOS technology, synthesized by ABC.

MIXSyn exhibits promising results for logic synthesis of SiNWFET-based circuits. The hybrid optimization procedure allows us to extract XOR functions that have an advantageous implementation with these transistors, while still maintaining efficient manipulation of AND/OR dominated portions of the logic circuit. The technology-mapping step is designed to preserve such extracted functions and enable area-delay optimization, therefore extending the capability of the previous version of *MIXSyn* [13]. As a result, controllable-polarity transistor logic expressive power is better exploited with *MIXSyn* than with traditional synthesis flows. Note that, since XOR gates are usually part of the critical path in many practical digital circuits, the advantage of using controllable-polarity transistors translates in a marked delay reduction compared to traditional CMOS, on top of the corresponding area reduction.

22nm node	Double-Gate SiNWFETs									CMOS FinFET		
MCNC benchmarks	MIXSyn			BDS			ABC			ABC		
	Area (μm²)	Gate count	Delay (ns)	Area (μm²)	Gate count	Delay (ns)	Area (μm²)	Gate count	Delay (ns)	Area (μm²)	Gate count	Delay (ns)
C1355	67.76	199	0.19	67.71	204	0.22	71.79	229	0.22	92.95	211	0.30
C6288	424.26	1419	0.79	432.93	1408	0.80	430.09	1453	0.79	543.18	1555	1.15
des	687.51	3106	0.20	722.93	3320	0.21	716.11	3312	0.21	745.14	3534	0.31
pair	310.76	1543	0.28	324.50	1548	0.26	315.84	1569	0.28	318.67	1585	0.39
C499	68.37	192	0.18	70.05	216	0.22	72.73	235	0.18	90.42	203	0.28
C1908	75.47	298	0.32	83.96	316	0.33	86.65	332	0.30	85.69	283	0.46
C7552	320.10	1418	0.30	372.03	1533	0.32	363.06	1533	0.30	396.11	1567	0.40
misex3	298.87	1457	0.23	371.80	1832	0.24	321.42	1585	0.24	360.20	1753	0.28
seq	691.80	3391	0.21	870.77	4212	0.21	764.72	3730	0.20	787.05	3920	0.26
Average	327.21	1447	0.30	368.52	1621	0.31	349.16	1553	0.30	379.93	1623	0.43
Improvements												
MIXSyn	-	-	-	-12.6%	-12.0%	-4.1%	-6.7%	-7.3%	-0.7%	-16.1%	-12.2%	-41.8%
BDS	11.2%	10.7%	3.9%	-	-	-	5.2%	4.2%	3.2%	-3.1%	-0.1%	-36.3%
ABC	6.3%	6.8%	0.7%	-5.5%	-4.4%	-3.3%	-	-	-	-8.8%	-4.5%	-40.8%
ABC (CMOS)	13.9%	10.9%	29.5%	3.0%	0.1%	26.6%	8.1%	4.3%	29.0%	-	-	-

VI. CONCLUSION

In this paper, we presented a complete design framework of DG-NWFET technology involving process, design and automated tools. In particular, we introduced results coming from fabricated devices and showed their interest from a circuit perspective. Then, regular arrangements were described as a promising solution to mitigate the impact of additional gate. Finally, we provide a benchmarking study which aims at evaluating the performance of the technology and the associated methodologies with regards to advanced baseline CMOS. To take advantage of the higher expressive power of the technology, we introduced a novel logic synthesis methodology, *MIXSyn*, that produces near optimal results for both AND/OR- and XOR/XNOR-intensive logic. Finally, we showed that NWFETs with controllable polarity lead to circuit implementations, on average, 13.9% smaller and 29.5% faster than in FinFET CMOS technology.

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