Journal of
Low Power Electronics
Vol. 8, 1–11, 2012

Inter-Plane Communication Methods for 3-D ICs

Somayyeh Rahimian*, Vasilis F. Pavlidis, and Giovanni De Micheli

LSI-EPFL, Lausanne, 1015, Switzerland

(Received: 27 November 2011; Accepted: 6 February 2012)

Three-dimensional (3-D) integration is an emerging candidate for implementing high performance multifunctional systems-on-chip. Employing an efficient medium for data communication among different planes is a key factor in achieving a high performance 3-D system. Through Silicon Vias (TSVs) provide high bandwidth, high density inter-plane links while facilitating the flow of heat in 3-D circuits. This paper provides an overview of the diverse applications of TSVs within 3-D circuits and surveys the manufacturing and design challenges relating to these interconnects. Inter-plane communication through AC-coupled on-chip inductors is also discussed as an alternative to TSVs. Although there have been several efforts that model the electrical characteristics of these inter-plane communication schemes, the effect that heat can have on the performance of the inter-plane link implemented with either means has not sufficiently been investigated. Consequently, some insight on the effects of thermal gradients on the performance of these links is offered. Results indicate that the electrical performance of TSV is not susceptible to temperature variations. Signal integrity can, however, be degraded in the case of pronounced thermal gradients in contactless 3-D ICs, as demonstrated by a decay of the *S*-parameters for the investigated inductive links.

Keywords: 3-D Integration, Through Silicon Via, Inductive Links, Temperature Gradient.

1. INTRODUCTION

Three-dimensional (3-D) or vertical integration is a design and packaging paradigm that can mitigate many of the increasing challenges related to the design of modern integrated systems.[1] 3-D circuits have recently been at the spotlight, since these circuits provide a potent approach to enhance the performance and integrate diverse functions within a multi-plane stack.

There are different inter-plane communication schemes for 3-D integration. The contactless 3-D ICs are formed by bonding, typically, bare dice with a diversity of methods.[2] In these circuits, communication among circuits in different planes is achieved through AC-coupling which uses the transitions of a digital signal as the useful part of information and discards the DC component. Specialized links transfer data among the planes either capacitively[3] or inductively.[4] Capacitively coupled links use a single metal layer in each plane to form a capacitor, whereas in inductive links spiral inductors (which can require several metal layers) are utilized. Inductive links are a promising candidate for inter-plane wireless communication due to the better performance for larger communication distances as compared to capacitive links. Contactless links are employed to transfer the AC signal among the planes. The power of the transferred signal can be adapted by different circuit parameters, such as the number and the width of the inductor turns.[4] Contactless links are implemented with standard CMOS processes, which reduce the manufacturing complexity as compared to wired vertical links.

Alternatively, inter-plane communication can be provided by galvanic connections, which are vertically formed through the planes of the 3-D stack widely known as *through silicon-vias* (TSVs). Specific 3-D manufacturing processes also support extremely short vertical interconnections, similar to common metal contacts, producing multiple device layers.[5] These processes known as monolithic 3-D integration are not discussed in this paper, since presently these techniques are less mature than multi-plane stacked systems with TSVs.

This work consequently emphasizes the TSVs, which are employed by the majority of the 3-D fabrication processes. Through-silicon-vias are tens of micrometers long and are fabricated with aspect ratios up to 1:10, where a 1:6 ratio is typically used.[6] TSVs produce the highest interconnect bandwidth within a 3-D system as compared to wire bonding, peripheral vertical interconnects, and solder ball arrays.[1]

*Author to whom correspondence should be addressed.
Email: Somayyeh.rahimianomam@epfl.ch

Inter-plane signaling, however, is only one of the usages of TSVsin 3-D circuits. TSVs are also used to distribute power and ground throughout a 3-D stack. In addition, due to the high thermal conductivity of these interconnects, TSVs can alleviate the thermal problems in 3-D integrated circuits. These links reduce the temperature fluctuations caused by local hot spots within the volume of the 3-D stack. Different models have been presented to describe the thermal conductivity of TSVs. The effect of thermal gradients on the signal integrity of vertical links, however, has not been explored for both the TSVs and the inductive links. Consequently, one of the contributions of this paper is to analyze the behavior of these communication schemes under a variety of thermal profiles that can potentially manifest within the planes of a 3-D circuit due to the expected high power densities. Signal integrity, however, is only one of the metrics used to decide upon the suitability of the inter-plane communication mechanisms. To allow, therefore, a fairer comparison, the pros and cons of the TSVs and the inductive links are discussed. To this end, a succinct overview precedes the research contribution where the primary functions and related challenges of these two approaches are presented. The contributed analysis and comparison adds another useful aspect in characterizing the two types of inter-plane links.

Consequently, the remainder of the paper is organized as follows. In the following section, the manufacturing methods of TSVs and inductive links are reviewed. In Section 3, the multifold role of the TSVs in 3-D ICs is discussed. Design challenges for TSVs and inductive links are discussed in Section 4. In Section 5, the research contribution, which is a performance comparison between TSVs and contactless links under different thermal profiles, is presented. A variety of potential thermal gradients is explored. The major points of the paper are summarized in the last section.

2. MANUFACTURING PROCESS FOR TSVs AND INDUCTIVE LINKS

Exploiting vertical inter-chip interconnects can improve the performance of the system by decreasing the length of the long interconnects. To increase the signal bandwidth in 3-D systems while saving or, at least, not increasing the power, TSVs should be fabricated to have low impedance characteristics. Manufacturing issues are one of the primary challenges for TSV based 3-D circuits. Fabricating high performance, reliable, and cheap vertical interconnects, which do not affect the neighboring active devices is an important requirement in 3-D systems towards high volume production.[1]

TSVs are, usually, manufactured as tapered wires (e.g., copper, tungsten or poly silicon), surrounded by a thin dielectric layer (liner) to insulate the metal from the semiconducting substrate.[6] There are three main approaches for manufacturing TSVs. The "via first" approach where the TSVs are formed before the devices (i.e., *front end of the line* (FEOL)), the "via-middle" approach where TSVs are fabricated after the transistors but before the backend interconnect (i.e., *back end of the line* (BEOL)), and the "via last" method where the TSVs are fabricated after or in the middle of the back end interconnect process.[6] In the "via first" technique, the TSVs connect the topmost metal layer of one plane with the first metal layer of another plane. The TSVs presented in Refs. [9, 10] are fabricated with the "via-first" method and have diameters between 12 μm to 18 μm and the length of 30 μm to 50 μm where the first one is a poly silicon TSV with a resistance of 1.3 Ω to 5 Ω and the second is a metal TSV with a resistance of 230 mΩ.

In the "via last" approach, the topmost metal layers of adjacent planes are connected together using TSVs. For the "via-last" approach, the TSVs have to be etched through the substrate and the metal layers. Consequently, "via-last" typically requires longer TSVs. This situation can lead to either higher aspect ratio increasing the manufacturing complexity or larger diameter increasing the area overhead of TSVs. As an example consider the process in Ref. [8], which produces TSVs 150 μm long and 5 to 15 μm wide with a TSV resistance of 9.4 mΩ to 2.6 mΩ. The "via-first" methods also pose several changes on the front end processing of the wafers. For these reasons, the "via-middle" approach appears (for the time being) as the proper compromise between the TSV size and manufacturing complexity.

The basic steps of a typical "via-middle" TSV fabrication process are shown in Figure 1. The first step is to process each plane separately with some reserved area for TSVs, afterwards a deep trench is opened through the inter layer dielectric (ILD) and device layers. The depth of this trench is mainly determined by the resulting aspect ratio of the TSV process and the wafer thinning capabilities. The trench sidewall is isolated from the conductive substrate and the opened trench is filled with metal, such as tungsten (W) or copper (Cu) as depicted in Figure 1(b). Then the metal layers are added to the top of silicon substrate and the wafer is thinned as shown in Figure 1(c). Before stacking the planes, the wafers are typically thinned to decrease the overall length of the TSVs. An example of via middle TSVs is presented in Ref. [7] where the TSVs are 25 μm long and 5 μm wide with a resistance of 20 mΩ. A reduced wafer thickness, however, cannot sustain the mechanical stresses incurred during the handling and bonding phases of a 3-D process. An auxiliary wafer called "handle wafer" is attached to the original wafer as shown in Figure 1(d), thereby, providing the required mechanical durability for the bonding step. The alignment and bonding steps follow as illustrated in Figure 1(e). Finally, the handle wafer is removed from the thinned wafer. The resulting characteristics of different

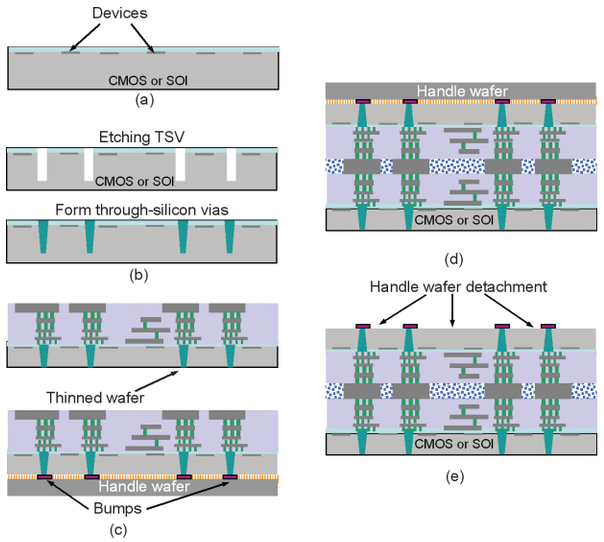

Fig. 1. Basic steps of TSV manufacturing for a "via-middle" process, (a) wafer preparation and FEOL, (b) TSV etching and metal filling, (c) wafer thinning and BEOL, (d) wafer bonding, and (e) handle wafer removal.

processes related to each of these approaches are listed in Table I.

Alternatively, inductive links can be fabricated with standard CMOS processes. Inductive links support communication at considerably larger distances. Consequently, there is no need for wafer thinning and using handle wafers. Eliminating these additional steps in the manufacturing process reduces the fabrication cost and can increase the yield for this type of 3-D circuits.

An inductive link consists of two spiral inductors and a current based transceiver. Spiral inductors are placed in the top metal layers and do not occupy the active area of the circuit. As shown in Figure 2(a), the transmitter converts the input voltage to current pulses, which are coupled through spiral inductors and recovered as voltage pulses at the receiver. There are different parameters that should be considered to design a proper inductive link. The inductor area should be minimized while providing the desired signal to noise ratio regarding the communication distance, signal power, and data rate.[4] The typical size of spiral

Table I. Physical and electrical characteristics of different TSV manufacturing approaches.

	Diameter (μm)	Length (μm)	Resistance (mΩ)	Bandwidth (Gb/s)
Via-first				
[9]	18	50	1.3–5	3
[10]	12	30	230	N/A
Via-middle				
[7]	5	25	20	N/A
Via-last				
[8]	5–15	150	9.4–2.6	N/A
[11]	~40	N/A	N/A	1.6

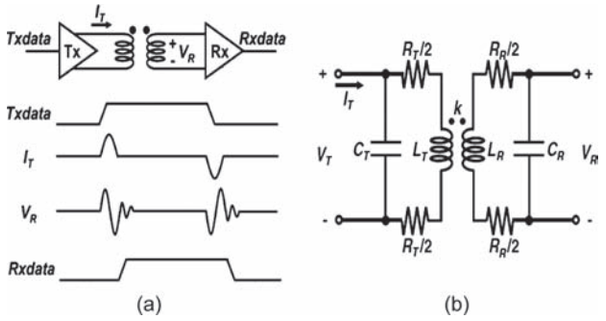

Fig. 2. Basic operation of an inductor link, where (a) is the inductively coupled transceiver and (b) is the equivalent circuit for the spiral inductor.[27, 28]

inductors utilized for inductive links is from 100 μm $\times$ 100 μm to 300 μm $\times$ 300 μm where the large inductors are used for clock distribution and the smaller inductors are exploited for data communication.[2, 4] The coupling coefficient of the link strongly depends on the communication distance. For a distance of 20 μm, a well-aligned inductive link can have a coupling coefficient of 0.25.[4] Inductive links have can achieve a data bandwidth that ranges from 1 Gb/s to 8 Gb/s. Designing low power transceiver circuits can make the inductive links a power efficient alternative for inter-plane signaling.

3. DIFFERENT APPLICATIONS OF TSVs IN 3-D ICs

Through-silicon-vias are one of the main candidates to form the vertical links for 3-D integrated systems. These vertical interconnects provide a high performance, high density path for inter-plane signaling. TSVs also play a vital role for distributing power and ground to those planes that do not support I/O and behave as thermal conduits for all but the plane, which is attached to the heat sink.[8] These functions of the TSVs are discussed in this section.

Each of these TSV usages can require particular and potentially conflicting characteristics for these wires. For signal TSVs, the important parameters are speed and power as discussed in Subsection 3.1, whereas for TSVs used for power distribution the voltage loss along the TSV is emphasized, as described in Subsection 3.2. For thermal TSVs, the superior heat conductivity of the vertical interconnects is discussed and enhanced thermal TSV models are described in Subsection 3.3.

3.1. Inter-Plane Signaling

TSVs exhibit quite different physical and electrical characteristics as compared to the horizontal interconnects (BEOL) in 2-D circuits. This situation carries substantial performance benefits, although the complexity of the interconnect analysis and design process increases due to the

different characteristics of the vertical links and the constraints that this type of interconnect poses on the physical design process. The heterogeneity of 3-D circuits, the diverse fabrication technologies, and the variety of the bonding style makes TSV modeling more challenging as compared to horizontal interconnects.

To provide high performance vertical links, proper electrical models for signal TSVs are required. To improve the speed of the circuit, low resistive and low capacitive TSVs should be used for signaling to decrease the *RC* delay of the vertical interconnects. Noise coupling between TSVs and/or the substrate is another important parameter that can affect the signal integrity in 3-D circuits and should be considered in the TSV modeling and design process. To reduce the current leakage to the substrate a thicker sidewall isolation layer (liner) or shorter TSVs can be employed. Increasing the thickness of the liner can result in higher area overhead and/or higher electrical resistance for the TSVs. If shorter TSVs are to be used, producing very thin wafers is the primary challenge. A variety of electrical models for TSVs have recently appeared in literature, relating the physical characteristics of the TSVs as determined by the different manufacturing methods with the electrical properties of these interconnects.[13–15]

A comprehensive *RLC* model for TSVs describing the high frequency behavior of TSVs is shown in Figure 3. Due to the geometry and manufacturing methods for the TSVs, the capacitance per unit length is typically higher, while the resistance per unit length is smaller as compared to a horizontal wire. Consequently, due to the significantly shorter length of the TSVs, the *RC* delay of these wires is low, allowing a significant reduction in the delay of the problematic global wires. The shorter interconnect length in 3-D circuits also results in reduced total capacitance of the interconnects, decreasing the power consumed by interconnects in 3-D circuits.

Another significant element that can affect the interplane signaling performance is the number of TSVs used for this purpose and the allocation of these TSVs within the planes. In present technologies, TSVs are much larger

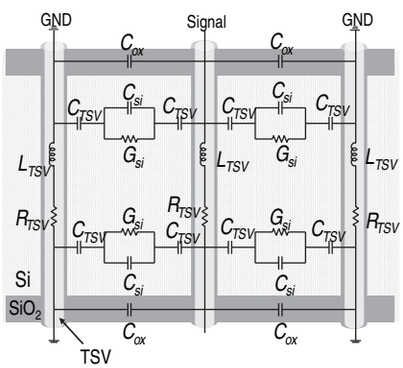

Fig. 3. An *RLC* model of a TSV.[10]

than the horizontal interconnects and the silicon area occupied by these interconnects is an important parameter that can affect the overall performance of a 3-D circuit.[16] Increasing the number of TSVs can increase the total area of the 3-D circuits and, hence, the total interconnect length. Alternatively, reducing the number of TSVs diminishes the benefits of vertical integration. Finding the optimal number of TSVs to minimize the total length of interconnect, can significantly improve the speed of a 3-D circuit. Without preserving some active area for TSVs during placement, the available TSVs can be located far from the connected cells causing the total interconnect length to increase as shown in Figure 4.[17] Several placement methods have been proposed to investigate the optimal number and location for TSVs to increase the speed of 3-D circuits.[16–18]

Noise coupling is an important issue that can degrade the signaling performance in TSV based 3-D circuits despite the short length of these interconnects. Increasing the speed of the link and TSV density increases both the noise coupling between adjacent TSVs (crosstalk) and the noise coupled to the substrate. Shielding the signal TSV with several grounded TSVs is an efficient way to reduce noise coupling in 3-D circuits.[19] Employing guard rings and *Deep n-wells* (DNW) are common methods to mitigate substrate noise in 2-D circuits, which can be applied also for 3-D circuits.[19] Another efficient approach to alleviate this problem is employing coaxial TSVs.[22, 23] These TSVs contain an extra layer of metal and liner surrounding the conventional TSV. Exploiting coaxial TSVs also increases the intrinsic decoupling capacitance. Although coaxial TSVs can potentially alleviate the substrate noise problem in 3-D circuits, the manufacturing implications of these TSVs on the design process of power distribution networks are not clear.

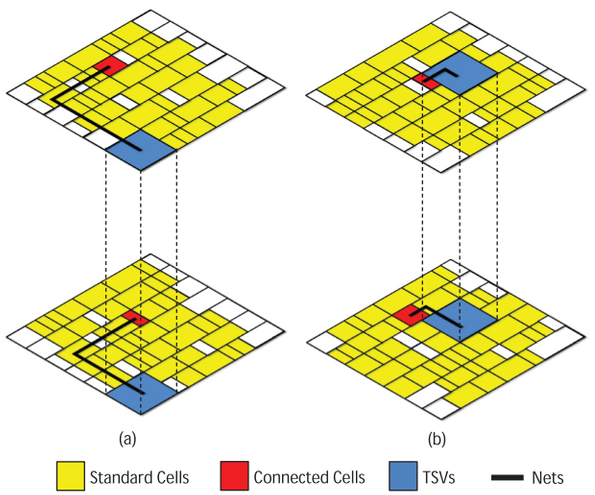

Fig. 4. Different TSV allocations for 3-D circuits where in (a) no active area for TSVs is reserved during placement and in (b) some active area for TSVs is reserved during placement.[13]

3.2. Power and Ground Distribution

Additionally to signaling, TSVs are used to distribute power and ground to all the planes, which are not connected to the package pins. An important parameter to evaluate the quality of a power distribution network is the voltage drop due to the dynamic and leakage power of the circuits. The reduced footprint of a 3-D circuit can result in higher current densities. In addition, the resistive path along the TSVs connecting the package pads with the power grids can also increase the static *IR* drop observed for specific planes. Using highly capacitive TSVs for power-ground distribution can increase the intrinsic decoupling capacitance, reducing in turn, the required amount of the extrinsic decoupling capacitance.

As discussed in Ref. [25], a crutial parameter for the *IR* drop on the top metal layer of each plane is the total area occupied by the TSVs. Assuming a specific area of the circuit is dedicated for power and ground TSVs, using more TSVs with smaller diameter results in lower voltage drop at the load. Simulation results indicate that by slightly increasing the density of the TSVs, a considerable reduction in the intra-plane power distribution resources can be achieved. According to Ref. [25], for a ten plane 3-D circuit with TSVs with a diameter of 10 μm, if the area occupied by TSV increases from 0.4% to 10% of the circuit area, the area required for the power/ground network can be reduced from 40% to 10% of the circuit area achieving the same *IR* drop.

The low resistance of the TSVs can efficiently be exploited to improve power integrity. For example, the TSVs can be connected to both the topmost and lowest metal layers of the power grid, providing additional current paths, which are shown in Figure 5.[26] These paths exhibit particularly low impedance characteristics supporting the distribution of large amount of current in the vicinity of a TSV without exceeding the allowed voltage drop.

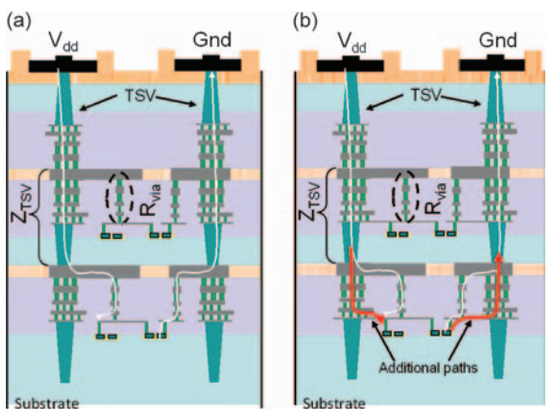

Fig. 5. Current paths within a 3-D circuit, (a) where the TSV is connected only to the topmost metal layer and (b) where the TSV is connected to the power lines on both the uppermost (MT) and the first (M1) metal layers of a circuit plane. TSVs are formed with a "via-middle" process.

Due to this low impedance path, stacks of common vias within this region are removed decreasing routing congestion without degrading power integrity. This improvement in power integrity can lead to a reduction in the required decoupling capacitance in the vicinity of the TSVs. The decoupling capacitance reduces up to 25% for the case investigated in Ref. [26].

The TSVs, however, occupy active silicon area and the TSV density cannot be considerably increased. Coaxial TSVs can also be of assistance in this case. A single coaxial TSV can be used to deliver both the power and ground by conducting the power through the inner metal and ground through the outer metal.[27] Merging power and ground TSVs reduces the area required for the power distribution network without increasing the *IR* drop.

3.3. Thermal TSVs

In 3-D integrated circuits, thermal issues are forecast to be a major challenge due to the high power density, the low thermal conductivity along the primary heat transfer path, and the smaller footprint area of the circuit attached to the heat sink. Several techniques have been developed to facilitate the heat transfer within 3-D circuits to reduce the temperature, such as *thermal through silicon via* (TTSV) planning, thermal wire insertion, liquid cooling, and thermal driven floorplanning.[28–30]

This type of TSVs is utilized to convey heat from the planes located far from the heat sink, such that the temperature limits are obeyed. These TSVs are typically interspersed within the white space that exists among the circuit blocks within each plane, where several techniques can be employed for this purpose.[25] Thermal TSV insertion has been shown to be a useful technique to reduce the local hot spots and decrease the maximum temperature of the circuit.

TTSV placement can significantly affect the thermal behavior of the 3-D circuits. Several methods of thermal via insertion are presented in Refs. [29–31], which can drastically reduce the maximum temperature of the 3-D circuit. These methods aim at distributing the thermal vias, such that the area occupied by both the TTSVs and the horizontal interconnects used to connect these TSVs is also reduced.

Improved modeling of the thermal behavior of the TTSVs can decrease the number of TTSVs used to transfer the heat to the ambient with considerable savings in area.[27] Analyzing how the TTSVs affect the developed temperature in 3-D ICs is important for efficient TTSV insertion. The thermal properties of TTSVs, in turn, depend upon several physical and technological parameters.

The traditional approach is to model a TTSV as a vertical lumped thermal resistor in each physical plane, which is proportional to the length and inversely proportional to the diameter of the TTSV. The TTSV is considered

as a one-dimensional network implying a flow of heat only in the vertical direction towards the heat sink of the system. This method is insufficient in capturing the thermal behavior of the TTSVs, since the lateral heat transfer through these structures is neglected. Compact thermal models as illustrated in Figure 6(a) can capture the major heat transfer paths by employing a small resistive network with few resistors. The thermal resistances are described by closed form expressions including the TSV geometry. Since the heat transfer process is highly complex, some fitting parameters are employed to improve the accuracy of this model. A more accurate model for TTSVs is illustrated in Figure 6(b), where each TSV is modeled as a distributed resistive network eliminating the requirement of curve fitting coefficients.

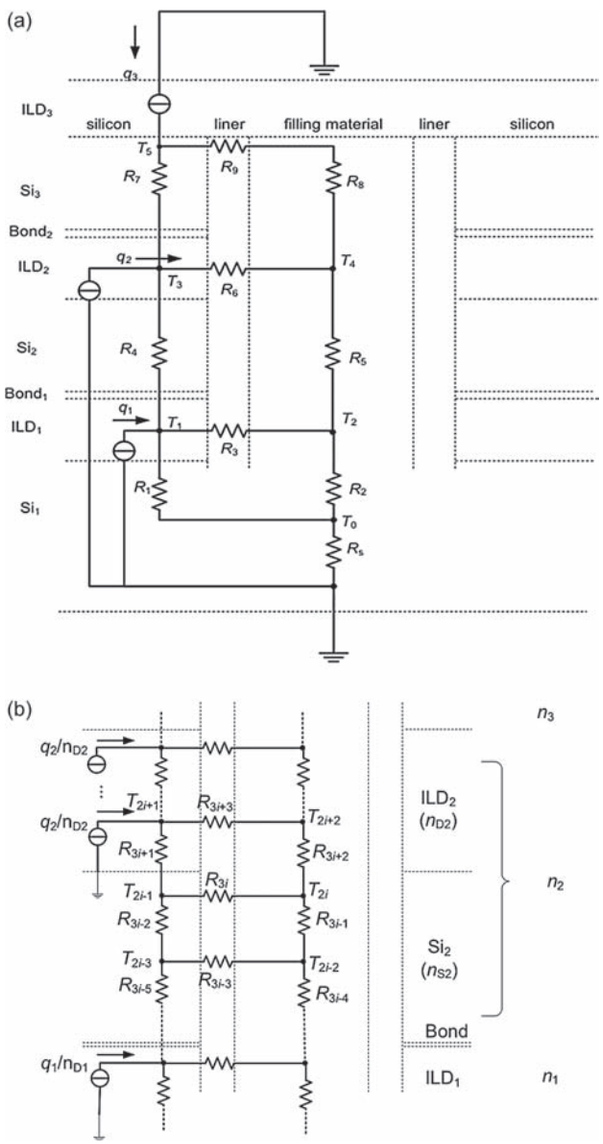

Fig. 6. Thermal model of a TTSV in a three-plane circuit where (a) is the compact model and (b) is the distributed model.

4. DESIGN CHALLENGES FOR TSVs AND INDUCTIVE LINKS

TSV manufacturing is a primary challenge that should be overcome if 3-D ICs are to be produced in high volume. Beyond manufacturing, however, there are several design challenges related to the different roles of TSVs within 3-D circuits. Specific design challenges are also associated with inductive links in contactless 3-D ICs. These challenges are briefly discussed in this section for both TSVs and AC-coupling based 3-D ICs.

4.1. TSV Related Design Challenges

A common issue among the different types of TSVs (assuming that some library of TSV cells can exist) is that the TSVs occupy silicon area and can block all of the metal layers. Consequently, the TSVs compete with the devices and the intra-plane wires for silicon and wiring resources, respectively. How to best place the TSVs becomes an important issue with implications to the delay of the inter-plane nets and routing congestion.[16, 18] Although, some techniques exist on placing the TSVs, there are still great margins for improvement.

For power/ground TSVs several issues also arise. Inserting TSVs within a circuit block has an adverse effect on the area and wirelength of this block and, often, the TSVs are considered to be placed at the periphery of this block. Placing the TSVs at the periphery of the block, however, means that longer current paths are formed. These paths can increase the *IR* drop on the load affecting power integrity. To address this situation, either the fineness of the power grid or the density of the TSVs can increase to lower the impedance of the paths.[25, 30] Several tradeoffs can be explored to determine the proper design that meets the power supply noise constraints, while not sacrificing excessive wiring and silicon resources.

Although power/ground and signal TSVs also behave as thermal conduits, the number as well as the allocation can be insufficient to mitigate thermal issues in 3-D circuits. To this end, thermal TSVs can be efficiently placed across the area of each plane. Many thermal-aware placement techniques have been developed with noteworthy results.[31] As the number of planes forming a 3-D system, however, increases the efficiency of the TTSVs degrades since the thermal paths to the heat sink become longer. The increase in the vertical thermal impedance, in turn, requires an increase in the TTSV density. Alternatively, increasing the TTSV density can adversely affect other important design objectives, such as speed, power, and area. Increasing, therefore, the density of the TTSVs may not be possible, which means that the TTSVs should be treated as an auxiliary means to reduce temperature.[19] Rather careful thermal-aware physical design should first be applied to manage the increased power densities in 3-D circuits.

Considering these challenges, the requirement is to manufacture and design TSVs such that signal, power, and thermal integrity within 3-D ICs is ensured. Addressing each of these objectives separately, which is the usual practice, may not result in the proper use of this expensive resource.

4.2. Design Challenges for Inductive Links

One of the main challenges in inductively coupled 3-D circuits is to transfer DC power via inductive links. Since these links use magnetic field to transfer the data, the only approach for transferring supply power is to convert the DC power to an AC signal, couple the AC signal through the inductive link, and rectify this signal to DC at the receiver side. Some transceiver circuits have been proposed for this purpose. In Ref. [20], a ring oscillator is used at the transmitter side to convert the DC power to an RF signal where in Ref. [21] an H-bridge transmitter is employed. Rectifiers are exploited to convert back the transmitted RF signal to the DC power. The efficiency of this links is dependent to the distance between the planes and typically is lower than galvanic connections due to the limited efficiency of the transceiver circuits. As shown in Ref. [21], to transfer 36 mW of DC power between two planes with a distance of 15 μm, a large inductor of 700 μm$\times$100 μm is employed where the efficiency of the power delivery is only 10%.

The quality of the magnetic coupling can also be affected by misalignment and interference. Although misalignments between the horizontal locations of the inductors in adjacent planes can affect the coupling coefficient, the effect is weaker as compared to TSVs where misalignments can result in defective and/or failed links.[32–34] This situation means that greater alignment margins can be supported by the inductive link, which facilitates manufacturing. Alternatively, design implications are raised for these links since larger interference or weaker coupling among the inductor is possible. These implications should, therefore, be considered in the design of these links.

5. THERMAL-AWARE SIGNAL INTEGRITY ANALYSIS FOR INDUCTIVE LINKS AND TSV STACKS

Thermal issues are one of the most important concerns in 3-D circuits, which can degrade the performance of the system. High circuit densities and the slow heat removal increase the vulnerability of 3-D ICs to thermal problems. Previous works, however, consider only the reliability of the circuit or, in other words, the goal is to avoid the thermal runaway of the circuit. Several techniques also target to prevent from hotspots that can accelerate the failure and/or aging mechanisms of a 3-D system. Care, however, has not been placed on the effect that thermal issues can have on signal integrity among planes. This effect of thermal gradients on the quality of inter-plane communication is investigated in this section. Note that although these thermal gradients can obey, for example, the reliability constraints of a 3-D system, the gradients can still affect signal integrity as shown in this section. The effect of thermal gradients for both the TSVs and inductive links is explored.

Intuitively, thermal issues can be more pronounced in contactless links, since the TSVs support faster heat conduction. Furthermore, due to the large size of the contactless links as compared to TSVs, horizontal thermal gradients also affect the performance of these links, while in TSVs the vertical gradients dominate the thermal behavior of these interconnects. Since the resistance of the metals is a function of temperature, thermal gradients can change the resistance of the links, which affects the signal integrity. Thermal gradients are assumed to affect only the resistance of the via and the on-chip inductor and the thermal dependency of the resistance of the silicon substrate is ignored for simplicity. Characterizing the TSVs and inductive links at high frequencies and considering the temperature dependency of the TSV impedance characteristics is a challenging task. Due to lack of experimental data or analytic models on the other parameters of the links, the capacitance and inductance are also treated as being independent of the temperature.

In all data communication processes, a certain amount of power is lost during data transformation, which degrades signal integrity. The parameter S_{21} is, typically, utilized to evaluate this power loss. S_{21} is one of the scattering parameters, used to describe linear networks. For a two-port network, S_{21} is determined as the output to input voltage ratio. This parameter has been utilized as a metric to evaluate signal integrity of different communication methods.

To investigate the effect of thermal gradients on the resistance of the inductor, a standard structure of an inductive link is investigated. Several equivalent circuits for spiral inductors have been proposed.[34–36] The equivalent circuit considered in this paper is depicted in Figure 2(b). The scattering parameter of this model can be described by

$$S_{21} = \frac{V_R}{V_T} = \frac{1}{1 - j\omega C_R R_R} \cdot j\omega k \sqrt{L_T \cdot L_R} \cdot \frac{1}{R_T + j\omega L_T} \quad (1)$$

The effects of temperature variation on S_{21} can be determined by

$$\frac{\partial S_{21}}{\partial T} = \frac{\partial S_{21}}{\partial R} \cdot \frac{\partial R}{\partial T} \quad (2)$$

where S_{21} changes with temperature since the resistance of the link is temperature dependent. The electrical resistance of a metal is typically approximated as a linear function of temperature, which is sufficiently accurate for the operating temperature range of integrated circuits. To analyze non-uniform temperature profiles, however, lumped

models of resistance as shown in Figure 2(b) are inefficient. Consequently, the total resistance of the metal is described by

$$R = \frac{1}{A}\oint_l \rho_0 \left[1 + \alpha_0 \left(T_x - T_0\right)\right] d_x \tag{3}$$

where ρ_0 and α_0 are the resistivity and temperature coefficients, respectively, of the material used for the inductor or the TSV (e.g., copper) at a reference temperature. The cross-sectional area is denoted as A and the integration is performed along the length of the metal.

5.1. Case Study

To describe the temperature variation effects on the inductive link, a pair of copper spiral inductors is employed. The coupling coefficient (k), which is assumed to be independent of temperature, is equal to 0.25. The number of turns is three where the width of each turn is 800 nm, the spacing between the turns is 4 μm, and the outer diameter of the inductor is 300 μm. This link is suitable for propagating the clock signal between two planes.[4]

A stack of three TSVs is used as a test structure to investigate the effect of temperature on signal integrity for signal TSVs. The *RLC* model introduced in Ref. [13] and shown in Figure 3 is used for a common TSV. In this model the capacitive coupling of the TSVs is modeled by $C_{\text{ox\_via}}$, C_{ox}, C_{sil} which indicate, respectively, the capacitance of the thin oxide layer surrounding the via, the capacitance due to the oxide layer (the liner) on the silicon layer, and the capacitance of the silicon substrate. L_{via} is the inductive component of the TSV which is determined by $L_{\text{via}} = L_{\text{via0}}/[1 + \log(f/108)^{0.26}]$ where L_{via0} is the inductance of the via at 0.1 GHz. The resistance of the via and silicon substrate is denoted by R_{via} and R_{sil} where $R_{\text{via}} = R_{\text{via0}}(1 + f/108)^{0.5}$ and R_{via0} is the resistance of the via at 0.1 GHz. The diameter of the TSVs is swept from 5 μm to 55 μm to support different types of TSVs. The length of TSVs is determined to support the proper aspect ratio for TSV diameter (i.e., an aspect ratio of 5 for thin TSVs and lower aspect ratio for thick TSVs). The extracted parameters are $C_{\text{ox\_via}} = 910$ fF, $C_{\text{sil}} = 9$ fF, $C_{\text{ox}} = 3$ fF, $G_{\text{sil}} = 1.69$ m/Ω.[13] The L_{via0} and R_{via0} for different TSV are determined after[15] and are listed in Table II.

Different temperature profiles can be considered for an integrated circuit due to different locations of local hot spots.[37] Three temperature profiles are used to model the thermal variations within an AC-coupled 3-D circuit.

Table II. Characteristics of different simulated TSVs.

Diameter (μm)	5	10	15	20	25	30	35	40	45	50	55
Length (μm)	25	50	75	100	125	150	150	150	150	150	150
R_{via0} (mΩ)	24	12	8	6	4.8	4	3	2.2	1.8	1.4	1.2
L_{via0} (pH)	7	15	22	30	38	46	43	41	39	37	35

These profiles include a linear change in temperature in the x-direction, a hot spot developed at the lower left corner of the inductor, and another hot spot is assumed to be developed at the center of the inductor. The temperature profiles are, respectively, described by

$$T(x) = T_{\text{C}} + 10^5 x \tag{4}$$

$$T(x, y) = T_{\text{C}} - \frac{2 \times 10^9}{3}[(x - 150\mu)^2 + (y - 150\mu)^2] \tag{5}$$

$$T(x, y) = T_{\text{C}} - \frac{5 \times 10^8}{3}(x^2 + y^2) \tag{6}$$

Similar profiles are considered for the TSV stack that can cause the same temperature gradient in the z-direction as shown in Figure 7.

Two temperature ranges are assumed, each corresponding to a low-power (LP) and high-performance (HP) 3-D circuit. As shown in Ref. [38], local hot spots with temperature up to 110 °C and temperature gradient of 25 °C can be generated in high performance 3-D circuits. Consequently a temperature range of 85 °C to 110 °C is considered to simulate the high performance scenario. For the low power scenario the same temperature gradient is considered. Since the absolute temperature for low power circuits is lower than high performance circuits, the local hot spots are assumed to have a maximum temperature of 60 °C and the temperature reduces to 27 °C at the cool regions of the circuit.

The TSV stack and the inductor pair are simulated using Cadence Spectre and the amplitude of S_{21} for these profiles is depicted in Figure 8. Increasing the temperature leads to higher metal resistance and higher power loss which reduces $|S_{21}|$. This degradation is more pronounced for the low power scenario since in the high performance scenario, the absolute temperature is higher and the effect of temperature gradient is less prominent.

As depicted in Figure 8(a), for inductive links in the low-power (LP) scenario, a 60 °C hot spot in the corner of the inductor decreases $|S_{21}|$ by 14% as compared to a uniform temperature of 27 °C. A hot spot at the center of the inductor causes a 7.8% decrease in $|S_{21}|$. Considering

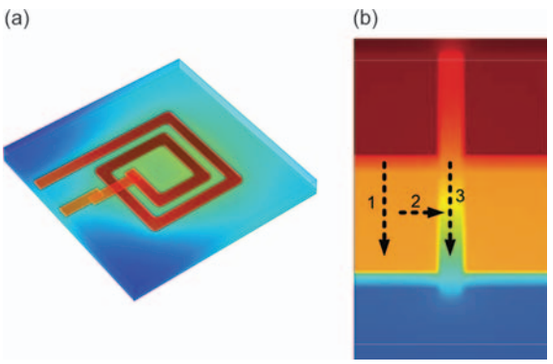

Fig. 7. Temperature variation (a) across an inductive link and (b) along a TSV.

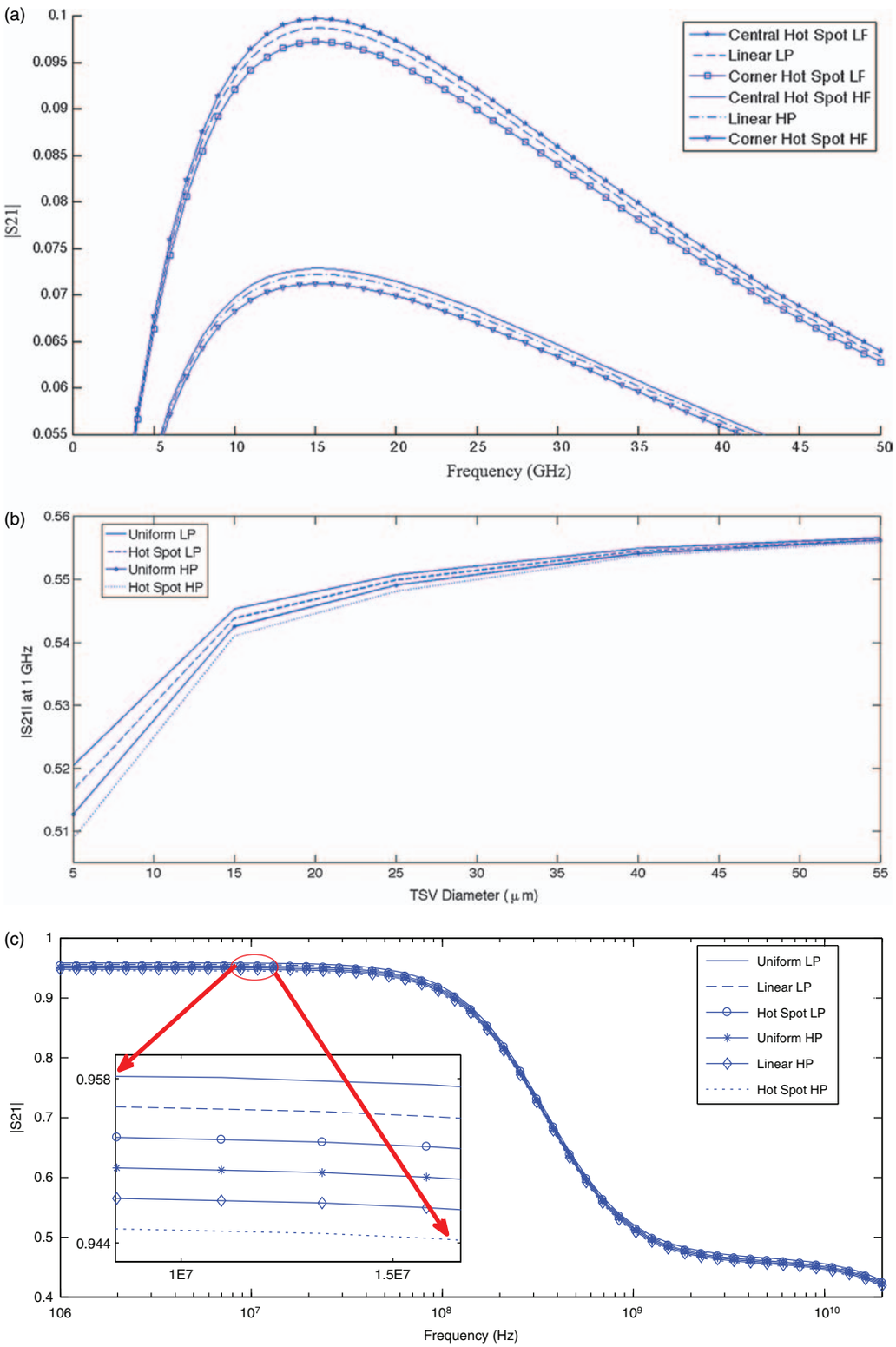

Fig. 8. Amplitude of $|S_{21}|$ for three temperature profiles (a) for an inductive link and (b) for TSV stack with different diameters at frequency of 1GHz, and (c) for TSV stack with diameter of 5 μm.

the case of a high-performance (HP) circuit with a hot spot of 110 °C to describe the corner of the inductor, $|S_{21}|$ is reduced by 9% in comparison to a uniform temperature of 85 °C. The corresponding decrease for a central hot spot and a linear profile is equal to 7% and 7.2%, respectively.

$|S_{21}|$ of the TSV stack for different diameters at the frequency of 1GHz is shown in Figure 8(b). Reducing the diameter of the TSV increases the resistance of the TSV which, in turn, decreases $|S_{21}|$. Consequently the highest performance degradation is seen for the smaller diameters. The $|S_{21}|$ parameter for TSV with a diameter of 5 μm is plotted in Figure 8(c) for different temperature profiles. The largest reduction in $|S_{21}|$ is caused by the hot spot in the centre of the stack. In the low power scenario $|S_{21}|$ decreases by 0.65% compared to a uniform temperature of 27 °C and in the high performance scenario this reduction is 0.52%.

Not surprisingly, the effect of gradient effects is much more evident for inductive links rather than TSVs. Due to the short length of TSVs, the change in the resistance of the vias as a result of temperature degradation is negligible. Furthermore, the power loss caused by the resistive voltage drop on the inductor turns is considerably higher for inductive links as compared to TSVs. Consequently, the resistance variation affects the performance of the inductive links more than a TSV stack. Simulation results confirm that TSVs are robust to thermal gradient effects. The same temperature variation that can decrease the $|S_{21}|$ of the inductive link by 14% has no noticeable effect ($<$1%) on the frequency characteristics of the TSV stack for a large range of the physical characteristics of these interconnects.

6. SUMMARY

This paper provides an overview of the different roles of TSVs where these wires constitute a precious interconnect resource for 3-D circuits. The different manufacturing and design objectives for signal, power/ground, and thermal TSVs are, respectively, discussed. The propagation delay for signal TSVs, *IR* drop for power/ground TSVs, and the thermal conductivity for TTSVs pose different design requirements for each TSV usage. The effect of the thermal gradients on the behavior of signal TSVs is investigated and compared to inductive links. Simulation results indicate that the TSVs are not susceptible to the temperature variations due to the short length, and low resistance as compared to typical horizontal interconnects. Alternatively, for inductive links, the large area of the inductors and lack of proper heat conductors between the planes make these links more vulnerable to thermal gradients.

Acknowledgments: This work is funded in part by the Swiss National Science Foundation (No. 260021_126517), European Research Council Grant (No. 246810 NANOSYS).

References

1. V. F. Pavlidis and E. G. Friedman, Three-Dimensional Integrated Circuit Design, Morgan Kaufmann Publishers **(2009)**.
2. N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, Analysis and design of inductive coupling and transceiver circuit for inductive inter-chip wireless superconnect. *IEEE Journal of Solid-State Circuits* 40, 829 **(2005)**.
3. E. Culurciello and A. G. Andreou, Capacitive inter-chip data and power transfer for 3-D VLSI. *IEEE Transactions on Circuits and Systems II: Express Briefs* 53, 1348 **(2006)**.
4. J. Xu et al., AC coupled interconnect for dense 3-D ICs. *IEEE Transactions on Nuclear Science* 51, 2156 **(2004)**.
5. S. K. Bobba et al., Performance analysis of 3-D monolithic integrated circuits, *Proceedings of the IEEE International 3D System Integration Conference* **(2010)**, pp. 1–4.
6. S. Tan, R. J. Gutmann, and R. Reif (eds.), Wafer Level 3-D ICs Process Technology, Springer **(2008)**.
7. G. Van der Plas et al., Design issues and considerations for low-cost 3-D TSV IC technology. *IEEE Journal of Solid-State Circuits* 46, 293 **(2011)**.
8. Henry et al., Low electrical resistance silicon through vias: Technology and characterization, *Proceedings of the IEEE International Electronic Components and Technology Conference* **(2006)**, pp. 1360–1365.
9. M. Kawano et al., Three-dimensional packaging technology for stacked DRAM with 3-Gb/s data transfer. *IEEE Transactions on Electron Devices* 55, 1614 **(2008)**.
10. R. S. Patti, Three-dimensional integrated circuits and the future of system-on-chip designs. *Proceedings of the IEEE* 94, 1214 **(2006)**.
11. U. Kang et al., 8 Gb 3-D DDR3 DRAM using through silicon-via technology. *IEEE Journal of Solid State Circuits* 45, 111 **(2010)**.
12. V. F. Pavlidis and E. G. Friedman, Interconnect-based design methodologies for three-dimensional integrated circuits. *Proceedings of the IEEE* 97, 123 **(2009)**.
13. D. M. Jang et al., Development and evaluation of 3-D SiP with vertically interconnected through silicon vias (TSV), *Proceedings of the Electronic Components and Technology Conference* **(2007)**, pp. 847–852.
14. I. Savidis and E. G. Friedman, Electrical modeling and characterization of 3-D Vias, *Proceedings of the IEEE International Symposium on Circuits and Systems* **(2008)**, pp. 784–787.
15. G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, Electrical modeling and characterization of through silicon via for three-dimensional ICs. *IEEE Transactions on Electron Devices* 57, 256 **(2010)**.
16. M. C. Tasi and T. T. Hwang, A study on the trade-off among wirelength, number of TSV and placement with different size of TSV, *Proceedings of the International Symposium on VLSI Design, Automation and Test* **(2011)**, pp. 1–4.
17. M. Hsu, Y. Chang, and V. Balabanov, TSV-aware analytical placement for 3D IC designs, *Proceedings of the IEEE Design Automation Conference* **(2011)**, pp. 664–669.
18. V. F. Pavlidis and E. G. Friedman, Timing driven via placement heuristics in 3-D ICs. *Integration, the VLSI Journal* 41, 489 **(2008)**.
19. J. Cho et al., Through silicon via (TSV) shielding structures, *Proceedings of the IEEE Conference on Performance of Electronic Packaging and Systems* **(2010)**, pp. 269–272.
20. K. Onizuka et al., Chip-to-chip inductive wireless power transmission system for SiP applications, *Proceedings of the IEEE Custom Integrated Circuits Conference* **(2006)** pp. 575–578.
21. Y. Yuxiang, Y. Yoshida, and T. Kuroda, Non-contact 10% efficient 36 mW power delivery using on-chip inductor in 0.18-μm CMOS, *Proceedings of the IEEE Asian Solid-State Circuits Conference* **(2007)**, pp. 115–118.

22. N. H. Khan, S. M. Alam, and S. Hassoum, Through-silicon via (TSV)-induced noise characterization and noise mitigation using coaxial TSVs, *Proceedings of the IEEE International Conference on 3D System Integration* **(2009)**, pp. 1–7.
23. W. S. Zhao, Y. X. Guo, and W. Y. Yin, Transmission characteristics of a coaxial through-silicon via (C-TSV) interconnect, *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility* **(2011)**, pp. 373–378.
24. M. B. Healy and S. K. Lim, Distributed TSV topology for 3-D power-supply networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 1 **(2012)**.
25. I. Tsioutsios, V. Pavlidis, and G. De Micheli, Physical design tradeoffs in power distribution networks for 3-D ICs, *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems* **(2010)**, pp. 435–438.
26. V. F. Pavlidis and G. De Micheli, Power distribution paths for 3-D ICs, *Proceedings of the International ACM Great Lakes Symposium on Very Large Scale Integration* **(2009)**, pp. 263-268.
27. N. H. Khan, S. M. Alam, and S. Hassoun, Power delivery design for 3-D ICs using different through-silicon via (TSV) technologies. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 19, 647 **(2011)**.
28. H. Xu, V. F. Pavlidis, and G. De Micheli, Analytical heat transfer model for thermal through-silicon vias, *Proceedings of the Conference on Design, Automation, and Test in Europe* **(2011)**, pp. 395–400.
29. B. Goplen and S. Sapatnekar, Thermal via placement in 3D ICs, *Proceedings of the International Symposium on Physical Design* **(2005)**, pp. 167–174.
30. G. Haung et al., Power delivery for 3D chip stacks: Digital modeling and design implication, *Proceedings of the IEEE on Electrical Performance for Electronics Packaging Conference* **(2007)**, pp. 205–208.
31. J. Cong and Y. Zhang, Thermal via planning for 3-D ICs, *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design* **(2005)**, pp. 744–751.
32. N. Miura et al., A 0.14 pJ/b inductive-coupling transceiver with digitally-controlled precise pulse shaping. *IEEE Journal of Solid-State Circuits* 43, 285 **(2008)**.
33. D. Mizoguchi et al., Measurement of inductive coupling in wireless superconnect. *Jpn. J. Appl. Phys.* 45, 3286 **(2006)**.
34. N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Analysis and design of inductive coupling and transceiver circuit for inductive inter-chip wireless superconnect. *IEEE Journal of Solid-State Circuits* 40, 829 **(2005)**.
35. S. S. Mohan et al., Simple accurate expressions for planar spiral inductors. *IEEE Journal of Solid-State Circuits* 34, 1419 **(1999)**.
36. J. C. Guo and T. Y. Tan, A broadband scalable model for on-chip inductors incorporating substrate and conductor loss effects. *IEEE Transactions on Electron Devices* 53, 413 **(2006)**.
37. A. H. Ajami, K. Banerjee, and M. Pedram, Modeling and analysis of nonuniform substrate temperature effects on global ULSI interconnects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 24, 849 **(2005)**.
38. B. Black et al., Die stacking (3D) microarchitecture, *Proceedings of the IEEE/ACM International Symposium on Microarchitecture* **(2006)**, pp. 469–479.

Somayyeh Rahimian

Somayyeh Rahimian *received the B.S. degree in electrical engineering from Sharif University of Technology and M.S. degree in electronics engineering from University of Tehran in 2004 and 2006, respectively. She is currently working towards the Ph.D. at Integrated Systems Laboratory, EPFL, Lausanne, Switzerland. Her research interests includes 3-D integration and mixed signal designs.*

Vasilis F. Pavlidis

Vasilis F. Pavlidis *(M'09) received the B.S. and M.Eng. degrees in electrical and computer engineering from the Democritus University of Thrace, Xanthi, Greece, in 2000 and 2002, respectively, and the M.Sc. and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, in 2003 and 2008, respectively. He is currently a post-doctoral researcher with the Integrated Systems Laboratory, EPFL, Lausanne, Switzerland. From 2000 to 2002, he was with INTRACOM S.A., Athens, Greece. In Summer 2007, he was with Synopsys Inc., Mountain View, CA. His current research interests include the area of interconnect modeling, 3-D integration, networks-on-chip, and related design issues in VLSI.*

Giovanni De Micheli

Giovanni De Micheli *(S'79-M'83-SM'89-F'94) is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He is program leader of the Nano-Tera.ch program. Previously, he was Professor of Electrical Engineering at Stanford University. His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies, networks on chips and 3D integration. He is also interested in heterogeneous platform design including electrical components and biosensors, as well as in data processing of biomedical information. He is author of: Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994, co-author and/or co-editor of eight other books and of over 400 technical articles. Professor De Micheli is the recipient of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He is a Fellow of ACM and IEEE. He received the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000. He received the 1987 D. Pederson Award for the best paper on the IEEE Transactions on CAD/ICAS, two Best Paper Awards at the Design Automation Conference, in 1983 and in 1993, and a Best Paper Award at the DATE Conference in 2005. He has been serving IEEE in several capacities, namely: Division 1 Director (2008–9), co-founder and President Elect of the IEEE Council on EDA (2005–7), President of the IEEE CAS Society (2003), Editor in Chief of the IEEE Transactions on CAD/ICAS (1987–2001). He is and has been Chair of several conferences, including DATE (2010), pHealth (2006), VLSI SOC (2006), DAC (2000) and ICCD (1989).*