Design of Resonant Clock Distribution Networks for 3-D Integrated Circuits

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Abstract. Designing a low power clock network in synchronous circuits is an important task. This requirement is stricter for 3-D circuits due to the increased power densities. Resonant clock networks are considered efficient low-power alternatives to conventional clock distribution schemes. These networks utilize additional inductive circuits to reduce the power consumption while delivering a full swing clock signal to the sink nodes. A design method for 3-D resonant clock networks is presented. The proposed design technique supports resonant operation for pre-bond test, an important requirement for 3-D ICs. Several 3-D clock network topologies are explored in a 0.18 μm CMOS technology. Simulation results indicate 43% reduction in the power consumed by the resonant 3-D clock network as compared to a conventional buffered clock network.

Keywords: 3-D integration, clock distribution networks, resonant clocking.

1 Introduction

Aprimary challenge in designing synchronous circuits is how to distribute the clock signal to the sequential parts of the circuit [1].This issue can be more challenging for 3-D circuits since a clock path can spread across several planes with different physical and electrical characteristics [2].

As the area of the integrated circuits increases, larger networks are required to distribute the clock signal, which results in higher capacitive loads and resistive losses of the interconnects degrading the signal integrity along these interconnects. A common solution to alleviate this problem is to insert clock buffers in the intermediate nodes of the clock network. Although buffer insertion improves clock signal integrity, clock buffers significantly increase the power consumed by the network. 3-D integration drastically decreases the interconnect length of the global wires, which can reduce the number of clock buffers and result in more power-efficient clock networks. Alternatively, thermal issues are more pronounced in 3-D integrated circuits. Clock networks consume a great portion of the power dissipated in a circuit [3].Consequently, designing low power clock networksfor 3-D circuits is aprimary challenge.

An efficient approach to eliminate the repeaters and reduce power is to use resonant clocking [8-10]. In this approach, on-chip inductance is added to the clock

J.L. Ayala et al. (Eds.): PATMOS 2011, LNCS 6951, pp. 267–277, 2011.

network and forms a resonant circuit with the interconnect capacitance, decreasing, in this way, the power consumed by the network, since the energy alternates between electric and magnetic fields instead of dissipating as heat.

Testing is another important issue in 3-D circuits. Pre-bond test, includes testing each plane before bonding to other planes and can improve the yield of 3-D systems [4]. 3-D clock networks often include several disconnected networks in some of the planes, which connect with through-silicon-vias (TSVs) to the plane where the main tree feeds the clock signal to the entire clock distribution network. To provide pre-bond test, each plane needs a complete clock tree. A technique to provide such a tree by employing additional wiring has recently been presented [5]. In another approach each disconnected clock tree is driven by a DLL, enabling pre-bond test for each plane of the 3-D system [6].

Both methods support pre-bond test for traditional clock networks by providing a means to connect the local networks within each plane. The nature of resonant clock networks, however, poses different constraints. For example, resonant operation should be achieved for each individual plane during testing irrespective of the employed pre-bond testing approach. The design of 3-D resonant clock networks and the related constraints have not been explored as compared to traditional planar clock networks [4-8]. Consider for example, a 2-D circuit that employs a monolithic *LC* tank to resonate. This design would be inadequate for a 3-D resonant clock network, since pre-bond test is not supported. The resonant 3-D clock network should be designed such that resonant operation at a specific frequency is individually achieved for each plane as well as for the entire 3-D system.

The contribution of this paper, consequently, is a novel design methodology that addresses these two objectives. The proposed 3-D resonant clock networks considerably lower the power of the clock distribution system, while pre-bond test is supported by the proper design and allocation of the *LC* tanks within each plane. In this way, resonant operation is ensured for each plane either in test or functional mode and the clock signal characteristics are maintained within each plane and for either operating mode. Different designs of a resonant clock network for up to eight-plane 3-D circuits are investigated. Simulation results indicate that using a resonant clock network can significantly decrease the power consumption of the clock tree in 3-D circuits. Furthermore, the results confirm that the power consumed in a 3-D clock network is lower than a 2-D clock network due to the shorter interconnect length.

In the following section, the design of resonant clock networks for 2-D circuits is reviewed. A design methodology for 3-D resonant clock networks supporting pre-bond test is proposed in Section 3. Simulation results are presented in Section 4 and some conclusions are drawn in the last section.

2 Resonant Clocking

A seminal work, introducing the concept and design of resonant transmition lines has been published in [7]. A design ofa global clock distribution network is presented in [8] in which four resonant circuits are connected to a conventional H-tree structure as illustrated in Fig. 1. Each quadrant consists of an on-chip spiral inductor that resonates with the wiring capacitance of the clock network and the decoupling

capacitor is connected to the other end of the spiral inductor.A simple lumped circuit model is utilized to determine the resonant inductance. The resonant frequency of the network is (in first-order) estimated by $f = \frac{1}{2 \cdot \pi \cdot \sqrt{LC}}$ where C and L, respectively, denote the equivalent capacitance of the network wiring and inductance of the spiral inductors. The decoupling capacitor is employed to provide a positive voltage offset on the grounded end of the resonant inductor and adapt the voltage level to the voltage supply level of CMOS logic [11]. This capacitor should be sufficiently large to guarantee that the resonant frequency of the decoupling capacitor $f_{decap} = \frac{1}{2 \cdot \pi \cdot \sqrt{L\, C_{decap}}}$ is much lower than the desired resonant frequency of the clock network.

Based on this structure, a design methodology for resonant H-tree clock distribution networks is proposed in [9]. In this work, the clock tree is modeled with a distributed *RLC* interconnect as illustrated in Fig. 2. This electrical model is utilized to determine the parameters of the resonant circuit and the output impedance of the clock driver such that the power consumed by the network and the clock driver are minimum, while a full swing signal is delivered at the output nodes.

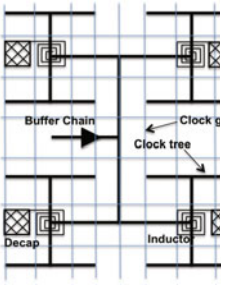

Fig. 1. Resonant clock network with four resonant circuits [8]

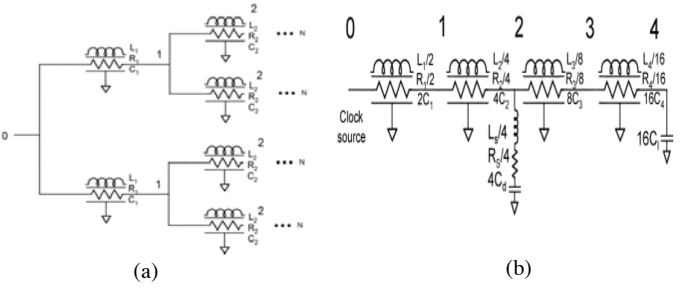

Fig. 2. *RLC* model of a 16-sink H-tree clock network where (a) is the distributed *RLC* model and (b) is the simplified *RLC* model of a resonant network [9]

To delivera full swing signal at the sink nodes, the magnitude of the transfer function of the network, H_{out}, should be close to one. This parameter is often fixed to 0.9 [9, 11] (for the remainder of the paper a "full swing signal" implies any signal swing that satisfies this specification). As shown in [9], when $|H_{out}|$ is fixed at 0.9, the driver resistance can be determined by

$$R_{driver} = \sqrt{\frac{\left|H_{\omega}(j\omega)\right|^2 \cdot \left|Z_{in\_\omega}\right|^2}{0.9^2} - Img(Z_{in\_\omega})^2} - Real(Z_{in\_\omega}) \ , \quad (1)$$

Where H_{ω} and Z_{in_ω} notate the transfer function and input impedance of the network.

Several resonant circuits can be utilized to improve the characteristics of the clock signal. In a symmetric H-tree clock network, the number of *LC* tanks (resonant circuits) also depends on the location of these circuits. If the resonant circuits are

placed closer to the driver, fewer circuits are needed and, alternatively, where these circuits are placed close to the sink nodes, more *LC* tanks are required. Since the equivalent inductance is the parallel combination of all the inductors as shown in Fig. 2, increasing the number of resonant circuits leads to a larger required inductance for each circuit. Using a higher number of larger inductors resultsin larger area occupied by the resonant inductors.

The number of resonant circuits also affects the output signal swing. As discussed in [11], by increasing the number of resonant circuits and placing these circuits closer to the sink nodes, each inductor resonates with a smaller part of the circuit resulting in lower attenuation of the output signal swing. Alternatively, increasing the number of resonant circuits and using larger inductors in each *LC* tank reduces the quality factor of the *LC* tanks, since in spiral inductors the effective series resistance (ESR) increases more aggressively than the inductance [9]. A lower quality factor for resonant circuits produces a higher signal loss and decreases the output signal swing.

Considering a clock network with 256 sinks driven by an ideal clock driver, $|H_{out}|$ for a different number of resonant circuits over a wide range of resonant inductance is shown in Fig. 3, where for fewer than 16 and more than 64 resonant circuits, the $|H_{out}|$ cannot meet the 0.9 signal swing depicted by the dotted line.

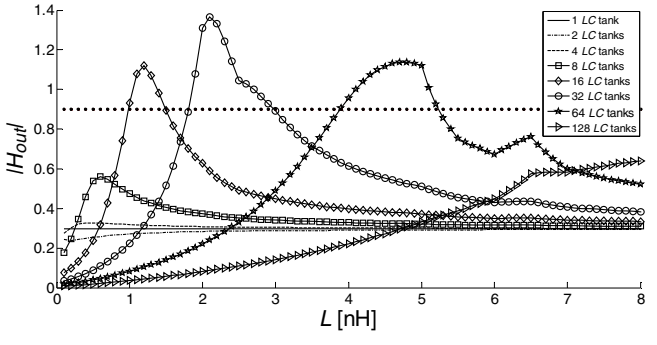

Fig. 3. $|H_{out}|$ for different number of resonant circuits

To determine the number of resonant circuits that maximize the output signal swing, one approach is to only consider the capacitance of the clock network and employ $f = \frac{1}{2 \cdot \pi \cdot \sqrt{LC}}$ to determine the total resonant inductance [11]. By doubling the number of *LC* tanks, the inductance of each tank is also doubled. In this approach, the inductive component of the network wires is not considered. In large clock networks with long interconnects, the inductance of the wires cannot be neglected [9]. Furthermore, this method assumes that placing the resonant circuit in different locations does not change the equivalent capacitance of the network (*i.e.* the capacitance seen by the primary clock driver). These simplifications can result in inaccurate estimation of the resonant inductance, adversely affecting the signal swing.

The signal swing for a clock network with 256 sinks using an ideal driver for different number of *LC* tanks is illustrated in Fig. 4. Employing any inductance within

the crosshatched ranges, this clock network can meet the signal swing specifications. The resonant inductance determined with the simplified approach is illustrated by the dotted lines, where due to imprecise estimation of the inductance, the clock network cannot deliver a full swing signal to the sinks (as required by the dashed horizontal line). As depicted in Fig. 4, using the simplified model from [11] can reduce $|H_{out}|$ from 0.9 to 0.65.

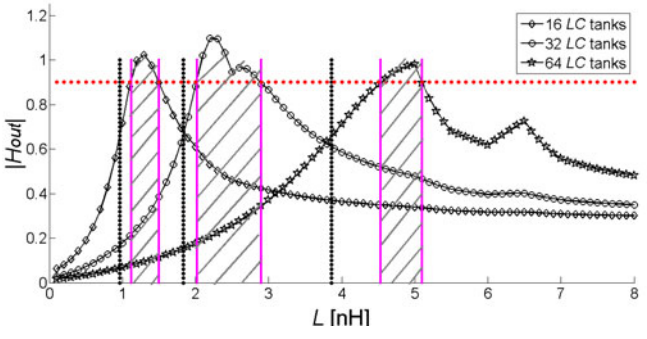

Fig. 4. $|H_{out}|$ for different number of *LC* tanks and resonant inductance using the model in [11] (dotted vertical lines)and the proposed approach (solid vertical lines)

In our approach, a distributed *RLC* model for the network wires is used to determine the required parameters for resonance. Different locations for the resonant circuits from the root to the sinks are investigated. For each location, the driver resistance is adapted to produce a transfer function magnitude of 0.9 for a wide range of inductor sizes using (1). The inductance for which the driver resistance is maximumor the power consumption is minimum (which do not necessarily occur for the same inductance) is determined.

3 Resonant Clocking for 3-D ICs

Different clock network topologies can be considered to adapt the conventional (planar) resonant clock networks to 3-D circuits [2]. In the first topology denoted as "symmetric topology", each plane contains resonant circuits and can be separately investigated. In another structure, denoted as "asymmetric topology", the resonant circuit is placed in only one plane and should resonate with the total capacitance of the 3-D stack at the desired frequency. During pre-bond test, each plane should separately resonate. Note that this requirement is an additional constraint specific to resonant networks and is completely different to the techniques that can be employed to connect the local networks [5, 6] in either a standard or resonant clock distribution approach. Consequently asymmetric structures, which can be considered as an extension of 2-D clock networks, do not support pre-bond test in a straightforward manner, since the resonant circuit is contained within only one plane.

The other important parameter in designing a resonant 3-D clock network is the number of TSVs used to connect the physical planes. From this perspective, different topologies can be explored, for example, using a single TSV in the center of each plane or by using multiple TSVs. In the multiple TSV structure, one of the planes contains a complete clock tree, where for the other planes the clock network consists of several disconnected local networks each connected to the first plane by TSVs. Increasing the number of TSVs provides more local networks increasing the area occupied by the TSVs. Four topologies for a two-plane 3-D circuit with 32 sinks are shown in Fig. 5. *RLC* models to analyze the different 3-D structures are depicted in Fig.6. In single-TSV topologies the equivalent resistance of the circuit is determined as the resistance of each plane divided by the number of planes. By increasing the number of TSVs and omitting some wires in the upper planes, the resistance of these wires is not divided by the number of planes which results in higher equivalent resistance for the 3-D circuit. Alternatively, increasing the number of TSVs results in decreased capacitance for the 3-D circuit.

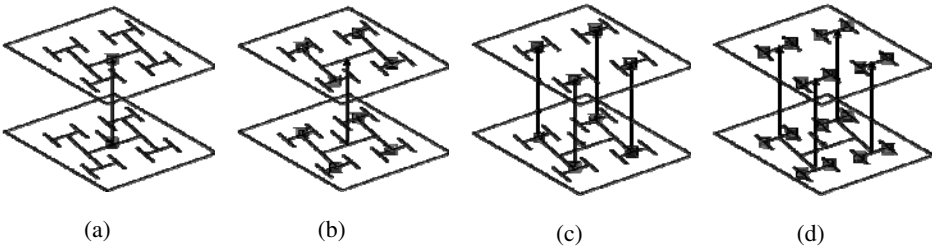

Fig. 5. Different topologies for a two-plane 3-D resonant clock network where (a) is a single TSV structure with one *LC* tank per plane, (b) is a single TSV structure with four*LC* tanks per plane, (c) is a four TSV structure with four *LC* tanks per plane, and (d) is a four TSV structure with eight *LC* tanks per plane.

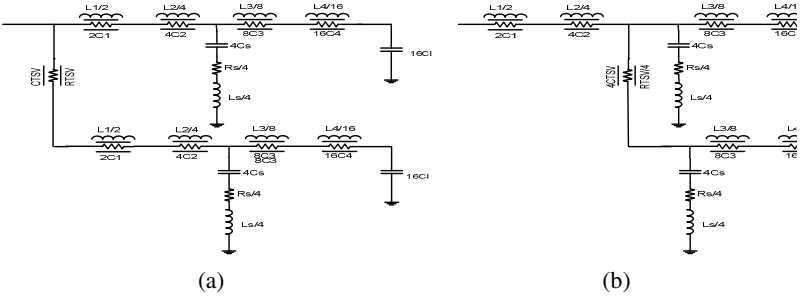

Fig. 6. *RLC* model for a two-plane 3-D circuit with four *LC* tanks where (a) is the model for the single-TSV and (b) is the model for four-TSV structures

To specify the parameters of resonance for a 3-D system with a specific number of TSVs, a distributed *RLC* model of the clock distribution network is employed. The

number of *LC* tanks in each plane is assumed to be more than the TSVssuch that at least one *LC* tank is connected to each local network. The location of *LC* tanks is swept from the TSVs to the sinks. The driver resistance described by (1) is plotted over the inductance to determine the resonant parameters, similar to the 2-D case. In the 3-D system the transfer function for different planes can be different due to the effect of the TSV. Not surprisingly, the last plane (the plane with the greatest distance from the clock driver) has the lowest signal swing. The driver size should be determined such that the signal swing for every plane meets the specifications. Consequently, the transfer function magnitude of the last plane should be used in (1). Following this process, the number of the *LC* tanks and the parameters of the resonant circuits are determined for normal operation.

For pre-bond test, the power consumed by the clock network within each plane is low as compared to the total power consumed by the 3-D system. Consequently, the power consumed by one plane during the pre-bond test mode is a secondary parameter and since the planes are not bonded, heat is removed faster and the thermal constraints are more relaxed. The predominant parameter in test mode is the voltage swing. The clock network should deliver a full swing clock signal to the sinks to test each plane.

During the test mode, each plane should consist of a complete clock network. Additional wiring can be used in each plane to connect local networks except for the first plane [5]. There are two important design parameters in pre-bond test, sizing the additional wires and clock drivers used only during testing. These parameters should be chosen such that a full swing signal is delivered to the sink nodes. There is a tradeoff for determining these parameters. If the wire width is decreased, a larger clock driver should be utilized. Alternatively, increasing the width of the wire results in a smaller clock driver but increases the area occupied by the redundant wires, which are used only during pre-bond test. One simplistic approach is to replicate the tree of the first plane for all the planes during the test mode and also use a driver with the same strengthas the main clock driver. This choice, however, leads to overdesign wasting silicon.

To determine these parameters, the wire width is swept and the related driver resistance is obtained by (1). The driver resistance for different wire width for a two-plane 3-D system with 8 TSVs and 16 resonant circuits is plotted in Fig. 7.

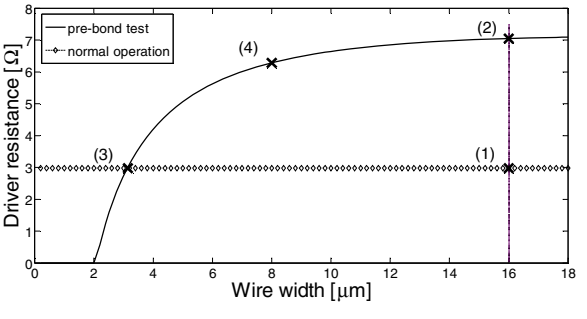

Fig. 7. Driver resistance *vs* wire size

The parameters estimated using the simplistic approach is shown at point 1. For points 2,3, and 4, the parameters are determined using our approach where for point 2 the driver resistance is maximum using the wire size of the first plane and for point 3 the wire size is minimum while employing a replica of the main driver. Point 4 provides a better tradeoff, since the wire width decreases to half of the wire width of point 2 andthe resistance of the driver decreases by only 15%.This resistance is twice as large as compared to the resistance of the driver used to drive the entire clock distribution network.

4 Simulation Results

Assuming an H-tree network as the preferred network in [9], the number of sinks is determined based on the circuit area A and the load capacitance that each sink drives, C_L. A case study of an H-tree resonant clock network with 256 leaves is considered. The load capacitance at each node is assumed to be 20 fF and the operating frequency is 5 GHz. The interconnect length can be determined from the total network area. For a circuit area of $A = l \cdot l$ the length of the longest and shortest interconnects is $l/4$ and $l/2^{n+2}$, respectively, where n indicates the number of sinks.

The PTM model for a 0.18 μm CMOS technology is used to estimate the resistance, inductance, and capacitance of the horizontal interconnects. The total area of the network is 3.4 mm $\times$ 3.4 mm. The parameters of the interconnects are listed in Table 1, where L_1 to L_8 indicate the different wire segments from the driver to the sinks.

Table 1. Interconnect parameters used in the investigated clock network.

	L1-L5	L6	L7	L8
R [Ω/mm]	2.75	5.5	11	22
L [nH/mm]	0.46	0.6	0.72	0.82
C [fF/mm]	254.6	175.4	130	103

For a conventional (non-resonant) clock network, inverters are properly inserted at the intermediate nodes to deliver a full swing clock to the output, while in the resonant clock network, resonant circuits are added to the clock tree to provide a proper clock signal at the output. The amount of the resonant inductance is determined as described in the previous section. The decoupling capacitor that should be sufficiently large not to affect the frequency of resonance is set to 60 pF. The effective series resistance (ESR) for the inductors is determined from [9].

Different topologies of 3-D circuits are explored. To form a 3-D system, the 2-D circuit is folded into several planes. The electrical and physical characteristics of the TSVs used to connect these planes are based on [13]. The number of *LC* tanks, the inductor size for each resonant circuit, and the clock driver resistance for normal and pre-bond operation are listed in Table 2. The size of the wiresin the upper planes for pre-bond test is determined and compared with the size of the wires in the first plane. The resulting decrease in wire width is also listed in this table.

Increasing the number of TSVs can result in a smaller primary driver and lower power due to the decreased capacitive load of the clock network. Alternatively, increasing the resistance of the circuit requires a larger primary driver, increasing the power consumed by the clock network. Predicting which behavior is dominant is not straightforward and strongly depends on the interconnect characteristics of the clock network. Using wide wires results in stronger capacitive behavior, while in long wires the resistive component can become dominant. For this case study, as shown in Table 2, there is not a uniform trend for the design parameters as a function of the number of TSVs.

The power consumed by different topologies for standard and resonant clock networks is listed in columns 7 and 8 of Table 2. As reported in this table, the power consumed by the resonant clock network is considerably lower than the standard network in 3-D circuits. This improvement is accompanied by an increase in the area occupied by the resonant circuits. The area of a resonant clock network increases due to these additional circuits, but alternatively, omitting the clock buffers can decrease the area of the resonant networks.

Increasing the number of planes decreases the length of the wires in the network for a specific number of sinks. Omitting long interconnects as required for some of the topologies shown in Fig. 5 reduces the resistive voltage drop and the capacitance of the network and decreases the power consumed by the network. For a 3-D circuit with two planes, the power consumption reduces up to 64%, where this reduction reaches to 70% and 72% for circuits with four and eight planes, respectively. Decreasing the equivalent capacitance of the network also results in larger resonant inductance and increases the area of the resonant clock network. Alternatively, by increasing the number of planes, the driver size and the width of the additional wires required for pre-bond test, reduces due to the smaller circuit area in each plane.

Table 2. Design parameters and power consumption for different topologies

		# *LC* tanks	*L* [nH]	R_{driver} [Ω]	R_{driver} [Ω] pre-bond	Wire width reduction (%)	Power [mW]	
							Standard	Resonant
2-D	-	32	2.2	1.2	-	-	543	310
3-D 2 planes	1 TSV	16	1.5	3.25	7.16	0	385	241
	2TSV	16	1.4	2.95	6.2	50	374	230
	4 TSV	16	1.5	2.77	6.1	50	353	244
	8 TSV	16	1.3	2.98	5.6	50	312	**196**
	16 TSV	32	3	2.55	5.7	50	347	218
	32 TSV	64	5	0.97	4.5, 2.4	25, 50	304	203
3-D 4 planes	1 TSV	16	1.8	2.15	8.8	0	308	190
	2 TSV	16	1.6	3.55	10	87.5	297	174
	4 TSV	16	1.7	3.9	10.8	81.5	289	**162**
	8 TSV	32	3.2	3.5	8.4	81.5	295	176
	16 TSV	64	6.5	3	6.9	75	308	184
3-D 8 planes	1 TSV	8	1	2.4	17.8	0	299	173
	2 TSV	16	2	3.5	20	87.5	283	**152**
	4 TSV	32	3	3.27	15	81.5	311	188
	8 TSV	64	5	2.65	9	50	307	181

The preferred 3-D structure that decreases the power consumption of the clock network by 72%, consists of eight planes which is the maximum number of planes investigated in this case study. Each plane connects to the others using 2 TSVs. 16 *LC* tanks are used in this structure (two *LC* tanks per plane) and the inductance for each *LC* tank is 2 nH. The number of planes and the number of *LC* tanks is determined such that the highest voltage swing is achieved (which implies that the Q-factor of the spiral inductors is also the highest).

5 Conclusions

A design methodology for resonant clock networks in 3-D circuits is proposed in this paper. The number of *LC* tanks, the resonant circuit parameters, and the driver size fornormal operation are determined such that a full swing signal is provided at the sink nodes and the power consumption of the circuit is minimized. The effect of different parameters including the number of planes and number of TSVs among the planes for designing 3-D resonant clock networks is investigated. An approach to minimize the additional wire width and clock driver size for pre-bond test is proposed. A 256-sink H-tree clock network operating at 5 GHz is considered as the case study where a power reduction of 72% is achieved for aneight-plane resonant clock network in comparison to a 2-D standard network.

Acknowledgements. This work is funded in part by the Swiss National Science Foundation (No. 260021_126517), European Research Council Grant (No. 246810 NANOSYS), and Intel Braunschweig Labs, Germany.

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