Vertically-Stacked Si Nanowire FETs with sub-µm Gate-All-Around polysilicon gates patterned by nanostencil lithography

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Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the planar transistor design. Considering novel device structures, the vertically-stacked nanowire (NW) channel transistor with gate-all-around (GAA) construction has been demonstrated to be one of the best structures in terms of electrostatic control and large drive current, thus enabling further device scaling [1]. We report on a fully CMOS compatible fabrication flow of vertically-stacked polySiNW GAA FETs by means of optimized Bosch process [2] and nanostencil lithography [3]. In a previous work, the authors envisaged stencil lithography [4] as a key enabler for gate patterning on 3D structures, such as vertically-stacked nanowire transistors [1]. In this work, nanostencil lithography is used to deposit the Al mask used to pattern sub-µm gate-all-around polysilicon gates deposited with LPCVD as alternative solution for patterning nanoscaled features having high aspect ratio, which is a non trivial issue in photoresist lithography. Preliminary electrical characterizations performed before the metal contact formation demonstrate functional memristive FET operation and confirming the behavior of previously reported devices fabricated with standard processing technology and µm-scale gate lengths [5]. The single-level and vertically-stacked nanowire devices are fabricated with yield larger than 70%, demonstrating a new method for 3D transistor fabrication with sub-µm nanostencil lithography.

The fabrication process starts by oxidizing 500nm of Si wafers in wet atmosphere. Then 50nm or 350nm polySi deposition is performed on different substrates, respectively. Individual or arrays of lines of widths of 50nm and length of 8µm are patterned with diluted HSQ using e-beam lithography (EBL). The HSQ lines are used as masks for the SiNW etching (Fig. 1a). In the case of thick polysilicon samples, 6 etching cycles are used to form stacks of 3 nanowires. Then 10nm dry oxidation followed by a 100nm LPCVD polySi deposition are performed (see Fig. 1b). A 40nm thick Al layer is deposited through the aligned nanostencil as an etching mask for the polysilicon (Fig. 1c), which is patterned to form pad areas for electrical characterization as well as polysilicon gates with lengths between 150nm and 500nm (Fig. 1d). A transistor with 3 vertically-stacked levels in a single horizontal strand is shown in Fig. 2. Gate length is 350nm and total stack height is 400nm. A transistor with a single-level horizontal nanowire array with 50nmx50nm square section and 350nm gate length is shown in Fig. 3. The Al mask deposited with the nanostencil guaranteed a very good 3D conformal etching, as confirmed by the electrical characterizations.

The nanostencil is made of 100nm thick LPCVD low stress SiN. The gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows.

Electrical characterization is carried out with a manual probe station connected to a Agilent B1500 semiconductor parameter analyzer. Tungsten tips are put in contact with the polySi source/drain pads and on the Al/polySi gate pad. The I_{ds}-V_{ds} curves (Fig. 4) show device ambipolarity with hysteresis related to the surface trapping sites at either the polysilicon grain boundary and at the gate oxide interface. More detailed explanation of the electrical behavior can be found for similar to previously reported devices [5].

In conclusion, a very versatile approach using nanostencil lithography to pattern sub-µm long gates is demonstrated with yield larger than 70% for different nanowire structures. The method provide excellent step coverage on either single and vertically-stacked nanowires. The electrical behavior confirms the results obtained from similar devices fabricated with a standard lithography approach while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling.

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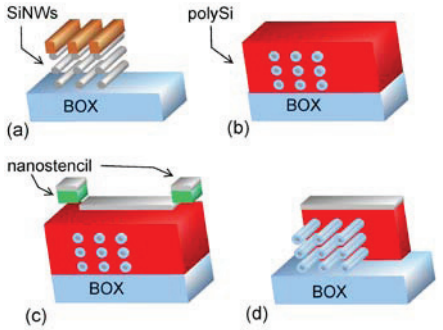

Figure 1. Fabrication flow of vertically-stacked SiNW transistors. (a) SiNWs are etched with Bosch process. (b) 10nm dry oxidation and 100nm LPCVD polySi is deposited. (c) 40nm Al mask is deposited through nanostencil. (d) polySi gate is patterned.

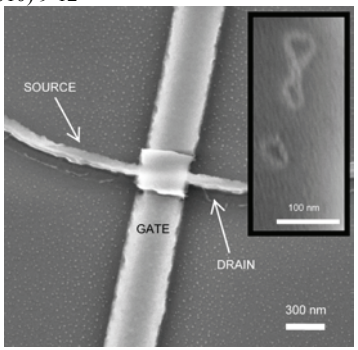

Figure 2. Si nanowire transistor with 3 vertically-stacked single-stranded 30nm diameter channels (see inset). Gate length is 350nm.

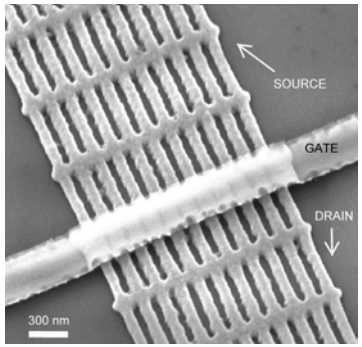

Figure 3. Si nanowire transistor with 11 channels with 50nmx50nm channel cross-section, 350nm long polysilicon gate.

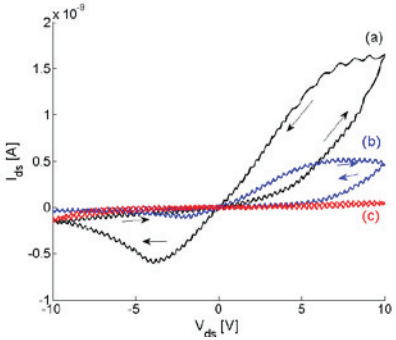

Figure 4. I_{ds}-V_{ds} hysteresis for a FET device with vertical-stacked nanowire channels: (a) V_{gs} = -5V. (b) V_{gs} = -3V. (c) V_{gs} = -1V.