Characterization of Memristive Poly-Si Nanowires via Empirical Physical Modelling

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Abstract—**Memristors are passive circuit elements that behave as resistors with memory. The recently illustrated experimental realization of memristive behaviour of Polysilicon Nanowires has triggered interest in this concept, which is promising to a wide variety of application areas that include neuromorphic circuits. In order to progress with practical implementations that use this technology we need to expand our understanding of the conduction mechanisms in these structures and of the underlying relationship between device behavior and process manufacturing parameters. In this paper we explore these mechanisms through detailed simulation, which includes model calibration and correlation with experimental results. Through fitting of the test results we identify a unique set of density of states that characterize the particular technology implemented.**

I. INTRODUCTION

In 1971, Leon Chua introduced the concept of a missing fundamental passive element in electronics called the memristor (short for memory resistor) [1]. The prediction of the discovery of the memristor was based on conceptual symmetry arguments which followed from the description of basic passive circuit elements as defined by the relation between two of the four fundamental circuit variables, namely voltage V, current I, charge q, and magnetic flux Φ. Chua demonstrated that memristors could not be obtained by any combination of the other three fundamental elements: resistors, capacitors and inductors. A memristor is characterized by its memristance M(q), which is the time-dependent rate of change of the magnetic flux with respect to the electric charge: $M(q(t))=d\Phi(t)/dq(t)$. Since magnetic flux is the time integral of voltage, whereas charge is the time integral of current I, one may write that: $M(q(t))=V(t)/I(t)$ which is more convenient since voltage and current can easily be measured experimentally. The essential property of a memristor is its memory – the dependence of resistance on the operational history of the device. At the time that the theoretical properties of a memristor were described, there was no experimental demonstration of a memristor as a two-terminal passive element. Chua proposed modelling of a memristor with the use of electric circuits, comprising at least 15 transistors and other passive elements [1]. Potential applications in programmable logic, signal processing, neural networks, and control systems have been proposed [2]. The ideal memristor response in terms of M(q(t)) is a step function at q = 0 between an ‘‘on” and an ‘‘off” state. Interest in memristors was recently renewed when Williams et al. [3] demonstrated the first memristor as a passive, two-terminal element made from a thin (5 nm) film of TiO_2sandwiched between two Pt metal electrodes. The memristance of the device was attributed to ion drift in the film and a subsequent modulation of the bulk conductivity [3]. It was further postulated that memristive behaviour should be common in nanoscale electronics devices, in which high electric fields can induce ionic motion. In terms of response, this was not an ideal memristor, and there was a transition region between the ‘‘on” and ‘‘off” states, as one would expect for a realistic material.

The significance of memristors arises from their natural existence in biological computational systems. For instance, ion diffusion is responsible of the time-dependant conductance of the neuron membrane in the Hodgkin-Huxley model [4], which is therefore modelled as a memristive device. Learning mechanisms are also explained using the memristive model of synapses [5] and they were demonstrated with single devices [6]. Self-programming circuits were demonstrated by embedding memrsitors into logic circuits [7].

The memristor effect, seen as the hysteretic behavior of the I-V curve, may be obtained by using circuitry that includes active elements and an internal power source [1, 8]. However, this solution is just an emulation of memristors and it consumes valuable chip area and power. With the scaling of device dimensions, new phenomena have been claimed to be responsible for the memristor behavior in monolithic devices. For instance, it has been demonstrated that a memristor effect arises naturally in nanoscale systems in which solid-state electronic and ionic transport are coupled under an external bias voltage [3]. Voltage driven memristor effects were demonstrated as well in Pt/organic/Ti [9], in PEO/PANI polymeric [6], on flexible materials [10] and in amorphous Silicon devices [11].

In this paper the transfer characteristics of a poly-Si nano wire field effect transistor (poly-SiNW FET) are studied through systematic analytical simulation and model calibration and correlation with test

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results. From the experimentally measured transfer characteristics of the device we can extract the important parameter "density of states (DOS)" of the nanowire, which characterize the behaviour of the Poly-SiNW. Through simulation, all the known physical models that govern our device's characteristics were identified and confirmed the operation; they are the classical drift-diffusion model, the generation-recombination (Shockley-Read-Hall, SRH) model and the Band to Band Tunneling (BBT) model.

II. PHYSICAL MODELING

A pictorial representation of the device is given in Fig. 1, whereas fabrication details are presented elsewhere [12]. Figure 2 plots the measured transfer characteristic of a fabricated back-gated device at V_{ds}=3.1V. The hold time is the time the voltage applied before the current is measured. The delay time is the delay between two successive measurements. The hysteresis loop which is clearly evident, is the signature of a memristive effect [3].

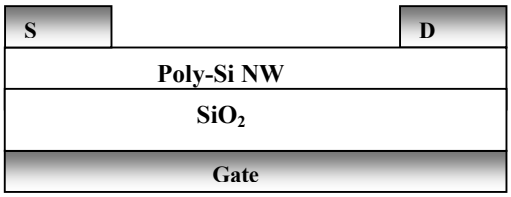

Fig. 1: Pictorial representation of Poly-SiNW FET

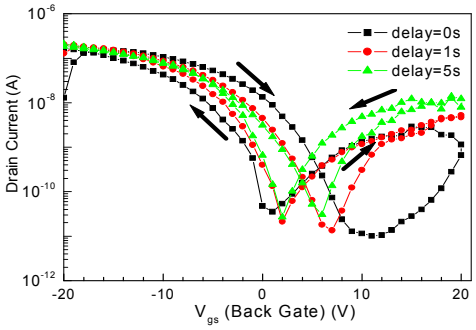

Fig. 2: Variation of hysteresis width of I_{ds}-V_{gs} (back-gated devices) at V_{ds}=3.1V. The delay time is a parameter of study and the hold time is 0s.

In order to analyse the electrical characteristics of the above fabricated Poly-Si Nanowire Transistors, 2-D numerical simulation was performed using the ATLAS advanced numerical simulator [13]. The simulation solves a set of fundamental field equations that link together the electrostatic potentials and the carrier densities, within the simulation domain. The system of equations solved includes (a) the Poisson's equation which relates the variations in electrostatic potential to local charge densities, and (b) the continuity and transport equations, which describe the evolution of free carrier density as a result of transport, generation and recombination processes.

The electrical characteristics of Poly-Si Nanowire Transistors are strongly influenced by the presence of traps. The trapped charge in the gap states contributes to the total space charge and strongly affects the generation-recombination rate. The above effect is accounted for in the simulation by using suitable expressions of the trapped charge in Poisson's equation and by modifying the expression of the generation-recombination rate in the continuity equations. In our model we assume traps to be uniformly distributed over the entire volume of the Poly-SiNW. This assumption is quantitatively justified because of the small grain size of the polycrystalline material under consideration. More specifically, negligible errors are introduced so long as the grain size is small and comparable to the Debye length associated with the local carrier concentration. In this case, no appreciable band-bending occurs within the grains, and the effect of a non-uniform trap distribution is smoothed out by statistical averaging. In the simulated devices the polycrystalline silicon active-layer is undoped; therefore, the above assumption appears to be reasonably-well fulfilled within the bulk.

Trap states are classified as acceptor and donor states. The acceptor states are electrically neutral when empty, hence they become negatively charged when trapping an electron; their concentration is larger in the upper half of the gap. The donor states become positively charged by emitting an electron, hence they are neutral when filled; typically, their concentration is larger in the lower half of the gap. Trap-states were taken into account through the use of an effective density of states (DOS) distribution within the poly-Si band-gap. The simulation enables modeling of the DOS either by four exponential terms, two of which are located in the lower half of the band-gap (donor-like) and two in the upper half of the band-gap (acceptor-like), by discrete trap levels, or by an exponential distribution for the tail states and a Gaussian distribution for the deep states, or through combination of the three cases.

III. RESULTS

Experimental results are compared with their simulated counterparts in order to draw conclusions regarding the transfer mechanisms of Poly-Si Nanowire Transistors. Fitting was achieved by using the classical drift-diffusion model, generation - recombination (Shockley-Read-Hall, SRH) and the Band to Band Tunneling (BBT). Other models such as impact ionization and various other tunneling or temperature dependent models did not have a noticeable effect on the on-current region

and were not considered further in modeling the transfer characteristics. The effective mobility was modeled using the Lombardi mobility model which takes into account the transverse and longitudinal field, the doping concentration, the interface roughness, and the scattering of carriers [13]. A fixed negative trapped charge of $2x10^{12}$ cm^2 at the interface Poly-Si/SiO_2 was included in the model.

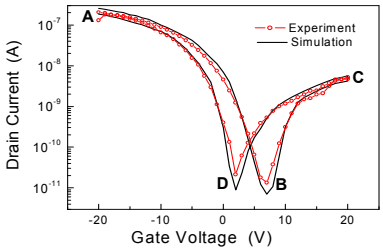

Fig 3. Comparison between experimental transfer characteristics at V_d = 3.1 V for back gate measurements and simulation results from ATLAS 2-D simulator. The active layer thickness is 20 nm and the active channel length is: 20 μm.

As far as the simulation is concerned, in addition to the physical models selected and referred to above, a parameter of great influence on the electrical characteristics of the Poly-Si Nanowire Transistors, is the density of states (DOS). In order to extract the unique DOS that characterizes the Poly-Si Nanowire Transistors under consideration, a 2-D simulation was used; through optimization, experimental results were fitted with the simulation results in the entire biased region (-20V to +20V) of the transfer characteristic of the specimen with V_d= 3.1 V. Simulation results are presented in Fig. 3, and they are in very good agreement with their experimental counterparts, thus proving that the established DOS used in the simulation, correctly models the polysilicon nanowire.

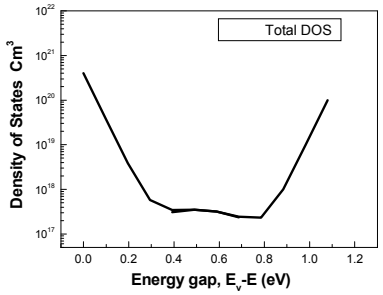

Fig.4. The density of states extracted from experimental data and used in2-D simulations for fitting the transfer characteristics of the back-gated device with a channel length of 20 μm.

This total density of states (DOS), described by the function g(E) as illustrated in Fig. 4 was modelled as the sum of two exponential terms, one for the tail band states near the conduction and one for the states near the valence band (a donor-like at the valence and an acceptor-like at the conduction) and two deep level bands with Gaussian distribution (one acceptor-like and the other donor-like). The model expression is given by (1):

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad (1)$$

where, E is the trap energy. The subscripts T, G, A and D stand for tail, gaussian (deep level), acceptor and donor states, respectively. The DOS distributions are defined as follows:

$$g_{TA}(E) = N_{TA}\exp\frac{[E-E_C]}{[W_{TA}]}; \qquad g_{TD}(E) = N_{TD}\exp\frac{[E_V-E]}{[W_{TD}]}$$

$$g_{GA}(E) = N_{GA}\exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^2\right]; \quad g_{GD}(E) = N_{GD}\exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \quad (2)$$

E_C and E_V are the conduction and valence band energies. For the exponential tail distribution, the DOS is described by its conduction and valence band edge intercept densities (NTA and NTD), and by its characteristic decay energy (WTA and WTD) and its peak energy/peak distribution (E_{GA} and E_{GD}).

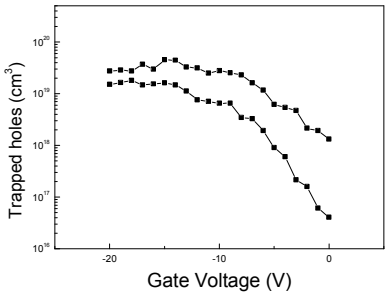

Fig.5. Simulated results for the trapped holes in the nanowire film from the fitting in Fig. 3

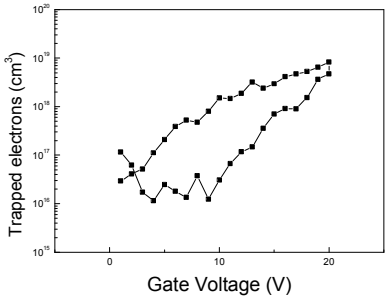

Fig. 6. Simulated results for the trapped electrons in the nanowire film from the fitting in Fig. 3

The simulations have confirmed that charge trapping and detrapping explains the hysteresis in Fig. 3. From (A) to (B), trapped holes at the SiO_2/poly-Si interface create positive fixed charges, and they become detrapped with increasing V_{gs}. Figure 5 plots the trapped concentration of holes for gate voltages 0V to -20V and can be seen that it

has a similar behaviour as the I_d-V_g curve in Fig 3. From (B) to (C), an electron channel is created. With increasing electron density, more electrons are trapped at the SiO_2/poly-Si interface, leading to a negative interface charge density. From (C) to (D), electrons are detrapped with the vanishing electron channel. Detrapping is a slower process than trapping, thereby explaining the hysteresis (B)-(C)-(D). Figure 6 shows the simulated results of the trapped electrons for gate voltages 0V to +20V and again the curves in this figure are similar to the I_d-V_g curve in Fig. 3 explaining that the hysterisis curve is related to the trapping and detrapping of the electrons. From (B) to (A), a hole channel is created and it increases the trapping probability for holes. This is a faster process than detrapping of holes, once again explaining the hysteresis (D)-(A)-(B). The off-current at (B) is lower than the one at (D) because of the additional probability of electrons being trapped in SiO_2 besides the electrons trapped at the SiO_2/poly-Si interface.

IV. CONCLUSIONS

In this paper, results obtained from numerical simulation of a poly-Si NW field effect transistors using a 2-D device analysis program (ATLAS) were presented. Through fitting of the tests results using physical modelling, a unique set of density of states was identified, consisting of two exponential terms for the tail trap states and two Gaussian terms for the deep states. This density of states matched successfully the data for the experimental transfer characteristics at positive and negative gate voltages. Experimental results showed an ambipolar hysteretic behavior of the realized structures. Numerical simulations confirmed that the hysteretic effect is due to charge trapping at the interface states between the channel and the gate oxide.

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