PHYSICAL DESIGN TRADEOFFS IN POWER DISTRIBUTION NETWORKS FOR 3-D ICs

Ioannis Tsioutsios, Vasilis F. Pavlidis, and Giovanni De Micheli
Integrated Systems Laboratory
EPFL
Lausanne, Switzerland
{ioannis.tsioutsios, vasileios.pavlidis, giovanni.demicheli}@epfl.ch

Abstract—**A physical model for the design of the power distribution networks in three-dimensional integrated circuits is proposed. The tradeoffs among the different design parameters are specified and analyzed. Different case studies are explored, indicating that smaller and denser TSVs can deliver power more efficiently as compared to larger and coarsely distributed TSVs. The interplay between the TSV count and the intra-plane power distribution network in reducing the power supply noise is also shown.**

Keywords: 3-D Integrated Circuits; Power Distribution Networks; Through Silicon Vias

I. Introduction

Three-dimensional integration, using Through Silicon Vias (TSV) to connect several dies together, is an emerging technology that can improve the integrating density and the performance of future ICs [1]. For this technology to become feasible, however, several technological and design challenges should be addressed.

Power integrity is an important and complex design issue in 3-D ICs [1]. The use of TSVs, creates longer current paths resulting in increased voltage drop across the planes. Considering that a TSV consumes silicon area, the density and dimensions of this novel type of interconnect are greatly restricted. Additionally, the allocation of the decoupling capacitors could become an issue due to the increased complexity of a 3-D grid [2]. To this end, the understanding of the design parameter tradeoffs, the careful allocation of the vertical and horizontal interconnects, and decoupling capacitors can improve the overall efficiency of the Power Distribution Network (PDN) within a 3-D IC.

There have been few research efforts for the modeling of power distribution networks for 3-D ICs. In [3], an analytical model is proposed to determine the power supply noise in the power distribution network of a 3-D circuit that is modeled by an *RLC* grid. An *RLC* grid is also utilized in [4] to analyze the behavior of a 3-D power distribution network. The power delivery task for different 2-D and 3-D circuits including resistive and inductive voltage drop is discussed in [5].

These models, however, do not offer any insight regarding the physical design of the power grids within a 3-D circuit. In addition, the inter-dependence of the TSVs and the intra-plane interconnects used for the power grid is not captured. To address these issues a new model that describes the voltage drop in a 3-D power grid, while including the physical traits of the TSVs and the intra-plane interconnects is presented. This model can be used to efficiently explore the tradeoffs among the different interconnects resources in the design process of 3-D power distribution networks.

The proposed voltage drop model is presented in Section II. In Section III, expressions describing the *IR* drop in each plane are obtained. The effect of the decoupling capacitors attached to the PDN of a 3-D IC is discussed in Section IV. The main points of the paper are summarized in Section V.

II. Model of Power Distribution Networks

The proposed voltage drop model for 3-D ICs is described in this section. There are two primary technologies for the fabrication of TSVs [6]. The "via last" approach, where the TSVs are fabricated during the back-end of the line, and the "via first" approach, where the TSVs are fabricated during the front-end of the line. In this paper a "via last" approach is assumed for the manufacturing of the TSVs within the 3-D circuit. The modeling approach, however, can also be applied to a "via first" approach with minor modifications.

The technology can allow wafer stacking in a back-to-front manner and each TSV connects the top metal layers of two adjacent planes. For the placement of the TSVs, a uniform distribution across the plane in power-ground pairs is adopted, as illustrated in Figure 1. The placement of power-TSVs next to ground-TSVs reduces the length of the return paths of the current, thereby, contributing to the reduction of the total loop inductance [7]. Expressions for the capacitance, self-inductance, and resistance of a TSV are given in [8].

Each plane is assumed to consume I_c current that is uniformly distributed across the area A_c of each physical plane. It has been shown in [9], that by partitioning a 2-D circuit into multiple regions and simulating one partition, the induced voltage drops are accurately described. Considering a 3-D circuit with uniform current demand across the planes, each plane can be partitioned to unit cells as illustrated in Figure 1. Each TSV pair acts as a low impedance path that locally supplies current to the cell area of each plane. No current is assumed to flow between cells. The area of each cell is given by the expression $A_{cell} = 2A_c/N_{TSV}$, where N_{TSV} is the total number of TSVs within each plane. The dissipated current in each cell, consequently is $I_{cell} = 2I_c/N_{TSV}$.

For the design of the intra-plane power distribution network a paired interdigitated grid is assumed as depicted in Figure 2. The pitch of the pairs is denoted as $P_{p,n}$, $S_{p,n}$ is the spacing between two pairs, and $H_{p,n}$ is the height of a metal line. The width of each metal line is $W_{p,n}$ and the separation distance between a power-ground pair of lines is $W_{min,p,n}$, where p and n indicate the plane and the metal layer within that plane, respectively. A method to determine the total voltage drop from the top to the bottom metal layer in 2-D circuits has been proposed in [10]. A similar approach is adopted to describe the total voltage drop within a cell shown in Figure 2. In this way, the equivalent resistance is obtained. The length of a metal wire between two vias, in metal layer n, is $l_{seg} = P_{p,n+1}$. The dissipated current along this segment is $I_{seg} = (I_c/A_c)P_{p,n+1}P_{p,n}$. Consequently, the voltage drop along this segment including the vias, is

$$V_{seg} = \frac{I_c}{A_c} P_{p,n+1} P_{p,n} \left(\frac{\rho P_{p,n+1}}{2W_{p,n}H_{p,n}} + R_{via} \right). \quad (1)$$

Denoting the number of parallel pairs of power-ground lines in the n^{th} metal layer of the p^{th} plane of a cell as $N_{p,n}$, the voltage drop within the cell at the n^{th} layer of the p^{th} plane can be obtained by multiplying and dividing (1) with $N_{p,n}N_{p,n+1}$,

$$V_{p,n} = I_{cell} \left(\frac{\rho P_{p,n+1}}{2W_{p,n}H_{p,n}N_{p,n}N_{p,n+1}} + \frac{R_{via}}{N_{p,n}N_{p,n+1}} \right). \quad (2)$$

The expression for the resistance of the intra-plane PDN is

$$R_{p-plane} = \frac{\rho\sqrt{A_{cell}}}{N_{p,M_p}W_{p,M_p}H_{p,M_p}} + \sum_{1}^{M_p-1} \left(\frac{\rho P_{p,n+1}}{2W_{p,n}N_{p,n}H_{p,n}N_{p,n+1}} + \frac{R_{via}}{N_{p,n}N_{p,n+1}} \right), \quad (3)$$

where M_p is the number of the top metal layer. The first term of (3) represents the resistance of the top metal layer of plane p.

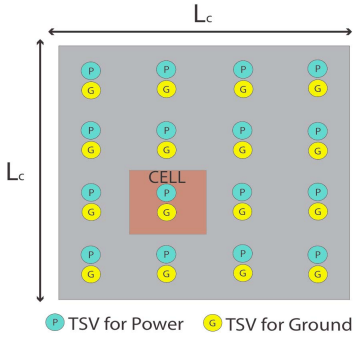

Figure 1. PDN top view-Placement of the TSVs.

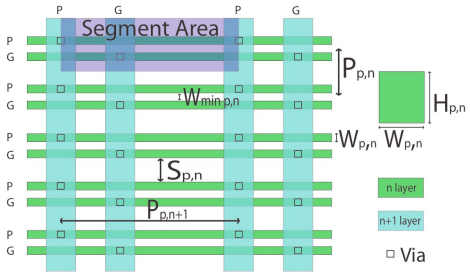

Figure 2. Top-view of the intra-plane power distribution network.

To model the inductance of a power distribution network, an expression for the sheet inductance of a paired interdigitated grid is employed [7]. In this paper, the cells are square so that the sheet inductance of each metal layer is given by

$$L_{sheet} = 0.4P_{p,n}\left(\ln\frac{S_{p,n}}{H_{p,n}+W_{p,n}} + \frac{3}{2} \right) \quad H, \quad (4)$$

and the total inductance of the intra-plane PDN is

$$L_{sheet} = \sum_{2}^{M_p} 0.4P_{p,n}\left(\ln\frac{S_{p,n}}{H_{p,n}+W_{p,n}} + \frac{3}{2} \right) \quad H. \quad (5)$$

Based on equations (3)-(5) and the model of TSVs described in [8], a model for the voltage drop within a cell is proposed and illustrated in Figure 3.

In this model, the nominal V_{Power_Supply} is assumed at the power pads of the topmost plane. The proposed model can be extended, however, to include the package impedance characteristics. A useful feature of this model is that all the lumped components, except for the decoupling capacitors, stem from the physical design parameters of the power distribution network. Consequently, the effect of each of these parameters on the power supply noise within a 3-D circuit is described. Using this model, the physical behavior of 3-D PDNs is investigated in the next section where design guidelines are also offered.

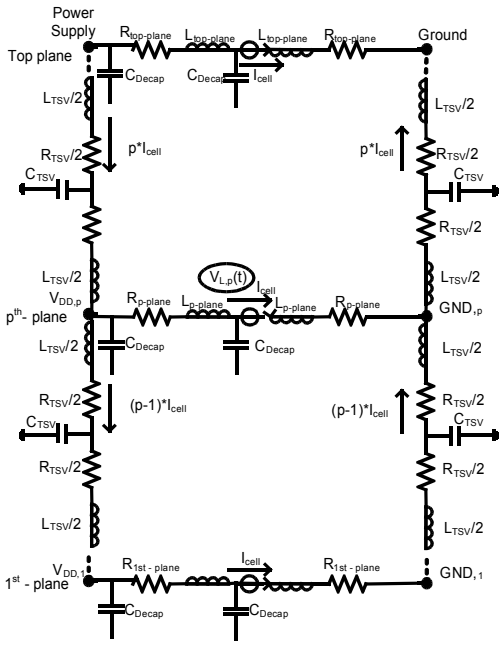

Figure 3. The equivalent *RLC* model describing the PDN of a cell.

III. *IR* Drop Analysis Based on Physical Design Parameters

An important choice for the design of the power distribution network in a 3-D circuit is the amount of the area that is dedicated for the TSVs as compared to the portion of the horizontal metal layers utilized for the intra-plane power distribution network. Allocating more resources than required can have a negative impact in the overall performance of the

circuit, since an overdesigned power distribution network can occupy excessive wiring area that otherwise is used for devices or signal routing. Alternatively, an underdesigned power distribution network can cause unacceptable voltage droops.

Assuming that there is uniform power consumption across each plane and that all planes have the same intra-plane power distribution network, the resistive voltage drop on the top ($V_{DD,p}$) and first metal layers ($V_{L,p}$) of plane p, are determined by:

$$V_{DD,p} = V_{Power\_Supply} - \sum_{k=p}^{N_p-1} kI_{cell}R_{TSV} \ , \quad (6)$$

$$V_{L,p} = V_{Power\_Supply} - \left[\sum_{k=p}^{N_p-1} kI_{cell}R_{TSV}\right] - I_{cell}R_{p-plane} \ , \quad (7)$$

where N_p is the number of planes comprising a 3-D circuit.

As a case study, a 3-D circuit at a 45 nm technology node, which is assumed to consist of ten planes, is considered. The area of each plane is assumed to be 2 cm × 2 cm. According to ITRS data, the power consumption at 45 nm fabrication technology is 64 A/cm^2 [11] and the supply voltage is 1.1 Volts. The TSVs are considered to have 100 μm length and 50 nm dielectric oxide thickness [8]. Each plane has twelve metal layers. The $S_{p,n}$ parameter is variable while $W_{p,n}$, $H_{p,n}$, and $P_{p,n}$ are fixed. The W and H for the first metal layer are 80 nm, and for the second until the ninth are 120 nm. The height of the last three metal layers is 0.3 μm, while the width is 0.3 μm for the tenth and eleventh, and 1 μm for the topmost layer. By changing the spacing $S_{p,n}$, the portion of the area that is dedicated to the intra-plane PDN is adjusted.

According to the proposed model, the critical parameter for the *IR* drop on the top metal layer of each plane (denoted as $V_{DD,p}$ in Figures 4 and 5) is the total area occupied by the TSVs (A_{TSV}). The behavior is the same where the circuit has more TSVs with lower diameter or fewer TSVs with increased diameter, as long as the total TSV area remains the same.

Alternatively, the voltage drop on the metal lines next to the load ($V_{L,p}$) differs, since the intra-plane power distribution network affects the overall behavior. Assuming that a specific area of the circuit is dedicated for power TSVs, using more TSVs with smaller diameter results in lower voltage drop at the load. This behavior is due to the denser TSVs. Since the cell area decreases, each TSV provides current within a smaller area through shorter resistive paths. The simulation results in Figures 5 and 6 illustrate how the $V_{DD,1}$ and $V_{L,1}$ vary with the increase in the number and the diameter of the TSVs, respectively. The area of the intra-plane power distribution network varies from 10% to 40% of the area of the circuit. Interestingly, by increasing the number of TSVs, assuming that only 10% of the horizontal resources are allocated to the PDN, the voltage difference between the first and the topmost metal layers decreases, satisfying the constraint of 95% V_{Power_Supply} (Figure 5). On the other hand, when only the diameter of the TSVs is increased and insufficient resources are allocated to the intra-plane power distribution network, the circuit may not meet the voltage constraint as illustrated in Figure 4. In Figure 6, the crosshatched region corresponds to a design space defined by a specific TSV and intra-plane power grid area notated as A_{TSV} and A_{PDN}, respectively. Within this region the 95% V_{Power_Supply} constraint is satisfied.

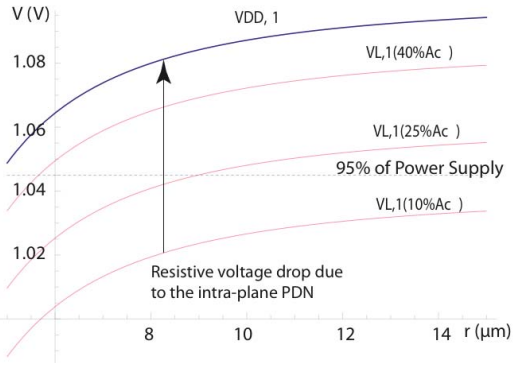

Figure 4. The voltage on the top and first metal layers of the plane located the farthest from the package pads for constant TSV number (10K) and varying TSV diameter is illustrated.

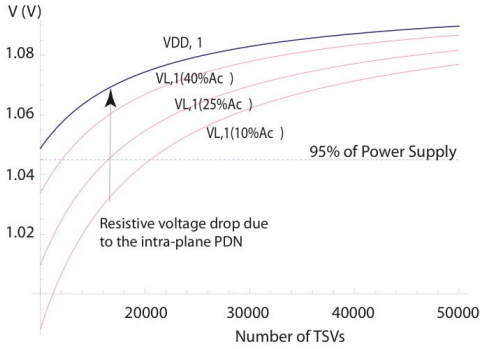

Figure 5. The voltage on the top and first metal layers of the plane located the farthest from the package pads for constant TSV diameter (5 μm) and varying TSV number is illustrated.

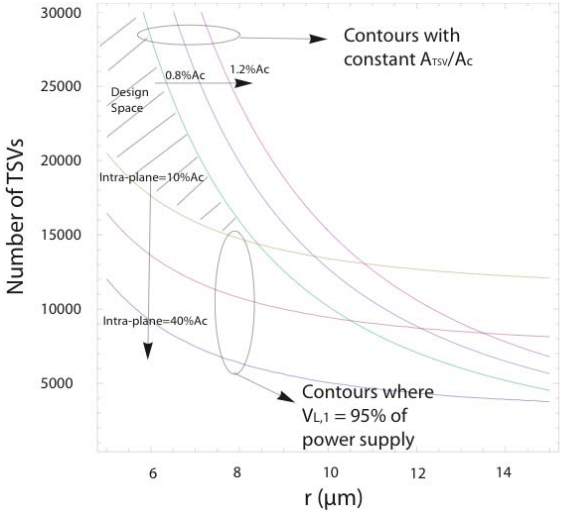

Figure 6. Design space defined by the contour plots $V_{L,1} = 0.95V_{Power\_Supply}$ and $(A_{TSV}/A_c) = constant$. This design space varies as a function of the area

allocated to the intra-plane power distribution network and the area that is occupied by the TSVs, as illustrated by the arrows.

As a case study, the same ten plane 3-D circuit but with TSVs of 10 μm diameter is assumed. If A_{PDN} and A_{TSV} is 40% and 0.4% of the circuit area, respectively, the circuit satisfies the constraint of $V_{L,I} \geq 95\%\ V_{Power\_Supply}$. If A_{PDN} is 10% of the circuit area the TSVs occupy 1.1% of the circuit area satisfying the same constraint. This result indicates that by slightly increasing the density of TSVs a great reduction in the intra-plane power distribution resources in favor of signal routing resources can be achieved.

Consider the same 2-D circuit (4 cm^2) as another case study implemented as a two-plane 3-D circuit by using TSVs with 10 μm diameter and 25% of the circuit area is dedicated to the intra-plane power distribution network. The required area of the TSVs becomes 0.56% of the total area of the circuit. If the number of planes increases the required TSV density increases linearly. This result indicates that the adoption of 3-D technology can improve the integration density with small cost in the silicon area occupied by power and ground TSVs.

IV. Effect of the Decoupling Capacitors in 3-D ICs

The proposed physical model is used in this section to investigate the inductive component of the power supply noise in 3-D ICs. The effect of decoupling capacitors in these circuits is also explored. For this analysis, SPICE simulations are performed using the proposed *RLC* model.

Decoupling capacitance has been modeled with two equally sized capacitors in each cell. One capacitor is located next to the load and the other capacitor is considered to be placed close to the TSV.

To better understand the effect of the decoupling capacitance in the overall PDN design, two different 3-D circuits are investigated. Both of these circuits are assumed to comprise four planes (2 cm × 2 cm) and TSVs with 5 μm diameter. In the first circuit, 10% of the area is dedicated to the intra-plane power distribution network while in the second 40%. Adjusting the number of power/ground TSVs so as $V_{L,I} = 0.98V_{Power\_Supply}$, the first circuit has more TSVs (0.62% of A_c) resulting in a smaller cell as compared to the second circuit which requires fewer TSVs (0.19% of A_c) and has a larger cell area. During the transient simulation all four current sources sink 10 mA modeled as a triangle pulse with rise and fall times of 50 ps and 100 ps, respectively.

For the circuits to have low rippling and meet the constraint of 95% V_{Power_Supply}, decoupling capacitors should be added. Simulation results show that the first circuit requires 473 μF/m^2, while the second circuit requires 124 μF/m^2. Assuming that the decoupling capacitors are MOS capacitors the first circuit needs 0.9% of the circuit area for decoupling capacitors, while the second 0.2%, based on the 45 nm technology data [11].

By dedicating more resources to the intra-plane power distribution network of the latter circuit, the need for decoupling capacitors decreases. This result is due to the efficiency of a decoupling capacitor that improves if the impedance of the path between the load and the capacitor decreases [7]. The results of DC analysis (Section III) indicate that the increasing density of TSVs suffices to fulfill the specified voltage drop constraint although there are few resources allocated to the intra-plane PDN (*e.g.*, 10%A_c). The inductive component, however, imposes a lower bound on the intra-plane resources, since further reducing the fineness of the power grid renders the decoupling capacitors inefficient.

V. Conclusions

An analytical model that relates the physical characteristics of the intra-plane power grids and TSVs is presented. The tradeoffs among the physical design parameters of 3-D power distribution networks are explored. Utilizing smaller and denser TSVs is a more efficient means to decrease the resistivity voltage drop in 3-D circuits as compared to larger and sparser TSVs. Furthermore, increasing the number of planes in a 3-D circuit does not lead to a considerable increase in the demand for power/ground TSVs. Consequently, the intra-plane metal resources for the power grids can be traded off for a higher TSV density, with a small overhead in silicon area. The inductive component of the power supply noise, however, sets stricter bounds on these interconnect resource tradeoffs due to the decreasing efficiency of the decoupling capacitance.

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