Clock and Power Distribution Networks for 3-D Integrated Circuits

Ioannis Savidis and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester,
Rochester, New York 14627, USA
{iosavid, friedman}@ece.rochester.edu

Vasilis F. Pavlidis and Giovanni De Micheli
LSI-EPFL
1015-Lausanne, Switzerland
{vasileios.pavlidis, giovanni.demicheli}@epfl.ch

Abstract – Global interconnect design for three-dimensional integrated circuits is a crucial task. Despite the importance of this task, limited results related to global issues have been presented. Challenges in reliably distributing power, ground, and the clock signal within a multi-plane integrated system are discussed in this paper. The design of two 3-D test circuits addressing these issues is described. Candidate 3-D topologies for both power and clock distribution networks are also presented. Design implications due to the different design approaches are discussed. Experimental and simulation results of the 3-D clock and power distribution architectures, respectively, are provided. Both of the test circuits are fabricated by the 3-D fabrication process developed at MIT Lincoln Laboratories (MITLL). The design of the clock and power distribution networks is discussed.

I. Clock Distribution Networks for 3-D ICs

Distributing the clock signal in 3-D ICs is a complex and challenging task as sequential elements synchronized by the same clock signal can be located on multiple planes [1]. In 2-D circuits, symmetric interconnect structures, such as H- and X-trees, are widely utilized to distribute the clock signal across a circuit [2]. An extension of an H-tree to three dimensions does not guarantee equidistant interconnect paths from the root to the leaves of the tree. The impedance of the TSVs can increase the time for the clock signal to arrive at the leaves of the tree on specific planes as compared to the time for the clock signal to arrive at the leaves of the tree located on the same plane as the clock driver [3]. Consequently, asymmetric topologies can be potential candidates for distributing the clock signal in a 3-D integrated system.

Another fundamental issue in the design of clock distribution networks is low power consumption, since the clock network dissipates a significant portion of the total power consumed by a synchronous circuit [2]. This demand is stricter for 3-D ICs due to the increased power density and related thermal concerns.

A test circuit investigating the distribution of the clock signal has been recently designed. The test circuit is fabricated by the MITLL process which is a fully depleted silicon-on-insulator process (FDSOI). The minimum feature size of the devices in this test circuit is 180 nm, with one polysilicon layer and three metal layers interconnecting the devices on each wafer. The dimensions of the TSVs in this test circuit are 1.75 µm × 1.75 µm [5]. Each block contains about 30,000 transistors and includes the same logic circuit but implements a different clock distribution architecture.

The function of the logic circuit common to the three blocks is to emulate different switching patterns and load conditions for the clock distribution networks under investigation. Random switching patterns are generated in each block by combining pseudorandom number generators and several groups of four-bit counters that switch current loads over different time intervals.

Each of the three blocks includes a different clock distribution structure, which are schematically illustrated in Fig. 1. The dashed lines depict vertical interconnects implemented by TSVs. These architectures combine different topologies, such as H-trees, rings, and meshes [2]. The fabricated 3-D test circuit is illustrated in Fig. 2. The highest operational frequency is 1.4 GHz. Clock skew measurements indicate that the topology in Fig. 1a produces, on average, the lowest skew as compared to the other two topologies. The clock skew among the planes is greater for the local mesh topology (see Fig. 1b) as compared to the H-tree topology, primarily due to the unbalanced clock load for certain local meshes. Alternatively, the clock distribution network that includes the global rings exhibits the highest clock skew among all topologies due to the greater difference in distance that the clock signal traverses on each plane [7].

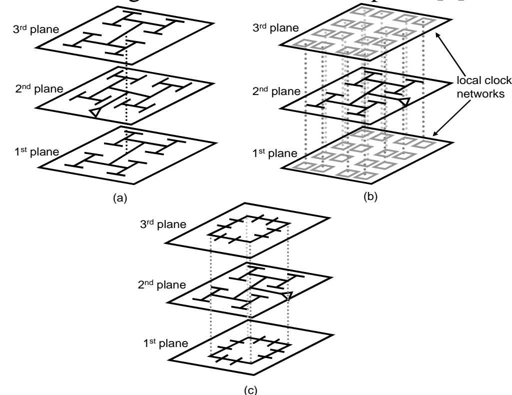

Fig. 1 Three 3-D clock distribution networks within the test circuit, (a) H-trees, (b) H-tree and local meshes, and (c) H-tree and global rings.

II. Power Distribution Networks for 3-D ICs

Another important global issue is the design of robust power distribution architectures for 3-D ICs [8]. In planar ICs where flip-chip packaging is adopted as the

packaging technique, an array of power and ground pads are allocated throughout the surface of the die to provide the necessary current for the circuit to operate properly. Increasing current densities and faster current transients, however, further complicate the design of power distribution networks. Three-dimensional integration alleviates the restraints on using interconnect metal layers for power distribution networks through topologies that are not available in two-dimensional circuits. With 3-D technologies, individual planes can potentially be dedicated to power delivery. Three different 3-D power distribution networks are proposed for the first time. A comparison of the noise on both the power and ground networks for all three topologies is provided. Several tradeoffs among different TSV densities are also explored.

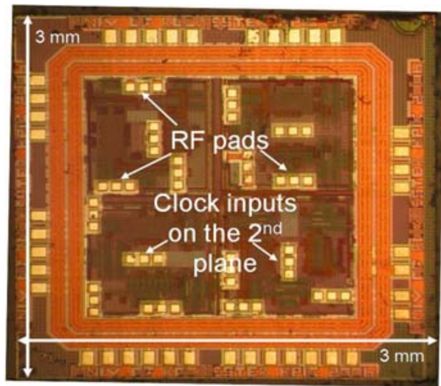

Fig. 2 Fabricated 3-D circuit investigating different clock distribution schemes.

The power networks are included on a test vehicle, which will also be fabricated by MITLL. The target technology is a fully depleted silicon-on-insulator (FDSOI) 150 nm process, where the dimensions of the TSVs have been scaled to 1.5 μm × 1.5 μm [6]. The topologies explored on this test circuit are schematically illustrated in Fig. 3.

Interdigitated power/ground lines are used in all of these topologies where a grid is desirable. There are two primary objectives for the test circuit: *i)* to explore the benefits of a dedicated power/ground plane, and *ii)* to investigate the effect that a higher TSV density has on the noise characteristics of the power network. The upper left and lower topologies shown in Fig. 3 are used to address objective *(i),* while the upper two topologies address objective *(ii)*. The difference between the upper left and upper right topologies is the number of TSVs, where the latter topology includes 50% more TSVs. The TSVs are only located on the periphery of the upper left power distribution network, whereas the upper right topology includes additional TSVs on the power lines crossing the middle of the circuit block.

Each test block includes identical circuitry. The basic logic blocks are shown in Fig. 4. Power supply noise generators draw varying current from the power lines. These noise generators are placed on each plane of each power network topology. Voltage sense circuitry is included on all of the planes within each test block to measure the noise on both the power and ground lines. The only plane that does not include any circuitry is the plane for power and ground (see Fig. 3c). An average of the output voltage from the sense circuitry on each plane within each test block is used to compare the three topologies depicted in Fig. 3.

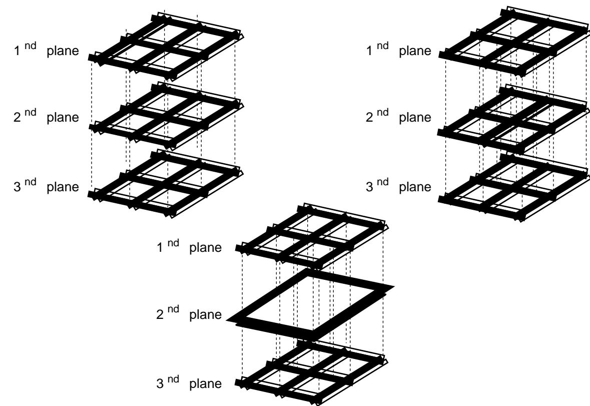

Fig. 3 Three 3-D power distribution networks within the test circuit, (a) TSVs only on the periphery, (b) 50% higher TSV density as compared to (a), and (c) dedicated plane for power and ground distribution.

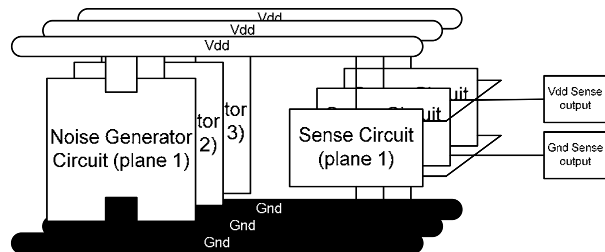

Fig. 4 Power supply noise generators and voltage sense circuitry included in the circuit blocks depicted in Fig. 3.

REFERENCES

[1] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann Publishers, 2009.

[2] E. G. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proceedings of the IEEE,* Vol. 89, No. 5, pp. 665-692, May 2001.

[3] I. Savidis and E. G. Friedman, "Electrical Modeling and Characterization of 3-D Vias," *Proceedings of the International IEEE Symposium on Circuits and Systems*, pp. 784-787, May 2008.

[4] V. Arunachalam and W. Burleson, "Low-Power Clock Distribution in a Multilayer Core 3D Microprocessor," *Proceedings of the ACM International Great Lakes Symposium on VLSI*, pp. pp. 429-434, May 2008.

[5] "*FDSOI Design Guide,*" MIT Lincoln Laboratories, Cambridge, 2006.

[6] "*FDSOI Design Guide,*" MIT Lincoln Laboratories, Cambridge, 2008.

[7] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D Integrated Circuits," *Proceedings of the IEEE International Conference on Custom Integrated Circuits,* pp. 651-654, September 2008.

[8] G. Huang *et al.,* "Power Delivery for 3D Chip Stacks: Physical Modeling and Design Implication," *Proceedings of the IEEE Electrical Performance of Electronic Packaging Conference*, pp. 205-208, October 2007.