# Design of Compact Imperfection-Immune CNFET Layouts for Standard-Cell-Based Logic Synthesis

Shashikanth Bobba[1], Jie Zhang[2], Antonio Pullini[1], David Atienza[3] and Giovanni De Micheli[1]
[1]LSI-EPFL, [3]ESL-EPFL, Lausanne (Switzerland), [2]Stanford University, Stanford (USA)
{shashikanth.bobba, antonio.pullini, david.atienza, giovanni.demicheli}@epfl.ch and zhangjie@stanford.edu

***Abstract* – The quest for technologies with superior device characteristics has showcased Carbon Nanotube Field Effect Transistors (CNFETs) into limelight. Among the several design aspects necessary for today's grail in CNFET technology, achieving functional immunity to Carbon Nanotube (CNT) manufacturing issues (such as mispositioned CNTs and metallic CNTs) is of paramount importance. In this work we present a new design technique to build compact layouts while ensuring 100% functional immunity to mispositioned CNTs. Then, as second contribution of this work, we have developed a CNFET Design Kit (DK) to realize a complete design flow from logic-to-GDSII traversing the conventional CMOS design flow. This flow enables a framework that allows accurate comparison between CMOS and CNFET-based circuits. This paper also presents simulation results to illustrate such analysis, namely, a CNFET-based inverter can achieve gains, with respect to the Energy-Delay Product (EDP) metric, of more than 4x in delay, 2x in energy/cycle and significant area savings (more than 30%) when compared to a corresponding CMOS inverter benchmarked with an industrial 65nm technology.**

***Keywords – Carbon Nanotube Transistors, Logic Synthesis, CNT, Imperfection Immune, Misaligned Immune, CNFET.***

## I. INTRODUCTION

FORESEEING the trends dictated by Moore's law and anticipating the fundamental limits of CMOS technology in the near future [1], the semiconductor industry is in a quest for a successor technology to CMOS. Among the technologies being considered, *Carbon Nanotube Field Effect Transistors (CNFETs)* appear to be one of the promising successors to MOSFETs due to their superior device characteristics [2, 3, 18]. Among the different types of CNFETs (Schottky Barrier CNFET, MOSFET-like CNFET, Band-To-Band-Tunneling CNFET) [4], in this paper we consider Top-gated MOSFET-like *CNFETs (MOS CNFETs)* [3]. For the sake of simplicity, we will refer to MOS CNFETs as just CNFETs from here on. A representative CNFET configuration is shown in Figure 1(a). Highly doped Carbon

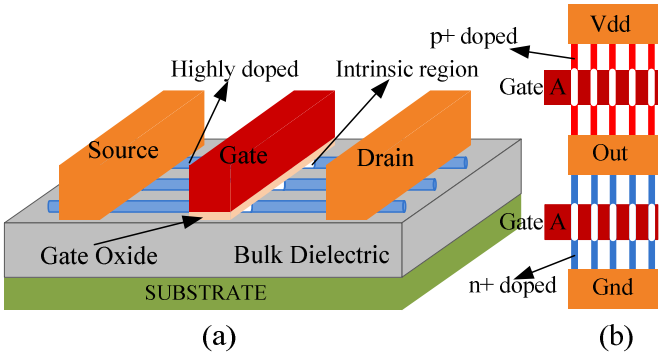


Figure 1 (a) Carbon Nanotube Field Effect Transistor. (b) CNFET Inverter.

Nanotubes (CNTs) over the bulk form the channel between the source and the drain contacts. However, during the doping process the gate is self-aligned thereby having the intrinsic CNT region under the gate [17]. The current carriers in the CNT channel are controlled by the electric field applied to the gate and the type of doping realized on both sides of the un-doped region. For example, assuming that the blue segments of the CNT are n-doped, applying a positive voltage to the gate would turn on the transistor, hence n-CNFET. Figure 1(b) depicts the basic CNFET inverter, illustrating the doping profile of the CNTs. CNTs in red are p+ doped where as CNTs in blue are n+ doped, the same nomenclature is followed in the entire paper.

In spite of superior device characteristics, CNFET circuits are difficult to realize at large scale because of some serious manufacturing challenges [21] like variations in doping and diameter of CNTs, metallic CNTs and mispositioned CNTs. Though the diameter and doping variations in CNTs cause drain current variations, the major challenge is towards handling metallic and mispositioned CNTs as they affect the functionality of the gate [6, 23]. A part of this work is focused on a design technique to build compact layout technique for handling mispositioned CNTs on a full-wafer-scale. In a CNFET, any mispositioning of CNTs would lead to an ambiguous condition which might compromise the functionality of the logic comprising multiple transistors. Since mispositioned CNTs cannot be avoided by the current CNFET manufacturing technology, [6] has proposed a layout technique that is functionally immune to the mispositioning of CNTs which is referred as "misaligned-CNT-immune layouts". In this paper we propose a new misaligned-CNT-immune layout which ensures 100% functionality while requiring less area when compared to the layout scheme proposed in [6]. We also show in this work that this new layout scheme can be built respecting the design rules of commercially available technologies, by performing our studies on a commercial 65nm technology, and proving the viability of our approach to be embedded into traditional CMOS standard-cell design flows.

While the integration of CNFETs in upcoming circuit designs promises substantial advantages, it also brings to the foreground new challenges and mandates a symbiotic development of manufacturing techniques and CAD tools. In this work we developed a complete CNFET *Design Kit (DK)* to enable the synthesis, from RTL to GDSII, of circuits based on CNFETs. Our DK features the new misaligned-CNT-immune layouts, developed using standard Cadence Design Flows for 65nm technology node. This DK allowed us to benchmark CNFET circuits over CMOS circuits, showing

978-3-9810801-5-5/DATE09 © 2009 EDAA

Energy-Delay-Area Product (EDAP) gains in the order of ~12x over equivalent CMOS at 65nm technology node.

The paper is organized as follows. In Section 2 we discuss the background and related work of CNFET technology in detail. In Section 3 we explain imperfection-immune layouts, emphasizing the problem of mispositioning of CNTs, and present our new compact layout technique. Then, In Section 4 we present the CNFET DK and also detail the standardization of our new layouts. Next, in Section 5 we present the simulation results of our layout with equivalent industrial logic designs in 65nm CMOS. Finally, in Section 6 we summarize the main conclusions of this work.

## II. Background and Related Work

As mentioned before the two main technology constraints that limit the viability of CNFET technology are the mispositioning of CNTs and the presence of metallic CNTs among the semiconducting CNTs, while the CNTs are grown or transferred over a substrate [7]. Metallic CNTs are highly undesirable as they short-circuit the drain and the source of the CNFET. Electrical burning and Chemical etching of the metallic CNTs [8, 18] are the major techniques addressed so far to remove or break them. Zhang et al [9] derive practical processing guidelines for metallic CNT growth and removal, showing that major technology level advancement is necessary for VLSI scale CNFET circuit to be possible. Since the metallic CNT constraint would mainly be handled during the manufacturing stage, we assume that no metallic CNT remains as starting scenario for the application of our work during the rest of the paper. On the other hand, we take up the challenge of addressing the issue of mispositioned CNTs. Though there are a few ways at the physical level to achieve well aligned arrays of CNTs [7], a small percentage of CNTs tend to still get misaligned, thereby not solving the problem.

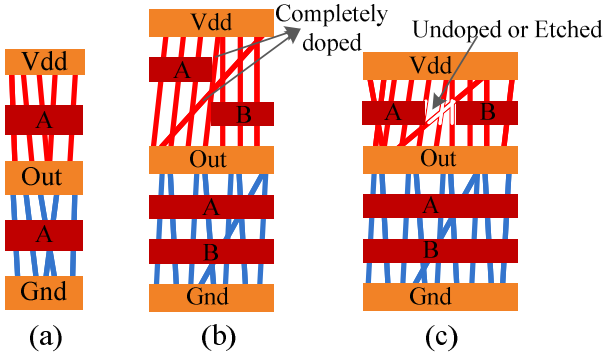


Figure 2 (a) CNFET inverter (b) Misaligned-CNT-vulnerable NAND layout (c) Misaligned-CNT-immune NAND layout.

Figure 2(a) shows an inverter layout when subjected to the mispositioned CNTs. Even though the CNTs are mispositioned the logic functionality of the inverter is not affected. However, for the NAND layout mispositioning of CNTs change its functionality, as shown in the Figure 2(b); hence, Figure 2(b) shows what is called as misaligned-CNT-vulnerable layout [6]. The mispositioned CNTs in Figure 2(b) shorts Vdd to the output (Out) as they are completely doped (p+ doped). During the doping process, gates act as masks thereby resulting intrinsic CNT region under the gate [16]; here, the mispositioning causes few CNTs to be fully doped instead. Patil et al [6] propose layout techniques to handle mispositioned CNTs by using undoped or etched regions. Figure 2(c) illustrates their technique applied to the NAND2, 2-input NAND, cell in Figure 2(b). However, their technique comes at an expense of extra undoped or etched regions. In this work we propose a new compact layout technique which has high area efficiency while abiding to the conventional lithography design rules.

Transistor modeling is one of the basic building blocks of CAD tools for IC design. The popularity of CNFET technology showcased large interest by several researchers to develop fast and accurate electrical models for CNFETs [10, 11, 12, 13, 14, 15]. Among them, one of the interesting modeling works is the one by Jie Deng et al. [14, 15], who presents a complete circuit-compatible CNFET model taking into account a number of essential device non-idealities, such as channel elastic scattering, the doped source/drain region, Schottky barrier (SB) resistance, multiple CNTs per device and other non-idealities. We leverage this study as one of the foundations of our CNFET design kit development.

## III. Mispositioned-Immune CNFET Layouts

In this section we describe our contribution to build CNFET layouts tolerant to mispositioning of CNTs. Though [6] presents a first layout technique addressing the misalignment problem (see Figure 2c), realizing it in an optimal (i.e., compact) way poses additional technical challenges. Indeed, adding undoped or etched regions at the crucial parts of the layout retains the functionality of the cell, but the added undoped region brings in extra cost in terms of area, processing steps (lithography mask) and matured technology featuring vertical gating. One simple way to avoid the extra lithography step is by opting for etched regions instead of undoped regions, as etching the small region fits within the cell boundary etching step [6]. Figure 3(a)

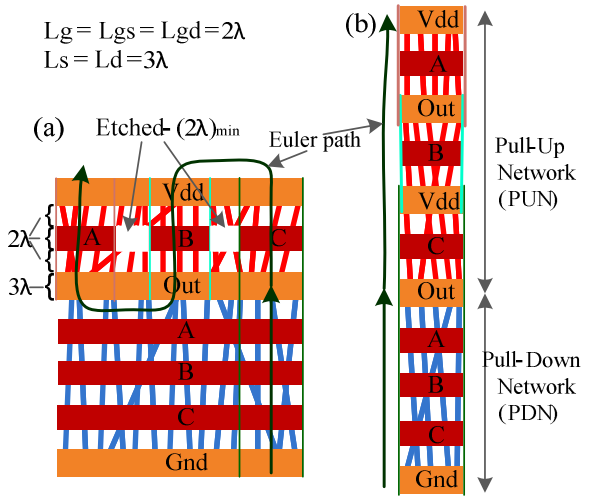


Figure 3 NAND3 cell (a) Misaligned-CNT-immune layout with etched regions (b) New Misaligned-CNT-immune layout

illustrates a misaligned-CNT-immune NAND3 cell, which has 2 etched regions in the PUN between the gates A-B & B-C. The minimum size of the etched region is limited by lithography, i.e. 2λ (65nm) in 65nm technology; thereby widening the PUN by at least 4λ. Moreover intra-cell routing, connecting the gates together in the PUN and the PDN, needs advanced lithography features like vertical gating (*Via* on top of the gate region). For example, in Figure 3(a), the only way to connect gate B in the PUN and PDN is by having a *Via* on top of the gate region in the PUN. However, conventional lithography rules do not allow to have a *Via* on top of an active region (gate region). Assuming vertical gating is possible in the future process, still we need to contemplate on the fact that the size of the *Via* is larger (~3λ) than the gate length (2λ); thereby costing some more area.

Taking into account all the costs involved in the presented layout technique in Figure 3(a), we propose an optimized layout technique illustrated in Figure 3(b). Figure 3(a, b) demonstrates the procedure to map the misaligned-CNT-immune NAND3 layout to the new immune counterpart without using etched regions. The procedure to obtain the new layout, figure 3(b), is by drawing an Euler path [19] from the *Vdd* to the *Gnd* traversing both the PUN and the PDN. The Euler path is drawn considering the metal contacts (*Vdd/ Out/ Gnd*) as nodes and gates (*A/ B/ C*) as edges in a graph. The final layout is obtained by placing the metal contacts and gates with respect to the Euler path. This procedure leads to redundant metal contacts where necessary rather than having an etched region. The only difference in both the layouts, figure 3(a, b), is in the PUN, whereas the PDN are similar. The width of the PDN in both the layouts can be varied so as to achieve similar resistance as their respective PUNs, n-CNFETs are three times bigger than the p-CNFETs for a NAND3 cell. Hence the difference in area between the two layouts can be calculated by considering their respective PUNs. Figure 3, also illustrates the lithography rules in lambda convention. "Lg, Ls and Ld" stand for length of the gate, source and drain respectively. "Lgs and Lgd" stand for the distance between the gate and source/drain. Taking into account the active region of the layout and assuming similar complexity in intra-cell routing, our new layout (Figure 3b) is 16.67% smaller than the layout presented in Figure 3(a) for a p-CNFET width of 4λ. Table 1 presents the difference in area, for different logic gates, of our new layout technique with respect to the technique presented in [6] assuming the same design rules as shown in Figure 3. The difference in area depends on the *fan-in* and the size of the transistor.

| Cell Type | Transistor size in terms of λ | | | |
|---|---|---|---|---|
| | **3λ** | **4λ** | **6λ** | **10λ** |
| Inverter | 0 | 0 | 0 | 0 |
| NAND2 / NOR2 | 17.18% | 14.52% | 11.67% | 9.25% |
| NAND3 / NOR3 | 19.64% | 16.67% | 13.45% | 10.71% |
| AOI22 (OAI22) | 32.2% | 27.7% | 22.5% | 14.9% |
| AOI21 (OAI21) | 44.3% | 40.6% | 36.4% | 32.5% |

Table 1. Area difference between the new and old [6] layout

As a generalized case we present our layout technique for an And-Or-Inv (AOI31) logic as illustrated in Figure 4. The chosen logic function is a simple example explaining the tips for implementing the layout where the logic is expressed in terms of Sums-of-Products (SOP), Products-of-Sums (POS) and combination of both. In fact, the proposed layout technique could be applied to the logic function ***(ABC+D)'*** either by mapping from a misaligned-CNT-immune layout [6] or by choosing an Euler path stretching from *Vdd* to the *Gnd*. A basic layout is presented in Figure 4(a) with a separated PUN and PDN. PDN constitutes to a case of SOP{ABC + D} and PUN constitutes to a case of POS{(A+B+C) × D}. In the case of SOP form, for each product term all the gates are realized in series and terminated by metal contacts at both ends. For example in Figure 4(a), the product term ABC is realized by having all the three gates in series and terminated

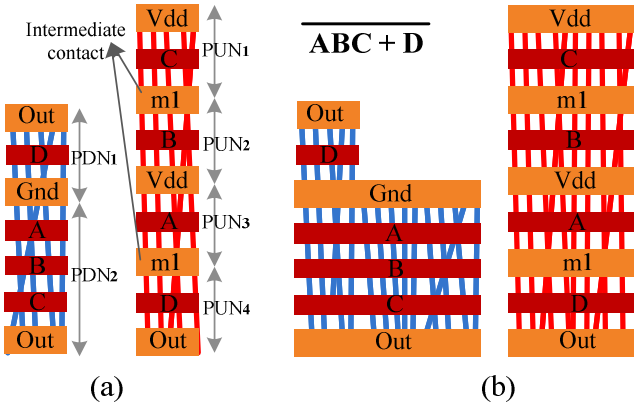


Figure 4 Misaligned-CNT-immune And-Or-Invert (a) Basic layout (b) Symmetric layout

by a metal contact (*Gnd* and *Out*) on either sides. Similarly gate D, being the only product term, is also realized in between *Gnd* and *Out*. In the case of POS form, each sum term can be analyzed in SOP form inherently while the product of sum terms introduces an intermediate metal contact for the product operation. For example sum term A+B+C results in $PUN_1$, $PUN_2$ and $PUN_3$ realized in between *Vdd* and *m1* (intermediate metal contact). Once we have the basic layouts we can vary the width of each of the sub-networks ($PDN_1$, $PDN_2$, $PUN_1$, $PUN_2$, $PUN_3$ and $PUN_4$) to attain symmetric PUN and PDN. Figure 4(b) depicts one of the configurations with a balanced PUN and PDN. $PDN_2$ is three times wider than $PDN_1$, where as all the PUNs are two times wider than $PDN_2$.

The other advantage of the new layout is the simplicity of the intra-cell routing. All the gates in the PUN and the PDN can be connected to their respective ones, even without having the via on top of the active region, which is essential for realizing layouts by abiding to the conventional 65nm node design rules. In the following section we demonstrate the extension of our basic layout to standard cell layout models emphasizing two different layout schemes; thereby leading to slight variations in the intra-cell routing.

## IV. CNFET DESIGN KIT

In this section, a complete CNFET Design Kit (DK) is presented along with the standard cell design aspects of the new layout technique robust to mispositioning of CNTs. Having a standard cell library with the cells immune to imperfections of CNTs, leads to a scenario where we need to incorporate minimal changes to the conventional design flow for realizing CNFET gates in full-wafer scale.

Design kit development makes sense only if the technology node is taken into consideration. In our case, we have chosen industrial 65nm CMOS design platform as a basic starting point from which we customize, strictly binding to the design rules, to achieve CNFET design platform. This design platform provides the necessary support for realizing CNFET circuits in order to be gauged against CMOS circuits at the 65nm common node. Figure 5 presents the CNFET DK comprising all the main blocks which help to realize a logic-to-GDSII flow. Process Design Kit (PDK) defines the process technology and also emulates the environment for CNFET design platform; thereby creating necessary environment in Cadence Virtuso for drawing layouts and eventually developing the CNFET standard library. Post-layout analysis kit allows us to extract the parasitics of the layouts; thereby helping to realize a complete spice simulation with the parasitics. One of the most important parts of the Design Kit is the CNFET hspice electrical model that includes practical device non-idealities [20]. Furthermore, the CNFET model is customized to the technology rules defined by 65nm industrial technology. However, the basic layers of the 65nm technology are altered so as to realize CNFETs. For example, we define a CNT plane over a 10µm SiO2 which is on top of

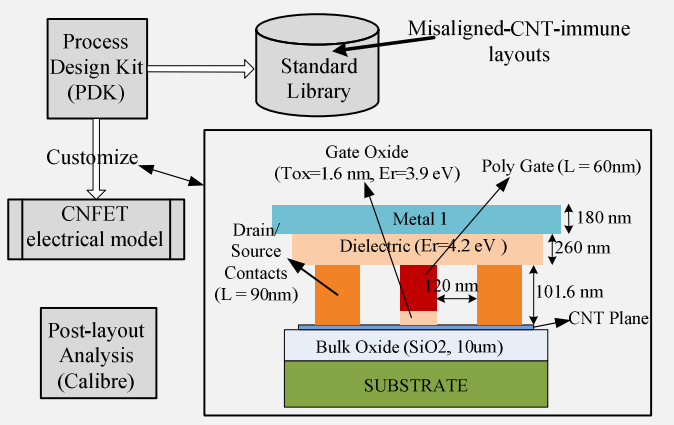


Figure 5 CNFET Design Kit

a substrate. From the CNT plane to the top metal layer all the technology rules are maintained, hence reusing the layers from Polysilicon to Metal7 for routing. The customize pointer in Figure 5 gives a deeper glimpse of the technological parameters till the level of metal 1, whose information is needed to build a CNFET electrical model. Though most of the CNFET realized upto-to-date use metal gates and high-K dielectric [22, 2, 4], we tried to customize CNFET electrical model to Polysilicon gating and low-K dielectric, so that we can make a good study when compared to CMOS at 65nm. Our assumption of realizing CNFETs with poly-silicon gating and low-k dielectric is validated by our technology partners. The DK also includes the standard cell library where the cells are designed using our new layout technique.

### A. CNFET Standard Library

The new layout technique is adapted to the conventional way of building standard libraries, eventually integrating them into the logic-to-GDSII design flow. Figure 6 illustrates the two possible schemes of a NAND cell, with their corresponding Virtuoso snapshots, that can be derived from the basic layout. Scheme 1 is similar to CMOS layouts, having the PUN on top of the PDN separated by spacing for intra-cell routing. Then, the Scheme 2 shown in Figure 6 is completely novel and target the particular compact features of CNFET-based standard cell designs, as we have the PUN and the PDN next to each other. All the cells in the library are designed with reference to the smallest inverter (INV1X) realizable by the chosen 65nm technology node. Transistor sizing for each logic gate is determined by loading a certain number of INV1X corresponding to the driving strength of the gates.

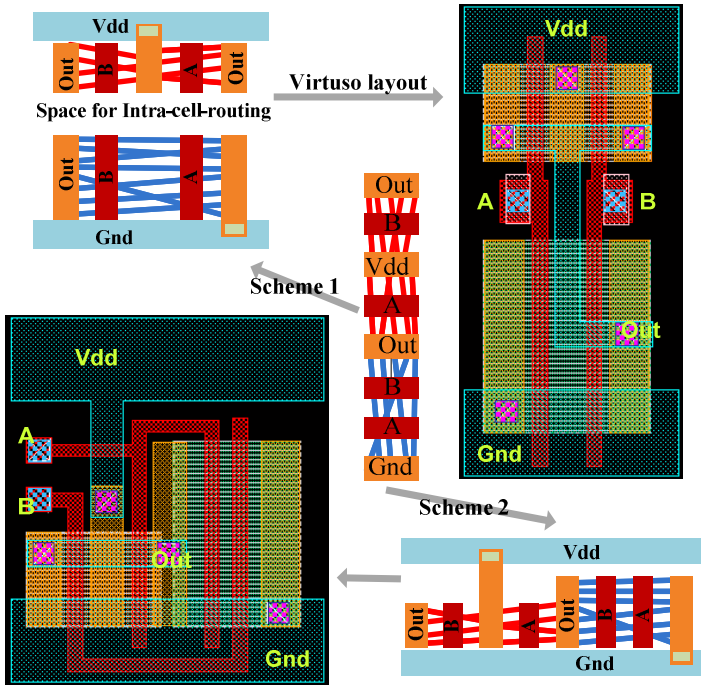


Figure 6 CNFET Standard cell design using Scheme 1 and 2

*Important features of both Scheme 1 and Scheme 2*

1. Scheme 1 is similar to CMOS layouts, hence libraries comprising of this scheme could be easily integrated into the conventional design flow for realizing logic-to-GDSII. The distance between PUN and PDN is limited by the size of the input pins *A or B*, which is greater than the lithography limit 2λ, where as in CMOS the separation is defined by lithography as a minimum distance between the n-diffusion and p-diffusion (10λ at 65nm node).
2. Scheme 2 gives the flexibility of placing the PUN next to PDN, thereby shrinking the height of the standard cell. This

advantage could be contemplated when looking at the area utilization of a synthesized layout while using many logic gates of minimum-to-medium sizes. The input-output pins can be located either to the top or the bottom of the PUN-PDN pair. This flexibility in choosing the pin location can be used by the CAD tools for reducing the routing complexity while placing the layouts. Combined with this feature, compact layouts can be realized by using cells that are not normalized to the standard cell height. A detailed explanation is presented in the next section.

## V. Experimental Results

So far this paper has discussed the main pragmatic issues of realizing a complete CAD tool for CNFETs, which builds up a perfect stage for comparing CMOS and CNFET technology at 65nm node. The circuit simulations in this paper employ industrial 65nm design library for CMOS and CNFET HSPICE model that includes practical device non-idealities [20]. In this section Case-study 1 presents a technology comparison of CNFET with CMOS by analyzing a simple inverter chain and finding the optimum number of CNTs for 65nm technology node. Then, in case-study 2, we look at the performance gains by realizing a simple full-adder and thereby emphasizing the future challenges in CAD for CNFET technology.

### *A. Case study 1*

A five stage FO4 inverter chain is considered as the basic simulation setup, where the 3rd stage inverter is analyzed for comparing both the CNFET and CMOS technology at 65nm. A 1V power supply is used for both inverter chains. Figure 7 illustrates the FO4 delay gains of CNFET inverter over the CMOS one, with respect to the number of CNTs per inverter. The gate width is kept constant while increasing the number of CNTs. The CNFET inverter with a single CNT per transistor is ~2.75× faster and has ~6.3× lower switching energy/cycle compared to an equivalent CMOS inverter. In reality, the higher the number of CNTs, the higher the drive current is; thereby leading to an improvement in FO4 delay, as depicted in Figure 7. However, increasing the CNTs for a fixed transistor width leads to reduced gate-to-CNT capacitance as a result of increased inter-CNT screening effect; thereby worsening the delay. Hence, there exists an optimal CNT-pitch, inter-CNT distance, where we can achieve the best delay gains. At an optimal pitch of 5nm we observe an FO4 delay improvement of 4.2x and 2x lower switching energy/cycle. Further, we define optimal range of CNT pitch from 4.5nm - 5.5nm, leading to 1% FO4 delay variation, considering the pitch variations during the CNT growth process. However, Jie Deng et al [21] reports a 4nm optimal pitch for 32nm technology. Prime reason for this difference is the chosen technology. In our case, the process technology uses low-k dielectric and polysilicon gates. Hence, this leads to the conclusion that the optimal pitch is a technology parameter, which has to be first determined for a given process technology and then handed to the chemists for growing the CNTs on the substrate. In order to quantify area gains let us take into account transistor sizes of CNFET inverter "nCNFET = pCNFET" (due to similar electrical characteristics) and the separation between the PUN and PDN "Dis_PDN_PUN = 6λ" (limited by lithography, 2λ, or the input pin size, 6λ) with respect to the corresponding CMOS inverter (pMOS =1.4*nMOS; Dis_PDN_PUN = 10λ) at 65nm node. We can notice area gain of 1.4X for a 4λ width of an n-FET. However, for bigger transistor widths the area gain declines as the distance between the PUN and the PDN is fixed.

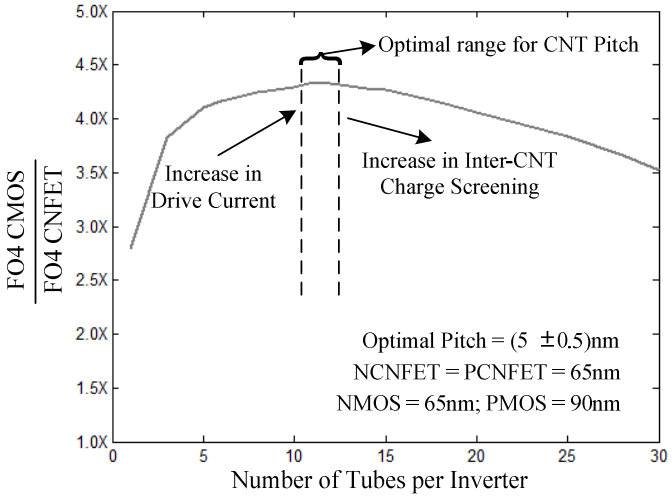


Figure 7 FO4 delay gains as a function of number of CNTs

### *B. Case study 2: Design of a Full Adder using the optimal CNFET cells*

Having analyzed CNFET delay and power gains over corresponding CMOS, and building upon this, we present a case study emphasizing the area optimization for standard cell design approach. The area gains of ~1.4× mentioned in the case study 1 are measured taking into account customized layouts, however when standardizing the layouts to our two layout schemes (section 4) we come across interesting results. A simple full adder (Figure 8a), built using NAND2 and Inverter with varying driving strengths, is employed for studying the area optimization. All the gates are sized at their optimal EDP point. The average delay and energy/cycle improvement for CNFET over CMOS full adder is ~3.5× and ~1.5× respectively. Figure 8(b, c) illustrates the standard cell placement of CNFET gates employing scheme-1 and scheme-

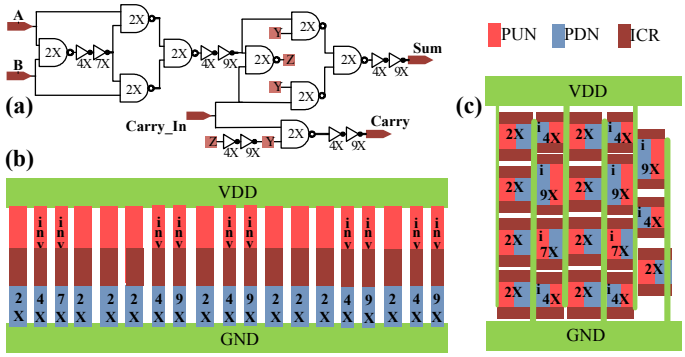


Figure 8(a) Full adder composed of Nand2 and Inverter. Full adder layout (b) using scheme 1 and (c) using scheme 2.

-2 respectively. Figure 8(b) is similar to a CMOS cells and could be easily handled by the conventional place and route tools. However the area-utilization of these layouts depends on the maximum cell height, minimum cell height before standardization and the number of undersized cells used. As an intuitive example we can see from the figure that Inv4X and Inv9X occupy the same height, due to standardization. For CMOS layouts this area-utilization is never optimized as the optimization is done for having one p-well in the PUN thereby saving costs in lithography. Since CNFET technology does not have this constraint the area utilization factor should be taken into account for place and route of the cells. Figure 8(c) is a standard cell layout using Scheme 2, built using the original sizes of each cell thereby having an optimum area utilization factor. Employing Scheme 1, Figure 8(b), we achieve an area gain of ~1.4× where as employing Scheme 2, Figure 8(c), we obtain ~1.6× area gain over CMOS standard cell. Figure 9 illustrates a virtuoso snapshot of the Figure 8(c). Since conventional design tools cannot handle such layouts all the cells are manually connected. However, building such layouts for complex logic needs new placement tools taking into account IR drops and routing complexity. Moreover, a combination of scheme-1 and scheme-2 would lead to optimized layouts with efficient routing.

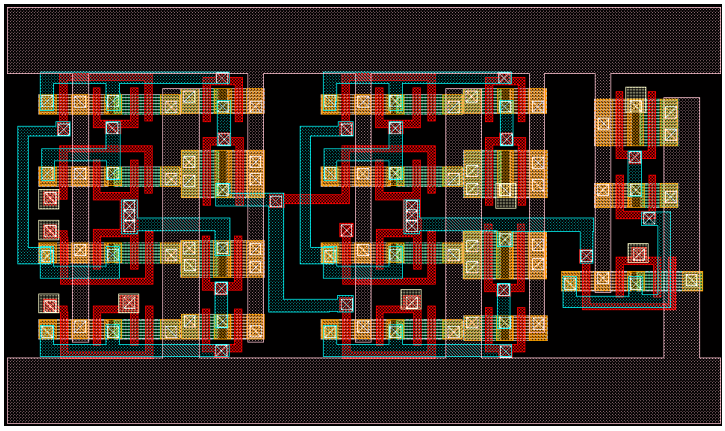

Figure 9 Full adder scheme 2 virtuoso layout.

## VI. Conclusions

In this paper, we have presented a new compact misaligned-CNT immune layout technique for realizing reliable CNFET circuits and we have validated them by developing a Design Kit compatible with the 65nm technology rules. Our new CNFET-based layouts can achieve significant area reductions and Energy-Delay Product (EDP) with respect to circuits implementing the same functionality in CMOS-based 65nm technology. Indeed, our simulations have shown that CNFET inverters can achieve more than 10× EDP improvement over the corresponding CMOS ones. Furthermore, we have postulated two variations of these layouts for a standard-cell design approach. In addition, we have defined the area optimization problem in the context of the flexibility offered by CNFET layouts, and applying our compact layout techniques for the assumed CNFET-based technology, a simple full-adder can achieve significant area savings (more than 30% and 50% for scheme 1 and scheme 2, respectively) with respect to CMOS-based 65nm technology. Our future research work will cover the development of a specific placement tool to handle both layout schemes for achieving layouts with high area utilization factor and efficient routing.

## VII. Acknowledgments

The authors would like to thank Prof. Subhasish Mitra, Stanford University, for his technical advice and useful feedback in the definition and feasibility of the misalignment-immune CNFET layouts presented in this paper. This work is partially supported by the GALAXY Project funded by the European Community's 7th Framework Programme, Contract FP7-ICT-214364.

## VIII. References

[1] Semiconductor Industry Association, Int. Technology Roadmap for Semiconductors (ITRS), 2006, http://public.itrs.net.

[2] H.-S.P Wong., *et al.*, "Carbon nanotube field effect transistors - fabrication, device physics, and circuit implications", ISSCC. 2003

[3] Yu-Ming Lin., *et al*, "High-performance carbon nanotube field-effect transistor with tunable polarities", IEEE Transactions on Nanotechnology, Sept. 2005.

[4] Raychowdhury A., *et al.* "Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits; DC Analysis and Modeling Toward Optimum Transistor Structure", *IEEE Trans. on Electron Devices,* 2006

[5] Javey A., *et al.*, "Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-K Gate Dielectrics," In Nano Letters, vol. 4, pp. 447-450, 2004.

[6] N. Patil, *et al.* "Automated Design of Misaligned-Carbon-Nanotube-Immune Circuits," In Proc. of DAC, 2007.

[7] Li Y., *et al*., "Preferential Growth of Semiconducting Single- Walled Carbon Nanotubes by a Plasma Enhanced CVD Method," In Nano Letters, vol. 4, pp. 317, 2004.

[8] Collins P. G., *et al.*, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," Science, 2001.

[9] Jie Zhang, Nishant Patil, Subhasish Mitra. "Design Guidelines for Metallic-Carbon-Nanotube-Tolerant Digital logic Circuits". Proc. Design Automation and Test in Europe, March, 2008.

[10] K. Natori, *et al*., "Characteristics of a Carbon Nanotube Field-Effect Transistor Analyzed as a Ballistic Nanowire Field-Effect Transistor," Journal of Applied Physics, 2005.

[11] J. Guo, *et al*., "Performance Projections for Ballistic Carbon Nanotube Field-Effect Transistors," *Physics Letters*, 2002.

[12] A. Raychowdhury, *et al.* "A Circuit-Compatible Model of Ballistic Carbon Nanotube Field-Effect Transistors," *IEEE Trans. on CAD of Integrated circuits and Systems* , 2004.

[13] C. Dwyer, *et al*., "Semi-empirical SPICE models for carbon nanotube FET logic", IEEE Conf. on Nanotechnology, 2004.

[14] J. Deng and H.-S. P. Wong "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part I: Model of the intrinsic channel region," *IEEE Trans. Electron Devices*, Dec. 2007.

[15] J. Deng and H.-S. P. Wong "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part II: Full device model and performance benchmarking," *IEEE Trans. Electron Devices*, Dec. 2007.

[16] Chen, J., *et al*., "Air-stable chemical doping of carbon nanotube transistors [CNFETs] *Device Research Conference*, June 2004.

[17] Zhang G., et al., "Selective Etching of Metallic Carbon Nanotubes by Gas-Phase Reaction", Science, November 2006.

[18] http://domino.watson.ibm.com/comm/pr.nsf/pages/news.20020520_nanotubes.html

[19] Jan M. Rabaey, "Digital Integrated Circuits: A Design Perspective", Prentice Hall, ISBN 0-13-178609-1.

[20] http://nano.stanford.edu/model.php?id=23

[21] Jie Deng., et al., "Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections", In Proc. of IEEE ISSCC, 2007.