Complete Nanowire Crossbar Framework Optimized for the Multi-Spacer Patterning Technique

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ABSTRACT

Nanowire crossbar circuits are an emerging architectural paradigm that promises a higher integration density and an improved fault-tolerance due to its reconfigurability. In this paper, we propose for the first time the utilization of the multi-spacer patterning technique to fabricate nanowire crossbars with a high cross-point density up to 10^{10} cm^{-2}. We propose a novel decoder fabrication method that can be included in a process dedicated to the multi-spacer patterning technique. We address the technology problems consisting in the variability and fabrication complexity at the design level by optimizing the encoding scheme. We show an overall reduction of the variability by 18% and a cancelation of the fabrication complexity overhead.

Categories and Subject Descriptors

C.5.4 [**Computer System Implementation**]: VLSI Systems; B.8.1 [**Performance and Reliability**]: Reliability, Testing, and Fault-Tolerance

General Terms

Experimentation, Design

Keywords

Emerging Technologies, Crossbars, Nanowires, Spacer Technique, MSPT, Decoder, Gray Code

1. INTRODUCTION

Silicon nanowires (SiNW) are expected to enhance the performance of *metal-oxide-semiconductor field effect transistors (MOS FETs)* and to increase the integration density of very large scale systems. There are different fabrication techniques of SiNWs, which can be divided into *bottom-up* and *top-down* approaches. Bottom-up techniques are based on the growth of NWs from a catalyst, while top-down techniques use any type of patterning, including photolithography.

Silicon nanowires offer the opportunity of implementing a different circuit architecture from conventional *complementary metal-oxide-semiconductor (CMOS)* circuits. This novel paradigm, the *crossbar architecture*, is based on the arrangement of arrays of parallel nanowires perpendicular to each other in a crossbar fashion. Such circuits can perform logic or store information at the cross-points [15, 16]. It is expected that crossbars will be defined within CMOS circuits [6]. A link between the CMOS and the crossbar parts is therefore a fundamental element of the crossbar circuit. This function is implemented by the decoder, which insure a unique addressing of every nanowire in the crossbar by the CMOS part.

Previous approaches have been focusing separately on these two parts of the crossbar circuit: the crossbar including the cross-points, and the decoder performing the link between the cross-points and the CMOS part. When it comes to the crossbar, different fabrication techniques have been suggested; and the most successful one is based on the nanomold imprint lithography [15]. This technique consists in transferring a pattern of parallel nanowires onto a different substrate. The technique is fast, however its alignment to previous process steps is difficult, and it produces mostly metallic instead of silicon nanowires. However, silicon nanowires are preferable because they can be used as *silicon nanowire field effect transistors (SiNW FETs)*. On the other hand, the decoder fabrication and design approaches proposed sofar highly depend on the underlying nanowire technology [7, 12, 1, 9], and some of them have a large area overhead in order to insure a reliable addressing of the nanowires.

In this work, we consider both parts of the circuit. We utilize the spacer technique [5] in order to fabricate large layers of parallel nanowires, and we demonstrate for the first time the ability of this technique to yield arrays of crossing nanowires in a crossbar fashion. We also introduce a novel fabrication concept of the decoder part in the considered technology, and we show a methodology that yields the optimum decoder design.

This paper is organized as follows. Following the introduction, Section 2 surveys the different nanowire fabrication technologies and focuses on the spacer techniques. Section 3 introduces the crossbar architecture and systems based on

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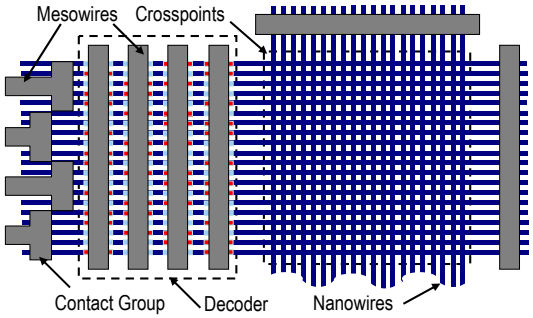

Figure 1: Baseline architecture of a crossbar circuit

it. Section 4 explains the multi-spacer patterning technique utilized in this work in order to fabricate the nanowires and it demonstrates the obtained results. Section 5 introduces a novel decoder fabrication concept for the considered technology. Section 6 presents the problem of designing the decoder and gives the optimal solution. Section 7 discusses the challenges of the presented technology. Finally, the paper is concluded with Section 8.

2. NANOWIRE TECHNOLOGIES

Nanowire fabrication techniques can be divided into bottom-up and top-down approaches. Bottom-up techniques are those where nanowires are grown on a silicon substrate from catalyst seeds. Then, they are collected in a solution and dispersed on top of the substrate on which the operational circuit will be defined [14]. In top-down approaches, nanowires are directly defined on the functional substrate by accurately controlling the deposition, oxidation and etching rates [11, 4], or by using nanometer-scale molds whose pattern can be transferred onto another substrate using the nanomold imprint lithography [15]. Nanowires can be either differentiated or undifferentiated. Differentiated nanowires have different doping profiles, and they are fabricated with bottom-up techniques. Undifferentiated nanowires have the same doping level (or they are undoped), and they are generally fabricated with top-down techniques.

The spacer technique has been suggested as a possible top-down fabrication technique that yields parallel nanowires by using only CMOS processing steps. This technique allows for the control of the device dimensions below the photolithographic limit [5] and yields sub-lithographic nanowires. The approach is based on the definition of a spacer by conformally depositing a material at the edge of a sacrificial layer and then anisotropically etching it. The thickness of the deposited material defines the width of the spacer. This thickness can be controlled accurately without any dependence on the photolithographic limit. By removing the sacrificial layer, the spacer can be used as a hard mask to define structures in the underlying layers.

The spacer patterning technique is an attractive alternative way to fabricate nanowires with very thin dimensions, since it is maskless and self-aligned. It can be iterated several times, resulting in the *multi-spacer patterning technique (MSPT)*. The iterative approach follows two roads: the *multiplicative* and the *additive* road [4]. With the multiplicative approach, every spacer can be used as a sacrificial layer for the following one, thus, reducing the lithographic pitch by a factor of 2^n, with n the number of iterations. With the additive road, successive spacers are defined by alternating semiconducting (poly-Si) and insulting materials (SiO_2) defined on the edge of the same sacrificial layer.

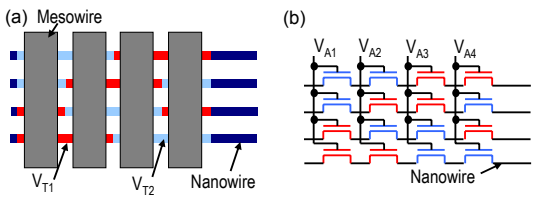

Figure 2: Baseline architecture of a crossbar decoder: (a) Decoder layout. (b) Decoder circuit.

In this work, we demonstrate the ability of the multi-spacer patterning technique to yield crossing arrays of parallel nanowires and we introduce a novel concept of a compact decoder especially optimized for the MSPT-based nanowires, which can be designed in an optimal way so that the fabrication complexity and the overall variability are minimized. In order to present the results at the fabrication and design levels, the crossbar circuit architecture is first introduced in the following section.

3. CROSSBAR CIRCUITS

In this section, we introduce the overall organization of crossbar circuits. Then, we survey some of the most relevant circuit architectures based on nanowire crossbars. Then, we focus on the nanowire decoder design.

3.1 Organization of a Crossbar

The baseline organization of a nanowire crossbar circuit is depicted in Fig. 1. The crossing of two orthogonal layers of parallel nanowires defines a regular grid of cross-points. The spacing between the crossing nanowires can be filled with phase-change materials or molecular switches. The cross-points can then perform information storage, interconnection or computation [6]. A set of contact groups is defined on top of the nanowires through an ohmic contact. The role of a contact group is to make a full nanowire bundle addressable by the outer lithographic wires, or *mesowires*. Given the difference in pitch between nano- and mesowires, a mesowires can only match the size of a contact group, but not the size of a single nanowire.

Every set of nanowires within a contact group is connected to the outer CMOS circuit through a set of mesowires. A decoder is utilized in order to make every nanowire within this set uniquely addressable by the outer circuit. It is formed by a series of transistors along the nanowire body, controlled by the mesowires and having different threshold voltages (V_T's) [2], as shown in Fig. 2(a) and 2(b). Depending on the distributions of threshold voltages of the series transistors along the nanowires and on the sequence of applied voltages in the decoder (V_A's), one single nanowire in the array can be made conductive, which is required for a correct addressing operation.

3.2 Crossbar-Based Architectures

Several crossbar prototypes were fabricated with different sizes [15], and the basic function that those prototypes implemented is information storage. Crossbars implementing computational units are also possible. For instance, the

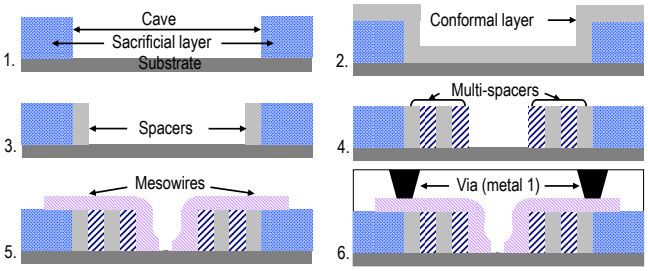

Figure 3: Main process steps: (1) Definition of sacrificial layers (2) Conformal deposition of poly-Si. (3) RIE etch. (4) Alternation of poly-Si/SiO_2 spacers. (5) Definition of the gate stack. (6) Passivation and metallization.

nanoPLA [6, 8] architecture is a concept based on semiconducting *silicon nanowires (SiNWs)* organized in a crossbar fashion with molecular switches at their cross-points. The switches can be programmed in order to perform either signal routing or wired-OR logic function. The output of the crossbar is routed to a second crossbar, in which the signals can be inverted by gating the nanowires carrying the signals. A cascade of these two planes is equivalent to a NOR plane. Two back-to-back NOR planes are universal gates, and they can implement the traditional AND-OR PLA by applying DeMorgan's theorem.

On the other hand, the CMOL [6] approach combines CMOS with molecular and one-dimensional devices. The basic idea is to define a grid of CMOS lines that are terminated by pointed metallic pins with two different heights. Then, a nanowire crossbar is defined after the back-end steps of the CMOS processing. By a sequence of etching and planarization, the two layers of nanowires can be contacted by the CMOS pins depending on their height. In order to insure the alignment between the nanowires and the CMOS lines defined at two different scales, the crossbar is tilted by a certain angle with respect to the CMOS grid; thus making every nanowire connected by two pins.

3.3 Nanowire Decoders

Differentiated nanowires have an axial or a radial doping profile which is defined during the nanowire growth process. An axial decoder has been presented in [7], in which the distribution of the threshold voltages along the decoder part of the nanowire is fully random. The nanowires are dispersed parallel to each other and they are uniquely addressable when they have different threshold voltage patterns. The probability that their addresses are different may be increased by increasing the number of addressing wires. In a similar way, the radial decoder [12] relies on nanowires with several radial doping shells.

A mask-based decoder has been presented in [1] and its ability to control undifferentiated nanowires has been demonstrated. The mesowires are separated from the nanowires by a non-uniform oxide layer, using both high- and low-κ. The high-κ dielectric amplifies the electric field generated by the mesowires relatively to the low-κ dielectric. Consequently, the field effect control by the mesowires happens only at the NW regions lying under the high-κ dielectric.

Undifferentiated nanowires were encoded within other approaches that are not mask-based. For instance, a random contact decoder has been presented in [10, 9], where the fully random connections between mesowires and nanowires through randomly deposited impurities define the patterns of the nanowires.

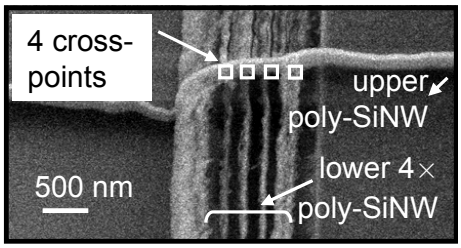

Figure 4: SEM images of a small 4×1 crossbar with 1 upper and 4 lower poly-Si spacers.

4. CROSSBAR FABRICATION WITH THE SPACER TECHNIQUE

The main idea of the process is the iterative definition of thin spacers with alternating semiconducting and insulating materials, which result in semiconducting and insulating nanowires (Fig. 3). First, we define a SiO_2 sacrificial layer (step 1) on a Si substrate. Then, we deposit a thin conformal layer of poly-Si (step 2). Subsequently, we etch this layer with a *reactive ion etching (RIE)*. This step removes the horizontal layer and keeps the sidewall as a spacer (step 3). Then, we deposit a conformal insulating layer of *low temperature oxide (LTO)*. The deposited LTO is etched in a RIE etchant in order to remove the horizontal layer and just keep the vertical spacer. We perform these two operations (poly-Si and LTO spacer definition) several times in order to obtain a multi-spacer of alternating poly-Si and SiO_2 nanowires (step 4). The fabrication of a crossbar framework necessitates the definition of two perpendicular layers identical to the previously explained multi-spacer, separated by a thin insulator. These steps are not shown in Fig. 3. In order to characterize a single access device operating as s *poly-crystalline SiNW FET (poly-SiNW FET)*, one single layer is defined. Then, we define a gate stack with different gate lengths (step 5). The drain and source regions of the undoped poly-SiNW are defined by the evaporation of Cr and $Ni_{0.8}Cr_{0.2}$ (step 6).

We first assessed the structural properties of arrays of parallel nanowires fabricated with the proposed technique. The nanowires are parallel and have a length of hundreds of micrometers. Their yield is close to 1, in the sense that there is not interruption along their axis. The number of nanowires in a multi-spacers could be set to more than 10, and it is possible to increase it further. The width of the nanowires is given by the thickness of the deposited materials, and could be set down to $\sim$ 20 nm. The possible use of the MSPT for the fabrication of two perpendicular layers of crossing NWs is illustrated in Figure 4 with one poly-SiNW crossing 4 poly-SiNWs underneath it. The first nanowire to the right is wider than the three others because it was defined with a thicker deposited poly-Si layer. The cross-point density in this small array is about 10^{10} cm^{-2}.

The access to the nanowires in order to control the current flow through them requires the definition of access transis-

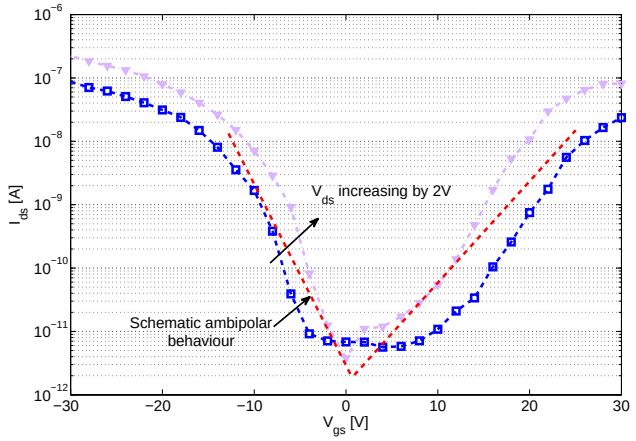

Figure 5: I_{ds}-V_{gs} curve of an undoped single poly-SiNW with a back-gate and nickel silicide drain/sourse ($L = 20$ μm, $W = 67$ nm).

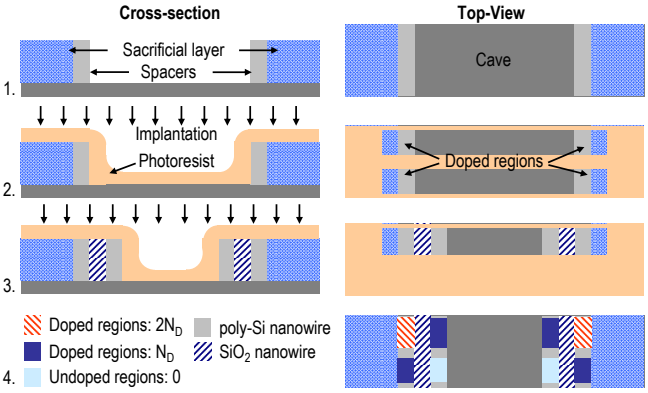

Figure 6: Decoder-aware enhanced fabrication flow: Definition of first poly-Si nanowire (1), photolithography and doping of first poly-Si nanowire (2), photolithography and doping of second poly-Si nanowire (3), final doping patterns (4).

tors having a poly-Si spacer as a channel. We characterized undoped poly-SiNW FETs (single poly-Si spacer) with $Ni_{0.8}Cr_{0.2}$ drain and source contacts and with a back gate length $L = 20$ μm and a gate width $L = 67$ nm. The I_{ds}-V_{gs} curves show an ambipolar behavior, with a current conductance under either high positive or negative gate voltage (Figure 5). Such an ambipolar behavior of undoped SiNW FETs with nickel silicide contacts has already been reported and explained in literature [13].

The ability to control the devices in a FET fashion proves their possible use as access devices to the NW layer. The access transistors are the fundamental elements of the decoder, whose fabrication concept with the MSPT is presented in the next section.

5. NANOWIRE DECODER WITH THE SPACER TECHNIQUE

It is easy to define a pattern on the nanowire during its growth process in bottom-up approaches; however, it is more difficult to define it with top-down approaches. As a matter of fact, the MSPT yields a regular array of undifferentiated nanowires if the bare procedure depicted in Fig. 3 is applied. Once the array is defined on a sub-lithographic scale, it is difficult to pattern it with standard photolithographic means, unless expensive high-resolution and time-costly methods, such as electron-beam lithography, are applied. Consequently, it is desirable to pattern the nanowires while they are defined: *i.e.*, whenever a new spacer is defined, it has to be patterned before the next spacer is defined.

The fabrication flow that includes the decoder is illustrated in Fig. 6 and it represents an extension inserted between steps 3 and 4 in Fig. 3. Other steps remain unchanged. The additional steps are lithography patterning and doping after every spacer definition step, using p-type (n-type) doping to increase (decrease) the total doping level. Specific regions from every poly-Si nanowire are defined and doped in this way. Nanowires are fragile and thin structures, and they should be doped carefully with light doses. The total doping level of a specific region is the sum of all (positive and negative) doping levels accumulated in this region throughout the definition of the whole array, as illustrated in step 4 of Fig. 6. An optimized choice of the lithography/doping sequences and the doping doses may result in the desired nanowire pattern.

This decoder fabrication concepts resolves the issue of differentiating top-down nanowires by doping them during the fabrication procedure. However, it raises several questions. First, this differentiation technique does not insure that every nanowire has a unique doping profile that makes it uniquely addressable. Second, the doping profiles are obtained through cumulation of different doping doses instead of single doping operations, which results in a higher variability, given the fact that every doping operation contributes to the overall variability of the doped regions. Finally, every photolithography and doping step increases the fabrication complexity and cost. Thus, this approach may result in a large overhead in terms of fabrication cost. In order to answer these three questions, the technology problem is addressed at the design level, by looking at the problem of searching the encoding scheme that *i*) insures the unique addressability of every nanowire, *ii*) reduces the overall variability and *iii*) minimizes the fabrication complexity. This problem is addressed in the following section.

6. ADDRESSING CROSS-POINTS

The decoder fabrication technique introduced in the previous section yields a decoder operation identical to the description in Sec. 3.3. However, the layout differs in the fact that the nanowires lie within parallel caves having a symmetry axis going through their central axis (Fig. 3 and 6). The unique addressing of every nanowire in a half cave insures the unique addressing of every nanowire in the whole array. We will therefore consider only half caves in the rest of the paper.

Every half cave contains N nanowires having M doping regions each. The pattern is the sequence of threshold voltages and the doping profile is the sequence of dopant concentrations along the doping regions of the nanowire. Let $\mathbf{P}_i = \left[P_i^0 \dots P_i^{M-1}\right]$ and $\mathbf{D}_i = \left[D_i^0 \dots D_i^{M-1}\right]$ be the pattern and doping profile of the nanowire i respectively. For the considered technique, whenever a nanowire i is patterned

by receiving a doping dose, all nanowires $k = 0, \ldots, i-1$ receive the same doping dose simultaneously. Consequently, the doping profile of a nanowire i depends not only on its own doping dose but also on all doping doses received by the nanowires $k = i+1, \ldots, M-1$. We therefore need to determine the analytical multivariable application that links P_i^j and D_i^j for $i = 0, \ldots, N-1$ and $j = 0, \ldots, M-1$, in order to specify whether we can find a set of doping profiles that results in a given set of patterns.

Assuming that a set of doping profiles exists for any set of patterns, it is possible to optimize the choice of patterns according to different cost functions. We consider first the impact of this decoding technique on the fabrication cost. The nanowire profile implies a certain number of lithography/doping steps per nanowire, ϕ_i for $i = 0, \ldots, N-1$. From the fabrication point of view, it is of the highest importance to reduce the total number of lithography/doping steps, *i.e.* $\sum \phi_i$. We therefore need to establish the link between P_i^j and ϕ_i in order to minimize $\Phi = \sum \phi_i$.

Then, we consider the impact of this decoding technique on the circuit yield by analyzing the variability of the decoder. Every doping region j of the nanowire i, referred to as region (i, j), receives successive doping doses bit by bit. With every additional doping dose, the variability of region (i, j), quantified as the standard deviation of the threshold voltage of this region Σ_i^j, accordingly increases. It is therefore desirable to establish the link between P_i^j and Σ_i^j and to optimize the choice of the patterns in order to minimize the variability.

In [3] we defined the technology cost functions as Φ (the sum of all ϕ_i) and $\|\Sigma\|_1$ (the 1-norm of Σ, *i.e.*, the the sum of all elements of Σ). Then, we established the following multi-linear link between the technology cost functions and the encoding scheme:

$$\Phi = \sum_{i=0}^{N-2} \tau_i + k_1$$

$$\|\Sigma\|_1 = (\sum_{i=0}^{N-2} (i+1) \cdot \tau_i + k_2) \cdot \sigma_0^2$$

with: τ_i the Hamming distance between code words i and $i+1$, k_1 and k_2 constant numbers that depend on the choice of the first code word in the code space and σ_0^2 is the unit variance of the threshold voltage induced by one single doping step.

It is known that *tree codes (TCs)* can be arranged in such a way that the Hamming distance between every successive code words is minimized. The obtained code is the *Gray code (GC)*. Moreover, the elements of the GC can be arranged in such a way that the number of transitions is balanced between the different digits, resulting in the *balanced Gray code (BGC)*. Similarly, at least a large set of hot codes (HC) can be arranged into the *arranged hot codes (AHCs)* so that the Hamming distance is minimized. The definition and construction rules of these codes are explained in [3].

We calculated the technology complexity Φ for different code and logic types. The results, plotted in Fig. 7 for $N = 10$ show that Φ is constant for all binary codes and equal to the double of the number of nanowires in a half cave. Higher logic level was suggested as a way to reduce the area overhead of the decoder [2]. However, Fig. 7 shows

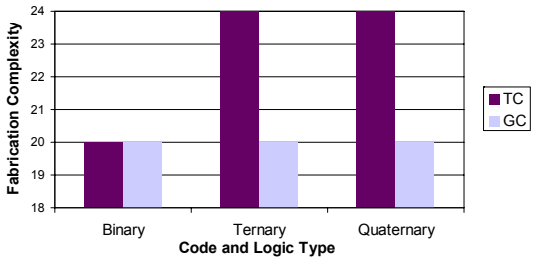

Figure 7: Fabrication complexity in terms of number of additional steps for different code types and logic levels

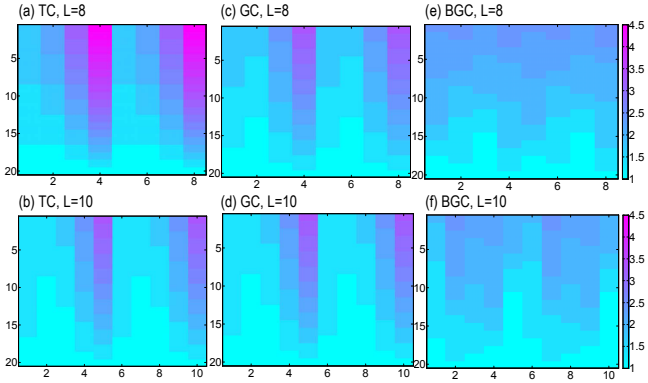

Figure 8: Square root of the elements of the variability matrix Σ (normalized to σ_0) for different binary code types and lengths. The x- and y-axis represent the digit position (1 to 8) and the nanowire number (1 to 20) respectively. The color scale represents the variability.

that the higher logic level comes with some fabrication cost: 20% more steps for the tree code. For ternary and quaternary logic, the Gray code performs better than the tree code (17%) by completely canceling the fabrication complexity overhead.

The variability matrix was calculated for various types of binary codes. N was set to 20 and the plots in Fig. 8 show the variability level at every digit in the $N \times M$-matrix Σ, as square roots of elements of Σ normalized to σ_0. By comparing Fig. 8(a), 8(c) and 8(e), we see that the Gray code and its balanced version reduce the variability level at every digit in comparison to the tree code. The balanced Gray code distributes the variability more evenly than the other codes. In this way, the average variability $\|\Sigma\|_1/(N \cdot M)$ could be reduced by 18%. Similar results were obtained for these codes with a higher logic level, as well as for hot codes and their arranged version. Next, we compared the distribution of the elements of Σ for a fixed code type and different code lengths (Fig. 8(a), 8(c) and 8(e) vs. Fig. 8(b), 8(d) and 8(f)). We noticed that longer codes have less digit transitions and help reduce the average variability.

This decoder design concept resolves at the design level several issues coming from the technology, and represents an interesting way to enhance the crossbar with a compact decoder in order to obtain an autonomous and full crossbar platform. The MSPT however faces some challenges mainly

due to the iterative approach. The questions related to these challenges will be addressed in the next section.

7. DISCUSSIONS

The cost of the additional conformal deposition and RIE etch steps is one of the fundamental questions that challenge the MSPT-based crossbars. Assuming a 8 kB memory, the fabrication time needed for a 256×256 nanowire crossbar would be tremendous if 2×256 deposition/etch operations were required. Fortunately, the MSPT can be parallelized in different ways. On the one hand, within-die parallelization can be achieved by using n parallel sacrificial layers instead of one. Then, the number of deposition/etch steps is divided by n. On the other hand, the technique allows for parallel batch processing, *i.e.*, any two different batches can be processed together during the deposition/etch steps as long as the thickness of the conformal layers is the same.

Within-die parallelization is the simplest solution to speed the MSPT and reduce the fabrication time and cost. The factor n is chosen in such a way that the number of nanowires in every half-cave has a size that can be matched by at least one contact group. The number of nanowires in every cave is in the range $\sim 3 \times L_{\mathrm{l}}/L_{\mathrm{n}}$, with L_{l} the lithography half-pitch and L_{n} the nanowire half-pitch. The factor ~ 3 comes from the symmetry of the caves and the possible need for some overhead in order to bridge the lithographic and sub-lithographic dimensions [2]. For instance, at the 65 nm technology node ($L_{\mathrm{l}} = 2 \times 65$ nm) and with 20 nm wide nanowires ($L_{\mathrm{n}} = 2 \times 20$ nm), n should be chosen such that every cave has ~ 10 parallel nanowires. Given the symmetry of the cave, the number of deposition/etch procedures is only ~ 5 per layer (10 for 2 layers) instead of 256 per layer (512 for 2 layers).

Another important question about the proposed technique is related to the lower mobility of current carriers in the poly-Si used to define the structure, compared to crystalline Si. The problem exists for any nanowire material: the structure length and small cross-section induce a slower signal propagation and a higher resistance. The benefit of crossbars is parallelizing memory and computation in a grid with a large number of small crossbars, rather than using a limited number of large crossbars.

8. CONCLUSIONS

The fabrication of nanowire crossbars is proposed in literature with different approaches, for which specific decoders are required in order to make the nanowire array addressable by the outer CMOS circuit. In this paper, we proposed for the first time the fabrication of nanowire crossbars with the multi-spacer patterning technique. We demonstrated the feasibility of the approach with a small 4×1 crossbar showing a cross-point density of 10^{10} cm^{-2}. The nanowires can be operated as poly-SiNWs in order to address the cross-points through the decoder. We proposed a novel decoder fabrication concept in this technique, and we addressed the problems coming from the technology (variability, fabrication complexity) at the design level by optimizing the encoding scheme.

9. ACKNOWLEDGMENTS

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