

# Crosstalk Delay Analysis using Relative Window Method

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**Abstract --- In this paper, we propose a new method to deal with crosstalk effects in timing analysis. The method can handle the timing between victim and signal arrival times and the dynamic changes due to the input-pattern dependence of the arrival times. Solutions for the crosstalk problems using the method are also presented.**

## I. INTRODUCTION

The growing complexity of LSI systems is strongly encouraging design intellectual property (IP) reuse, and the integration of many components designed under different environments on the same chip will soon be common. At the same time, LSI performance has improved year by year, and operating frequencies of several GHz will be common in the next decade. Thus, verifying the timing constraints for each IP is becoming more important. Among the many hurdles that must be overcome to achieve higher-frequency operation, the problems related to crosstalk are becoming more serious, because the ratio of the lateral capacitance to the whole capacitance is increasing as process technologies advance [1,2]. It has been predicted in [1] that the minimum metal pitch will be reduced to 0.26-0.39  $\mu\text{m}$  in 2003, and the ratio of the lateral capacitance will be more than 70-80%.

Crosstalk causes two major problems: noise and delay degradation [3]. The noise is an especially critical problem in dynamic circuits because there is no way to restore lost node information, thus noise causes function failure. Static circuits also suffer from noise, but are much more robust than dynamic circuits. However, although noise problems are eliminated in static circuits, we still have to deal with delay degradation problems, especially for high-performance LSIs.

Several papers have reported on the potential seriousness of the delay degradation problem [4,5,6]. For example, [4] presented an analytical delay model to consider the crosstalk effects. In this model, the differential equation representing a capacitively coupled line was solved exactly in the frequency domain, and the worst-case delay was approximated using the first-order moment matching method. According to the result, the delay time changes with a factor of 5 or more depending on the signal transition on adjacent wires. The results obtained in past works are useful for obtaining a rough understanding of the problem, but, have several limitations when applied to actual designs

because they were based on restricted conditions.

One of the major limitations is related to the complexity of the signal transition time on adjacent wires. The timing combination between the signal arrival time on a wire (the victim) and that on the adjacent wire (the aggressor) affects the delay time. A widely used method to deal with this problem is to double the coupling capacitance to simulate the worst-case transition condition. When the victim driver and the aggressor driver have the same strength and the signal transitions happen simultaneously (this situation is actually very rare), the doubling method provides a good estimation. However, the doubling method does not provide the worst-case value [5]. Another limitation is that the signal arrival time on each wire changes dynamically depending on the input patterns. This makes the problem more difficult to handle. Until now, these two difficulties have not been addressed together, and there has been no fast calculation method to deal with the problem.

## II. RELATIVE WINDOW METHOD

The change in the delay degradation depends on the combination of the victim signal arrival time (VSAT) and the aggressor signal arrival time (ASAT). Figure 1 shows an example, where an increased delay in the victim signal is simulated for several combinations of VSAT and ASAT. Here, the out-phase-transition was used; if the in-phase-transition is used the delay decreases. From now on, we concentrate on the out-phase-transition, but, the basic idea is also valid for the in-phase-transition.

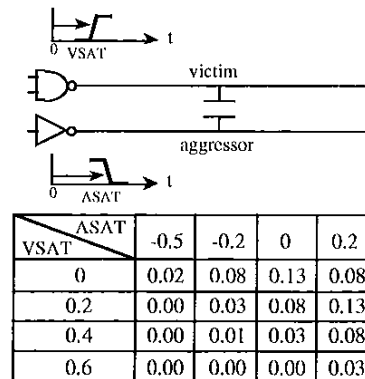


Fig. 1: Increase in delay time depending on the combination of victim and aggressor signal arrival times

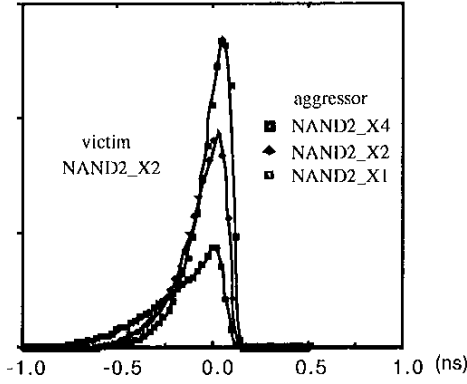


Fig 2: Increase in delay time as a function of the relative signal arrival time (RSAT)

The degradation becomes large when the signal arrival times are the same or close to each other. When we used a process technology of 0.35  $\mu\text{m}$  or older, using the value from the worst-case or the simultaneous transition case was permissible because the degradation was small and did not greatly affect the cycle time. However, as the degradation increases, using the values from those cases becomes too conservative, and the combination of VSAT and ASAT must be considered to estimate the delay degradation precisely.

Though the delay increase was written in a two-dimensional form in Fig. 1, it can be reduced to a one-dimensional form by measuring the ASAT relative to the VSAT to determine the relative signal arrival time (RSAT) of the aggressor. The increase in delay in a circuit with two two-input NAND gates is shown in Fig. 2 as a function of RSAT. Here, the strength of the aggressor driver was set at three levels. The figure illustrates three major points.

- A) The increase in delay time is strongly dependent on the RSAT.
- B) The RSAT that affects the delay time is limited to a specific range.
- C) The delay time is strongly dependent on the driver strength.

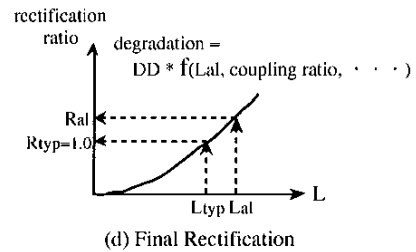
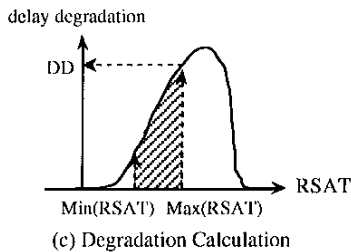
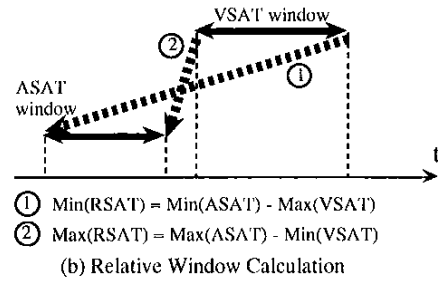
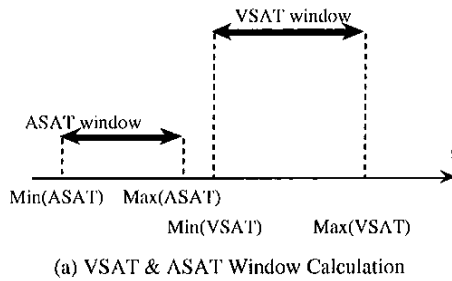


Fig. 3: Relative window method

The first finding shows the inefficiency of using the worst-case delay. The second one shows that even if we have aggressors in the circuit, we can ignore them if their RSATs are outside the relevant range. The third one shows that the driver combination between the victim and the aggressor must be considered in the analysis.

By using the RSAT, we can deal with the delay degradation precisely without depending on the worst-case analysis. However, to use the delay degradation calculated from the RSAT, we have to know the exact signal arrival times for both the victim and the aggressor. Unfortunately, it is practically impossible to deal with all possible combinations of VSAT and ASAT because the signal arrival times change dynamically depending on the input patterns. Thus, we cannot use the RSAT directly to calculate the delay degradation. We can only determine the minimum and the maximum signal arrival times of the victim and the aggressor through a static timing analysis. However, even without knowing the exact RSAT, we can know the minimum and the maximum RSAT (the relative window) from the result of the static analysis. The maximum degradation can be obtained from the relative window through the procedure described below (Fig. 3).

- a) Calculate the signal-arrival-time window for the victim and the aggressor: the victim window is from Min (VSAT) to Max (VSAT) and the aggressor window is from Min (ASAT) to Max (ASAT).
- b) Calculate the minimum and the maximum RSAT using the two windows obtained in a).  
 $\text{Min (RSAT)} = \text{Min (ASAT)} - \text{Max (VSAT)}$   
 $\text{Max (RSAT)} = \text{Max (ASAT)} - \text{Min (VSAT)}$
- c) Calculate the delay degradation by sweeping the range (Fig. 2) between Min (RSAT) and Max (RSAT) and taking the worst value in the range.
- d) Rectify the degradation value by multiplying it with a function of parameters such as the adjacency length and the coupling ratio.

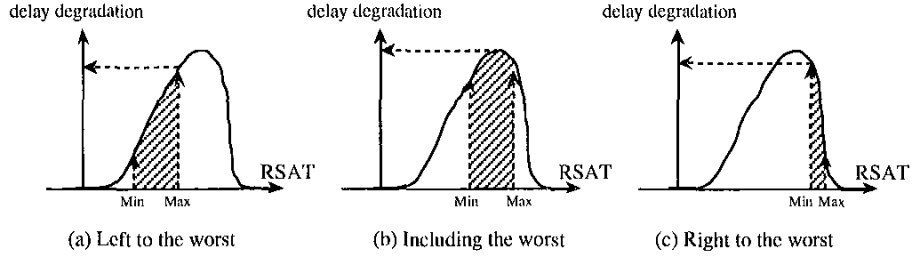


Fig. 4. Relative window categories

Note that we usually don't need to actually sweep the degradation table in step c), and can save the effort if we can know which category the analyzing case falls under (Fig. 4). The possible categories, shown in Fig. 4, are:

- 1) Relative window left of the worst-case RSAT (Fig. 4(a))
- 2) Relative window includes the worst-case RSAT (Fig. 4(b))
- 3) Relative window right of the worst-case RSAT (Fig. 4(c))

It is possible to keep the worst-case RSAT when the table of the delay degradation values as a function of RSAT is prepared. By comparing the Min (RSAT) and the Max (RSAT) with this worst-case RSAT, we can categorize the analyzing case. When the analyzing case falls under category 1) or category 3), we need only pick up the degradation corresponding to, respectively the Max (RSAT) or Min (RSAT). When the analyzing case belongs to category 2), we only need to pick up the worst-case degradation. This is based on only one assumption: that the degradation decreases monotonously as the RSAT decreases on the left side of the worst-case RSAT and as the RSAT increases on the right side of the worst-case RSAT (it is easily observed that this assumption is satisfied in almost all cases).

As mentioned, degradation occurs only when the RSAT is inside a limited range, so the sweeping span can be restricted in the RSAT axis. If Max (RSAT) obtained from step b) is smaller than the lowest value in the range (the minimum critical RSAT), steps c) and d) do not need to be performed and the degradation is immediately calculated as zero. Likewise, if Min (RSAT) obtained from step b) is larger than the highest value in the range (the maximum critical RSAT), we can deal with it similarly. Thus, we can separate two new categories from categories 1) and 3) (Fig.

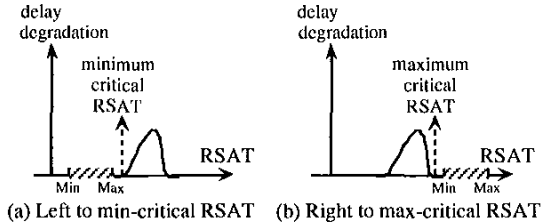


Fig. 5: Additional relative window categories

- 4) Relative window left of the minimum critical RSAT (Fig. 5 (a))
- 5) Relative window right of the maximum critical RSAT (Fig. 5 (b))

### III. APPLICATION TO ACTUAL DESIGN ANALYSIS

Our total analysis flow is shown in Fig. 6.

To apply the relative window method to the analysis of an actual design, a degradation table for each combination of the victim driver and the aggressor driver has to be prepared

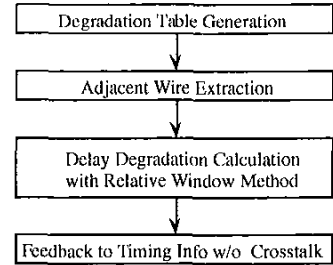


Fig. 6: Total analysis flow

as a crosstalk library. The table is constructed through circuit-level simulations using a capacitively coupled n-stage  $\pi$  circuit with a typical line length (Fig. 7). A table must be prepared for the rising transition case and for the falling transition case. First, the input to the aggressor driver is stabilized and the output delay of the victim receiver is measured. Next, the input to the aggressor driver is stimulated at several time points around the victim stimulus time. The difference between the output delay of the victim receiver is used as the degradation. The RSAT is measured

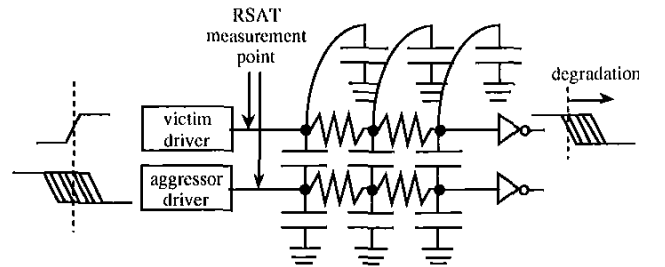


Fig. 7: Degradation-table (crosstalk library) generation

as the difference in the transition start time between the outputs of the victim and the aggressor drivers.

In each design, adjacent wires (victim-aggressor pairs) are extracted from the geometry information generated by the physical design tool. The delay degradation is then calculated by using the relative window method for each wire pair. The calculated degradation is fed back to the timing information that does not reflect the crosstalk effect, and timing information that accounts for the crosstalk effect is thus obtained.

#### IV. EXPERIMENTAL

We applied the relative window method to the analysis of an IDCT circuit generated by a logic synthesis tool and physically designed with an automatic place-and-route tool. The process technology used is summarized in Table 1. Assuming that each block would be implemented with only lower layers, we used three metal layers for all cell-to-cell connections. The degradation was calculated with the worst-case transition method, the simultaneous transition method, and the relative window method. The results are compared in Table 2 for ten critical paths.

When we ignored the crosstalk delay degradation, all of the paths had a smaller delay than the delay constraint(5 ns). However, when we calculated the crosstalk effect with the worst-case transition method, the delay time increased by up to 18% and several of the delays exceeded the constraint. On the other hand, when the relative window method was used, the degradation values were lower than the worst-case values because we could precisely quantify the degradation by considering the combination of the VSAT and ASAT. The ratios of the degradation to the worst case degradation varied from 13% to 97% depending on the path. To determine the cause of this variation, we compared paths #9 and #10. Five major crosstalk pairs are shown in Fig. 8 with their victim window, aggressor window and relative window. In path #9, the relative windows in most crosstalk pairs fully overlapped the crosstalk ranges and included the worst-case RSAT. Therefore, the degradation was almost

the same as the worst-case value. In path #10, the relative windows did not completely overlap the crosstalk ranges in most pairs and did not include the worst-case value, resulting in little delay degradation. Incidentally, when the simultaneous transition method was used, the delay degradation was smaller than the worst-case value, but cannot handle the timing combination as well as the worst-case analysis.

Even though the reductions when using the relative window method compared with the worst-case method were not large in all cases, it implies one important fact. That is, we have not been utilizing the relative window characteristic. If we can ensure that the relative window is outside the crosstalk range, we can avoid delay degradation. Although we cannot always put the relative window completely outside the range in practice, we can reduce the degradation by creating a situation as shown in Fig. 4 (a) or (c). This approach can be used in logic synthesis and also in physical design (Fig. 9). In logic synthesis, we can reduce the possibility of crosstalk occurring by balancing the signal arrival times (Fig. 9 (a)). Even though the wire geometry is still uncertain in logic synthesis phase, reducing the relative window globally will help alleviate the delay degradation. In the physical design, the method can be used more specifically (Fig. 9 (b)). When there are several alternative wire arrangements, the delay degradation can be eliminated by picking up an alternative where the relative window is outside the crosstalk range. These are just a few examples of the potential applications.

#### V. CONCLUSIONS

Relative window method can handle the timing between victim and signal arrival times and the dynamic changes due to the input-pattern dependence of the arrival times. Experimental results showed that a worst-case analysis provides pessimistic results in many cases. Relative window method quantifies crosstalk effects more accurately, and will be useful for logic synthesis and physical design to solve crosstalk problems.

Table 2: Comparison of delay calculation (crosstalk free, worst-case transition, simultaneous transition, and relative window method)

path number	delay w/o xtalk (ns)	delay increase				
		worst-case (%)	simultaneous	ratio to worst	RWM	ratio to worst
#1	4.95	0.638 (12.8)	0.619	0.97	0.445	0.70
#2	4.81	0.299 (6.2)	0.284	0.95	0.274	0.92
#3	4.80	0.499 (10.4)	0.456	0.91	0.399	0.80
#4	4.73	0.496 (10.5)	0.471	0.95	0.424	0.86
#5	4.59	0.818 (17.8)	0.711	0.87	0.716	0.87
#6	4.57	0.713 (15.6)	0.595	0.83	0.478	0.67
#7	4.48	0.170 (3.8)	0.156	0.92	0.113	0.67
#8	4.41	0.165 (3.7)	0.159	0.97	0.112	0.68
#9	4.38	0.296 (6.8)	0.273	0.92	0.286	0.97
#10	4.07	0.029 (0.7)	0.027	0.95	0.004	0.13

## ACKNOWLEDGEMENTS

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Table 1: Process features

Lg	0.15 $\mu\text{m}$
Vdd	1.2V
# of metal layers (lower only)	3
Metal pitch	0.4 $\mu\text{m}$
Rwire	300 ohm/mm
Cvertical	0.06 pf/mm
Clateral / Cvertical	4

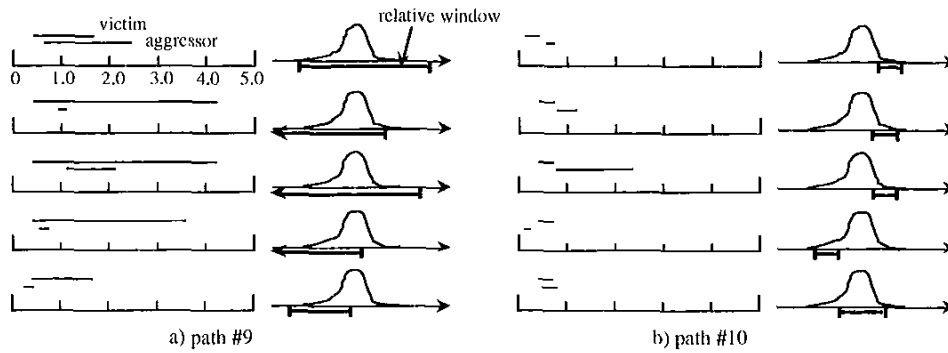


Fig. 8: Relative window variation depending on the critical path

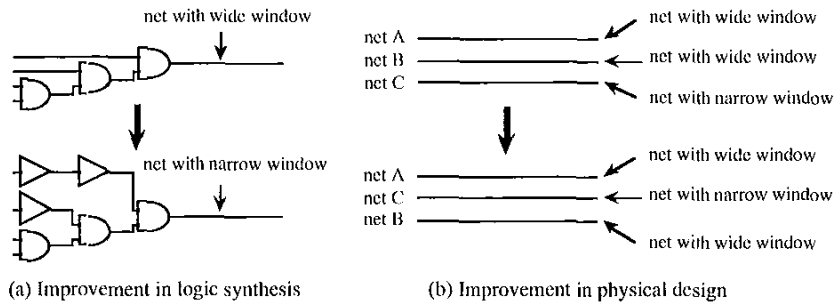


Fig. 9: Relative window improvement