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SWITCHING-TIME AND MOS TRANSISTOR SIZE IN PRESENCE OF INDUCTIVE EFFECTS

The optimization of transistor widths or width/length ratios (w/l) for the minimization of propagation delay in static CMOS transistors is provided. The optimal w/l for a CMOS gate is found to be a function of the inductive effects introduced by power and ground busses as well as the capacitive and resistive loads, respectively introduced by the transistor, and the power and ground busses. Because induction increases with current, it is found, in contrast to the presently standard belief in the art, that it is not always possible to decrease propagation delay by increasing the current drive and w/l ratio of a CMOS transistor.

Using a CMOS complementary transistor inverter pair as a test circuit, with a power line voltage v_{dd}, and ground line, inductances and resistances L and R associated with the power and ground lines, and capacitance C loading the output, both linear and nonlinear models for the test circuit may be provided. The linear model is simplified by assuming that the pMOS transistor of the pair starts conducting when the input voltage goes below a certain treshold (v_h), that the input ramp is fast enough to allow only a negligible charge to flow through the nMOS transistor, and that the pMOS transistor can be modeled by a time-invariant linear transistor R_{eq}. With v being defined as the gate output voltage and v(0) = 0, and with a step function u(t) being applied to the circuit to apply the voltage v_{dd}, the state equation of the circuit is:

$$LC\, d^2v/dt^2 + R'C\, dv/dt + v = V_{dd}u(t) \qquad (1)$$

where R' is equal to the sum of the resistance R associated with the voltage line and the resistance RF_{eq} of the transistor. Where the inductance L is assumed to be zero, equation (1) is easily solvable for v(t), and through integrating equation (1), a determination of the time it takes the voltage to reach the threshold voltage v_h is found to equal

$$R'C \ln [(V_{dd}-V_h)/V_{dd}].$$

Thus, where the inductance introduced by the power and ground lines is zero, it will be appreciated that the propagation time decreases monotonically as the w/l ratio of the transistor increases.

Where the inductive effects of the power and ground lines are nonzero, the solution to equation (1) changes. First, it can be shown that to avoid pure oscillatory voltage output behavior, the w/l ratio of the transistor must be less than:

$$k/[2(L/C)^{1/2} - R] \qquad (2)$$

Equation (2) therefore sets an upper bound on the w/l ratio of a transistor for given circuit parameters R, C, and L. Secondly, it will be seen that different solutions are set forth depending on whether R' is less than $2(L/C)^{1/2}$ or not. If R' is greater than the said value, any increase in the w/l ratio will decrease the propagation time, provided of course that equation (2) is satisfied. If R' is less than $2(L/C)^{1/2}$, a minimum value for R which will correspond to a minimum propagation time may be found numerically.

Where a nonlinear behavior is assumed for the transistors of the test circuit, it has been found that for some values for the parameters R, C, and L, there exists an optimum w/l transistor value which minimizes propagation delay. This is particularly true where the inductance in the voltage and ground lines reaches a certain threshold. Since inductance increases with increased current (i.e., increased w/l), the w/l values of a transistor must be carefully chosen to take into account inductive effects.

Using a computer simulation of nonlinear behavior, w/l ratios of transistors were varied from 5 to 40, capacitance (C) was varied from 50 to 400 fF, resistance (R) was varied from 10 to 80 ohms, and inductance (L) from 1 to 250 nH. It was found that for a small R, C, and L, the propagation delay decreased as the w/l ratio increased. However, for larger values of L (64 to 250 nH), the propagation delay had a minimum for w/l = 20. Where R was small, and C was larger (100 - 400 fF), it was found that the propagation delay decreased with increasing w/l ratios when L was smaller than an upper bound which increased with C (L < 128 nH for C = 100 fF; L < 256 nH for C = 200 fF). However, for values of L larger than that upper bound, the propagation delay had a minimum when w/l = 20. Finally, where R was larger (40 to 80 ohms), and C was small, the propagation time decreased as the w/l ratio increased provided L was smaller than an upper bound which increased as C increased. For values of L larger than that upper bound, the propagation time had a minimum where the w/l ratio was 10. However, for larger values of C (200 - 400 fF), the propagation time decreased as w/l increased regardless of the inductance L.