NEW ALGORITHMS FOR TIMING ANALYSIS OF LARGE CIRCUITS

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ABSTRACT: Timing simulation is a simplified form of circuit simulation in which the circuit equations are decoupled at each node to take advantage of the relative inactivity of large digital networks. Conventional integration schemes applied to tightly-coupled, bidirectional circuit elements either exhibit significant regions of instability or inaccuracy, or do not provide the necessary node decoupling. This paper examines a variety of implicit-explicit hybrid algorithms, classified as variable-in-time or variable-in-space, which are suitable for timing simulation. The floating capacitor, common in MOS circuits, is used as a test problem.

1. INTRODUCTION

While circuit simulators (e.g. [1],[2]) can provide accurate time-domain current and voltage waveforms from a device level description of an integrated circuit, as the size of the circuit increases the cost and memory requirements of such an analysis become prohibitive. For small circuits, the simulation time is generally dominated by the time required to evaluate device model equations [3] but as circuit size increases, or if more efficient modeling techniques are used, an increasing fraction of time is spent solving the sparse-matrix circuit equations [1].

Timing simulators decouple the circuit equations using nonlinear simultaneous displacement [4] or successive displacement [5],[6] methods. For most circuits, this decoupling maintains a linear relationship between the number of circuit elements and the simulation time required per timepoint of the analysis. An added advantage of the decoupled analysis is that event-driven selective trace algorithms may be used easily and independent control of the timestep at any node of the circuit is also possible. These techniques can provide substantial savings in large digital circuits where often only a small fraction of the circuit nodes are actively changing state at any one time [7].

A major drawback with the use of timing analysis is that tightly-coupled feedback loops, or bidirectional circuit elements, can cause severe inaccuracies and even instability during the analysis. For this reason, special techniques must be used to process such elements. One such element that has limited the application of timing analysis is the floating capacitor [8].

2. ALGORITHMS FOR FLOATING CAPACITORS

Floating capacitors play an important role in the analysis of MOS circuits. Often, the solution of networks containing arbitrary interconnections of a large number of floating capacitors is required. Such an analysis performed with ordinary implicit methods [9] would be extremely time consuming, because it requires the solution of a set of equations at each timestep. The use of explicit methods would reduce the computational effort, but requires small stepsize for stability reasons. The use of mixed implicit-explicit algorithms reduces the computational effort and allows, under certain conditions, the choice of optimal stepsize with regard to accuracy considerations while ensuring stability.

Two classes of algorithms are described here and referred to as "variable-in-space" and "variable-in-time" algorithms. We define an algorithm to be "variable-in-space" if different types of integration (implicit or explicit) are used for different components of the circuit at the same timepoint. We define an algorithm to be "variable-in-time" if different types of integration are used for the whole circuit at different timepoints. In the general case an algorithm can be both variable in space and time and different timesteps are used for implicit and explicit integration.

In the circuit that we use to test the algorithm we suppose that capacitors and conductances are linear for ease of proving algorithmic properties. For MOS circuits, where each node is assumed to have a capacitance to ground [7], the node equations are of the form:

$$C\dot{x}=Gx \quad x(0)=x_0 \quad x\in R^n \quad C,G\in R^{(n\times n)} \tag{1}$$

where x is the vector of node voltages. Eq.(1) can be rewritten in normal form[10]:

$$\dot{x}=Ax \quad A\in R^{(n\times n)} \tag{2}$$

with $A=C^{-1}G$. In order to study stability, we associate to each algorithm a companion matrix $M\in R^{(n,n)}$ such that:

$$x_{k+p}=M_p x_k \tag{3}$$

Then to ensure stability of the method we require the spectral radius [1] $\rho(M_p)\leq 1$ being all eigenvalues of modulus unity simple [11].

There are two basic approaches to "variable-in-space" algorithms, "partitioning of variables" or "guess of variables". The former requires an implicit integration on a subset of variables and an explicit integration for the remaining ones [12]. The latter is based on the guess at step $k+1$ of some quantities which are related to the values they had at the previous steps $k,k-1,\ldots,k-q$. In this paper we concentrate on the "guess of variables" method. Suppose we are integrating the set of equations defined by Eq.(2) using an implicit method such as Backward Euler (B.E.). At each step we have to solve the linear system:

$$[I-hA]x_{k+1}=x_k \tag{4}$$

To solve Eq.(4) we need a L.U. factorization of $[I-hA]$, which is very time consuming if we are dealing with a large system. Let us decompose A into the sum of two matrices

$$A=A_i+A_g \tag{5}$$

being A_i either lower or upper triangular. Eq.(4) is equivalent to

$$[I-A_i]x_{k+1}=x_k+A_g x_{k+1} \tag{6}$$

If we make the "guess" $A_g x_{k+1}=A_g x_k$ we must solve:

$$[I-hA_i]x_{k+1}=[I+hA_g]x_k \tag{7}$$

where we do not need any factorization since $[I-hA_i]$ is triangular. The companion matrix is $M_1=[I-hA_i]^{-1}[I+hA_g]$.

We will now restrict our analysis to the unit-cell which models a MOS transistor for timing analysis. From the circuit point of view we can refer to voltage guess methods and current guess methods:

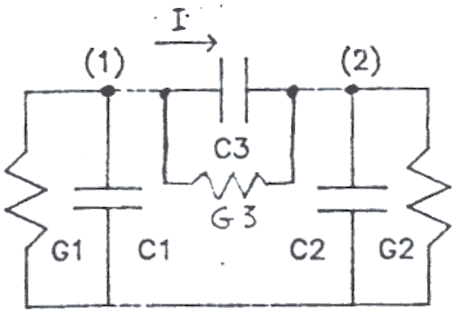

Fig.1 Floating Capacitor Test Problem

[1] The spectral radius of a matrix M is defined to be $\rho(M)=\max\{|\lambda| \ \lambda\in\sigma(M)\}$ where σ is the set of all the eigenvalues (spectrum) of M

(a) Let us consider first the most simple voltage guess method. Let us use B.E. integration, substitute the companion model for capacitors and apply nodal analysis to the circuit of Fig (1). By taking $A=C^{-1}G$ in Eq.(4) and multiplying both members by $\frac{C}{h}$ we obtain:

$$[\frac{C}{h}-G]x_{k+1}=\frac{C}{h}x_k \tag{8}$$

or more explicitly:

$$\begin{bmatrix} C_1+C_3+\frac{(C_1+C_3)}{h} & -C_3-\frac{C_3}{h} \\ -C_3-\frac{C_3}{h} & C_2+C_3+\frac{(C_2+C_3)}{h} \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \end{bmatrix}_{k+1} = \begin{bmatrix} \frac{(C_1+C_3)}{h} & -\frac{C_3}{h} \\ -\frac{C_3}{h} & \frac{(C_2+C_3)}{h} \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \end{bmatrix}_k \tag{9}$$

Let us use the guess $v^2_{k+1}=v^2_k$ in the first equation Then:

$$\begin{bmatrix} C_1+C_3+\frac{(C_1+C_3)}{h} & 0 \\ -C_3-\frac{C_3}{h} & C_2+C_3+\frac{(C_2+C_3)}{h} \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \end{bmatrix}_{k+1} = \begin{bmatrix} \frac{(C_1+C_3)}{h} & C_3 \\ -\frac{C_3}{h} & \frac{(C_2+C_3)}{h} \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \end{bmatrix}_k$$

and the companion matrix is

$$M_1 = \begin{bmatrix} C_1+C_3+\frac{(C_1+C_3)}{h} & 0 \\ -C_3-\frac{C_3}{h} & C_2+C_3+\frac{(C_2+C_3)}{h} \end{bmatrix}^{-1} \begin{bmatrix} \frac{(C_1+C_3)}{h} & C_3 \\ -\frac{C_3}{h} & \frac{(C_2+C_3)}{h} \end{bmatrix}$$

The method is absolutely stable for the test circuit. Fig.(2) shows the root locus and all roots stay within the unit circle for all values of circuit parameters

If C_1 and C_2 are small with respect to C_3, $C_3>0$ and the stepsize is increased, a pair of complex conjugate roots appears. These roots may cause an oscillatory error component in the resulting circuit waveforms, and therefore degrade the accuracy of the analysis. As it can be seen from the root locus, there exists a critical maximum timestep h_{crit} under which the roots are real and the solution is accurate.

(b) Another voltage guess method described in [8] can be achieved by decoupling Eq.(9) by taking the voltage at node (2) one step back in time to solve the first equation. This corresponds to guess

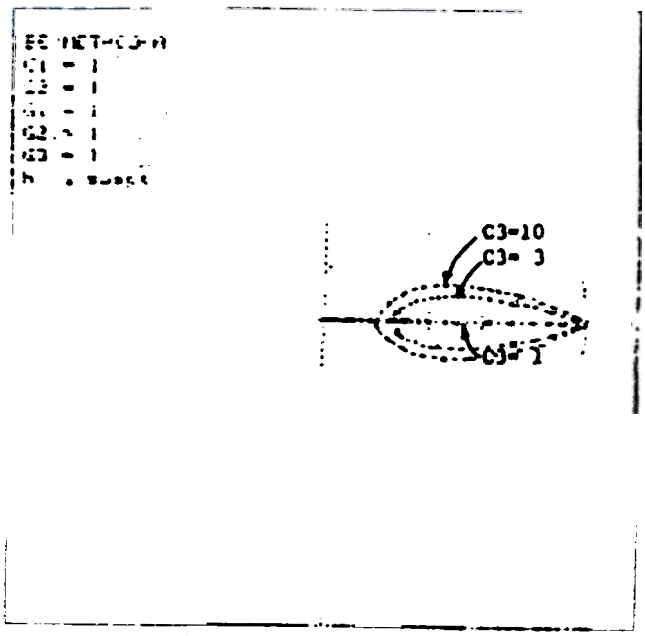

Fig.2 Root Locus for Method (a)

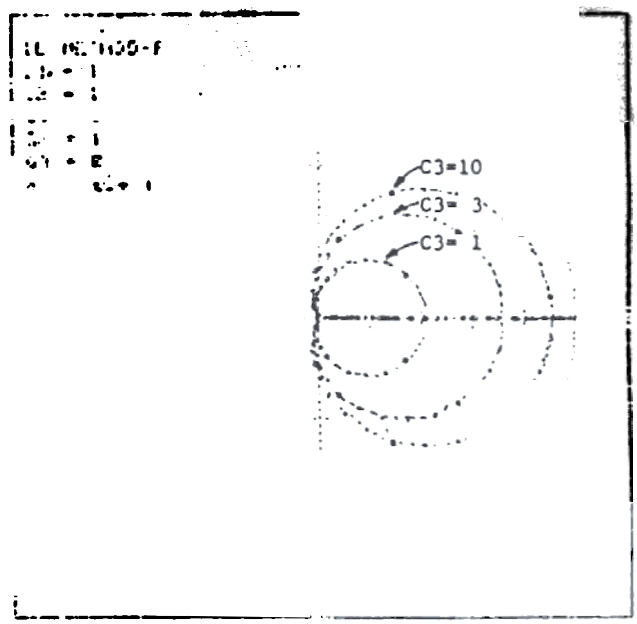

Fig.3 Root Locus for Method (b)

$C_3 v_{k+1}^2 = C_3 v_k^2$ and considering the current i through the floating capacitor as given by $\frac{C_3}{h}[(v_{k+1}^1 - v_k^1) - (v_k^2 - v_{k-1}^2)]$. Stability considerations are similar to method (a) though ringing appears in the case $C_3=0$, and h_{crit} has different values. Fig(3) shows the root locus versus h for different values of the floating capacitor.

(c) To avoid the ringing in the solutions given by methods (a) and (b) we can perform a so called "double crossed voltage guess". We refer now to Eq.'s(2),(4) and (5) applied to the test circuit. The method has two steps, modeled as Eq.(6). In the first one, $A_l = A_l$ is lower triangular and the guess $A_{g1} v_{k+1}^2 = A_{g1} v_k^2$ is used in the first equation to solve for v_{k+1}^1 and v_{k+1}^2. In the second step $A_l = A_u$ is upper triangular and the guess $A_{g2} v_{k+2}^1 = A_{g2} v_{k+1}^1$ is used in the second equation to solve for v_{k+2}^1 and v_{k+2}^2. The companion matrix is :

$$M_2 = [I - hA_u]^{-1}[I + hA_{g2}][I - hA_l]^{-1}[I + hA_{g1}] \qquad (10)$$

The method is stable for the test circuit and the eigenvalues are real for all values of circuit parameters.

Now we consider current guesses.

(d) The first approach is to remove the floating elements and substitute them with a current source, whose value is determined by an explicit predictor. B.E. integration scheme is used for node voltages, and leads to the set of decoupled equations:

$$v_{k+1}^1 = v_k^1 + \frac{h}{C_1}(-G_1 v_{k+1}^1 - i_{k+1}^p)$$

$$v_{k+1}^2 = v_k^2 + \frac{h}{C_2}(-G_2 v_{k+1}^2 + i_{k+1}^p) \qquad (11)$$

$i_{k+1}^p = i^{predicted}$

The simplest predictor we can use is $i_{k+1}^p = i_k$ where i_k is the current computed from the circuit equation at timestep k. Another method consists of predicting the voltage on the floating element v_{k+1}^f by means of a Forward Euler (F.E.) integration step and then solving for i_{k+1}^p. At each timestep the current i_k is evaluated and compared with i_k^p, if $|i_k - i_k^p| > \varepsilon$ the step is rejected and i_k^p is computed again with smaller stepsize. A more formal way of viewing the problem is to use modified nodal analysis for the circuit using i as appended variable and guessing its value as equal to the previous one. Using B.E. as the integration rule, we obtain:

$$\begin{bmatrix} 1+h\frac{G_1}{C_1} & 0 & 0 & 0 \\ 0 & 1+h\frac{G_2}{C_2} & 0 & 0 \\ 0 & 0 & 1+h\frac{G_3}{C_3} & -\frac{1}{C_3} \\ & -1 & -1 & 0 \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \\ v^3 \\ i \end{bmatrix}_{k+1}$$

$$\begin{bmatrix} 1 & 0 & 0 & -\frac{1}{C_1} \\ 0 & 1 & 0 & \frac{1}{C_2} \\ 0 & 0 & 1 & \underline{0} \\ 0 & 0 & 0 & \underline{0} \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \\ v^3 \\ i \end{bmatrix}_k$$

The method has proved to be unstable if C_3 is large with respect to C_1 and C_2, but stability does not depend on stepsize.

(e) We now take advantage of the possibility of computing exactly the time derivatives of the node voltages at each timestep and add these equations to the integrating equations for node voltages. Using B.E. integration scheme for the test circuit of Fig(1) we obtain:

$$\begin{bmatrix} 1+\frac{h}{t1} & 0 & -mh & -ah \\ \frac{1}{t1} & 1 & -m & -a \\ -hn & -hb & 1+\frac{h}{t2} & 0 \\ -n & -b & \frac{1}{t2} & 1 \end{bmatrix} \begin{bmatrix} v^1 \\ \dot{v}^1 \\ v^2 \\ \dot{v}^2 \end{bmatrix}_{k+1} = \begin{bmatrix} v^1 \\ 0 \\ v^2 \\ 0 \end{bmatrix}_k \qquad (12)$$

$$t1=\frac{C_1+C_3}{C_1+C_3} \quad t2=\frac{C_2+C_3}{C_2+C_3} \quad a=\frac{C_3}{C_1+C_3}$$

$$b=\frac{C_3}{C_2+C_3} \quad m=\frac{C_3}{C_1+C_3} \quad n=\frac{C_3}{C_2+C_3}$$

by choosing as guess matrix:

$$A_g=\begin{bmatrix} 0 & 0 & -mh & -ah \\ 0 & 0 & -m & -a \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \qquad (13)$$

then:

$$A_1 x_{k+1} = [I+A_g]x_k \qquad (14)$$

and $M=A_1^{-1}[I+A_g]$. The stability of the method is not affected by the value of C_3, but the stepsize must be larger than a critical value. The major drawbacks are larger matrix dimension and the loss of accuracy if h is forced to be large. This might lead to the loss of fast transients when C_1 and C_3 are small with respect to C_2. In the case $C_3=0$ only the guess $\dot{v}^2_{k+1} = \dot{v}^2_k$ is performed which corresponds to guessing the current through C_2.

As a final remark, for the current-guess methods it should be pointed out that the best strategy as far as stability and accuracy are concerned is to guess the current through the smallest capacitor.

The following table summarizes stability considerations for the methods described above.

Next we focus our attention now on the "variable-in-time" algorithms. "Variable-in-time" algorithms have the advantage of reducing the total number of implicit integration steps and therefore the number of factorizations. In this case we combine a strictly stable algorithm (B.E.) with an explicit one (F.E.). We refer now to Eq.(2) and consider first the case where we have each

method	C_1	C_2	stepsize	stability	accuracy
a	any	any	$h<h_{crit}$	yes	yes
a	any	any	$h>h_{crit}$	yes	no
a	0	any			
b	any	any	$h<h_{crit}$	yes	yes
b	any	any	$h>h_{crit}$	yes	no
c	any	any	any	yes	yes
d	0	$C_3<C_3$	any	yes	
e			$h>h_{crit}$		
e		any	$h<h_{crit}$	no	no

* for no ringing

Table 1. Stability and accuracy of guess methods

implicit step with stepsize h_b followed by an explicit one with stepsize h_f. The companion matrix is:

$$M_2=[I+h_f A][I-h_b A]^{-1} \qquad (15)$$

By the spectral mapping theorem [13]:

$$\sigma(M_2)=\left\{\frac{1+h_f\lambda}{1-h_b\lambda} \;\; |\lambda\epsilon\sigma(A)\right\} \qquad (16)$$

and stability is ensured if $\rho(M_2)<1$. The algorithm is stable if:

$$h_b-h_f>\frac{2\,Re\,\lambda}{|\lambda|^2} \;\; |\lambda\epsilon\sigma(A) \qquad (17)$$

This condition requires the knowledge of the eigenvalues λ of A. It is easy to see that by taking $h_b \geq h_f$, condition (17) is always satisfied, provided we deal with a stable system. As a further generalization of this class of algorithms let r implicit steps with stepsize h_{bj} be mixed with s explicit steps with stepsize h_{fj}, where $s+r=p$ and s, r coprime. In this case:

$$\sigma(M_p)=\left\{\frac{\prod_{j=1}^{s}(1+h_{fj}\lambda)}{\prod_{j=1}^{r}(1-h_{bj}\lambda)} \;\; |\lambda\epsilon\sigma(A)\right\} \qquad (18)$$

and stability is ensured by $\rho(M_p)<1$

3. SUMMARY

This brief overview of mixed algorithms is far from exhaustive. Its purpose is only to point out the potential reduction in total computational effort provided by these methods and the related stability problems. The stability analyses must be extended to more general networks typical of large integrated circuits. At present, some of the algorithms are under test in a timing simulator and will be used for the analysis of large MOS circuits.

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