

An Image Decoding ASIC for Space-Based Applications

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Abstract

The multi-anode microchannel array (MAMA) is a photon counting detector with primarily astronomical applications which decodes the position of an event through coincidence discrimination. The decoding algorithm which associates a given event with the appropriate pixel is determined by the geometry of the anode array. A space-based realization of the MAMA detector requires that the decoding circuit be an Application Specific Integrated Circuit because of power, size and weight constraints. A 1.5 micron CMOS gate array version of the decoder has been fabricated and tested. The chip's development and characteristics are presented, and the ASIC decoder is contrasted with existing discrete component decoders in terms of size, speed, power, reliability, and operational flexibility. A new algorithm incorporated into the ASIC decoder which doubles the pixel spatial resolution is also described.

1. Introduction

The multi-anode microchannel array (MAMA) detector employs a photocathode for photon/electron conversion, a microchannel plate (MCP) for electron multiplication and an anode array combined with charge amplifiers for event detection. Digital decoding electronics interpret the charge amplifier outputs to determine the pixel position of an event. The block diagram of a MAMA detector is shown in Figure 1.

The current generation of MAMA detectors employ arrays which consist of two sets of interleaved anodes in a repeating series (see Figure 2). For historical reasons these are called "fine-fine" anode arrays. The first set of anodes consists of n anodes (which repeats for $n+2$ cycles) and the second set consists of $n+2$ anodes (which repeats for n cycles), resulting in a total of $n*(n+2)$ pixels, where n must be even to insure unique decoding over the entire array. The interleaving of the two sets of anodes is analogous to two waves of slightly different frequency beating against each other for one complete cycle. Another pair of anode sets (not shown in Figure 2) of m and $m+2$ anodes run underneath and perpendicular to the first pair of anode sets, resulting in a total of $m*(m+2)$ pixels in the perpendicular axis.

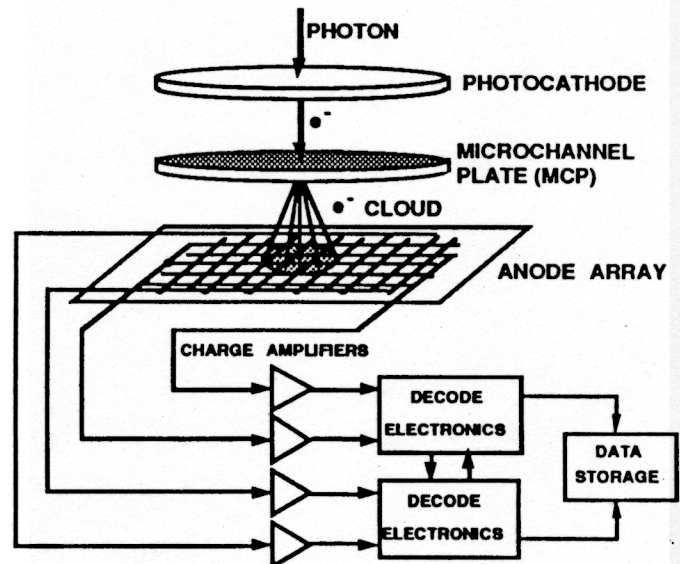


Figure 1. MAMA block diagram

The spread of the electron cloud due to a single photon event varies depending on the MCP's characteristics as well as bias voltages applied to the photocathode, MCP and anode array. The size of an electron cloud is quantized by the total number of anodes illuminated in a given axis, also referred to as the order of the fold. For example, a three-fold designates the situation in which three contiguous anodes are struck by sufficient numbers of electrons to have voltages greater than some user-specified threshold. A subsection of a scaled-down version of one axis of a fine-fine anode array ($n=4$) with one-, two-, three-, and four-folds is shown in Figure 2. The electron cloud spread must be sufficiently large to illuminate at least two anodes (a two-fold) in order to allow for the unique decoding of the position of the event. However, owing to size variations in the electron cloud from the MCP, the decoding algorithm must be capable of coping with higher-order folds. As Figure 2 illustrates, every higher-ordered fold can be reduced to an equivalent two-fold (that two-fold which occupies the same pixel as the higher-ordered fold); in the case of an odd-fold there are two possible equivalent two-folds. A decoder's function is to take an arbitrarily ordered fold and infer the correct pixel position of the

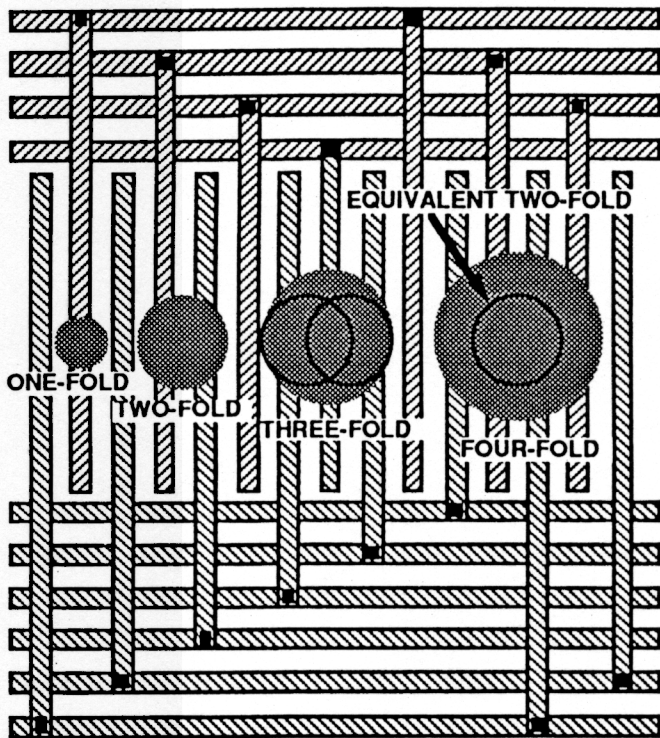


Figure 2. Fine-fine array single axis with multi-folds

event in the anode array. Since there is one decoder input for each anode, a single axis requires $2n+2$ inputs. A typical value for n is 32, in which case the decoder must accommodate 66 inputs for a single axis of the detector. Because of the large number of inputs and complicated requirements for legal events, event decoding cannot easily be reduced to a single step process. The algorithm for event decoding is therefore divided into two stages: anode encoding, which is the process of converting a k -fold into the equivalent two-fold for arbitrary k (see Figure 2); and pixel decoding, which is the process of translating the equivalent two-fold into the correct pixel position. Typically the anode encoding operation reduces the datapath width from 66 bits to 11 bits, thereby simplifying the pixel decoding operation.

To date, all MAMA detector systems have had circuitry composed of discrete parts, suitable for ground-based astronomy or use on sounding rockets. However, in the near future MAMA detectors will be employed in satellite systems such as the Solar Heliospheric Observatory (SOHO) and the Space Telescope Imaging Spectrograph (STIS). Space-based MAMA detectors require (relatively) radiation-hard decoding circuitry with lower power, weight, and size as well as higher reliability than their ground-based counterparts, preferably in the form of a single chip or a pair of chips. The obvious solution to this problem is an Application Specific Integrated Circuit (ASIC). An ASIC-based design has fewer components and therefore higher reliability than the the same circuitry constructed with discrete parts. Power constraints dictate that the ASIC be of the CMOS type.

2. Design Methodology

Because of their relatively low cost, massive functional capacity and fast production time, CMOS gate arrays were selected as the target technology for space-based MAMA decoders, and LSI Logic was selected as the vendor by virtue of their high performance and high-capacity commercial and radiation-hard gate arrays. A prototype decoder has been designed and fabricated in commercial technology and has been successfully evaluated in end-to-end system tests at Stanford University.

Major portions of the MAMA decoder chip were designed with computer-aided synthesis tools which are part of the Olympus system developed at Stanford University. The circuit was modeled in a high level language, called HardwareC, which was compiled into a logic netlist, then optimized and mapped into an interconnection of cells of the chosen target library. Specific blocks like ROMs were explicitly declared in the HardwareC description so that their functionality and modularity were preserved through the synthesis process. The gate level netlist was generated in a format compatible with the LSI Logic Design and Simulation (LDS) tools which were used for gate level simulation and electrical evaluation of the circuit. The LDS tools allowed critical areas of the circuitry to be identified and fine-tuned to optimize performance. In addition, the LDS tools performed the simulation of all legal anode input combinations for two-, three-, four-, five- and six-folds over a wide range of temperature and supply voltage conditions. Finally chip-finishing tasks such as floorplanning and assignment of bonding pads were performed with the LDS tools. The design was then fabricated in 155 pin and 299 pin PGA packages; the larger package incorporates a large number of diagnostic test points for testing and characterization purposes and the smaller package is targeted for satellite flight systems.

3. Circuit Description

A simplified block diagram of the gate array realization of the MAMA decoder is shown in Figure 3. Transient inputs (which are not always precisely coincident in time or of uniform length due to sensitivity and speed variations in the individual charge amplifiers) are stored in edge-triggered flip-flops. Because the decoder inputs are connected directly to the clock pins of the flip-flops, the flip-flops act as edge-triggered latches. The occurrence of an event in any one of the input lines initiates a sequence of actions within the timing and control state machine. The maximum allowed delay between the earliest and latest charge amplifier outputs from a single event is called the amplifier skew. After a user-controlled period corresponding to the amplifier skew, the state machine connects the Q outputs with the D inputs of the input flip-flops, thereby freezing the state

output of any of the currently existing MAMA detectors which utilize the fine-fine anode arrays. For example, a 360 by 1024 pixel MAMA detector would require one decoder chip for the 360 pixel axis and another for the 1024 pixel axis. Although both of these decoder ASICs are identical, one chip would act as the timing master and the other chip would serve as the timing slave, with communication between the two carried out by dedicated handshake lines. In the event that the slave detects an event input when the master does not, the slave can send a handshake signal to the master causing the master to reset itself as well as the slave, leaving both chips ready to accept new event inputs.

There are several error prevention features built into the decoder ASIC. One-folds and simultaneous events are both rejected automatically because they cannot be associated with any given pixel through coincidence discrimination. Similarly, folds whose order is greater than six and occurrences of events containing any non-contiguous anodes are also rejected. Because the inputs are edge-triggered, malfunctioning charge amplifier outputs which are stuck at zero or one are ignored. Metastability protection is designed into both the data path and the state machine; the expected mean time between metastability failures is two billion years given a worst case scenario of a 50 MHz clock and a 6.25 MHz event rate at 125 °C combined with a 4.5 volt supply. Schmitt trigger input buffers are employed wherever possible for improved noise immunity, and control inputs have built-in pull-up or pull-down resistors to force them to a default operational configuration should they

somehow be disconnected.

The 155 pin and 299 pin ceramic PGA packages which house the gate arrays are shown in Figure 5. Both of the PGA's are constructed in the cavity downwards configuration to improve heat handling characteristics. A pair of gate arrays requires less than 0.4 watts to perform decodes with a pulse pair resolution of 160 nanoseconds when clocked at 50 MHz. Each gate array is composed of approximately 23,000 gates, of which 18,000 are ROM LUTs. Normal commercial fabrication was used for initial evaluation of the gate array, and it is not yet clear whether fabrication of the chips in radiation-hardened technology will be necessary. The expected lifetime radiation dose for the STIS and SOHO systems is less than 30 kRad. The spacecraft electronics will be exposed to a wide variety of energetic particles, including a significant number of massive particles such as protons. A 299 pin decoder ASIC was subjected to proton bombardment for a total dose of 30 kRad and survived in good working order. The chip was tested both during and after the proton exposure, and a sample combinational logic path was monitored for variations in propagation delay. After exposure to 30 kRad, the propagation delay had increased by 8%, well within tolerable limits.

In contrast to the ASIC version of the MAMA decoder, an example of the latest generation of decoder constructed at the Ball Aerospace Systems Group from discrete components is shown in Figure 6. The discrete component decoder is more than two times slower and uses more than six times the power of its ASIC counterpart. The discrete component decoder occupies 8.4

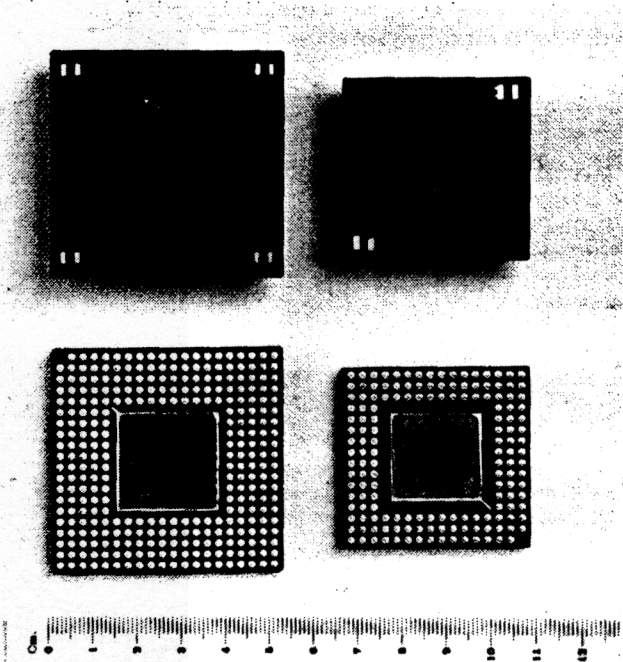


Figure 5. MAMA ASIC decoder PGA packages

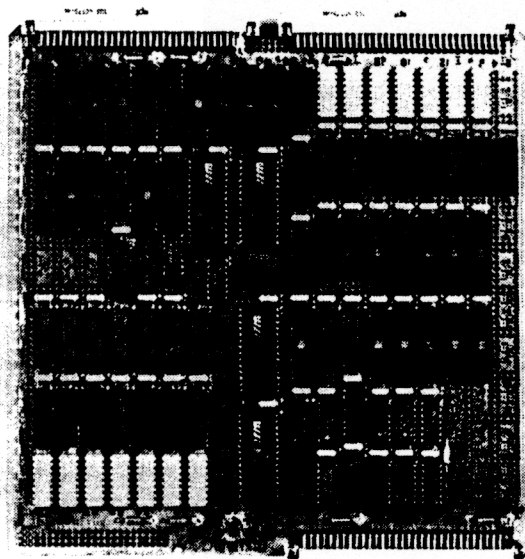


Figure 6. Discrete component MAMA decoder

times the area of the ASIC, thereby presenting a larger cross section to radiation and making it less reliable for space-based applications, as well as less desirable from the standpoint of size and weight. In addition the ASIC has greater flexibility in that it can decode any size array and can accommodate either active high (used in older systems) or active low (used in next generation systems) charge amplifier outputs. The discrete component decoder is limited to a single array size and can only be used with active high charge amplifier outputs. Table 1 summarizes the major differences between the ASIC and discrete component decoders.

	ASIC DECODER	DISCRETE DECODER
POWER	0.4W	2.5 W
PULSE-PAIR RESOLUTION	160 nS adjustable	350 nS fixed
SIZE	35 cm ²	295 cm ²
DECODES	224 x 960 360 x 1024 1024 x 1024	360 x 1024
FOLDS SELECTABLE?	YES	NO
METASTABILITY PROTECTION?	YES	NO
CHARGE AMP OUTPUTS	active high or active low	active high only

Table 1. ASIC decoder vs. discrete component decoder

4. High Resolution Decoding

A special feature incorporated into the MAMA decoder ASIC is high resolution decoding. In a standard MAMA detector pixel size is equal to the spacing of the anodes, but the spatial resolution of the MCP is generally about twice that of the anode array. This implies that the detector is capable of spatial resolution twice as high as that achieved with the original fine-fine decoding scheme. It is possible to increase the resolution of the detector without changing the detector itself, but only by altering the readout electronics. One technique for doubling the spatial resolution is called even-odd discrimination and this algorithm is incorporated into the decoder ASIC; this is the first time it has ever been employed in any decoding circuit. Even-odd discrimination involves discriminating between even-folds and odd-folds to generate a single least significant bit (LSB), thereby doubling the detector's spatial resolution. The value of the least significant bit depends on whether the throw left or the throw right option is used for handling odd-ordered folds. In the case of throw left, the LSB is high only if the event is an odd-

fold, whereas in the case of throw right, the LSB is high only if the event is an even-fold and is low otherwise. This operation can be performed in parallel with the standard decoding procedure with no loss of decoder speed and necessitates the addition of minimal hardware to the standard decoding circuitry (although the memory size must be quadrupled). Figure 7 illustrates normal resolution (top) versus high resolution achieved with even-odd discrimination (bottom). Standard pixels are twice the size, and span from the center of one anode to the next, whereas the even-fold pixels are centered between the anodes and the odd-fold pixels are centered on the anodes themselves. The performance of this algorithm depends in part on the number of even-folds being comparable to the number of odd-folds. MAMA detectors can usually be configured to satisfy this condition, as was illustrated in Figure 4 in which 52% of the events detected were even-folds and 48% were odd-folds. The even-odd discrimination algorithm has been successfully tested in preliminary imaging experiments at Stanford University. Figure 8 shows two spots, created by placing a mask with two holes in front of an ultraviolet light source, imaged by the decoder ASIC. The smaller pair of spots on the left were imaged in normal resolution mode; the pair of larger spots on the right are the same two spots imaged in high resolution mode with even-odd discrimination. Thus far, higher spatial resolution has clearly been achieved, and more precise tests are being carried out to measure the exact degree of resolution.

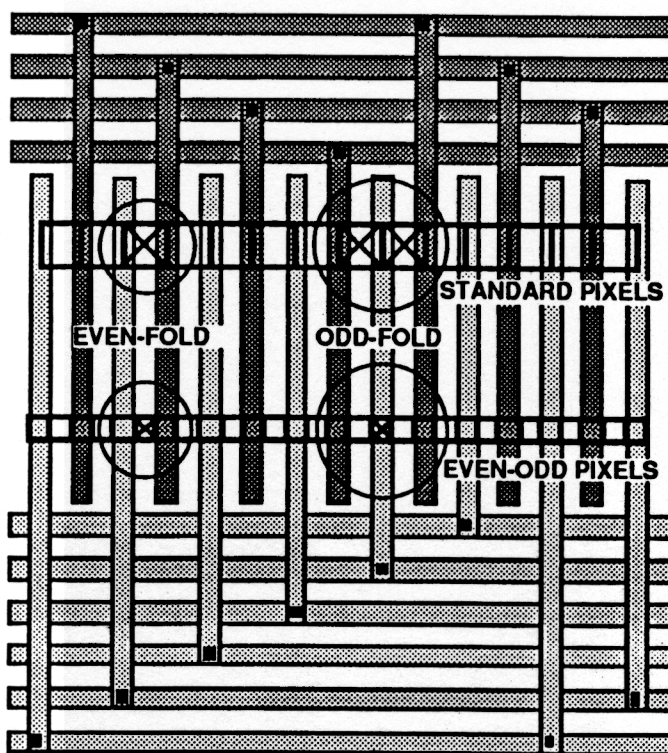


Figure 7. High resolution : even-odd discrimination

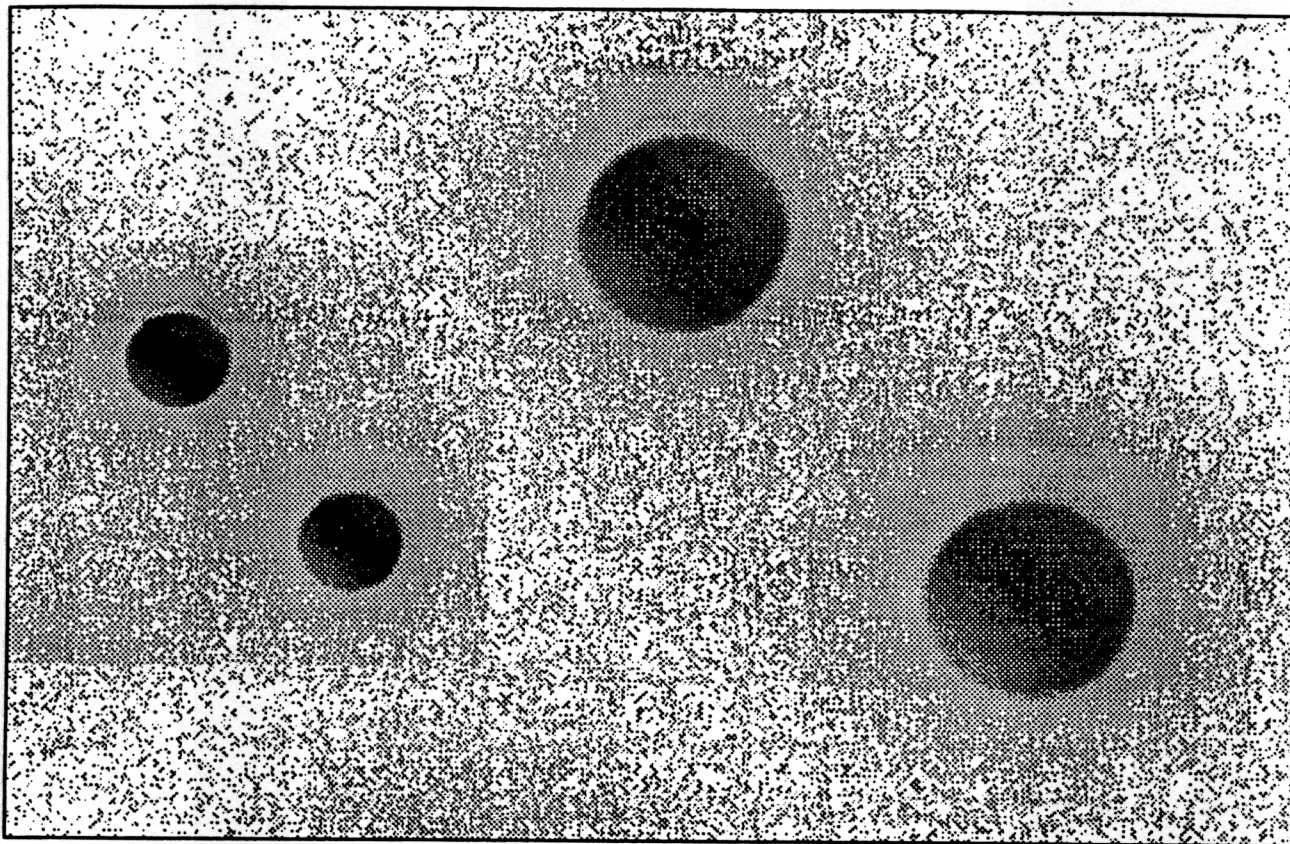


Figure 8. Normal resolution image of two spots combined with high resolution image of the same two spots

5. Summary

An ASIC version of a MAMA digital decoder, suitable for space-based applications, has been designed, fabricated and tested successfully. The design was fabricated in commercial 1.5 micron CMOS gate array technology, and the chip is smaller, faster, incorporates more features and uses less power than previous discrete component decoders. The chip has performed well in preliminary radiation exposure tests and incorporates a new algorithm which doubles the detector spatial resolution.

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References

1. D.B. Kasle, "Decoding Techniques for fine-fine-geometry multi-anode microchannel arrays", SPIE Ultraviolet Technology II Vol. 932, pp. 280-284, 1988.
2. D.B. Kasle, "High resolution decoding techniques and single chip decoders for multi-anode microchannel arrays", SPIE Ultraviolet Technology III Vol. 1158, pp. 311-318, 1989.
3. G. De Micheli, D. Ku, F. Mailhot, T. Truong, "The Olympus Synthesis System for Digital Design", IEEE Design & Test, October 1990, pp. 37-53.
4. J.G. Timothy, "Electronic readout systems for microchannel plates," IEEE Transactions on Nuclear Science Vol. NS-32, No. 1, pp. 427-432, 1985.
5. J.G. Timothy and R.L. Bybee, "High-resolution pulse-counting array detectors for imaging and spectroscopy at ultraviolet wavelengths," SPIE Ultraviolet Technology Vol. 687, pp. 109-116, 1986.
6. J.S. Morgan, et. al., "High Time-Resolution Imaging with the MAMA Detector Systems," SPIE Instrumentation in Astronomy Vol. 1235, No. 7, pp. 347-356, 1990.