Guest Editorial Design and Automation for Quantum Computation and Quantum Technologies

QUANTUM computation is a promising field of research that will shift the computation paradigm for data and information processing with quantum parallelism. This Special Issue of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) is dedicated to showcasing the latest research progress on the design and automation for quantum computation and quantum technologies.

Although the pursuit of fault-tolerant, large-scale quantum computation may still have a long way to go, rapid progress is being made thanks to worldwide efforts of extensive and intensive research. As a matter of fact, near-term intermediate-scale quantum (NISQ) devices have been demonstrated helpful in various applications. Various quantum computation platforms have been developed and are even available on commercial cloud services.

To enable quantum computation, one has to resort to hardware and software solutions as well as scientific and engineering challenges. These tasks require interdisciplinary studies. In particular, from the hardware perspective, quantum processor and interface circuit designs need expertise in device physics and circuit and system engineering. From the software perspective, quantum program compilation and design with quantum technologies require expertise in software engineering and design automation.

This Special Issue intends to provide a comprehensive collection of the state of research in the area of design and automation for quantum computation and quantum technologies. In the review paper [A1], De Micheli *et al.* survey the recent progress in different levels of the abstraction stack of quantum computation. It covers challenges and advances in quantum architecture, programming languages, software compilation, and hardware synthesis with quantum technologies. Also, through a rigorous review process, only ten research papers were accepted for publication. They can be classified into four categories: 1) applications of quantum computation models, 2) quantum architecture design and profiling, 3) quantum program compilation, and 4) design and automation for quantum technologies.

I. Applications of Quantum Computation Models

The central ideas of quantum computation are to exploit the extraordinary properties of quantum mechanics to achieve data and information processing more efficiently than classical computation. In this aspect, this Special Issue contains two articles.

In [A2], Kishi *et al.* propose a graph kernel that exploits the quantum superposition property to take all subgraphs into account for similarity characterization. The corresponding quantum algorithm achieves better classification accuracy than existing graph kernels in the studied bioinformatics application.

In [A3], Giuffrida *et al.* exploit the classical-quantum hybrid Grover Adaptive Search (GAS) procedure for the Quadratic Unconstrained Binary Optimization (QUBO) problem-solving. The authors study various strategies and parameters in the GAS procedure for a number of applications.

II. Quantum Architecture Design and Profiling

Quantum processors are the hardware engine that hosts the execution of quantum algorithms. The architecture of a quantum processor plays a decisive role in computation quality and efficiency. The following two articles study this subject.

In [A4], Lin *et al.* propose a methodology to customize the qubit connectivity of a quantum processor architecture with respect to a given input quantum circuit. This article demonstrates that such customization may substantially improve computation fidelity.

In [A5], Yang *et al.* aim to profile how “quantum” a quantum processor may exhibit in terms of quantum nonlocality. A scalable method for testing the violation of Bell inequality is proposed and applied to the IBM quantum devices.

III. Quantum Compilation

For a quantum algorithm to be conducted on a quantum processor, the corresponding quantum program has to be correctly compiled into a sequence of primitive quantum gates (unitary operations) for execution. Three articles in this Special Issue investigate the compilation issues.

In [A6], Jiang *et al.* take a hypercube viewpoint to guide the synthesis of reversible circuits. The authors demonstrates that the method is beneficial in reducing the gate count in compiling reversible functions.

In [A7], Peham *et al.* are concerned with the correctness of quantum program compilation. The authors explore the

Digital Object Identifier 10.1109/JETCAS.2022.3207268

feasibility of ZX-calculus, a quantum circuit rewriting system, in equivalence checking of quantum circuits.

In [A8], Yu performs a case study of mapping the quantum algorithm of association rules mining (qARM) for quantum processor execution. This article provides a manual compilation by designing a quantum circuit of qARM for execution on IBM quantum devices.

IV. Design and Automation for Quantum Technologies

Various technologies beyond CMOS are under active development. Different technologies possess different characteristics, yielding distinct strengths and weaknesses in serving as a computation platform. System design under a target technology requires special domain knowledge and customized design automation tools. In this Special Issue, three articles cover the design and automation issues under their target technologies.

In [A9], Gys *et al.* present a co-design and co-simulation methodology for the silicon spin qubits in quantum dots and the cryo-CMOS interface circuitry. The authors integrate the spin qubit model into the conventional design flow.

In [A10], Gemma *et al.* aim to provide a solution to the characterization, control, and fine-tuning of photonic integrated chips (PICs) as basic building blocks of photonic quantum computers. This article features electronic and optical modules for sensing and control with software optimization and image processing algorithms.

In [A11], Mamdouh *et al.* design the building blocks in artificial intelligence (AI) accelerators under the QCA model. The authors present a low-cost, high-throughput, and energy-efficient QCA design for AI acceleration.

With these review and research papers, we hope this Special Issue may inspire and invite researchers to tackle challenges and contribute to making reliable, large-scale quantum computation viable soon.

Acknowledgment

We would like to express our gratitude to the authors for their high-quality work contributing to this Special Issue. Their endeavors provide comprehensive coverage of the main themes of design and automation for quantum computation and quantum technologies. We also thank the anonymous reviewers for their timely reviews giving valuable comments and suggestions for the submitted papers. We are grateful to Prof. Matthew Amy for his contribution to the proposal of this Special Issue. Last but not least, we thank the former Editor-in-Chief (EiC), Prof. An-Yeu (Andy) Wu, for motivating the initiation of the Special Issue, and EiC, Prof. Ho Ching (Herbert) Iu, Associate EiC, Prof. Carl Ho, as well as the Senior Editorial Board for their support, guidance, and advice.

Jie-Hong R. Jiang, *Corresponding Guest Editor*
Department of Electrical Engineering
National Taiwan University
Taipei 10617, Taiwan
e-mail: jhjiang@ntu.edu.tw

Giovanni De Micheli, *Guest Editor*
Institute of Electrical Engineering and Computer Science
École Polytechnique Fédérale de Lausanne (EPFL)
1015 Lausanne, Switzerland
e-mail: giovanni.demicheli@epfl.ch

Kaitlin Smith, *Guest Editor*
Department of Computer Science
University of Chicago
Chicago, IL 60637 USA
e-mail: kns@uchicago.edu

Mathias Soeken, *Guest Editor*
Quantum Team
Microsoft
8058 Zürich, Switzerland
e-mail: mathias.soeken@outlook.com

Appendix: Related Articles

[A1] G. D. Micheli, J.-H. R. Jiang, R. Rand, K. Smith, and M. Soeken, "Advances in quantum computation and quantum technologies: A design automation perspective," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3205174.

[A2] K. Kishi, T. Satoh, R. Raymond, N. Yamamoto, and Y. Sakakibara, "Graph kernels encoding features of all subgraphs by quantum superposition," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3200837.

[A3] L. Giuffrida, D. Volpe, G. A. Cirillo, M. Zamboni, and G. Turvani, "Engineering Grover adaptive search: Exploring the degrees of freedom for efficient QUBO solving," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3202566.

[A4] W.-H. Lin, B. Tan, M. Y. Niu, J. Kimko, and J. Cong, "Domain-specific quantum architecture optimization," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3202870.

[A5] B. Yang, R. Raymond, H. Imai, H. Chang, and H. Hiraishi, "Testing scalable Bell inequalities for quantum graph states on IBM quantum devices," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3201730.

[A6] Y. C. Jiang, K. C. Tseng, C. Y. Hua, S. Y. Kuo, Y. H. Chou, and S. Y. Kuo, "A novel hypercube-based heuristic for quantum Boolean circuit synthesis," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3202840.

[A7] T. Peham, L. Burgholzer, and R. Wille, "Equivalence checking of quantum circuits with the ZX-calculus," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3202204.

[A8] C. Yu, "Experimental implementation of quantum algorithm for association rules mining," 2022, *arXiv:2204.13634*.

[A9] B. Gys, R. Acharya, S. Van Winckel, K. D. Greve, G. Gielen, and F. Catthoor, "A co-simulation methodology for the design of integrated silicon spin qubits with their control/readout cryo-CMOS electronics," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3201980.

[A10] L. Gemma, M. Bernard, and D. Brunelli, "An optical tool to optimize the output of a photonic integrated chip architecture," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3200937.

[A11] A. Mamdouh, M. Mjema, G. Yemiscioglu, S. Kondo, and A. Muhtaroglu, "Design of efficient AI accelerator building blocks in quantum dot cellular automata (QCA)," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 3, Sep. 2022, doi: 10.1109/JETCAS.2022.3202043.

Jie-Hong R. Jiang (Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 1998, respectively, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA, USA, in 2004.

He is a Professor with the Department of Electrical Engineering and the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan. He leads the Applied Logic and Computation Laboratory and has worked extensively on logic synthesis, formal verification, electronic design automation, and computation models of biological and physical systems.

Dr. Jiang is a member of Phi Tau Phi and the Association for Computing Machinery.

Giovanni De Micheli (Fellow, IEEE) received the Nuclear Engineer degree from Politecnico di Milano in 1979, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of California at Berkeley in 1980 and 1983, respectively.

He was a Professor of electrical engineering at Stanford University. He was the Director of the Electrical Engineering Institute (IEL), EPFL, from 2008 to 2019, and a Program Leader of the Swiss Federal Nano-Tera.ch program. He is currently a Research Scientist in electronics and computer science. He is credited for the invention of the Network on Chip design automation paradigm and for the creation of algorithms and design tools for Electronic Design Automation (EDA). He is a Professor and the Director of the Integrated Systems Laboratory at EPFL Lausanne, Switzerland. His current research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies. He is also interested in heterogeneous platform design, including electrical components and biosensors, as well as in data processing of biomedical information. He is the author of *Synthesis and Optimization of Digital Circuits* (McGraw-Hill, 1994), and a coauthor and/or co-editor of ten other books and of over 900 technical articles. His citation H-index is above 100, according to Google Scholar.

Prof. De Micheli is a Fellow of ACM and AAAS, a member of the Academia Europaea, and an International Honorary Member of the American Academy of Arts and Sciences. He is also a member of the Scientific Advisory Board of IMEC (Leuven, B) and STMicroelectronics. He is the recipient of the 2020 IEEE/TC Achievement Award in Cyberphysical Systems, the 2020 IEEE/CEDA Richard Newton Technical Impact Award, the 2019 ACM/SIGDA Pioneering Achievement Award, the 2016 EDAA Lifetime Achievement Award, the 2016 IEEE/CS Harry Goode Award for seminal contributions to design and design tools of Networks on Chips, the 2012 IEEE/CAS Mac Van Valkenburg Award for contributions to theory, practice, and experimentation in design methods and tools, and the 2003 IEEE Emanuel Piore Award for contributions to the computer-aided synthesis of digital systems. He also received the D. Pederson Award for the Best Paper on the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS (IEEE CAD/ICAS) in 1987 and 2018, and several best paper awards, including DAC (1983 and 1993), DATE (2005), Nanoarch (2010 and 2012), and Mobihealth (2016). He has been serving IEEE in several capacities, namely: Division 1 Director (2008–2009), Co-Founder and President Elect of the IEEE Council on EDA (2005–2007), President of the IEEE CAS Society (2003), Editor-in-Chief of the IEEE CAD/ICAS (1997–2001). He has been the Chair of several conferences, including Memocode (2014), DATE (2010), pHealth (2006), VLSI SOC (2006), DAC (2000), and ICCD (1989).

Kaitlin Smith (Member, IEEE) received the B.S. degree in mathematics and electrical engineering and the M.S. degree in electrical engineering from Southern Methodist University (SMU) in 2014 and in 2015, respectively, and the Ph.D. degree in electrical engineering from SMU in December 2019. She is a CQE/IBM Postdoctoral Scholar in the Department of Computer Science, University of Chicago. Within the focus of quantum computing, her work involves technology-aware programming, computer architecture, distributed computing, and security. She was named a 2021 MIT EECS Rising Star and is the recipient of the 2021 IEEE Computer Society Technical Committee on Multiple Valued Logic (TC-MVL) Kenneth C. Smith Early Career Award in microelectronics.

Mathias Soeken (Member, IEEE) received the Ph.D. degree (Dr.-Ing.) in computer science from the University of Bremen, Germany, in 2013. From 2009 to 2015, he worked at the University of Bremen, Germany, where he was a Co-Founder of RevKit, a framework for reversible logic synthesis. From 2015 to 2020, he has been with École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, as a Postdoctoral Scientist, where he pioneered the EPFL Logic Synthesis Libraries, a set of industrial-strength academic logic synthesis tools, which today are the backbone of many logic synthesis and quantum compilation tools. He currently works with the Quantum Team, Microsoft. His research interests are logic synthesis, quantum computing, and formal verification.