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Operation regimes and electrical transport of steep slope Schottky Si-FinFETs

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In the quest for energy efficient circuits, considerable focus has been given to steep slope and polarity-controllable devices, targeting low supply voltages and reduction of transistor count. The recently proposed concept of the three-independent gated Si-FinFETs with Schottky-barriers (SBs) has proven to bring both functionalities even in a single device. However, the complex combination of transport properties including Schottky emission and weak impact ionization as well as the body effect makes the design of such devices challenging. In this work, we perform a deep electrical characterization analysis to visualize and decouple the different operation regimes and electrical properties of the SB Si-FinFETs using a graphical transport map. From these, we give important guidelines for the design of future devices. *Published by AIP Publishing.*
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I. INTRODUCTION

Energy efficient devices and circuits are essential to enable a higher complexity of integration with manageable power consumption in nomad applications and to prevent power constrains such as dark silicon in highly integrated circuits. Therein, steep switching slope devices, such as Tunnel Field-Effect Transistors (TFETs), aim to maintain a quadratic reduction of dynamic power consumption vs. conventional field-effect transistors (FETs) due to the continuation of threshold and supply voltage scaling.[1] An alternative towards energy reduction being recently investigated is the use of polarity-controllable devices that have the ability of providing p- and n- type characteristics within the same device.[2,3] These have shown to be able to substantially reduce the transistor count and therefore power consumption in demanding applications, such as arithmetic circuits.[4,5] Recently, both TFETs and polarity-controllable FETs have been highlighted as being among the most promising device types for the potential use in hardware security.[6]

Polarity controlled (or reconfigurable) transistors, leading a novel device concept, are typically based on source and drain junctions containing Schottky-barriers (SBs).[2,3,7] The predominant charge carrier type (electrons or holes) in these polarity controllable transistors can be tuned electrostatically by an additional gate (so-called polarity gate (PG) or program gate), instead of using impurities of opposite type for each device polarity. This could provide a new paradigm of CMOS technology with dopant-free processing with reduced thermal budget.[8–10] It has been recently reported that SB Si-FinFETs with *Three-Independent Gates* (TIG) in addition to showing polarity control can deliver a very steep subthreshold swing (SS) ($SS = dV_g/d[\log(I_d)]$) of 6 mV/decade over five decades of drain current due to a positive feedback and weak impact-ionization.[11]

In this paper, the electrical properties and unique transport mechanism in SB Si-FinFETs with TIG for tuning the polarity of charge carriers were investigated in detail, through analysis of contour maps of drain current (I_d) and activation energy (E_a) considering different bias conditions of the three individual gates and drain. In addition, transconductance (g_m) behavior was compared to that of a conventional SB transistor configuration. This work provides novel information for a better understanding of the physical operation of SB Si-FinFETs with TIG for further development of practical applications including novel reconfigurable circuits with low power consumption.

II. EXPERIMENTAL PROCEDURES

For this study, the SB Si-FinFETs were fabricated on SOI wafers with 2 μm buried oxide (BOX) and a lightly p-type doped Si body of 340 nm thickness. Figure 1(a) displays a scanning electron microscopy (SEM) image and schematic view of the completed devices. The fins were patterned to be 40–60 nm wide and have a total length of 800 nm, which is sub-divided into three sequentially gated regions, each approximately 200 nm in length. The central gate is the *Control Gate* (CG) and the two neighboring gates coupling the source and drain junctions are the *Polarity Gates* (PG). The gate insulator consists of 15 nm thick

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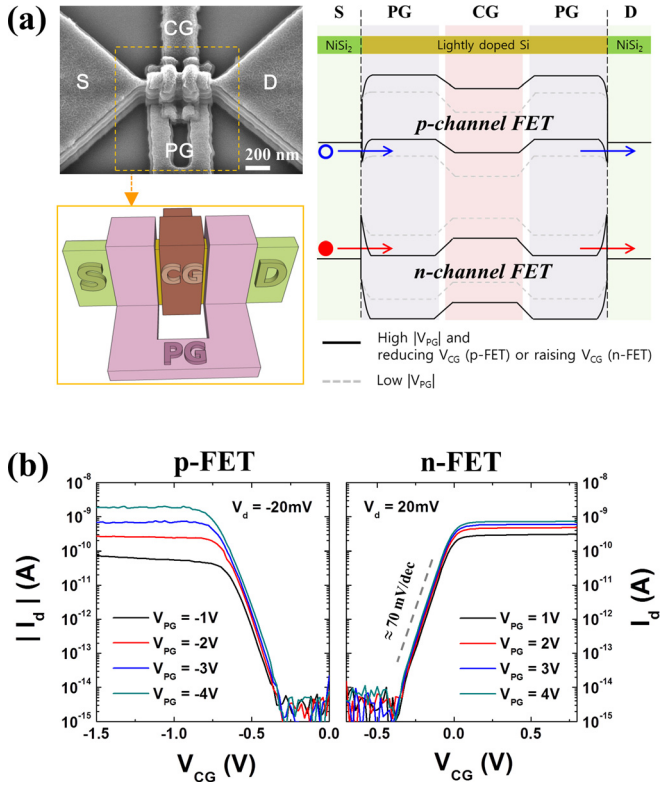

FIG. 1. (a) SEM image and schematic showing the completed SB Si-FinFETs (left), and the illustrated band diagram describing the unique reconfigurable operation principle with different V_{PG} and V_{CG} (right). (b) I_d vs. V_{CG} with varying V_{PG} representing both p-FET and n-FET reconfigurable operation in a single SB Si-FinFET.

thermal SiO_2. The source and drain contacts are silicided with Ni to become metallic Ni_xSi_{1-x} introducing Schottky junctions to the Si channel. Further details about the fabrication procedure have been described previously.[11] The I–V current-voltage characteristics were recorded at different temperatures (22 °C, 57 °C, and 92 °C) using an Agilent B1505A measurement unit.

III. RESULTS AND DISCUSSION

Figure 1(b) shows typical transfer curves with a small drain bias $|V_d| = 20$ mV showing both p-FET and n-FET operation of the SB Si-FinFETs, in a single physical device. With V_{PG}, the polarity of the transistor can be selected by tuning the effective SB width between Ni_xSi_{1-x} and Si simultaneously at both the source and drain. At the same time, V_{CG} modulates the potential barrier in the channel like gate of a conventional transistor as previously shown by De Marchi *et al.*[12] A positive V_{PG} results in a reduced SB width for electrons and thus raises the injection probability of electrons by tunneling through the thinned SB to the silicon conduction band.[13] Similarly, a negative V_{PG} induces the hole injection as a majority carrier with a thinned SB towards the silicon valence band. The band diagram illustrated in Fig. 1(a) describes the unique reconfigurable operation principle in the SB Si-FinFETs with different polarity gate and control gate voltage (V_{PG} and V_{CG}) conditions. The asymmetric trend between n-FET and p-FET on the I_d vs. V_{CG} according to varying $|V_{PG}|$, as shown in Fig. 1(b), is attributed to a higher SB height value for electrons (≈0.66 eV) vs. that for holes (≈0.46 eV) at the Schottky-junction as reported in Ref. 14 and as will be reconfirmed later.

Figure 2 shows a drain current contour map for a simpler understanding of carrier transport controlled by the parameters V_d, V_{CG}, and V_{PG} in the SB Si-FinFETs, as previously applied to Schottky FETs.[15] Different colors in the contour map denote the amplitude of $\log|I_d|$. For p-FET operation with a negative V_{PG} in Fig. 2(a), the holes dominate the overall operation of the device for small and moderate values of $|V_d|$. However, the electrons also start to be injected from the drain-side with a further increasing $|V_d|$. The hole dominated conduction regime, electron dominated conduction regime, and mixed regime of both carriers according to varying V_d, V_{CG}, and V_{PG} can be identified and are highlighted in Fig. 2(a) by the dotted white line in the contour map. Moreover, the horizontal dotted line, upon which the electron injection is dramatically raised, can be assumed to be the effective flat-band condition at the drain-side junction. One can also observe that the flat-band position moves from ≈−1.75 V ($V_{PG} = -2$ V) to ≈−3.75 V ($V_{PG} = -4$ V) as V_{PG} is lowered. In addition, a similar trend with opposite polarity of V_{CG} and V_d was investigated for n-FET operation with a positive V_{PG} as shown in Fig. 2(b). However, the dotted white border line distinguishing the electron conduction regime in the right contour map of Fig. 2(b) is not perpendicular to the V_{CG}-axis anymore, due to the change of threshold voltage presumably resulting from impact ionization at a higher V_{PG} and V_d. Next, this region is analyzed in more detail.

A steep SS below 60 mV/decade at room temperature (thermal limit) was observed at $V_d > 2.5$ V and $V_{PG} = 4$ V as shown in Fig. 3(a). The steep SS behavior can be explained by the following 3 factors as proposed in Ref. 11: (1) weak impact ionization generating electron/hole pairs; (2) a positive feedback with lowering the potential barrier under V_{CG} due to the accumulated holes; and (3) the further enhanced electron injection with thinning SB width caused by the generated holes at the source-side. Fig. 3(b) represents the contour map of the slope $= d[\log|I_d|]/dV_{CG}$ extracted from the transfer curves in Fig. 3(a). The contour map clearly shows a distribution of the slope values according to V_d and V_{CG} bias conditions. Moreover, one can easily define a specific bias regime, where the SS corresponds to a value of below 60 mV/decade. In the contour map of Fig. 3, this regime is coded by a red color.

Temperature dependent transfer curves were measured and the corresponding Arrhenius plot was used to extract the activation energy (E_a) for the different operation points in order to get a deeper insight into the carrier transport mechanism in the SB Si-FinFETs (see supplementary material). Figure 4(a) shows a contour map of E_a as a function of V_{CG} and V_d with $V_{PG} = -4$ V, i.e., for p-FET operation. The energies are determined for holes E_h having the source electrode as the reference, i.e., $V_s = 0$ V. As an example, for $V_d = -3$ V the activation energy is plotted vs. V_{CG} in Fig. 4(b). The schematic band diagram in Fig. 4(b) helps to describe the model proposed next. Two regions with different slopes can be

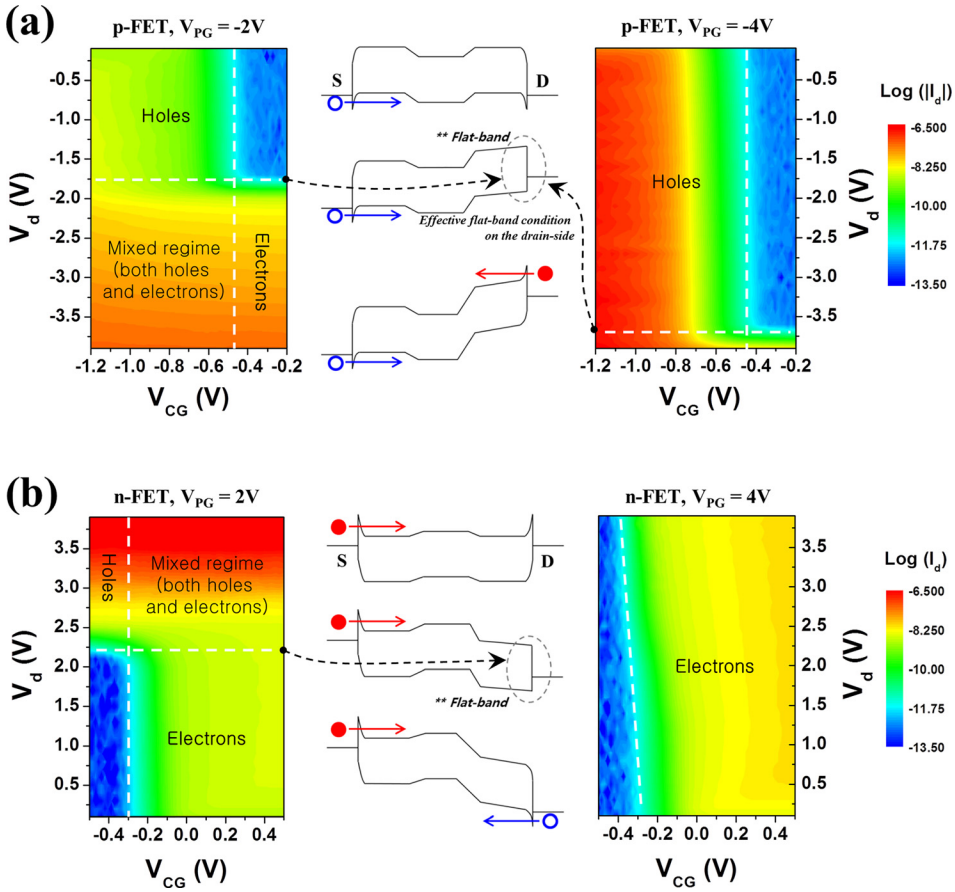

FIG. 2. Drain current contour map clearly showing carrier transport behavior controlled by V_d, V_{CG}, and V_{PG} in the SB Si-FinFETs for both (a) p-branch and (b) n-branch.

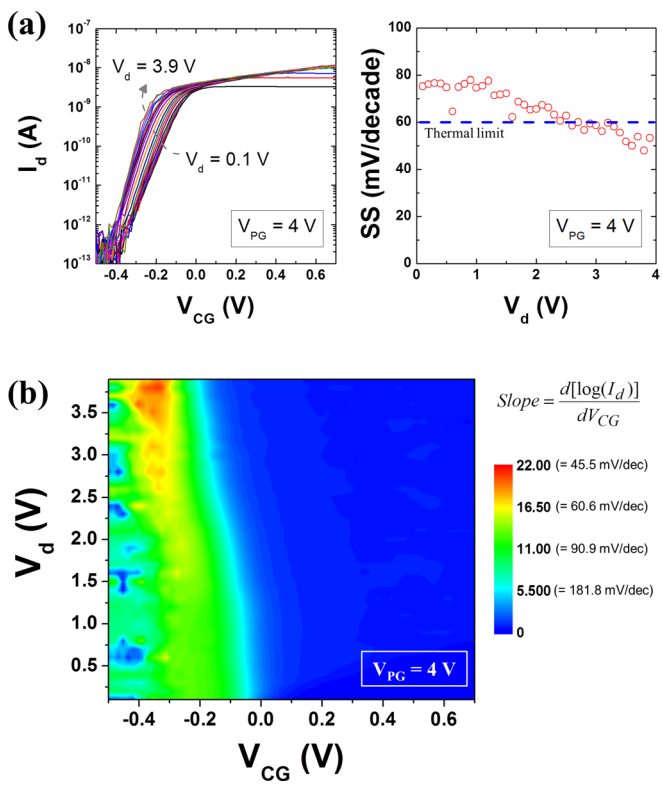

FIG. 3. (a) Transfer curves with varying V_d (left) and SS vs. V_d (right) for n-FET with $V_{PG} = 4$ V, a steep SS of below 60 mV/decade was observed at a higher V_d (>2.5 V), due to the effect from impact ionization induced positive feedback. (b) Subthreshold slope (=$d[\log(I_d)]/dV_{CG}$) contour map clearly showing a steep slope regime in red color.

identified and divided by a deflection point. First, from $V_{CG} = -0.4$ V to -0.8 V, E_a is controlled linearly by V_{CG} having a slope $d(E_a)/d(V_{CG})$ of unity as shown in Fig. 4(b). This describes a one-to-one movement of the energy bands by the control gate bias in the middle of the channel as can be seen from the solid purple potential lines in Fig. 4(b). Thus, it can be assumed that the junctions do not limit conductance here and that the switching mechanism is similar to that of conventional MOSFETs. For this particular situation, $d(E_a)/d(V_{CG})$ is equivalent to the well-known body factor m in conventional FETs, with $m \cong (1 + \frac{C_{dm}}{C_{ox}})$, where C_{dm} is the capacity associated with the depletion width maximum and C_{ox} the oxide capacitance of the control gate.[16,17] $m \approx 1$ is satisfied for $C_{ox} \gg C_{dm}$, showing the excellent gating condition of the fin body by the control gate. This is translated into a subthreshold swing SS close to the ideal value of

$$SS = \frac{dV_g}{d(\log_{10} I_d)} = \frac{dV_g}{d\phi_s} \times \frac{d\phi_s}{d(\log_{10} I_d)} \cong m \times \ln 10 \times \frac{kT}{q}, \text{ i.e., } 60\,\text{mV/dec at } 300\text{K}, \quad (1)$$

where ϕ_s is the surface potential of the channel. The second region in Fig. 4(b) is entered, when the barrier height E_a is smaller than 0.1 eV, which corresponds to a control gate voltage $V_{CG} \sim -0.8$ V. In this region, E_a is only weakly influenced by V_{CG}. As proposed in the schematic band diagram, the channel surface potential below the control gate ($q \cdot \phi_{min}$) becomes higher than the effective barrier for holes at the source Schottky junction. The limiting transport mechanism is

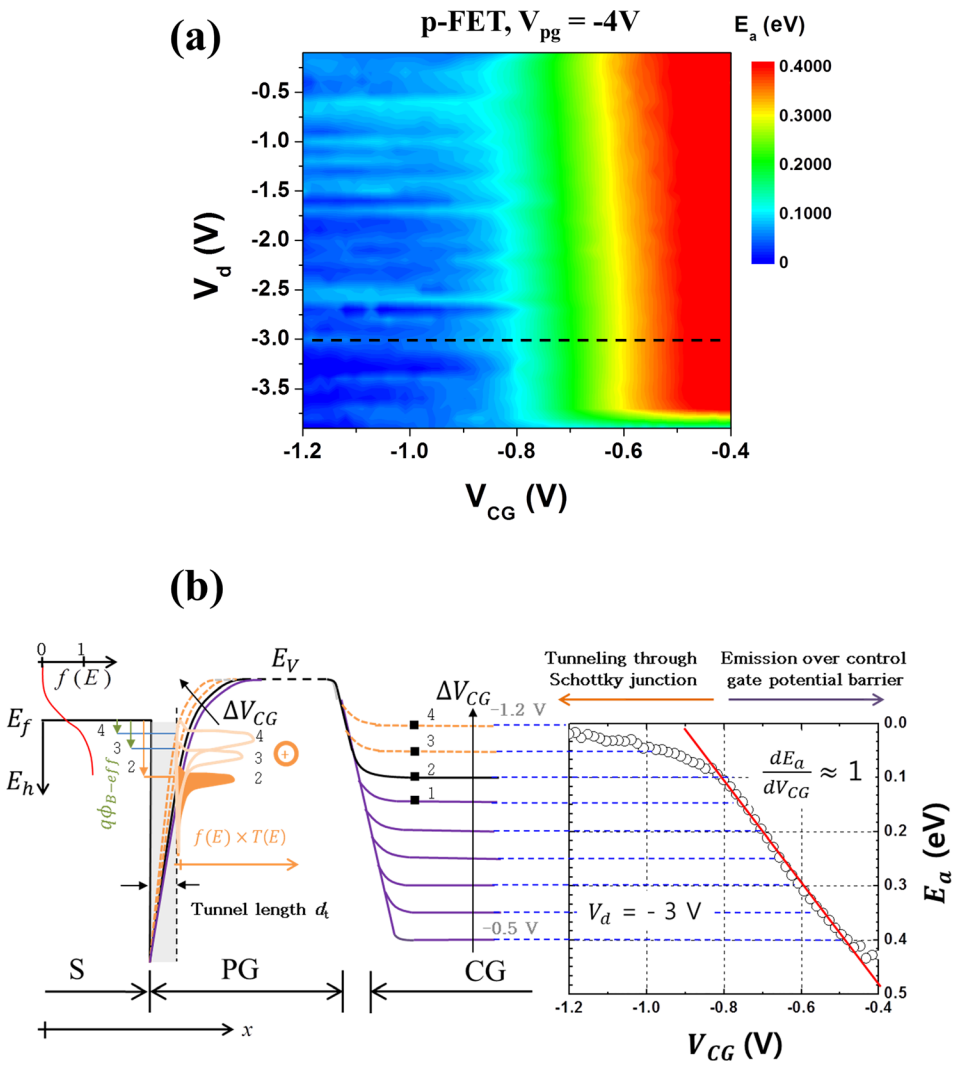

FIG. 4. Activation energy E_a contour map as a function of V_{CG} and V_d with (a) $V_{PG} = -4$ V for p-FET. The activation energy was extracted by temperature dependent transfer curves and Arrhenius plots for an in-depth study with respect to carrier transport mechanism in the devices. (b) E_a vs. V_{CG} with $V_d = -3$ V and illustration of corresponding energy band profile.

thus thermally assisted tunneling into the valence band E_v through a thinned and triangularly shaped energy barrier. Note this is a realistic assumption for the low doping level of the Si fin. See the dashed orange line in Fig. 4(b). The total hole injection current density J through the barrier is given by the energy dependent Fermi Dirac distribution $f(E)$ at the source electrode and the tunneling probability $T_t(E)$ assuming a constant density of states in the metal and constant unoccupied states in the semiconductor[18]

$$J = \int_{E_F}^{E} f(E,T)T_t(E)dE. \tag{2}$$

Following the Wentzel-Kramers-Brillouin (WKB) approximation for a triangular barrier, the tunneling probability is:

$$T_t(E,\varepsilon) \sim \exp\left[-\frac{K(q\cdot\phi_B - E)^{3/2}}{q\varepsilon}\right], \tag{3}$$

where K is a constant and ε is the electric-field across the junction. Fig. 4(b) schematically shows the product $f(E,T) \times T_t(E)$ and associated integral of Equation (2).

The activation energy where tunneling dominates can still be tuned with V_{CG}, down to a value of ≈0.02 eV. This is attributed to the effect of fringing fields from the control gate electrode penetrating into the V_{PG} gated Si region. Following the simplification introduced by Knoch *et al.*, for Schottky-FETs in Ref. 19, the activation energy E_a in the tunneling-limited regime can be associated with an effective SB height $q\cdot\phi_{B\text{-eff}}$ upon which the tunneling probability approaches unity. This is assumed when the typical barrier thickness in Si is equal to or thinner than the tunneling distance (d_t) in Si, see the grey region in Fig. 4(b). Excluding substantial energy losses within the first gated region, the injected charge carriers have sufficient energy to surpass the potential energy at the control gate thus resulting in a drain current, since $q\cdot\phi_{min} < q\cdot\phi_{B\text{-eff}}$. (Conversely, as the gate length is comparatively long the fringing fields of V_{PG} do not affect the minimum barrier height $q\cdot\phi_{min}$ in the control gate region.) Interestingly, the deflection does not have a strong dependence on V_d as seen in the map of Fig. 4(a). This is attributed to the strong capacitive coupling of the program gate in the tri-gate structures.

The E_a contour map for the n-FET operation with $V_{PG} = 4$ V is shown in Fig. 5(a). In contrast to the p-type operation, one can find a valley shape in the E_a contour map of

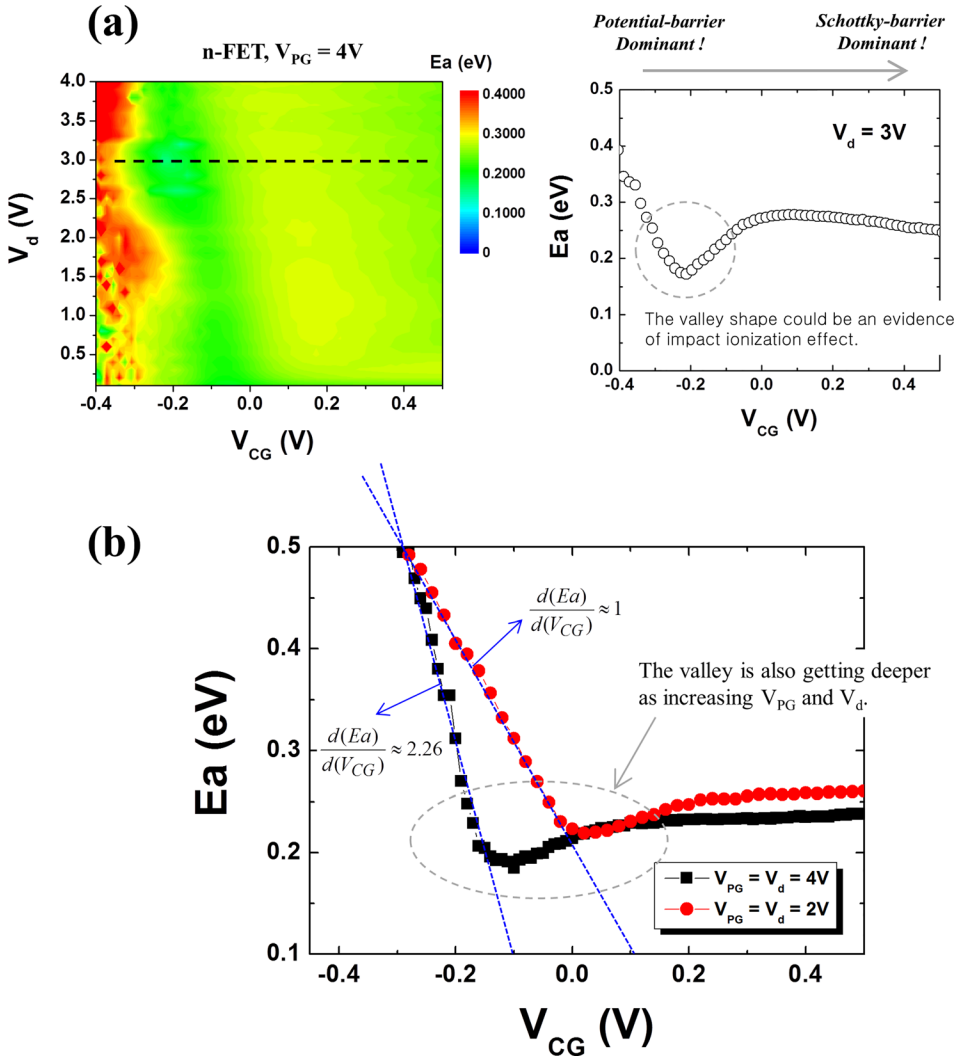

FIG. 5. (a) E_a contour maps as a function of V_{CG} and V_d with $V_{PG} = 4$ V for n-FET. (b) E_a vs. V_{CG} for $V_{PG} = V_d = 2$ V and $V_{PG} = V_d = 4$ V. A deeper valley shape with $d(E_a)/d(V_{CG}) > 1$ could be induced by the enhanced impact ionization effect at a higher V_{PG} and V_d.

Fig. 5(a). The valley shape is a result of competing transport mechanisms. To understand the different regimes in n-type operation, Fig. 5(b) depicts extracted E_a vs. V_{CG} plots for two different cases namely, $V_{PG} = V_d = 4$ V and $V_{PG} = V_d = 2$ V. For comparatively low voltages $V_{PG} = V_d = 2$ V, the switching mechanism is similar to the p-case. From $V_{CG} = 0$ V to -0.3 V, the slope $d(E_a)/d(V_{CG})$ is about 1 consistent with the thermionic emission over the control gate barrier. However, for $V_{PG} = V_d = 4$ V, the efficiency of moving the control barrier by V_{CG} is boosted by a factor of about 2.26. This is the result of a positive feedback effect. As proposed in Refs. 11 and 20, the high channel fields between the middle gated region and the drain bounded gated region induce weak impact ionization of electrons. The generated holes accumulate at the potential pit under the control gate giving the observed positive feedback and steep subthreshold slope. The generation of free charge carriers by weak impact ionization also implies a substantial amplification effect on the term $\frac{d(\log_{10} I_d)}{d\phi_S}$ within Equation (1), surpassing the value of $q/(kT \times \ln 10)$. This further contributes to a steep subthreshold slope behavior. It should also be noted that the generation current by impact ionization has an inverse temperature dependence as compared to thermionic emission,[21] principally contributing to a lower E_a for a fixed V_{CG}. Nevertheless, in a temperature series it is difficult to decouple both effects from each other, since the injection current initiating impact ionization is thermally activated through the described thermally assisted tunneling at the source Schottky junction and subsequent thermionic emission of electrons above the control gate potential barrier. Further, we focus on the E_a valley in Fig. 5(b). As the bands below the control gate are lowered by increasing V_{CG}, the substantial amount of accumulated holes can be emitted over the source-sided energy barrier, rather than over the higher drain-sided barrier. This effect is expected to reduce the channel potential at the source sided junction thinning down the SB for electron injection and thus leading to a lower effective barrier height $q \cdot \phi_{B\text{-}eff}$ for electrons and therefore enhanced electron current. As holes are depleted and electrons are injected at the source junction, $q \cdot \phi_{B\text{-}eff}$ ($V_{CG} > -0.1$ V) rises again. A deeper valley on the E_a behavior is observed in Fig. 5(b) with a higher $|V_d|$ and $|V_{PG}|$ possibly owing to an enhanced impact ionization rate and related higher hole concentration. In the on-state, E_a remains fairly constant in contrast to the p- program case in Fig. 4. This can be an effect of the larger SB height of electrons vs. holes. As a result, it is more difficult to tune its transparency with the fringing fields of V_{CG}.

Next, the electrical properties of the SB Si-FinFETs were compared to those in a typical configuration of the SB transistor, in terms of transconductance g_m behavior as

shown in Fig. 6. The operation of a conventional SB transistor is possible if the PG and CG in the SB Si-FinFETs are connected together as shown in the illustration of Fig. 6(b). It is well known that g_m of conventional SB transistors is not degraded even at a high gate bias, since carrier injection is also increased through the progressively reduced SB width with raising gate bias.[22] That is why the g_m in Fig. 6(b) is continually rising. However, the SB Si-FinFETs with the separated V_{PG} show a peak and then degradation behavior of g_m as shown in Fig. 6(a). This feature can be explained by a relatively pinned carrier injection related to the nearly fixed SB width with a given V_{PG}. The carrier injection rate is already determined by the fixed SB with $V_{PG} = -4$ V. Therefore, a mobility degradation and series resistance at contacts with the fixed carrier injection rate can cause the degradation of g_m in the SB Si-FinFETs, like in a conventional MOSFET with highly doped source/drain regions.

Finally, some prospects towards optimizing the SB steep slope Si-FinFETs are given. For a simple implementation of the device in the steep slope mode, all supply voltages have to be reduced. It is known that the minimum energy required for igniting impact ionization is 1.5 times of the band gap E_g.[23,24] For Si channels, this implies a minimal V_d of $\approx$1.68 V. In addition, steep slope behavior would be required for both n- and p- type devices. The potential use of low band gap $Si_xGe_{(1-x)}$ as well as Ge channels and a PN-body tied structure in SOI based FETs could help to reduce V_d.[25,26] It could also allow steep slope operation for the p- operation, since the impact ionization coefficients for holes α_p are not only substantially higher than in Si but also closer to the ionization coefficients for electrons α_n in $Si_xGe_{(1-x)}$ and Ge material.[27,28] Also the on-currents would be enhanced, as lower SB heights can be obtained. In turn, the leakage currents would increase but they can be principally managed by the choice of an appropriate program gate bias V_{PG}.

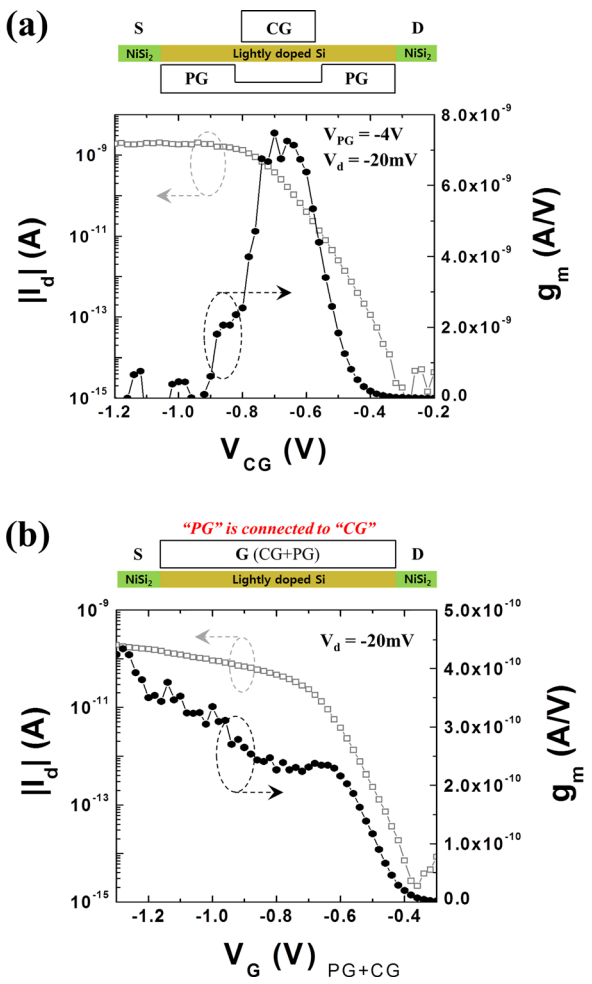

FIG. 6. Transconductance g_m as a function of control gate bias in both (a) SB Si-FinFETs with the separated PG and (b) a conventional SB transistor configuration with connecting CG and PG as shown in the illustration.

IV. CONCLUSIONS

Electrical properties and operation regimes of polarity tunable and steep slope Si-FinFETs were discussed in detail. Drain current and subthreshold slope contour maps clearly showed the hole or electron dominant conduction regime and mixed regime of both carriers according to varying V_d, V_{CG}, and V_{PG} bias conditions. The effective flat-band position on the drain-side can also be estimated from the specific point where the injection of the opposite type of carrier is dramatically increased in the drain current contour map. In addition, an activation energy contour map elucidates the different transport regimes differentiating the individual contribution of thermionic emission, thermally assisted tunneling through the Schottky-barrier (SB), positive feedback effect, and weak impact ionization. The understanding of the involved carrier transport mechanisms and the boundaries between these helps to design future SB Si-FinFET devices for potential multifunctional logic and steep slope operations.

SUPPLEMENTARY MATERIAL

See supplementary material for extraction of activation energy and temperature dependent transfer curves with different bias.

ACKNOWLEDGMENTS

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