Spintronic majority gates

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***Abstract*—In this paper we present an overview of two types of majority gate devices based on spintronic phenomena. We compare the spin torque majority gate and the spin wave majority gate and describe work on these devices. We discuss operating conditions for the two device concepts, circuit implication and how these reflect on materials choices for device implementation.**

I. Introduction

Beyond CMOS devices are being intensively studied to expand functionally for future technology nodes. Amongst the Beyond CMOS devices, those based on spintronic effects are very interesting for logic applications as they can provide new functionality. Spintronic logic devices can enable a) non-volatility; b) ultra-low power operation; and c) improved circuit efficiency [1]. Spin logic devices are particularly amenable to building majority gates which in their turn could improve efficiency of certain circuits by reducing circuit complexity. In this paper, we focus on majority gates as they are one of the key devices that could revolutionize circuit design [2]. Majority gates are devices that can have a large number of inputs, a large number of outputs and a certain number of control gates. The simplest majority gates, like those described here, have 3 inputs and one output.

The truth table of the simplest majority gate is shown in Table 1. Unlike NAND based logic where only one logical operation type is needed, to build universal logic with majority gates, inverters are also required. Several proposals for spintronic majority gates exist. Here we focus on and compare spin torque majority gates (STMG) and spin wave majority gates (SWMG) and summarize our work on these concepts.

Majority Logic Gate			
Input 1	*Input 2*	*Input 3*	*Output*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 1: Truth table of a 3 input 1 output majority gate.

STMG (Fig. 1) rely on the propagation and interaction of magnetic domain walls. Domain walls are interfaces separating regions with different magnetization direction. SWMG (Fig. 2) rely on propagation and interference of spin waves. Spin waves are low-energy collective excitations in magnetic materials. They are also known as magnons.

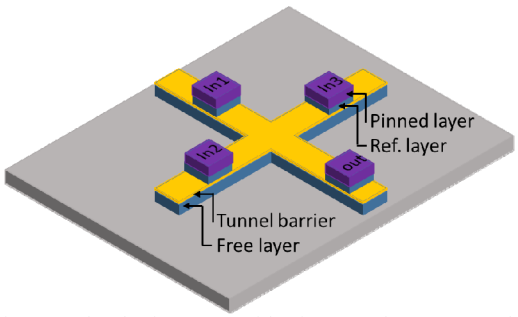

Figure 1: Sketch of a STMG with 3 inputs and one output. The device has 4 magnetic tunnel junctions sharing a common free layer.

See table 2 for a comparison of STMG and SWMG. It is important to note that for neither STMG nor SWMG full experimental demonstrations exist in literature. However, several building blocks exist. Here we detail our work towards fabricating and understanding these devices.

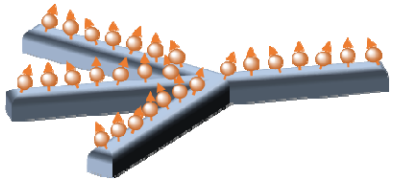

Figure 2: Sketch of a spin wave majority gate with 3 inputs and one output. The waves propagating in the 3 input arms interfere in the central region to perform the computation.

Majority gates employing interference of other waves such as plasmons and phonons have been proposed but they are beyond the scope of this article. Majority gates based on different spintronics concepts have also been proposed. Amongst those, all spin logic [3] using nanomagnets with in-plane magnetization that communicate via spin coherent

	Spin torque majority gate	Spin wave majority gates
Physics principle	Domain wall motion/ exchange	Interference of spin waves
Write	Spin transfer torque/ MTJ	Magnetoelectric element
Read	Tunnel magneto-resistance	Magnetoelectric element
Non-volatile	Could be	Could be
scalability	scalable	not clear how far
multiplexing	Unlikely	Proposals exist
Inverter	Proposal exists but difficult	Proposals exist
Cascading	Non-trivial	Proposals exist
Materials	Comparable to MRAM	Piezoelectrics and magnetostrictives
Experimental demo	N/A	Full demo not available but components in [10] and [11]

Table 2: Comparison of STMG and SWMG. Note that full experimental demonstrations are still lacking for both.

currents is one of the most investigated ones. STMG is using instead magnetic materials with perpendicular magnetization as it is expected to be more energy efficient.

II. Spin Torque Majority Gates

The STMG concept was proposed in Ref. [4]. A sketch of the device is shown in Fig. 1. It consists of a cross-shaped free layer common to 4 magnetic tunnel junctions (MTJs). The state variable is the magnetization in the free layer and it can be written via spin transfer torque (STT) provided by the current applied through the MTJ. The output is measured via tunneling magnetoresistance (TMR). STMG has the marked advantage compared to SWMD that uses the same materials as those for magnetic RAM (MRAM). Thus it is expected that their experimental implementation is easier by comparison.

The STMG promises to be area scalable and non-volatile. However, the existing proposals for inverters [5] are difficult to produce experimentally. Cascading these devices is also non-trivial but proposals exist [5].

We use micromagnetic simulations to validate device function and understand possible failure modes. In the analysis below, we assume perpendicular magnetic anisotropy.

Fig. 3 shows one of the most difficult input conditions: two inputs are in the magnetization down state while the third one is in the magnetization up state. The expected state at the output is magnetization down (Fig. 3b), however, if the current applied or the pulse length are not long enough, the device fails to switch (Fig. 3c).

Based on micromagnetic simulations, we observe that there is a critical current density below which the devices do not switch. This current varies with the input combination and it is found to be highest for the configuration depicted in Fig. 3a. This critical switching current is consistent with that for STT and increases with decreasing applied pulse time approximately as $(I-I_c)*T_{sw}$=const. See Fig. 4 for the threshold current dependence on pulse length for magnetic parameters of standard MRAM materials. Note the relatively high current needed for these devices to switch, which results in relatively high operation energy. Voltage induced switching would improve energy projections for the STMG.

Even if the applied current pulses provides enough energy to switch the area under the tunnel junctions, other failure modes can appear. Most common one is the majority domain wall becoming stuck at the crossing or in one of the arms. See Fig. 3d for a sketch of this failure mode. In general, this failure mechanism takes place if the width of the cross exceeds a certain value. We find that this value increases linearly with

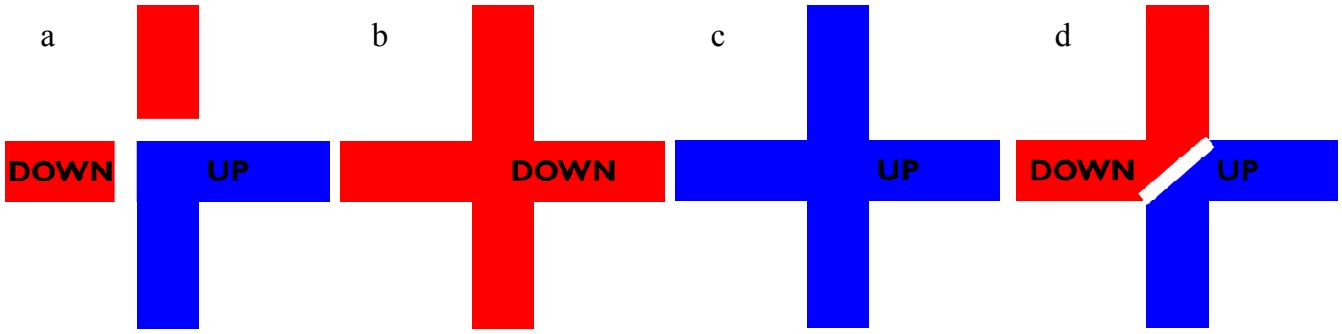

Figure 3: STMG. The left, up and down arms are inputs, while the right one is output. Sketch based on micromagnetic simulations of: **a**. initial state of the device after the write operation. Two arms are put in the magnetization down, one is put in the magnetization up state. Note the magnetic domain walls forming. The output arm has not switched state yet. **b**. expected outcome after computation when the domain walls have merged. **c**. Failure mode if the inputs do not provide enough energy. **d**. failure mode where the domain wall formed becomes "stuck" at the crossing.

increasing effective anisotropy (see Fig. 5). For typical anisotropy values this critical size is as low as 15-20nm, which makes these devices difficult to demonstrate experimentally. Different device geometry could increase device CDs.

In addition to the challenges of patterning devices with small size and tight pitch between the MTJs, the device fabrication requires a very challenging etch of the magnetic

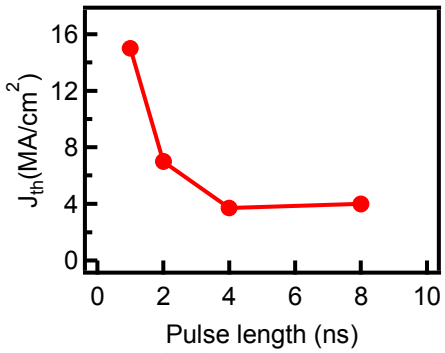

Fig. 4: STMG. Typical threshold current density vs. applied pulse length for the device to switch. Note the relatively high currents needed for these devices, which results in relatively high operation energy/power. Voltage induced magnetic switching would improve energy projections.

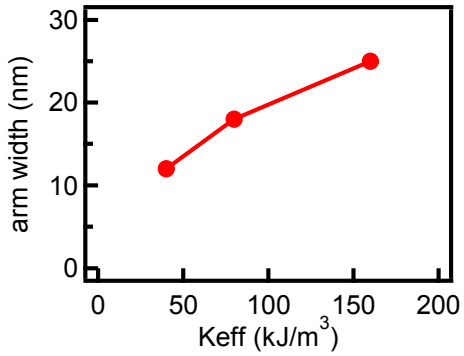

Fig. 5: STMG. Device arm width vs. effective anisotropy. Above this arm width, the failure mechanism where the domain wall becomes stuck is dominant. For K_{eff} in agreement with standard MRAM stacks, the arm width has to be lower than ~15-25nm for proper device function. Different device geometry could increase device CDs.

stack stopping at the tunnel barrier. The tunnel barrier has to be intact over the whole body of the device to prevent loss of perpendicular magnetization in the common free layer. Fig.6 shows a TEM cross-section of such layers with the bright layer being the tunnel barrier. The darker layers above are remnants of the reference layer which was not completely removed. Ongoing work is focused on developing the processes needed for device fabrication. Several routes are being investigated for this challenging etch process. One route is targeting stopping at or in the tunnel barrier layer, a very challenging task as this is a less than 2 nm thin layer. A second route is investigating dynamic etching and chemical modification of the fixed magnet above the tunnel barrier. Insets in Fig 6 show further examples for developments of patterning of MTJs and free layer towards full STMG device demonstration.

In addition to the process development needed for device demonstration, improvement in the energy needed to operate

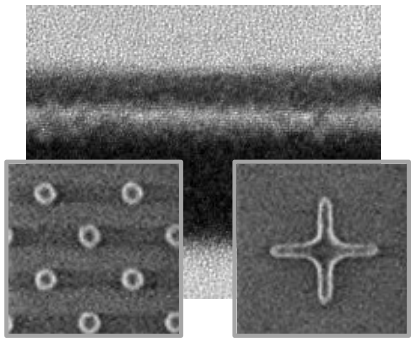

Fig. 6: STMG. TEM cross-section of etch stopping close to the tunnel barrier interface. Insets are top-view SEM pictures of the MTJ pillars and the cross-shaped free layer. All developments are performed on 300mm wafers in the imec fab.

these devices is required. Such improvement could come from different physics governing the magnetic switching.

III. Spin Wave Majority Gate

The SWMG has been investigated intensively and proposals how to handle the computation exist [6]. The information can be encoded in either the amplitude or the phase of the spin wave [7]. By their nature, these devices may allow frequency multiplexing if non-linear dispersion can be mitigated.

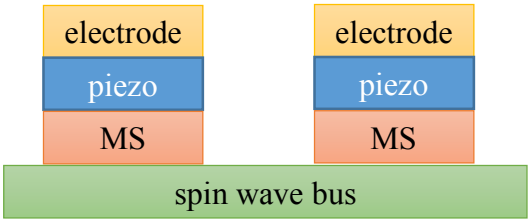

Fig. 7. SWMG. Schematic representation of magnetoelectric elements (ME) on a spin wave bus. The ME consists of a piezoelectric which converts applied voltage to deformation and a magnetostrictive material which converts mechanical deformation to change in magnetization. The MEs are both input and output devices.

Unlike STMG, where the conversion from charge domain is done via STT and thus current driven, for SWMG the conversion is done via the multiferroic effect and voltage driven. The input and output devices for SWMG are magneto-electric cells (ME). The conversion from the voltage domain to the spin wave domain is performed via a synthetic hybrid multiferroic material which consists of a piezoelectric material and a magnetostrictive material, as depicted in Fig. 7. The energy carried by spin waves is very low (~ 20-40 kT), so two strategies exist to enable magnetization switching by the spin wave. 1) Extra energy is provided by an external circuit such as a clocking circuit [8]. 2) As used further in this paper, canted magnetization states are implemented in the ME (see Fig. 8 for a vector depiction), allowing for a strong interaction due to the nature of magnetic torque ($\mathbf{m}_{out}X\mathbf{H}_{sw}$). Thus the energy

provided by the incoming spin wave is sufficient to toggle the state of the ME.

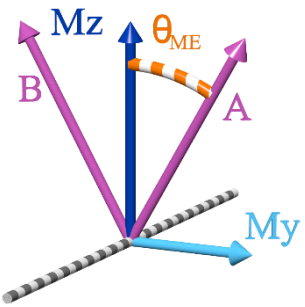

Fig. 7: SWMG. Vector representation of the magnetization in the magnetostrictive material. To allow for incoming spin waves to switch the state of magnetization, canted states are used, rather than change of vector angle by 180°

	Majority gate	Inverter
Area (μm^2)	0.03456	0.006912
Delay (ns)	0.42	0.42
Energy (J)	4.33E-23	1.44E-23

Table. 7: SWMG. Circuit component specification for spin wave devices.

Since the SWMGs employ conversion to and from the charge domain by voltage control, they are expected to be more energy efficient than STMG. By using micro-magnetic modeling for the spin wave propagation and the magnetic behavior of the ME and combining it with majority-based circuit synthesis, we benchmark spin wave technology with CMOS circuits. Basic device assumptions for spin waves are listed in Table 3. Calculations include sense amplifiers as detailed in [9]. We find that the spin wave circuits take on average 3.5 times less area and about 400 times lower power that the equivalent circuit in CMOS. However, the spin wave circuits are on average 12 times slower. According to [1] STMG circuits have about 10x smaller area and use about 5x lower power than CMOS. However, the very long delays associated with these circuits make them less efficient than equivalent CMOS. This is in contrast to SWMG and likely can be explained by the fact that in STMG the switching is current controlled, while for SWMG it is voltage controlled.

We have presented here a comparison of two types of spintronic majority gates and highlighted their challenges. We find that magnetoelectric spin wave devices could have a large power reduction compared with CMOS, however the materials required (magneto- and piezo-electric materials) are very different than current technology. Spin torque majority gates are technology friendly from a materials standpoint; however, further advances are needed to improve their performance. We also touch upon our work to demonstrate experimentally these devices.

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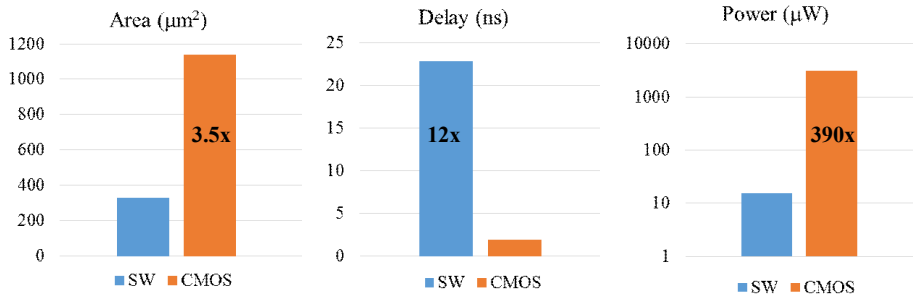

Fig. 8. SWMG. Comparison of area, delay and power for circuits synthesized with spin wave majority gate and CMOS N10. Graphs represent aggregate improvement over 10 large circuits benchmarks. The circuit benchmarks included here are: 2-operand 64-bit Brent-Kung Adder, 4-operand 64-bit Han-Carlson Adder, 4-operand 64-bit Carry-Skip Adder, 2-operand 32-bit Dadda tree Multiplier, 2-operand 32-bit Wallace tree Multiplier, 2-operand 64-bit Dadda tree Multiplier, Mastrovito multiplier for irreducible polynomial: x^17+x^8+x^3+x^1+1, 3-operand 32-bit (7,3) counter tree MAC, 2-operand 32-bit Divider, Cyclic redundancy check XOR tree used in Ethernet. The spin wave devices are slow, however, aggregate ~400x reduction in power compared to CMOS is expected.