Towards Functionality-Enhanced Devices: Controlling the Modes of Operation in Three-Independent-Gate Transistors

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***Abstract*— In this paper, we introduce the different modes of operation achievable with *Three-Independent-Gate Field-Effect Transistors* (TIGFETs) and report results on fabricated devices including: (i) the dynamic reconfiguration of the device polarity; (ii) the dynamic control of the threshold voltage; and (iii) the dynamic control of the subthreshold slope.**

I. Introduction

As the semiconductor industry is approaching the ultimate limits of conventional silicon-based transistors, researchers are focusing their efforts to identify possible approaches that will enable the continuation of Moore's scaling laws. In parallel to the focus on scaling, an interesting approach consists in increasing the functionalities of individual devices [1]–[6].

In this paper, we review the different modes of operations enabled by *Three-Independent-Gate Field-Effect Transistors* (TIGFETs). We report on fabricated Schottky-barrier FET transistors featuring three independent gate-all-around electrodes. The two gate electrodes in proximity to the source and drain Schottky contacts are used to dynamically modulate the barrier heights and tune the operation of the transistor, while the third gate electrode, acting on the center region of the channel, serves as standard gate. The additional gate terminals bring extended functionalities to the device such as (i) the dynamic reconfiguration of the polarity (*n*- or *p*-type) [4]; (ii) the dynamic control of the threshold voltage (V_T) that does not lead to any detriment of the *on*-state current [5]; and (iii) the dynamic control of the *Subthreshold Slope* (SS) allowing to trigger weak impact ionization and record an average SS of 6 mV/dec over 5 decades of current swings [6]. Devices with an enhanced set of functionalities are expected to extend the envelope of computation performance with high regularity and compactness, beyond the limits of scaling [7].

II. Three-Independent-Gate Device Overview

Fig. 1-a shows the structure of a TIGFET. The device exploits vertically-stacked nanowires as channel and metallic source and drain contacts. The channel electrostatics is controlled by three electrodes: The *Polarity Gate at Source* (PG_S) and the *Polarity Gate at Drain* (PG_D) modulate the Schottky barriers at source and drain; The *Control Gate* (CG) controls the potential barrier in the channel.

The TIGFET is fabricated with a dopant-free process on an SOI wafer [4]–[6]. The vertically-stacked nanowires are realized using a single *Deep Reactive Ion Etching* step [4]. Fig. 1-b shows an SEM image of the resulting silicon nanowire stack (length and diameter of 350 nm and 50 nm, respectively). After a 15 nm SiO_2 gate dielectric formation, two *Gate-All-Around* (GAA) 120 nm polysilicon structures are deposited to form PG_S/PG_D and CG is subsequently self-aligned to them. Finally, NiSi silicide is formed on the source and drain pillars to create mid-gap Schottky barriers. Fig. 1-c and Fig. 1-d show a top SEM image and a cross-sectional view of the final structure.

III. Modes of Operations

In a TIGFET, the control of carrier injection at the Schottky barriers by the PGs offers the capability to determine the operation modes of the device. In this section, we report on three different control mechanisms.

A. Polarity Control

In this case, we assume that the PG_S and PG_D terminals are connected together in a unique terminal called PG. Fig. 1-e presents a conceptual band diagram, showing the carriers involved in the device operation at different CG and PG biases. A positive PG bias enables electron conduction at the source and drain Schottky barriers, setting the device polarity to *n*-type, while a low PG bias leads to hole conduction and results in *p*-type behavior.

Polarity control on a fabricated device is observed in Fig. 1-f, where an increasing PG bias switches the device polarity from *p*- to *n*-type. I_{on}/I_{off} values ranging from 10^6 to 10^7 and subthreshold slopes of 64 mV/dec and 70 mV/dec were obtained, respectively, for the *p*- and *n*-branches in the same physical device [4].

B. Threshold Control

In this second case, the two PG terminals are biased separately. The independent Schottky biasing enables an efficient V_T control. Fig. 1-g and Fig. 1-h present the associated band diagrams for an *n*-type conduction.

Low-V_T *n*-type modes (Fig. 1-g) are similar to III-A. High-V_T *n*-type modes (Fig. 1-h) are obtained when PG_D=`1`, CG=`1` and PG_S controls the current flow. In the high-V_T *off* state, the opposite band bending at the Schottky contacts prevents both electron and hole injection into the channel. Note that the low-V_T and high-V_T configurations share the same *on* state, reducing performance degradation.

The performances obtained on a fabricated device are shown in Fig. 1-i. A threshold difference of 0.86 V is observed. The high-V_T *off*-state current reaches 1 pA compared to 4.6 pA

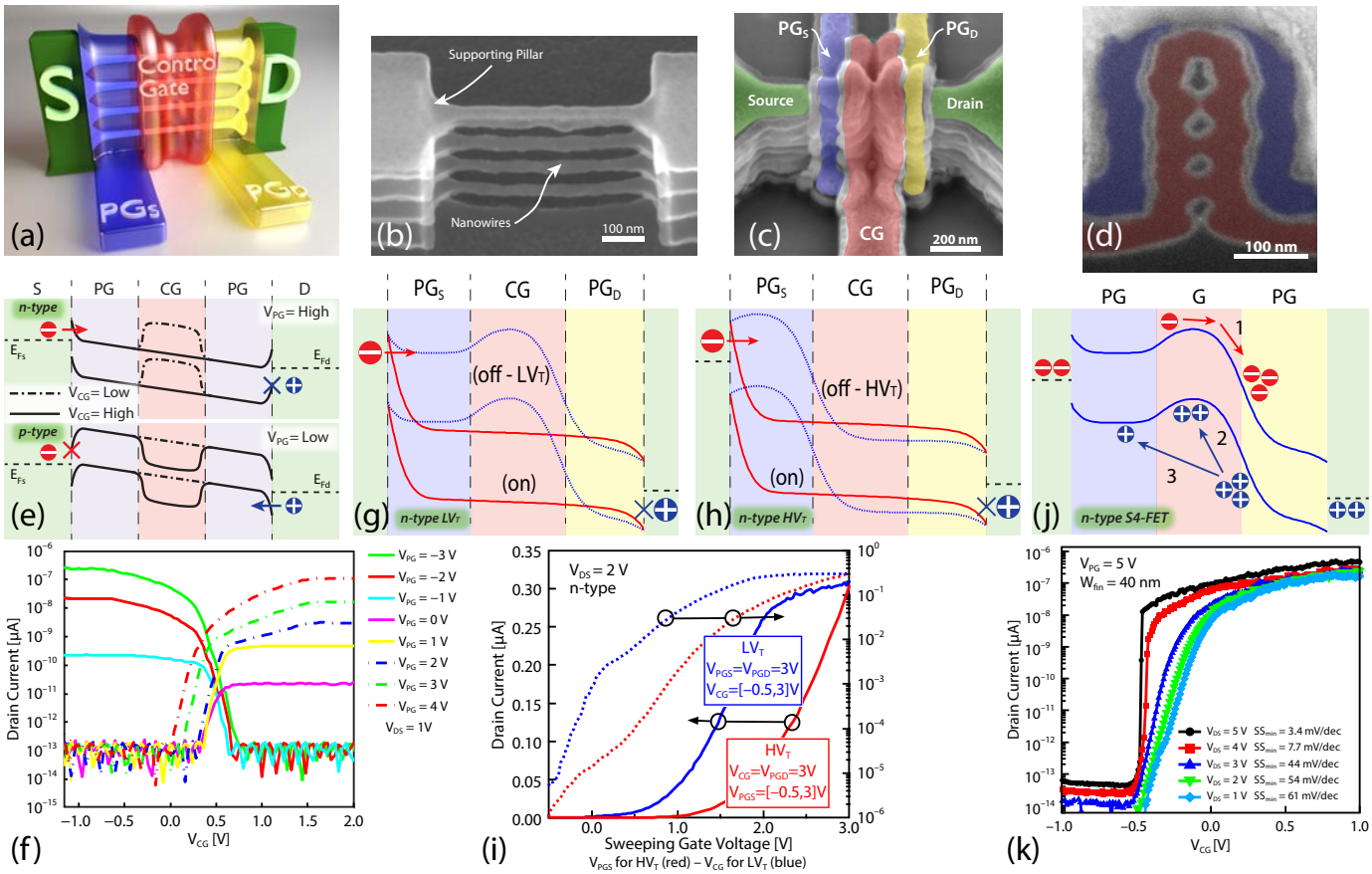

Fig. 1. **Device fabrication:** (a) Conceptual sketch of a TIGFET. (b) Tilted SEM image of the fabricated vertically-stacked nanowire channel. (c) Tilted SEM image of the fabricated TIGFETs. (d) Cross-sectional SEM of the device at the overlapped CG and PG_S region. **Polarity control:** (e) Conceptual band diagrams of the device in the polarity control mode. Four cases are shown according the four combinations of high/low bias applied on the PG and CG terminals. Electron paths are shown with red arrows/crosses. Hole paths are shown with blue arrows/crosses. (f) Logarithmic I_D-V_{CG} plot of the fabricated device at different V_{PG} biases. **Threshold control:** (g-h) Conceptual band diagrams of the device in the threshold control mode. Only *n*-type conditions are represented. Three combinations of (PG_S,CG,PG_D) are shown reflecting the *on* (1,1,1), the LV_T *off* (1,0,1) and the HV_T *off* (0,1,1) *n*-type states. (i) Measured linear and logarithmic I_D-V_{CG} *n*-type transfer characteristic showing the different V_T conditions. **Steep subthreshold control:** (j) Conceptual band diagrams of the device in the S4-FET configuration, illustrating the mechanism of the impact-ionization-induced positive feedback during the *on*-transition in the *n*-type configuration. (k) Logarithmic I_D-V_{CG} plot of the fabricated S4-FET device at different V_{DS} biases.

in low-V_T. Full characterization of *n*- and *p*-branches can be found in [5].

C. Steep Slope Control

In this third mode of operation, the two PGs are controlled together similarly to III-A. Here, we use the PGs to create a potential well under the gate and obtain a *Super-Steep Subthreshold Slope* device (S4-FET) [6]. The operation in *n*-type configuration is illustrated in Fig. 1-j. When electrons acquire enough energy, weak impact ionization is triggered and electron/hole pairs are generated (step 1). The generated holes accumulate in the potential well under the gate (step 2). This lowers the barrier and provides more electrons for impact ionization, thus establishing a positive feedback. During the transition, the energy band in the PG region is lowered (step 3), maintaining the potential well for the accumulation and improving the average SS over the subthreshold region.

Fig. 1-k shows the characteristics of the fabricated S4-FET [6]. Minimum SS of 3.4 mV/dec is achieved. An average SS of 6.0 mV/dec is observed for 5 decades of current. When decreasing V_{DS}, the impact ionization rate decreases, and the SS gradually degrades to 61 mV/dec at $V_{DS} = 1V$. Complete *n*-type and *p*-type characteristics are available in [6].

IV. Conclusions

In this paper, we reported on the different modes of operation achievable in TIGFETs. Polarity, V_T and steep subthreshold controls were demonstrated in fabricated devices showing a viable additional path to Moore's law for beyond-CMOS computing.

Acknowledgements

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