Heterogeneous Integration of ReRAM crossbars in a CMOS foundry chip

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Keywords: ReRAM, post-processing, crossbar

Resistive Random Access Memories (ReRAMs) are one of the most promising candidates to replace flash memories due to fast access speed, low voltage operation, simple structure and compatibility with current CMOS technology. Besides stand-alone memories [1], ReRAMs are a fundamental building block for applications such as neuromorphic circuits [2] and future generation FPGAs [3]. In this paper, we present a heterogeneous integration of ReRAMs with standard CMOS technology by post-processing the *Back-End-Of-the-Line* (BEOL) of fully finished CMOS chips.
The ReRAM device functionality is based on a solid-state redox process induced by oxygen migration creating conductive filamentary paths in an insulator material [4]. The reversibility of this process allows a hysteretic resistance that can be used as memory element, switching between a *High Resistance State* (HRS) and a *Low Resistance State* (LRS). We define as SET voltage the voltage needed to switch from the HRS to the LRS and corresponding to the creation of the conductive filaments. Similarly we define as RESET voltage the one to switch from the LRS to the HRS corresponding to the partial destruction of the filaments. In the list of possible transition-metal oxides for ReRAMs TaO_x has been selected as switching material for its outstanding retention and endurance characteristics [5].
We post-process a CMOS chip fabricated with a UMC 0.18 µm CMOS shuttle run. Fig. 1 shows an optical image of a post-processed chip. The chip includes an 8×8 crossbar array, single cross-points and various test structures. We deposited the TaO_x thin film element between the CMOS chips Metal 6 (M6) and Metal 5 (M5) lines. In Fig. 2 the process flow to fabricate ReRAMs cells is shown. We started creating a silicon-based carrier wafer by DRIE to allow the handling and the processing of the CMOS chip. After the chip embedding in the carrier wafer, we perform a parylene deposition to protect the chip and to ensure its mechanical stability during processing. Afterwards, we selectively etched the parylene layer by oxygen RIE to open the areas where the TaO_x must be deposited. Subsequently, we open the chip passivation down to M5 by BHF and we deposit TaO_x by sputtering. Fig. 3 depicts the Word line (in M6) and the Bit line (in M5) of an 8×8 crossbar memory array. The cross section A-A' on the bottom right shows a single cross-point sandwiched between M5 (bottom electrode) and an intermediate metal layer between M5-M6 (top electrode), which is used in the target CMOS technology to fabricate *Metal-Insulator-Metal* (MIM) capacitors. The deposited TaO_x creates a resistive switching layer between the boundaries of the top electrode and M5, as highlighted in the dashed circle.
Finally, electrical tests have been carried out as shown in Fig. 4. After a voltage-forming step, low-voltage operation has been observed with a SET voltage of -1 V and a RESET voltage of +1.3 V. The voltage levels are fully compatible with the used 0.18 µm CMOS technology. The 50 nm-thick integrated ReRAM has a resistance of 80 Ω in the LRS, and 320 Ω in HRS, making it a potential candidate for applications such as non-volatile FPGAs, where multiplexers can be replaced by ReRAM devices [3].

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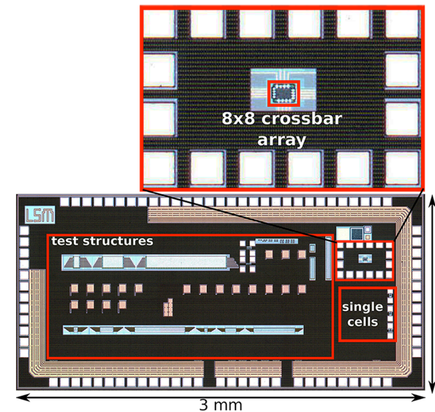

Figure 1. Micrograph of the post-processed CMOS chip. Inset shows the 8×8 array of TaO_x devices together with probe pads.

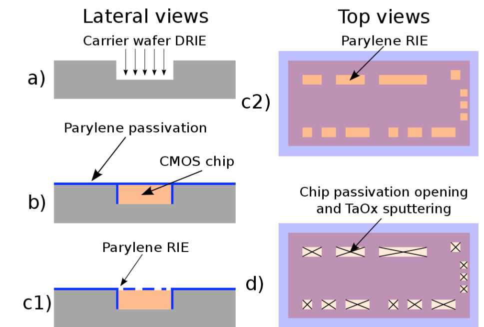

Figure 2. Process flow: a) Carrier wafer creation by Si DRIE; b) CMOS chip assembly and parylene coating c1) and c2) Parylene RIE; d) Chip passivation opening and TaO_x sputtering.

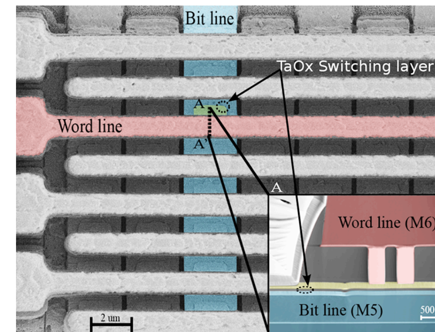

Figure 3. Scanning Electron Micrograph of an 8x8 array with Word and Bit lines in M6 and M5 metal lines. Inset shows the cross-point where the TaO_x active region is located after post-processing.

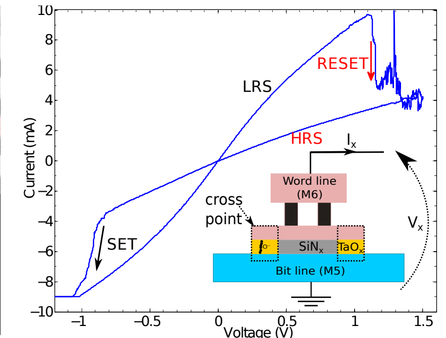

Figure 4. Measured I-V curve of an integrated TaO_x-based ReRAM device. Notice the low SET and RESET voltages compatible with low-voltage applications.