System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits

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The quest for technologies with superior device characteristics has showcased *Carbon-Nanotube Field-Effect Transistors* (CNFET) into limelight. In this work we present physical design techniques to improve the yield of CNFET circuits in the presence of *Carbon Nanotube* (CNT) imperfections. Various layout schemes are studied for enhancing the yield of CNFET standard cell library. With the help of existing ASIC design flow, we perform system-level benchmarking of CNFET circuits and compare them to CMOS circuits at various technology nodes. With CNFET technology, we observe maximum performance gains for circuits with gate-dominated delays. Averaged across various benchmarks at 16 nm, we report 8× improvement in *Energy-Delay-Product* (EDP) with CNFET circuits when compared to CMOS counterpart. We also study the performance of a complete OpenRISC processor, where we see 1.5× improvement in EDP over CMOS at 16 nm technology node. Voltage scaling enabled by CNFETs can be explored in the future for further performance benefits.

Categories and Subject Descriptors: B.7.2 [**Integrated Circuits**]: Design Aids—*Layout*

General Terms: Design, Algorithms, Performance

Additional Key Words and Phrases: Layout, carbon nanotube, CNFET, cell design

ACM Reference Format:
Shashikanth Bobba, Jie Zhang, Pierre-Emmanuel Gaillardon, H.-S. Philip Wong, Subhasish Mitra, and Giovanni De Micheli. 2014. System level benchmarking with yield-enhanced standard cell library for carbon nanotube VLSI circuits. ACM J. Emerg. Technol. Comput. Syst. 10, 4, Article 33 (May 2014), 19 pages.
DOI: http://dx.doi.org/10.1145/2600073

1. INTRODUCTION

Carbon Nanotube Field Effect Transistors (CNFETs) appear to be one of the promising successors to silicon CMOS due to their superior device characteristics [Avouris et al. 2007; Zhang et al. 2012; Wong et al. 2011; Wei et al. 2009a]. A representative CNFET structure is shown in Figure 1(a). Multiple semiconducting *Single-Walled Carbon Nanotubes* (SWCNTs, or simply CNTs) are grown on or transferred onto a substrate. The CNTs in the device act as transistor channels whose conductivity can be modulated

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DOI: http://dx.doi.org/10.1145/2600073

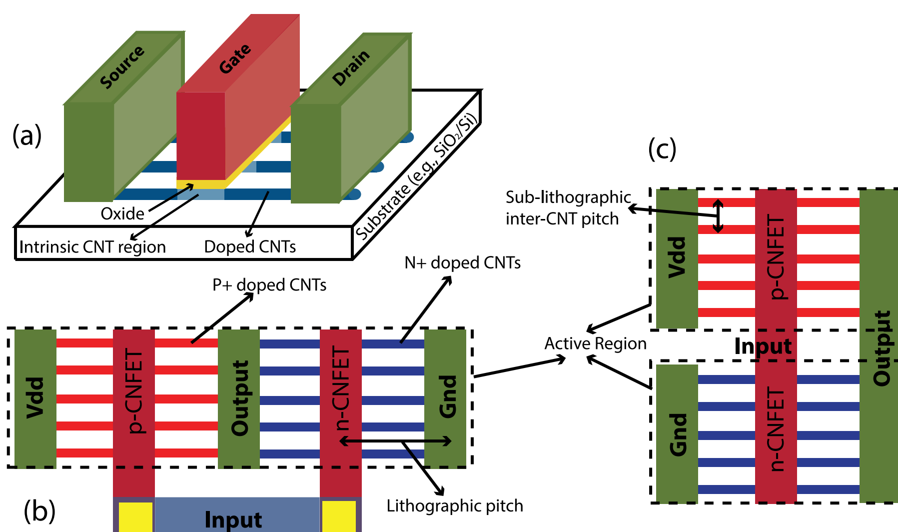

Fig. 1. (a) CNFET structure. (b) Top view of an *inverter* with CNFETs having the same CNTs (referred to as correlated CNFETs). (c) Top view of an *inverter* with un-correlated CNFETs.

by the gate. The source and the drain regions of CNTs are heavily doped. During the doping process the gate is self-aligned, thereby leaving the CNT region under the gate undoped (intrinsic CNT region). The current carriers in the CNT channel are controlled by the electric field applied to the gate and the type of doping realized on both sides of the un-doped region. Figure 1(b, c) shows the top view of complementary logic inverter with p-CNFET (p-type) and n-CNFET (n-type). The gate, source (and drain) contacts, and interconnects are defined by conventional lithography, whereas, inter-CNT pitch is limited by CNT synthesis (or growth process). In Figure 1(b), we observe that both the n-CNFET and p-CNFET have the same CNTs forming their channel region. In this work, we refer to this as CNFET correlation. On the other hand, in the inverter shown in Figure 1(c), the p-CNFET and n-CNFET are uncorrelated as they are formed by different CNTs. In Section 3, we present the effect of CNT-correlation on the overall yield of CNFET circuits.

CNFET devices fabricated with ideal CNT synthesis can potentially provide more than an order of magnitude benefit in *Energy-Delay Product* (EDP) over Silicon CMOS at 16 nm technology node [Patil et al. 2009a; Wei et al. 2009b]. Franklin et al., have demonstrated a sub-10nm CNFET, which outperforms its competing Si devices by more than four times in terms of normalized current density at low operating voltages of 0.5 V [Franklin et al. 2012], thereby making them ideal for both high performance and low power applications. However, significant challenges in CNT synthesis prevent CNFETs today from achieving such ideal benefits [Deng et al. 2007a]. CNFET technology is expected to have higher variability, as compared to CMOS, because of the following CNT-specific imperfections related to CNT-synthesis: 1. The presence of metallic CNTs (m-CNTs, versus the useful semiconducting or s-CNTs); 2. CNT diameter variations; 3. Mispositioned-CNTs; and 4. CNT density variations. A survey of these CNT-specific imperfections can be found in [Patil et al. 2009a].

All of these imperfections cause variations in the drive currents of CNFETs, which lead to delay variations and/or logic failure. Logic failures can be abstracted as stuck-open and bridging faults. The former case corresponds to having no CNTs, or no continuous CNTs, in a channel region. The latter corresponds to having either m-CNTs in

a channel region or mispositioned CNTs. For VLSI circuits with billions of transistors, CNT failures can substantially reduce the overall circuit yield.

In this article we address physical design techniques to minimize failure of CNFET circuits. Based on these techniques, we design a yield-enhanced standard cell library for realizing the complete IC design flow, in order to study the system-level performance of CNFET circuits at advanced technology nodes.

The main contributions of this work are the following.

(1) We propose physical design techniques to improve the yield of the CNFET circuit by taking advantage of CNT correlations. With *aligned-active* layout style, we demonstrate improvement in yield by correlating the critical transistors.
(2) We present mispositioned-CNT immune layout style based on Euler paths. Various mispositioned-CNT immune layout schemes are studied with respect to CNT correlation and cell routing.
(3) In order to improve the overall yield of CNFET circuits, we apply robust layout techniques to design the basic building blocks (standard cells) for CNFET circuits. A standard cell library is designed by applying both the aligned-active and mispositioned-CNT immune layout styles.
(4) Finally, by incorporating yield-enhanced standard cell library in the *integrated circuits* (IC) design flow we perform system level benchmarking of CNFET circuits when compared to CMOS circuits. To the best of our knowledge, we are the first to address system-level simulations comparing CNFET and CMOS at various technology nodes.

The design techniques presented in the preliminary version of this work [Bobba et al. 2009; Zhang et al. 2010] are applied here to improve the yield of CNFET standard cells (logic gates), by making the logic gates immune to mispositioned CNTs and by enhancing the yield by taking into account CNT correlations. By having the basic logic gates robust to CNT imperfections, we study the overall system level performance of CNFET circuits when compared to CMOS circuits at various technology nodes (32nm, 22nm and 16nm). From our simulations, we observe 5.7× improvement in EDP (averaged across various nodes), for CNFET circuits when compared to equivalent CMOS circuits. In this work we run all the simulations at a nominal voltage of 0.8V, however various voltage scaling techniques can be applied for CNFET circuits for optimal operation.

The remainder of this article is organized as follows. Section 2 presents our design methodology for mitigating CNFET failures for enhancing the overall yield. In Section 3, we study the impact of CNT-correlation to improve the yield of the CNFET circuits. Various mispostioned-CNT immune layouts styles are presented in Section 4. In Section 5, we extend the layout techniques to optimize the standard cell libraries. System-level benchmarking is discussed in Section 6. Section 7 concludes this article.

2. DESIGN METHODOLOGY

In this section, we present the design methodology for system-level analysis of CNFET circuits in connection with the underlying CNFET fabrication steps. The proposed flow starts from CNT synthesis and leads to complete IC design flow. Figure 2 illustrates our design methodology at various stages of designing CNFET circuits.

CNT fabrication. Carbon nanotubes are grown using chemical synthesis and the exact positioning and chirality of CNTs is very difficult to control. As a result, we have a mixture of semiconducting and metallic CNTs (5% to 50% m-CNTs). Since m-CNTs create short-circuit between the source and drain of the CNFET, we consider m-CNT removal process [Patil et al. 2009c] during the CNT fabrication.

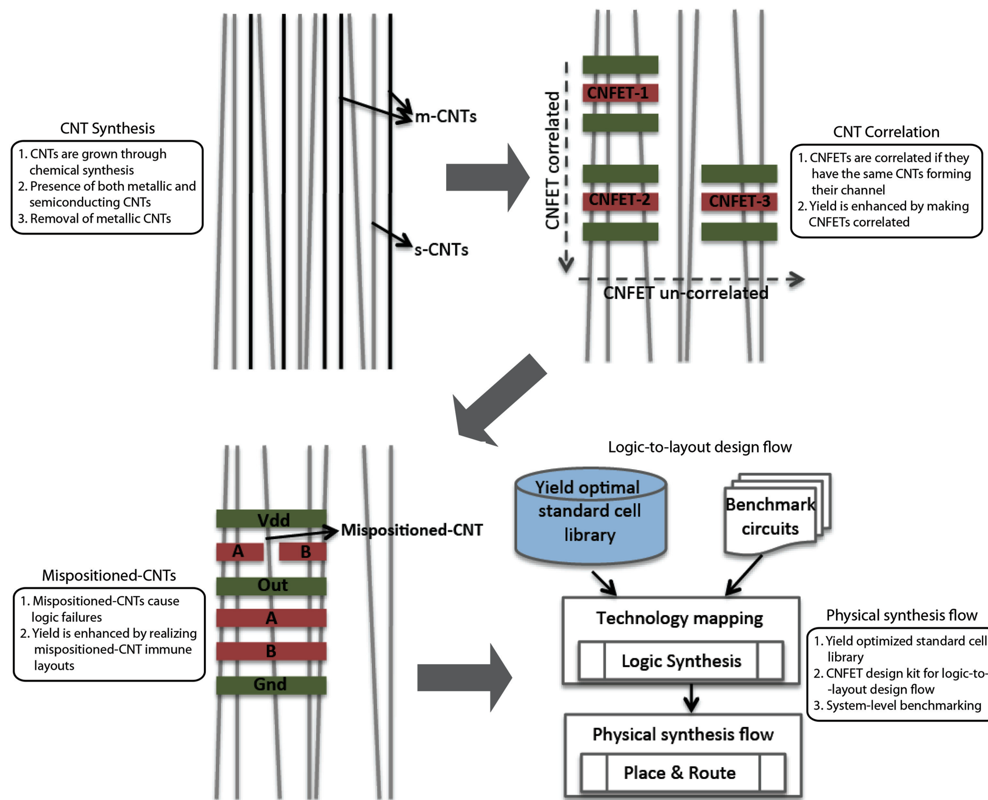

Fig. 2. Design methodology for improving the yield of CNFET circuits.

CNT correlation. Correlation of CNTs is a very unique feature of CNFET technology. CNFETs are correlated if they are aligned in the CNT direction, that is, CNFETs with similar CNTs forming their channel region. For example in Figure 2, large correlation can be observed in both CNT count ([Zhang et al. 2009b]) and CNT type (i.e., metallic or semiconducting [Lin et al. 2009]) for CNFET-1 and CNFET-2. On the other hand, CNFETs are uncorrelated if they have different CNTs forming their channel (e.g., CNFET-2 and CNFET-3). In the next section, we quantitatively show how CNT correlation can improve the yield of the circuit.

Mispositioned CNTs. During the CNT fabrication process, some CNTs are mispositioned due to the lack of control on CNTs position. As shown in Figure 2, mispositioned-CNTs can cause logic failures. With the help of mispositioned-CNT immune layout techniques, we can avoid these logic errors, thereby improving the yield of CNFET circuits.

IC design flow with yield-enhanced standard cell library. Both the CNT correlation technique and mispositioned-CNT immune layout technique are applied to the standard cell library in order to improve the overall yield of CNFET circuits. By incorporating the yield-enhanced cell library in the overall IC design flow, we study the system level performance of CNFET circuit at various technology nodes (32nm, 22nm, and 16nm).

3. YIELD OF CNFETS WITH RESPECT TO CNT-CORRELATIONS

In this section, we study the impact of CNT correlations on the overall yield of CNFET circuits. First, we present the basic model for CNT-count limited yield followed by a circuit level yield model. This is further extended to enhance the yield of CNFET standard cell library (see Section 5).

3.1. Model for CNT-Count Limited Yield

CNT count failure can be caused due to m-CNTs, CNT density variations and mispositioned CNTs. The effect of mispositioned CNTs within a CNFET has been found to be very limited [Patil et al. 2008], especially when the channel length is small or if directional CNT growth is adopted. Therefore, our model focuses on CNT count failure caused by m-CNTs and CNT density variations.

During CNT growth, assume each CNT has a probability p_m of being metallic and p_s (=1-p_m) being semiconducting. Consider an m-CNT removal process [Patil et al. 2009c], where p_{Rm} stands for the conditional probability of a CNT being removed given it is an m-CNT. For practical VLSI circuit applications, p_{Rm} of greater than 99.99% is required [Zhang et al. 2009b]. For most of the discussions in this article, we assume that $p_{Rm} \rightarrow 1$. As a side effect, m-CNT removal processes may also inadvertently remove some fraction of s-CNTs, and the conditional removal probability of a s-CNT is denoted by p_{Rs}. A single CNT can contribute to CNT count failure of a CNFET if it is an m-CNT or if it is an s-CNT but is removed inadvertently. Let p_f stand for this probability, we have

$$p_f = p_m + p_s p_{Rs}. \quad (1)$$

Consider a CNFET designed with width W, that has $N = N(W)$ CNTs prior to m-CNT removal. In the presence of CNT density variations, $N(W)$ has a statistical distribution, denoted by Prob$\{N(W)\}$. A model for the probability distribution of $N(W)$ as a function of W, and the mean and standard deviation of inter-CNT pitch (denoted by μ_S and σ_S), is presented by [Zhang et al. 2009b]. We utilize this model and keep the σ_S/μ_S ratio as reported in [Zhang et al. 2009b]. However, to enable a predictive analysis, the mean of inter-CNT pitch (μ_S) is assumed to be an optimized value of 4 nm [Deng et al. 2007].

We denote by p_F the probability of CNT count failure (or simply failure probability) of a CNFET. Assuming CNT failures are independent of each other, the CNFET fails only if all the $N(W)$ CNTs fail. Applying the law of total probability, we find p_F to be

$$p_F(W) = \sum_{N_i} p_f^{N_i} \text{Prob}\{N(W) = N_i\}. \quad (2)$$

Figure 3 illustrates the relationship of p_F vs. W for different processing conditions. For each case, p_F decreases exponentially with W, as can be seen from Equation (2). Therefore, upsizing CNFETs is an effective (but expensive) way to reduce p_F.

3.2. Circuit-Level Yield Model

To evaluate yield at the circuit level, we consider a chip consisting of M transistors (CNFETs) that are independent of each other, with W_i representing the width of the ith CNFET. The circuit-level yield is given by

$$Yield = \prod_{i=1}^{M} [1 - p_F(W_i)] \approx 1 - \sum_{i=1}^{M} p_F(W_i), \quad (3)$$

where $p_F(W_i)$ can be found using (2) or equivalently from Figure 3. Because $p_F(W_i)$ is sensitive to CNFET width W_i, most of the yield loss in (3) is due to small-width CNFETs.

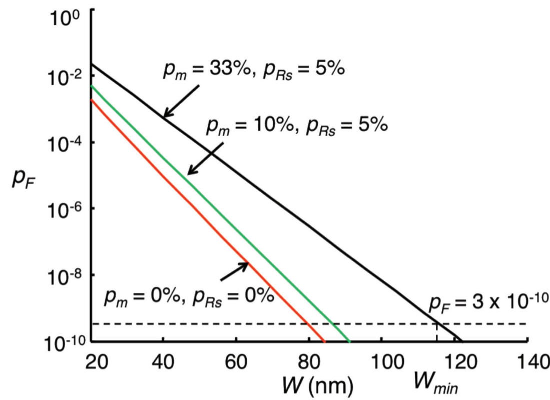

Fig. 3. CNFET failure probability vs. CNFET width ($p_{Rm} = 1$).

To optimize an existing circuit design to meet a certain yield, a simple strategy is to increase the sizes of the small-width CNFETs according to a *threshold width* (W_t). We further define W_{min} as the minimum possible W_t, such that a chip level yield requirement ($Yield_{desired}$) is met. Formally, W_{min} can be found by solving the following optimization problem

$$W_{\min} = \min(W_t) \quad (4)$$
$$s.t.\ Yield = \prod_{i=1}^{M} \{1 - p_F[U_{Wt}(W_i)]\} \geq Yield_{desired},$$

where $U_{Wt}(W_i) = \max(W_i, W_t)$ is an "upsizing" function. Finding the exact optimal solution to (4) can be tedious, but the problem can be substantially simplified by neglecting the yield loss in (3) due to non-minimum-sized transistors. That is, if there are M_{min} transistors with minimum size (W_t), then problem (4) can be rewritten as

$$W_{\min} = \min\ (W_t)$$
$$s.t.\ \prod_{i=1}^{M_{\min}} [1 - p_F(W_t)] \approx 1 - M_{\min} p_F(W_t) \geq Yield_{desired}. \quad (5)$$

The procedure for finding W_{min} according to (5) is straightforward: take a device-level p_F vs. W curve such as Figure 3, draw a horizontal line corresponding to (1-$Yield_{desired}$)/ M_{min} and the x-coordinate of the intersection gives W_{min}. Although estimating M_{min} for (5) can be iterative in nature, it is simple in practice especially for discrete sizing schemes adopted in standard cell based designs.

As a case study, we consider a transistor sizing distribution (shown in Figure 4(a)) extracted from an OpenRISC processor design (cache not included) [OpenCores 2009] synthesized with the Nangate 45nm Open Cell Library [Nangate 2009] using Synopsys Design Compiler. M_{min} can be estimated to contain the two left-most bins in Figure 4(a), which gives 33% of the total number of transistors M. If $M = 100$ million and the desired circuit yield is 99% (assuming $p_{Rs} = 5\%$), the W_{min} in this example is about 155 nm (illustrated in Figure 3). This result verifies the initial choice of M_{min} for containing only the first two bins.

Next, we discuss area and power penalties associated with upsizing small-width CNFETs. For standard cell-based designs, there is little area penalty for up-sizing the smallest cells, since there is enough free space available as the distance between the

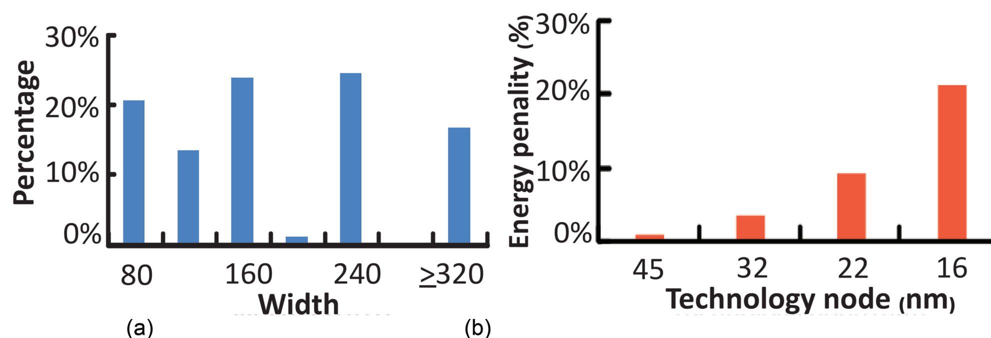

Fig. 4. Case study: (a) Transistor width distribution of an OpenRISC core synthesized using Nangate 45nm Cell Library. (b) Gate capacitance increase (penalty) vs. technology node associated with upsizing the small transistors to W_{min}.

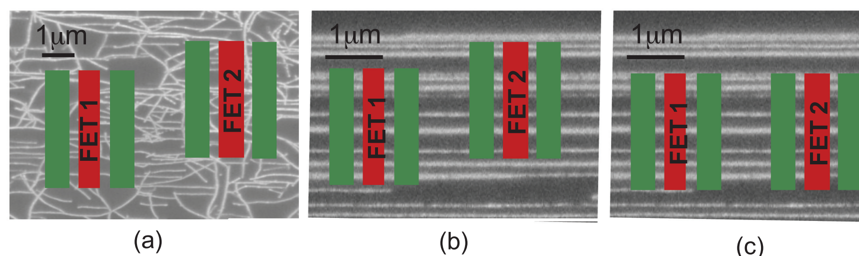

Fig. 5. (a) Nonaligned layout style on uncorrelated CNT growth. (b) Nonaligned layout style on directional CNT growth. (c) Aligned-active layout style on directional CNT growth.

rails is fixed. For example, none of the cells in our library requires an area increase to accommodate the upsized CNFET. Energy and power penalties, on the other hand, are unavoidable due to the capacitance increase. Figure 4(b) shows the energy penalty (%) associated with such upsizing calculated based on the power reports generated by Synopsys Design Compiler. A scaling analysis is also performed for different technology nodes beyond 45 nm by assuming that the CNFET dimensions scale linearly with technology node by 0.7× per generation, while the inter-CNT pitch (μ_S) remains constant at 4 nm. Analysis is not performed beyond the 16nm node due to the limitations of the CNFET Spice model [Deng et al. 2007b]. Placement of the circuits is performed using Capo [Roy and Markov 2007] and wire parasitics are estimated using FLUTE [Chu 2004] combined with parameters from Mead and Conway [1980]. Note that, because the value of W_{min} does not scale with technology, the amount of energy penalty is expected to increase significantly as technology scales down.

3.3. CNT Correlation for Enhancing the Yield of CNFET Circuits

The circuit-level yield (and therefore W_{min}) calculation in previous section is based on the assumption that failure probabilities (p_F) of all CNFETs are independent of each other. This assumption is close to reality if the CNFET circuit is fabricated using a growth that produces uncorrelated CNTs (e.g., Figure 5(a)). However, if directional CNT growth (Figure 5(b)) is used, this assumption is overly pessimistic. If two CNFETs have the same size and are aligned in the CNT direction (Figure 5(c)), large correlation can be observed in both CNT count ([Zhang et al. 2009a]) and CNT type (i.e., metallic or

semiconducting [Lin et al. 2009]) of the CNTs contained in the two CNFETs. To simplify the analysis, we assume that all CNTs have a fixed length L_{CNT}. Perfect correlation between CNFETs can be achieved if they are spaced within the CNT length, and CNFETs are completely uncorrelated when spaced beyond L_{CNT}.

To find a less pessimistic value of W_{min} for directional CNT growth, we assume that the whole circuit (consisting of M_{min} small-width CNFETs, as defined in Section 2.2) is distributed in K_R rows. CNFETs taken from different rows do not share common CNTs and are therefore independent with each other. The yield expression of (3) can be rewritten as

$$Yield = \prod_{i=1}^{K_R}(1 - p_{RF_i}) \approx 1 - \sum_{i=1}^{K_R} p_{RF_i} = 1 - K_R p_{RF}, \tag{6}$$

where p_{RFi} is the failure probability of row i, and p_{RF} is the chip-level average value of the p_{RFi}'s.

Calculating p_{RF} in a general case (allowing arbitrary positioning of the CNFETs) requires numerical methods. However, we realize that the minimum value for p_{RF} is achieved in the special case where all the minimum-sized CNFET active regions are strictly aligned to each other (as shown in Figure 5(c)). This layout style is defined as *aligned-active* layout. Because all the CNT counts and types are correlated in this case, the probability of having a failing row is the same as the probability of having one failing CNFET in this row, that is, $p_{RF} = p_F$. Comparing it with the fully independent case (2.4), the circuit failure probability (i.e., *1–Yield*) is reduced by M_{min} / K_R times. This ratio of M_{min} / K_R represents the average number of minimum-sized CNFETs in a row, which we denote by $M^R{}_{min}$. $M^R{}_{min}$ is largely determined by L_{CNT} and the average pitch between the small-width CNFETs (denoted by $P_{min-CNFET}$):

$$M^R_{\min} = L_{CNT}/P_{\min-CNFET}. \tag{7}$$

Hence, CNT growth with large L_{CNT} or designs with small $P_{min-CNFET}$ are both beneficial to the yield improvement. With the improved yield expression (6), the requirement that determines W_{min} in (5) can be relaxed by the exact same amount as the reduction in p_{RF}. A much lower W_{min} can therefore be expected.

4. MISPOSITIONED-CNT IMMUNE CIRCUITS

Various research groups have shown highly-aligned CNTs by growing them on single-crystal quartz [Kang et al. 2007; Patil et al. 2009b]. Nevertheless, a small percentage of CNTs tends to be mispositioned (mispositioned-CNTs). Mispositioned-CNTs affect the functionality of logic gates, by causing CNT short failures. Figure 6 shows a *2-input* NAND gate with transistors *A* and *B,* connected in series in the *pull-down-network* (PDN) and connected in parallel in the *pull-up-network* (PUN). The mispositioned-CNTs in the PUN do not pass under the gate region, hence are completely doped with p+ dopants, thereby creating an unnecessary short circuit between the supply (*Vdd*) and output (*out*). CNT short failures rise with the increase in distance between the gates (*A* and *B* in our example), leading to undesired logic errors.

4.1. Mispositioned-CNT Immune Layouts

A design technique, called mispositioned-CNT immune layout, to handle the errors caused by mispositioned-CNTs was presented in [Patil et al. 2008], where etched regions are realized to avoid unnecessary short circuits. Figure 7 illustrates an example of an *And-Or-Inv* (AOI21). Etched region is introduced between the gates A and B in the *pull-up network* (PUN), thereby breaking the CNTs that are not aligned to the

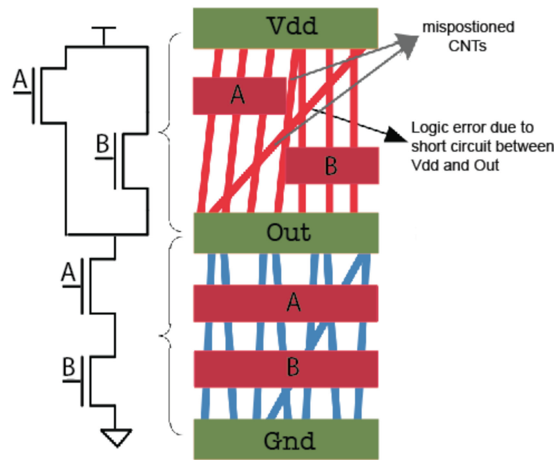

Fig. 6. Logic errors caused by mispositioned-CNTs.

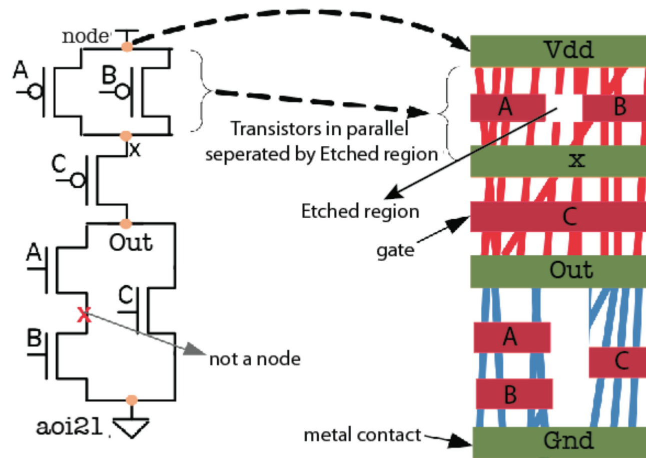

Fig. 7. Mispositioned-CNT immune layout [Patil et al. 2008].

gate. A general rule of thumb for mapping a generic schematic to mispositioned layout (shown in Figure 7) is given here.

—A node is mapped to a metal contact. In Figure 7, nodes Vdd, x, Out and Gnd are realized with a metal contact in green.
—CNTs between the parallel transistors are etched away. In the example shown in Figure 7, etched regions are introduced between transistors A and B in the PUN and transistors A-B and C in the PDN.
—Transistors in series have the same CNTs running under the gate region, hence not affected by mispositioned-CNTs.

In this work, we present novel mispostioned-CNT layout techniques based on Euler paths [Uehara and Van Cleemput 1979; Rabaey et al. 2002]. Figure 8 illustrates the two possible layout schemes of an AOI21 gate. In Figure 8(a), one Euler path is realized for each PUN and PDN. This technique is reminiscent to the existing CMOS layouts, where Euler paths are chosen with similar transistor ordering [Rabaey et al. 2002]. With

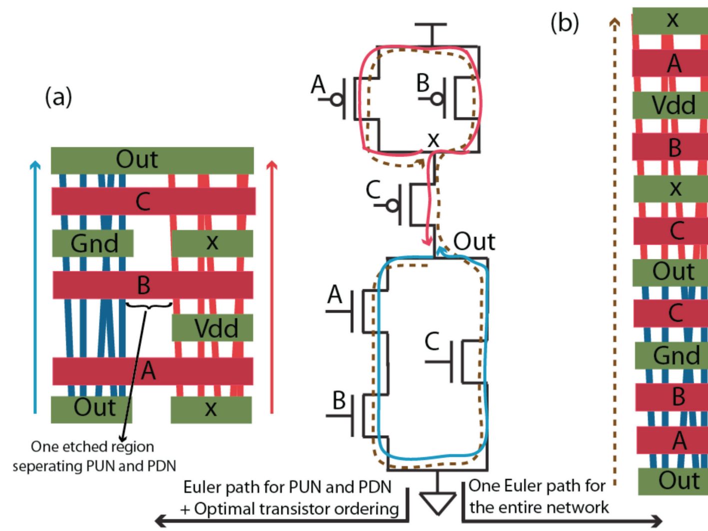

Fig. 8. Misaligned-CNT-immune layout based on Euler paths.

optimal transistor ordering, the intracell routing complexity is minimized, thereby leading to regular layouts. Figure 8(a) shows the layout of the AOI21. Since the PUN and PDN are realized with Euler paths, we can observe that the layout of networks is immune to mispositioned-CNTs. The CNTs between the PUN and PDN are etched away in order to avoid the logic errors caused by mispositioned-CNTs.

In an alternative approach, a simple layout can be realized by drawing one Euler path for the entire circuit covering both the PUN and PDN (see Figure 8(b)). We observe that mispositioned-CNTs have no effect on this layout style, as at any given point CNTs are either connected to a metal contact (node) or passing under a gate. As a further step, the sizes of the transistors can be varied for balancing the drive strength of the PUN and the PDN.

In the case of layout scheme presented in Figure 8(a), conventional CMOS layout techniques can be applied for generating the layout. On the other hand, for the novel layout scheme in Figure 8(b), the following heuristic can be applied for mapping a generic schematic.

—Create a graph of the circuit, with the contacts mapped as *nodes* and gates as *edges*, which connect the nodes.
—Draw an Euler path traversing all the nodes and edges of the entire network (no concept of PUN and PDN). Since we consider only one Euler path, transistor ordering need not be taken into account.

4.2. Mispositioned-CNT Immune Layouts with Respect to CNT Correlation and Cell Routing

From Section 3.3 we infer that yield of circuit is improved by maximizing the correlation between the transistors. Hence maximum yield is obtained by correlating all the CNFETs comprising the circuit. All the three layout techniques presented in Section 4.1 are analyzed here with respect to CNT correlation and cell routing complexity. This gives us the optimal choice of layout for designing the standard cell library.

As an example we study a *3-input* NAND gate realized with all the three layout styles. The schematic of the NAND gate is shown in Figure 9(a). In *Scheme-1*, etched regions are realized between the transistors in parallel [Patil et al. 2008]. In Figure 9(b)

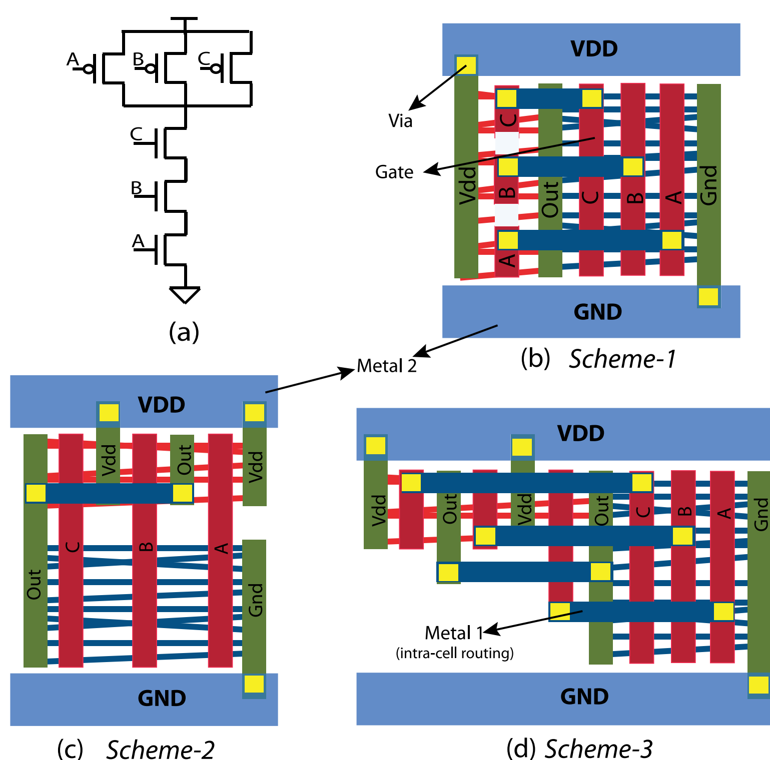

Fig. 9. NAND3 gate. (a) Circuit schematic. (b, c, d) Mispositioned-CNT-immune layouts.

two etched regions are realized between gates *A* and *B* and gates *B* and *C* of the PUN. Transistors in the PDN are in series, hence not affected by mispostioned-CNTs. It can be observed that all transistors in the PDN are correlated as they have the same CNTs forming the channel for all the three transistors. However, in the PUN all the three transistors are uncorrelated, thereby affecting the yield of the logic gate (see Section 3).

Scheme-2 and *Scheme-3* are obtained by drawing Euler paths (see Section 4.1). The layout style presented in *Scheme-2* (Figure 9(c)) is similar to the CMOS style layouts [Uehara and Van Cleemput 1979]. The PUN and PDN are separated by an etched region, thereby gaining immunity to mispositioned-CNTs. We can observe from Figure 9(c) that all the CNFETs in the PUN (and also in the PDN) are correlated. However, the PUN and PDN are not correlated. Hence any logic gate can be realized with just two aligned-active grids. The main advantage of this layout scheme is the intracell routing.

On the other hand, *Scheme-3* is the ideal layout style for correlating all the transistors of the network. Realizing a layout with only one Euler path inherently makes all the transistors correlated. Hence we can obtain maximum yield with *Scheme-3* layout style. However, the intracell routing to connect the gates in the PUN and PDN is complex, as an extra metal layer is needed. Hence, the regularity at the gate stack is compromised for making all the transistors correlated. Moreover, the layouts tend to be wider and shorter as we place the PUN next to the PDN [Bobba et al. 2009].

Table I reports various performance metrics (cell routing complexity, active area and the number of *Aligned-Active Grids* (AAG)) of the three layout schemes applied for various logic gates. In order to avoid technology dependency, we employ λ-based rules

Table I. Area, Routing Complexity (Minimum # Vias and ICRA), and AAGs for Mispositioned-CNT Immune Layout Schemes

Gates	Scheme 1				Scheme 2				Scheme 3			
	Area*	# Vias	ICRA*	# AAG	Area*	# Vias	ICRA*	# AAG	Area*	# Vias	ICRA*	# AAG
INV	168	4	33	1	216	2	6	2	168	4	33	1
NAND2	378	6	78	2	546	3	42	2	544	8	105	1
NAND3	812	8	135	3	1020	5	63	2	1128	11	279	1
NAND4	1254	10	204	4	1638	7	100	2	1920	15	510	1
AOI12	1156	8	180	2	1020	7	161	2	832	11	390	1

Area* – Area of the standard cell in λ^2
ICRA* - Intracell routing area (Metal 1 routing area in λ^2)
Vias – Number of Vias
AAG – Number of *aligned-active* grids

[Mead and Conway 1980] for calculating the area of the cell and *Intra-Cell Routing Area* (ICRA). The length of the transistor is set to 2λ with the minimum transistor width of 8λ. Transistor sizing is taken into account for all the gates. The number of AAGs varies for *Scheme-1* based on the function and *fan-in* of the logic gate. Intracell routing complexity for *Scheme-1* increases for complex gates and gates with high *fan-in*. In the case of *Scheme-2*, the intracell routing is simplified with the minimum number of AAGs set to two. On the other hand, for *Scheme-3,* extra resources in terms of cell area and intracell routing is needed for achieving minimum number of AAGs. Among the three layout schemes presented, we can observe that *Scheme-2* is preferable when considering all the performance metrics (cell area, intracell routing area, and the number of AAGs).

5. STANDARD-CELL LIBRARY DESIGN

Layout techniques to improve the yield of CNFET circuits (see Sections 3 and 4) are employed here to realize the desired standard cell library. From Section 4.2, we infer that *Scheme-2* is an ideal choice for realizing standard cells due to its simplified intracell routing as well as ease in aligning the critical transistors of the PUN and PDN. However, in order to improve the overall yield of the CNFET circuit, the aligned-active layout style requires the active regions not only within each individual cell, but also between different cells to be aligned to each other.

Hence, for designing a new standard cell library an aligned-active technique is added to the new set of *design-rules*. The aligned-active design rule ensures that an active-area grid is virtually marked where all the transistors of the PUN (and also of the PDN) are aligned. An optimal location of the active-area grid for a library of cells is an open research problem.

In this section, we study the impact on cell area and gate capacitance by applying the aligned-active design rule on existing libraries. We applied the aligned-active restriction to an existing standard cell library [Nangate 2009] by the following heuristic.

—Estimate W_{min} according to Equations (5) and (6).
—Find active regions corresponding to all the CNFETs with width smaller than W_{min} and perform upsizing. These active regions are called *critical active regions*.
—Place the n-type (same for p-type) critical active regions of all cells in the cell library in such a way that their y-coordinates match with each other.
—Modify the intracell routing as necessary.

Note that, although noncritical active regions have not been explicitly mentioned in the above heuristics, it is still beneficial to align them with the critical active regions as much as possible.

The standard cells in the Nangate Open Cell Library [Nangate 2009] were modified according to the aforementioned procedure for the enforcement of aligned-active

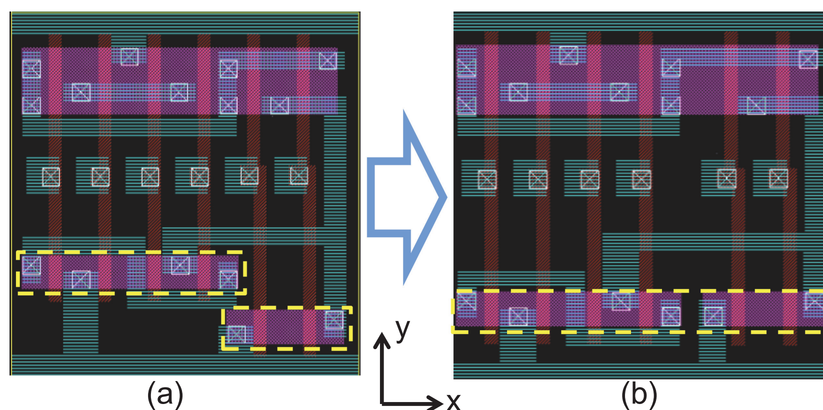

Fig. 10. Enforcing aligned-active layout style to the AOI222_X1 cell from the Nangate 45nm Open Cell Library.

restriction. Figure 10 illustrates one of the standard cells (AOI222_X1) before (a) and after (b) enforcing this restriction. The critical n-type active regions in this cell are highlighted in dashed yellow lines. After the modification, all the n-type active regions in the cell are aligned according to a globally defined grid. The cell width has increased by 9% as a result of this change.

We now discuss the area costs of strictly aligning the active regions of the critical transistors ($W < W_{min}$) in the standard cell library. Altering the positions of active regions in the critical cells will have an impact on the intracell as well as intercell routing. However, in order to minimize the penalty on intercell routing, we retained the location of the I/O pins as much as possible while modifying the cells.

Aligning to the optimal grid has an area impact on 4 cells (out of a total of 134 cells) from the Nangate Open Cell Library, including the AOI222_X1 cell shown in Figure 10. We have further extended our analysis to a commercial 65 nm standard cell library, having 775 cells. About 20% of the library cells have an impact on area while aligning the active regions. Overall we observe that aligning active regions becomes complex for gates with high fan-in as well as flip-flops and latches, thereby leading to area penalty. However, the area penalty can be minimized by increasing the number of *aligned-active* regions of the standard cells. For example by doubling number of AAR for both p-type and n-type CNFETs, instead of one, results in zero area penalty. However, the p_{RF} benefit is reduced by 2× (described in Section 3.3), which corresponds to <5% increase in W_{min}.

6. SYSTEM LEVEL BENCHMARKING

In this section, we perform the system level evaluation of CNFET circuits. Physical design techniques presented in the previous section are employed to design a yield-enhanced standard cell library, based on which we synthesize various benchmark circuits. Comparison with CMOS circuits is drawn considering delay, power and area at various technology nodes.

6.1. Experimental Setup

Figure 11 illustrates our design flow for studying the performance of CNFET circuits at system level. Our main contribution of this work is in the design of yield-enhanced CNFET cell library. CNT synthesis parameters like (p_{Rm}, p_{Rs}, and p_m) are needed to find the minimum width of the transistor. In order to reduce logic failures of CNFET circuits,

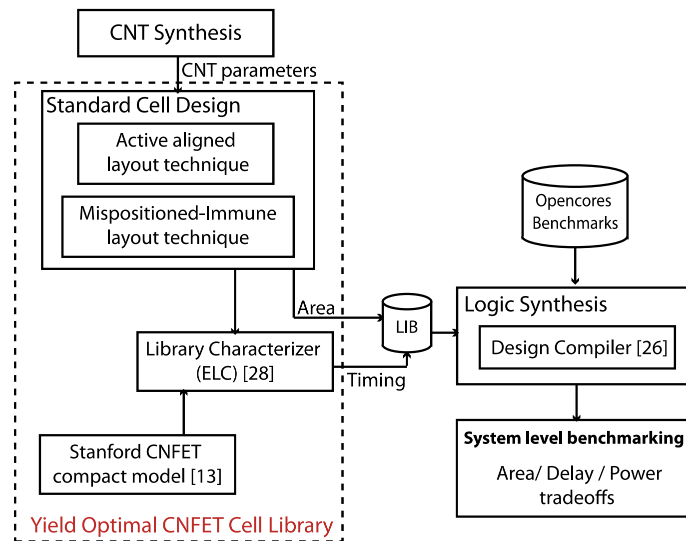

Fig. 11. Design flow.

we employ both the *aligned-active* and *mispositioned-immune* layout styles to design various standard cells. The set of standard cells consists of 32 combinational logic cells such as NAND2, NAND3, NOR2, AOI21, ... and a D flip-flop with asynchronous reset and preset. Electrical characterization of standard cells is done with Encounter Characterizer tool [ELC 2011] using the Stanford's CNFET compact model [Stanford]. To enable our performance evaluation of CNFET circuits, we generate libraries (*.lib files) for various technology nodes (32nm, 22nm, and 16nm) at a nominal voltage of 0.8V. CMOS counterpart libraries have been generated using PTM models [PTM]. The gates are characterized with industrial library characterizer (Encounter Library Characterizer), with the gate delays in a 7×7 matrix form characterized with respect to the input-slew and output-load. For technology mapping, we consider typical delay of the cells. The gate sizing respects the Nangate library [Nangate 2009] sizing and ideal transistor scaling have been applied for both logic and memory scaling between the different technology nodes. In addition to the gate characterization, a simple and ideally scaled model of the wire load is considered.

We then use a set of logic circuits taken from the OpenCores repository [OpenCores 2009]. These benchmarks illustrate various applicative constraints from simple gate dominated circuits (e.g., memory controller) and interconnection dominated circuits (e.g., ethernet) to complex blocks (OpenRISC processor). Synopsys Design Compiler [DC] does the synthesis of these circuits. *Timing*, *power* and *area* reports are considered to evaluate the impact of CNFET implementation when compared to CMOS counterparts.

6.2. Results and Discussion

6.2.1. CNFET vs. CMOS at Various Technology Nodes. In this section, we study critical path delay, dynamic power and area of CNFET and CMOS circuits. To achieve for a fair comparison, each benchmark is constrained with the same clock frequency for CMOS and CNFET at each technology node. The clock frequency is set to the maximum frequency achieved by the CMOS equivalent circuit. In Table II, we present the delay and dynamic power of various benchmarks taken from opencores [OpenCores 2009].

Table II. Critical Path Delay and Dynamic Power at Various Process Nodes for CMOS and CNFET Technologies

Benchmarks	Nodes	Clock	Critical path delay (ns)		Dynamic power (mW)	
			CMOS	CNFET	CMOS	CNFET
mem_ctrl # Cell = 26K # FF = 194	32 nm	0.34	0.34	0.2	8.88	8.7
	22 nm	0.32	0.32	0.13	8.61	2.9
	16 nm	0.3	0.3	0.1	6.7	2.01
eth # Cell = 51K # FF = 10K	32 nm	0.37	0.37	0.33	77.6	72.2
	22 nm	0.33	0.33	0.24	64.5	23.97
	16 nm	0.35	0.35	0.24	49.33	15.31
wb_conmax # Cell = 6279 # FF = 773	32 nm	0.43	0.43	0.14	8.78	7.66
	22 nm	0.41	0.41	0.1	6.66	3.55
	16 nm	0.37	0.37	0.09	5.9	2.73
wb_dma # Cell = 24K # FF = 578	32 nm	0.46	0.46	0.2	5.14	5.07
	22 nm	0.41	0.41	0.15	4.63	1.51
	16 nm	0.34	0.34	0.13	4.19	1.19

mem_ctrl : Memory Controller   eth : Ethernet IP core   # Cells = number of logic cells
wb_conmax : Wishbone IP core   wb_dma : Wishbone DMA IP core   # FF = number of flip-flops

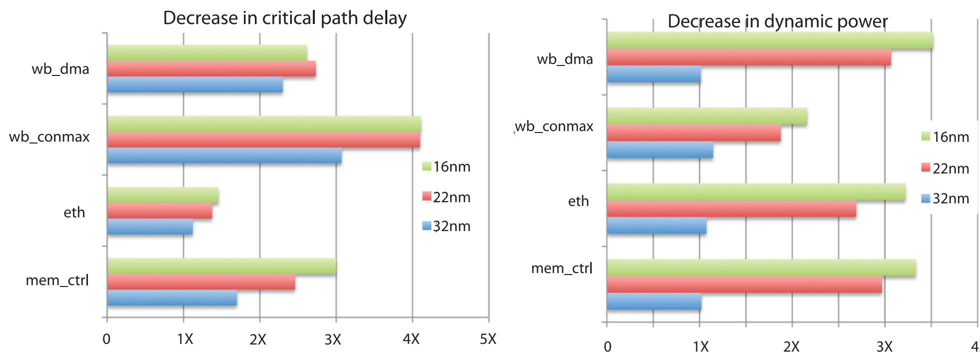

Fig. 12. Performance improvement of CNFET circuits when compared to CMOS circuits. (a) Decrease in critical path delay. (b) Decrease in dynamic power.

Figure 12(a) illustrates the decrease in critical path delay for various benchmarks. We observe that the maximum achievable frequency, set by CMOS gates, is easily met when mapped with CNFET libraries. For example, the minimum delay achieved for the *mem_ctrl* when mapped with CMOS 22nm technology is 0.32ns. This delay is set to the delay constraint when synthesizing the *mem_ctrl* with CNFET 22 nm library. The critical path of *mem_ctrl* with CNFET gates is 0.13ns when compared to 0.32ns delay set by CMOS gates. We observe two different trends for the benchmark circuits. On one hand, gate-dominated circuits like *wb_conmax* and *mem_ctrl* show significant improvement in delay characteristics with CNFET gates. For instance, more than 3× improvement in critical path delay is achieved at 16nm node. On the other hand, interconnect-dominated circuit (*eth*) shows marginal improvement (10%) in critical path delay, as the major part of the delay comes from the interconnect.

In Figure 12(b), we show decrease in the dynamic power for all the benchmarks with CNFETs when compared to CMOS. Dynamic power reported in Table II includes both the internal power and the net switching power. In our simulations, we observe decreasing trend in dynamic power with scaling (from 32nm to 16nm) for both the technologies. Maximum reduction in dynamic power is achieved at lower technology nodes (22nm and 16nm) for all the benchmarks. Averaged across all the benchmarks

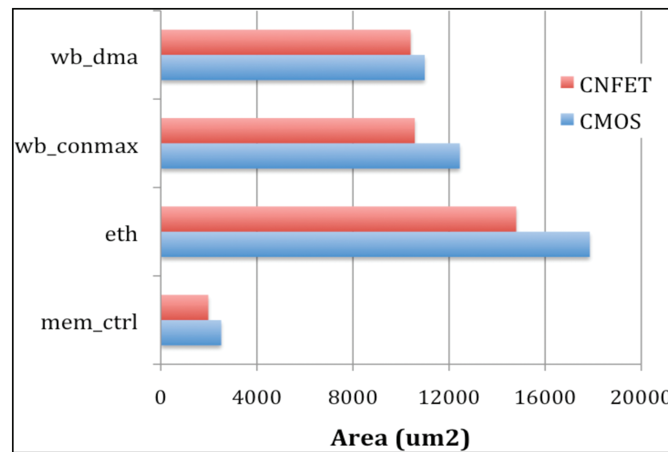

Fig. 13. Area comparison of various benchmarks after mapping with CNFET and CMOS libraries at 22 nm node.

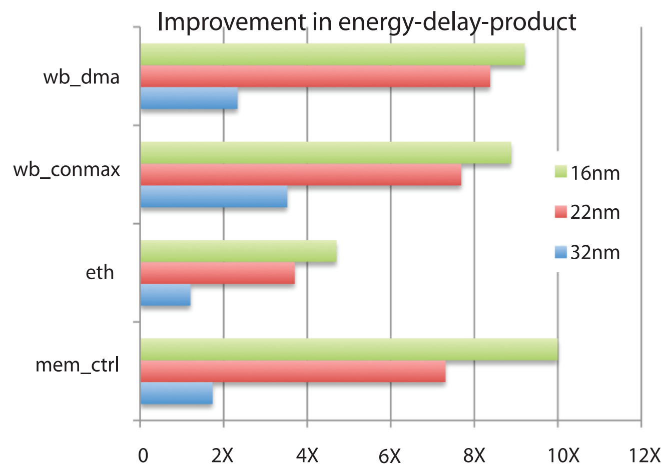

Fig. 14. EDP of various benchmarks with CNFETs when compared to their implementation with planar CMOS technology.

and nodes, we observe 2.3× improvement in dynamic power with CNFET technology over CMOS technology for the same frequency of operation.

In this work, we physically mapped a CNFET library from a CMOS library, by taking into account the width of the n-type transistor of standard cells. In the case of CNFET library, during the sizing of the pull-up-network and pull-down network, we consider both n-CNFET and p-CNFET to have similar performance [Deng et al. 2007]. In the over all area estimation after mapping the various benchmarks, we observe 15% (on average) area benefit for CNFET circuits when compared to CMOS counterpart. Figure 13 illustrates the area comparison of various benchmarks with CNFET and CMOS technologies at 22nm node. Similar results were obtained at other technology nodes.

Energy-delay-product (EDP) is an attractive metric to compare designs, as one can trade increased delay for lower energy per operation (e.g., by scaling down the supply voltage, we can trade the increase in delay with the decrease in overall energy

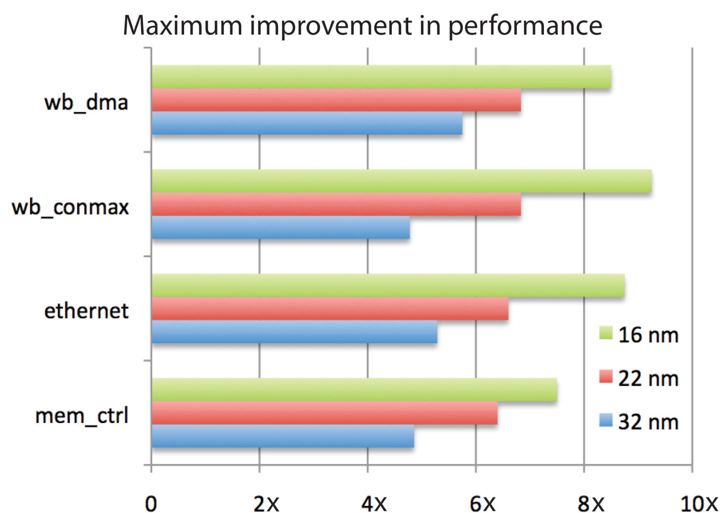

Fig. 15. Maximum frequency improvement with CNFETs when compared to CMOS technology.

consumption). Figure 14 shows the improvement in EDP with CNFET gates when compared to CMOS. We observe maximum EDP gains for gate-dominated circuits ranging from 2× to 8×. Averaged across all the benchmarks, CNFET circuits show 5.7× improvement in EDP when compared to CMOS circuits.

6.2.2. Maximum Performance. In the previous section, we studied the CMOS circuits and CNFET circuits operating at the same frequency. We observed that CNFET circuits meet the CMOS delay requirements with ease, due to the superior device characteristics of CNFETs. Here, we study the maximum frequency achieved by benchmark circuits with CNFETs. This study will shed some light on the impact of CNFET technology on high performance computational blocks, which are desired to operate at maximum possible frequencies. In order to maximize the performance, we synthesized the benchmarks with very low delay constraints. Figure 15 shows the maximum frequency improvement for various benchmark circuits. At 16nm we observe a maximum frequency gain of 8.5×, averaged across all the benchmark circuits. However, it has to be noted that the dynamic power increases with frequency. The increase in power can be kept under control by applying voltage scaling design technique. An optimal operating condition can be found by applying low power design techniques, considering various frequencies and supply voltages, in our system-level simulation framework. Finding the optimal voltage for each benchmark is beyond the scope of this work.

6.2.3. Case Study: OpenRISC Processor. In the previous two sections, we evaluated the performance improvement of various benchmarks circuits (*gate-dominated* as well as *interconnect-dominated*). Here, we study the impact of CNFET technology at a higher abstraction by mapping an OpenRISC processor with CNFET technology. We synthesized the OpenRISC 1200 processor [OpenCores 2009] at various lithography nodes for both CMOS and CNFET technologies. Our main motive is to find the maximum frequency achievable at each of the technology nodes. Figure 16(a) depicts the maximum frequency of an OpenRISC core for each node. Large memory banks have been used for the different nodes. We evaluated the performance by assuming the same ideal memory bank for both CMOS and CNFET processor. Optimized design with memory realized with CNFETs is out of scope of this work. We see that the CNFET technology outperform CMOS with a gain of up to 2.1× at 16 nm node, leading to a maximal

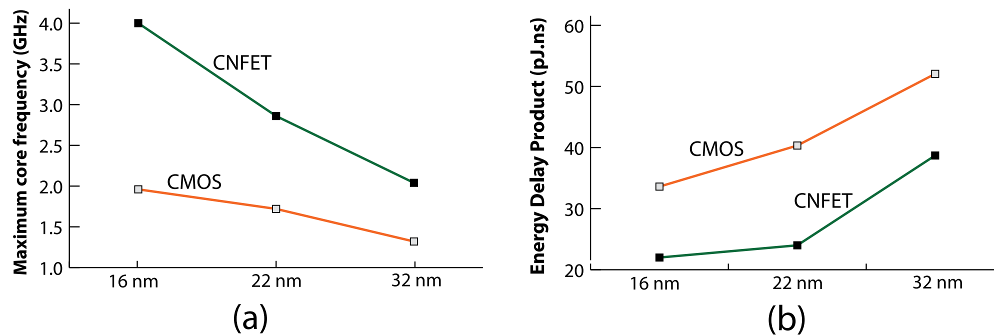

Fig. 16. OpenRISC 1200 casestudy at various technology nodes. (a) Maximal frequency achievable. (b) Energy-delay-product.

performance of 4 GHz. The performance improvement of CNFET processor does not match the results presented in Sec 6.2, where we showed 8.5× improvement at 16 nm node. The main reason comes for limited performance gain comes from the critical path delay to access the data from the memory bank. Further improvement in performance of CNFET processor can be envisaged by realizing the interconnect with CNTs [Srivastava and Banerjee 2005].

Figure 16(b) illustrates the energy-delay-product for the OpenRISC processor. EDP is extracted by assuming same clock constraints for CMOS and CNFET. Averaged across all the nodes, we observe 1.5× improvement in EDP with CNFET processor when compared to equivalent CMOS implementation.

7. CONCLUSION

In this work, we present system-level benchmarking of CNFET circuits with physical design techniques to improve the yield of CNFET circuits. Novel layout techniques are proposed to design standard cell libraries with improved yield. With the yield-enhanced standard cell libraries, we perform system-level benchmarking of CNFET circuits and compare them to their equivalent CMOS circuits at various technology nodes. We consider a nominal voltage of 0.8V for CMOS and CNFET circuits at all the nodes. Averaging across various benchmark circuits, at different technology nodes, we observe 5.7× improvement in EDP of CNFET circuit over CMOS circuit. Further performance benefits of CNFET circuits can be obtained by applying voltage scaling design technique. As a future extension of this work, we intend to study the impact of voltage scaling on CNFET circuits.

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Received December 2012; revised July 2013; accepted October 2013