An Enhanced Design Methodology for Resonant Clock Trees

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Clock distribution networks consume a considerable portion of the power dissipated by synchronous circuits. In conventional clock distribution networks, clock buffers are inserted to retain signal integrity along the long interconnects, which, in turn, significantly increase the power consumed by the clock distribution network. Resonant clock distribution networks are considered as efficient low-power alternatives to traditional clock distribution schemes. These networks utilize additional inductive circuits to reduce power while delivering a full swing clock signal to the sink nodes. A design method for applying the resonant clocking approach for synthesized clock trees is presented. The proper number and placement of LC tanks and the related resonance parameters are determined in the proposed method. This method attempts to minimize the number of LC tanks that can deliver a full swing signal to all the sink nodes by considering the capacitive load at each node to determine the location of LC tanks. Resonance parameters, such as the size of the inductor can be adapted to reduce the power consumption and/or area overhead of the clock distribution network. Simulation results indicate up to 57% reduction in the power consumed by the resonant clock network as compared to a conventional buffered clock network. Compared to existing methods, the number of LC tanks for the proposed technique is decreased up to 15% and the signal swing is also improved by 44%. Depending on whether power or area is the design objective, two different approaches are followed to determine the parameters of resonance. If the design objective is to lower the power consumed by the network, the power and area of the designed network improve up to 24% and 51%, respectively, as compared to state of the art methods. If a low area is targeted, the power and area improvements are 11% and 57%, respectively.

Keywords: 3-D Integration, Resonant Clocking, LC Tank.

1. INTRODUCTION

A primary challenge in designing synchronous circuits is how to efficiently distribute the clock signal to the sequential parts of the circuit.[1] As the area of the integrated circuits increases, larger networks are required to distribute the clock signal, which results in higher capacitive loads and resistive losses of the interconnects degrading the signal integrity along these interconnects. A common solution to alleviate this problem is to insert clock buffers at the intermediate nodes of the clock distribution network. Although buffer insertion improves clock signal integrity, clock buffers significantly increase the power consumed by the network.

An efficient approach to eliminate the repeaters and reduce power is to use resonant clocking.[2–4] In this approach, on-chip inductance is added to the clock network and forms a resonant circuit with the interconnect capacitance. The power consumed by the network decreases in this way, since the energy alternates between electric and magnetic fields instead of dissipating as heat. A recent implementation of a resonant global clock network within a commercial processor exhibited an over 25% reduction in the power consumed by this network, highlighting at the same time the challenges in the design process of resonant clock networks.[5] The global clock in Ref. [5] cannot directly be generalized to clock trees as it has been designed to satisfy the specifications and addresses the limitations of a specific processor design.

Several resonant circuits can be utilized to improve the characteristics of the clock signal. The number and the location of *LC* tanks (resonant circuits) are interdependent. In general, if the resonant circuits are placed closer to the driver, fewer circuits are needed and, alternatively, where

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these circuits are placed close to the sink nodes, more *LC* tanks are required. The number of resonant circuits also affects the output signal swing. Different methods for allocating the *LC* tanks in clock distribution networks have been presented in Refs. [6, 7]. In Ref. [6] a method for allocating *LC* tanks for H-trees is proposed. This method is applicable to symmetric structures where the location and number of *LC* tanks are interdependent and the number of *LC* tanks is a power of two. In Ref. [7], the *LC* tanks are placed at equidistant points from the root which is a proper method for symmetric clock trees, such as H-trees and binary trees. The performance of this method degrades for asymmetric clock trees since maintaining equal distances to the root results in sub-trees with dissimilar capacitance resonating with inductors of the same size.

The contribution of this paper is a methodology that determines the number of *LC* tanks that can deliver a full swing signal to the sink nodes in a synthesized clock tree and determines the proper resonant parameter for these *LC* tanks. The parameters of resonance can be determined to satisfy one of the two objectives, minimizing the power of the clock distribution network or the area of the inductors.

In the following section the concept of resonant clocking is reviewed. The proposed method for designing a resonant clock tree is introduced in Section 3. In Section 4, simulation results are presented and the proposed method is compared to previous design techniques for resonant clock networks. Some conclusions are offered in the last section.

2. RESONANT CLOCK NETWORKS

In this section several methods of designing resonant clock distribution networks are investigated. A design of a global clock distribution network is presented in Ref. [3], in which four resonant circuits are connected to a standard H-tree structure as illustrated in Figure 1. Each quadrant consists of an on-chip spiral inductor that resonates with the wiring capacitance of the clock network and a decoupling capacitor connected to the other end of the spiral inductor.

A simple lumped circuit model is utilized to determine the resonant inductance. The resonant frequency of the network is (in first-order) estimated by $f = (1)/(2 \cdot \pi \cdot \sqrt{LC})$ where C and L, respectively, denote the equivalent capacitance of the network wires and inductance of the spiral inductors. A decoupling capacitor is employed to provide a positive voltage offset on the grounded node of the resonant inductor and adapt the voltage level to the CMOS logic level. This capacitor should be sufficiently large to guarantee that the resonant frequency of the decoupling capacitor $f_{decap} = (1)/(2 \cdot \pi \cdot \sqrt{LC_{decap}})$ is much lower than the desired resonant frequency of the clock network.

Based on this structure, a design methodology for resonant H-tree clock distribution networks is proposed in Ref. [3]. In this work, the clock tree is modeled with a distributed *RLC* interconnect as illustrated in Figure 2.
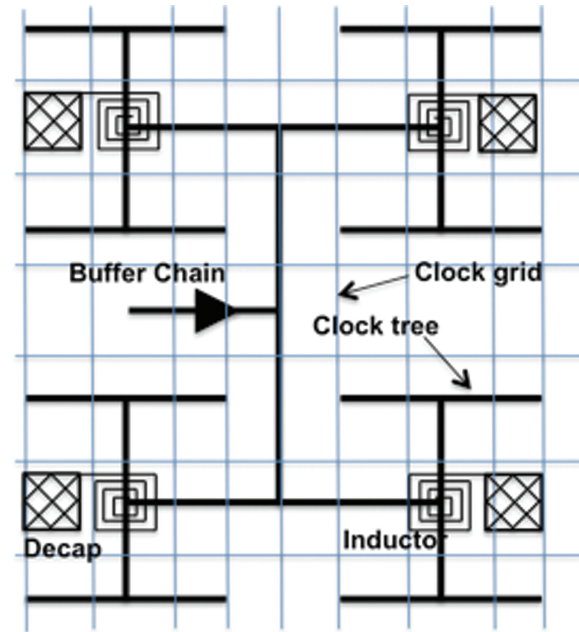

Fig. 1. Schematic of a typical resonant clock network.

This electrical model is utilized to determine the parameters of the resonant circuit and the output impedance of the clock driver such that the power consumed by the network and the clock driver is minimum, while a full swing signal is delivered at the output nodes.
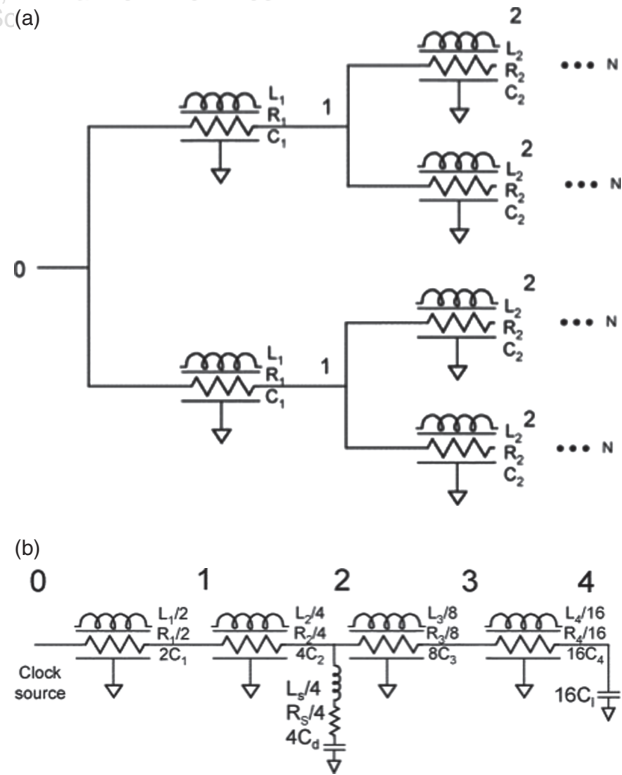
Fig. 2. RLC model of a 16-sink H-tree clock network where (a) is the distributed RLC model of the tree and (b) is the lumped RLC model of the resonant network.[3]

To deliver a full swing signal at the sink nodes, the magnitude of the transfer function of the network, H_{out}, should be close to one. This parameter is often fixed to 0.9,[3,7] (for the remainder of the paper a "full swing signal" implies any signal swing that satisfies this specification). As discussed in Ref. [7], by increasing the number of resonant circuits and placing these circuits closer to the sink nodes, each inductor resonates with a smaller part of the circuit resulting in lower attenuation of the output signal swing. Alternatively, increasing the number of resonant circuits and using larger inductors in each *LC* tank reduces the quality factor of the *LC* tanks, since in spiral inductors the effective series resistance (ESR) increases faster than the inductance.[3] A lower quality factor for resonant circuits produces a higher signal loss and decreases the output signal swing.

To determine the parameters of resonance one approach is to only consider the capacitance of the clock network and employ first-order estimation to determine the total resonant inductance.[2,4,7] By doubling the number of *LC* tanks, the inductance of each tank is also doubled. In this approach, the inductive component of the network wires is not considered. In large clock networks with long interconnects, the inductance of the wires cannot be neglected. Furthermore, this method assumes that placing the resonant circuit in different locations does not change the equivalent capacitance of the network (i.e., the capacitance seen by the primary clock driver). These simplifications can result in inaccurate estimation of the resonant inductance, adversely affecting the signal swing.

Another approach for determining the resonant parameters is proposed in Ref. [6] for H-trees where the location of *LC* tanks is swept from the root to the sinks. For each location the driver resistance is adapted to produce a transfer function amplitude of 0.9 for a wide range of inductor sizes. The driver resistance and corresponding power consumption are swept versus the inductance. The inductance for which the driver resistance is maximum or the power consumption is minimum (which do not necessarily occur for the same frequency) is determined.

An early method to apply resonant clocking to synthesized trees is proposed in Ref. [7]. This method allocates the *LC* tanks at equidistant points from the root node. The location of *LC* tanks is swept from the root toward the sinks to find the maximum signal swing. Maintaining the distance from the *LC* tanks to the root constant reduces the number of candidate *LC* tank locations which can degrade the performance of this method. In asymmetric clock networks, for long branches (can lead to lower signal swing at the corresponding sinks) placing the *LC* tanks closer to the sinks can improve the signal swing, which is not supported by this method.

Other approaches for applying resonant clocking for synthesized clock networks are presented in Refs. [8,9]. These methods are proposed for grid clock network structures where the capacitance of the network is almost equally distributed. LARCKS[10] chooses a small library of resonant inductors and for each node determines a vicinity of nodes so that the total node capacitance resonates with the employed inductance at the desired clock frequency. Using limited candidates for resonant inductance reduces the complexity of LARCKS but on the downside the performance of the method can degrade. The LARCKS method is also applicable to clock trees, but due to the highly irregular structure of trees determining the appropriate local regions (vicinities) to resonate with the same inductance can be a formidable task. The length of the tree branches and their related capacitance is not uniform in clock trees and, very often, the branches near the root are much longer than the interconnect segments near the sinks. In Fig. 3, a simple example of a clock tree is shown where the length and capacitance of W_1 and W_2 are much larger than W_3 to W_6. For node N_1, the vicinity includes W_1 or W_2 (or both) and for N_2, the vicinity includes W_3 and W_4; therefore the capacitance for the vicinity of N_1 is much larger than the capacitance for vicinity of N_2. The use of the same resonant inductance for these two vicinities results in quite different resonant frequencies.

To overcome these disadvantages, a novel method for applying resonant clocking to synthesized trees is presented in the next section. The *LC* tank location and resonant parameters are determined to deliver a full swing signal to the sink node while reducing power and/or area.

3. DESIGN METHODOLOGY

In this section a new method for applying the resonant approach to synthesized trees is introduced. An algorithm based on this method is described in Subsection 3.1. This method is a heuristic approach to minimize the number of *LC* tanks that suffice to deliver a full swing signal to all the sink nodes (i.e., a signal swing greater than 0.9). The important contribution of this method is to properly allocate the *LC* tanks along the clock network for any number
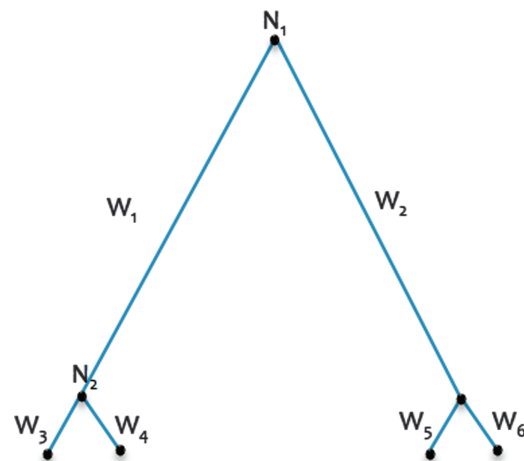

Fig. 3. Simple clock tree with unbalanced branches.

of tanks. Later in this section it is shown that the signal swing for the branches with higher impedance is lower as compared to other branches and resonant behavior can change the capacitive element of the network impedance. Consequently, locating the *LC* tanks considering the capacitive load of the nodes is a proper method to improve the signal swing. In the proposed method, there is at least one *LC* tank from the root to each sink. The method starts with the placement of one *LC* tank at the root. If a full signal swing for all the sinks is not achieved, the number of *LC* tanks is increased and the next candidate *LC* tank is added to the node with the highest capacitance. The number of *LC* tanks is increased until a full swing signal is delivered to all the sink nodes. For each number of *LC* tanks, the transfer function for all the sinks is determined for a wide range of resonant inductance. Using a distributed *RLC* model for the interconnects, the transfer function for each sink can be determined as a function of the resonant inductance. The area allowed for the on-chip inductors sets the upper limit for the inductance range. If there is an inductance range that can satisfy the output voltage swing requirement, the number and location of *LC* tanks have been determined. If increasing the number of *LC* tanks exceeds the upper bound of the permitted area in order to deliver a full swing signal to all the sinks, the *LC* tank locations and resonant inductance that result in the highest amplitude for the transfer function are utilized. After the algorithm has been applied to the clock tree network, other methods, such as buffer insertion can be employed to supply a full swing signal for the sinks.

In the range of inductors that can result in full signal swing, two approaches can be considered. In first approach, called *minPow* hereafter, the power consumption of the network is minimized and in second one called *minArea* the area overhead of the resonant inductors is minimized. The transfer function and power consumed by a clock tree are shown in Figure 4 where selecting L_1 as the resonant inductance for *minArea* reduces the area of these inductors and choosing L_2 for *minPow* results in lower power consumption for the clock network.
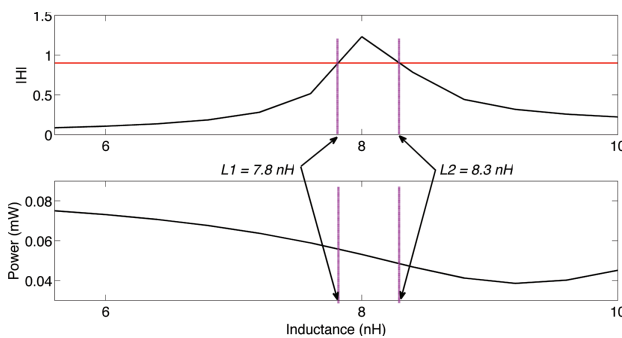
Compared to the method in Ref. [7], which is the only method presented for synthesized trees, the proposed method uses a more efficient parameter (i.e., node impedance) to locate the *LC* tanks and sweeping the resonant inductance results in better power and/or area rather than the first-order estimation used by Ref. [7]. Three basic features of resonant behaviour which are the foundations of the proposed methodology are described hereafter.

Feature 1. For two parallel branches, the branch with the higher impedance exhibits the smaller signal swing.

If we model the entire clock network with a single *RC* π-section as illustrated in Figure 5, the transfer function at the output node is determined by

$$|H| = \frac{1}{\sqrt{\left(1 + R_N^2 C_L C_N \omega^2\right)^2 + R_N^2 \cdot \left(4C_L^2 + C_N^2\right) \cdot \omega^2}} \quad (1)$$

which indicates that by increasing the resistance and capacitance of the clock network denoted by R_N and C_N, respectively, or the load capacitance C_L the amplitude of the transfer function decreases. Consequently, the branch with the higher impedance has the smaller transfer function and exhibits the lower signal swing.

Feature 2. Adding a shunt resonant inductor to a clock network can, simultaneously, reduce the power and improve signal swing.

Resonant behaviour occurs, where in a clock cycle the energy alternates between electric and magnetic fields. In an electric circuit, resonance occurs when the inductive and capacitive parts of the impedance cancel each other. Therefore adding the resonant inductor ideally cancels the imaginary part of the circuit impedance due to the capacitive components. In real (non-ideal) clock networks, since the capacitance is distributed along the interconnects, adding a lumped inductor to the network cannot completely cancel the capacitive part of the impedance. In the π-model of the interconnect, adding the resonant inductor in parallel to capacitance of the network, increases the capacitive part of the impedance. The input impedance of the network and output voltage transfer function can be described as

$$Z_{in} = R + \frac{1}{\frac{1}{X_C} + \frac{1}{R+X_L}} \quad (2)$$

$$\frac{V_o}{V_{in}} = \frac{X_L}{X_L + R} \cdot \frac{1}{1 + R \cdot \left(\frac{1}{X_C} + \frac{1}{R+X_L}\right)} \quad (3)$$
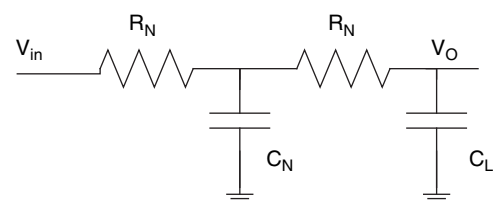

Fig. 4. Signal swing and power consumption versus resonant inductance.

Fig. 5. Lumped model for a clock distribution network.

where X_C and R stand for the capacitive and resistive parts of the clock network impedance, respectively, and X_L denotes for the impedance of the load. As shown in (2), by increasing X_C, the input impedance of the circuit increases, which results in decreasing the power consumed by the clock network where the signal swing is also increased as described by (3).

Feature 3. For a clock tree adding an *LC* tank to a node increases the signal swing of its descendant sinks more than other sink nodes.

A segment of a clock network with two parallel branches is shown in Figure 6. The transfer function from V_{O2} and V_{O3} to V_1 can be determined using (3). By adding the *LC* tank to the first branch, X_{C2} and, consequently, the V_{O2}/V_1 increases where V_{O3}/V_1 is constant.

3.1. LC Placement Algorithm

Based on these features, an algorithm is devised to find the proper location for the *LC* tanks. In a synthesized clock tree, the signal swing at different sink nodes is not equal. As described in Feature 1, the branch with higher impedance exhibits lower signal swing at the sink nodes. Consequently, to provide a uniform signal swing at the sink nodes the signal swing of high impedance branches should increase more than other branches. As mentioned in Feature 2, the signal swing improvement can be achieved adding resonant inductors. Feature 3 suggests adding the resonant inductor to the branches with lower signal swing (i.e., higher impedance) to better improve the signal swing of these branches. Based on these features, the proposed algorithm employs the input impedance of each node as a parameter to locate the *LC* tanks. Since the goal of this algorithm is to reduce the number of *LC* tanks, the algorithm starts with one *LC* tank located at the node with highest impedance (i.e. the root) and increases the number of *LC* tanks to reach the full swing signal at all sink nodes. In each step of the algorithm, the location of the new *LC* tank is determined concerning the input impedance of the intermediate nodes of the clock network.

The algorithm starts from the tree that represents the topology of the distribution network. "Breadth first" traversal is used where each node has a certain level (depth)
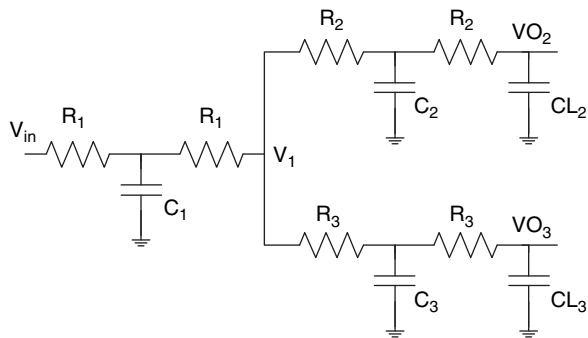
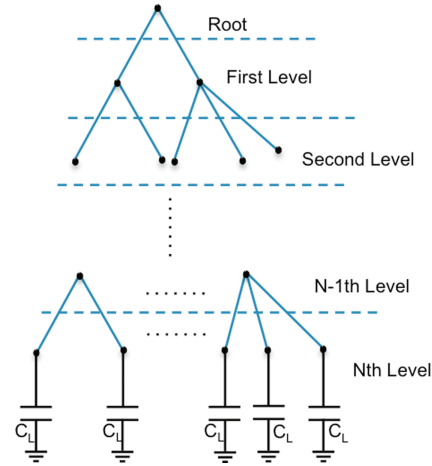

Fig. 6. Two parallel branches of a clock tree.

Fig. 7. Different levels of intermediate nodes for a tree with *N* levels.

in the tree as shown in Figure 7. The algorithm starts by adding one *LC* tank to the root node and evaluating the transfer function at all the sink nodes. A proper method to calculate the transfer function in tree structures is to use Direct Truncation of the Transfer Function (DTT).[11] DTT is a recursive method producing the transfer function of a tree structured interconnect based on the transfer function of the sub-blocks of the circuit. For the circuit shown in Figure 8 the transfer function of node k, $T_k(s)$ is determined as

$$T_k(s) = \frac{N_k(s)}{D_k(s)} \tag{4}$$

$$D_1(s) - N_1(s) = (s \cdot R_1 + s^2 L_1) \cdot \sum_k C_k \cdot N_k(s) \tag{5}$$

$$N_1(s) = D_l(s) \cdot D_r(s) \tag{6}$$

where $N_k(s)$ and $D_k(s)$ are the nominator and denominator of the transfer function at node k and D_l and D_r are the denominators of the transfer function for the right and left sub-blocks. L_k, C_k, and R_k are the inductance, capacitance and resistance at node k, respectively, as shown in Figure 8. This approach is quite convenient for adding and omitting *LC* tanks since each *LC* tank can be treated as a sub-block added in parallel to the clock network circuit.

If the amplitude of the transfer function for all the sinks is more than 0.9, the algorithm terminates. Otherwise, the candidate locations for *LC* tanks are at the nodes of "Level 1." The nodes of "Level 1" are sorted according to the capacitive load seen at each node. First, the *LC* tank is added to the node with the highest capacitive load. The number of *LC* tanks increases until a full swing signal is exhibited to all the sink nodes. If adding the *LC* tank to all the nodes in "Level 1" cannot support a full swing clock signal for the sinks, the algorithm progresses to the next level downstream. The algorithm iterates until the desired signal swing at all sink nodes is achieved or the upper bound for the area of the *LC* tanks has been reached.
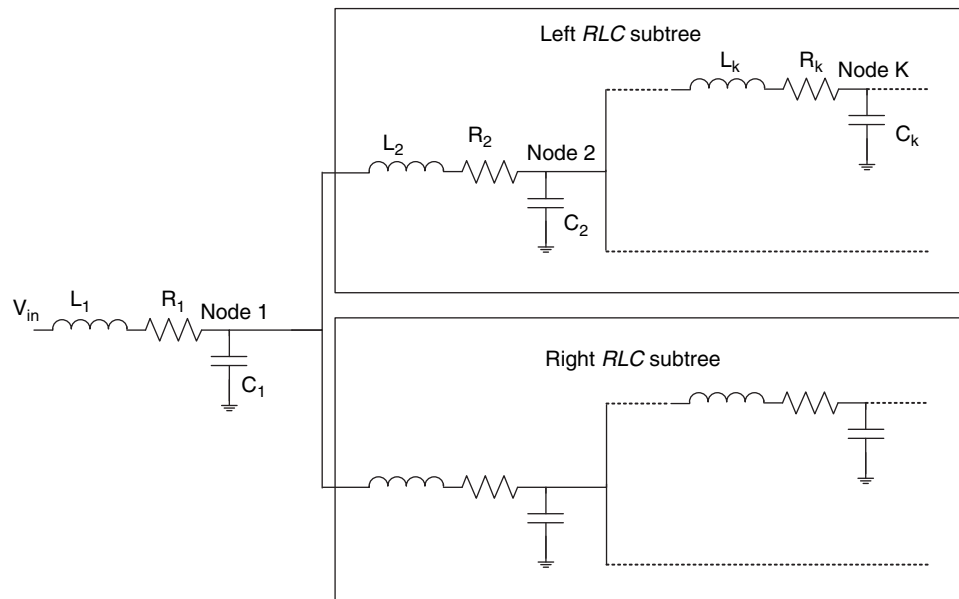
Fig. 8. Sub blocks of the circuit in DTT approach.[11]

ALGORITHM 1. **Pseudo code of LC tanks placement algorithm**

Main
N = Number of levels in tree
Cul = 1/*Current level */
H_{best} = 0
Put initial LC tank location at root
repeat {
    Determine the transfer function
    if (H(L) > Hbest) then
        H_{best} =H(L)
        Best Location = current LC tank location
        *Add-LC-ta*nk (Cul)
Until (voltage swing is satisfied)
Determine-resonant-inductance
}
Determine-resonant-inductance
Design objectives: {minPow, minArea}
for (L | H(L) > 0.9) {
    if minPow
        minimize (power(L)) /* plot power(L) and */
    else if minArea
        minimize (L)
}
return
Add-LC-tank (Cul)
If (CUL is full) {
    if (CUL = N) return
    CUL = CUL+1
}
determine the location of next LC tank
return

This algorithm can reduce the number of *LC* tanks as compared to the previous method of allocating resonant inductors for clock trees,[7] particularly for unbalanced clock trees. Consider the example clock tree shown in Figure 9 where allocating one *LC* tank on the root can provide a full swing signal for sink nodes s_1 to s_4. By using the proposed *LC* location algorithm, which places the second *LC* tank at node n_1, a full swing signal is delivered to nodes s_5 to s_7. In previous method,[7] the *LC* tanks are located at equal distance from the root and exploiting this method for this clock tree requires at least three *LC* tanks to provide a full swing signal for all the sinks.

4. SIMULATION RESULTS

In this section the proposed method is applied to the synthesized clock trees from the 2010 ISPD clock synthesis contest.[10] A clock frequency of 1 GHz is assumed and
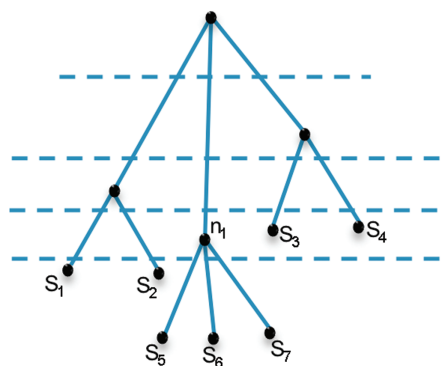

Fig. 9. An example of an unbalanced clock tree.

the technology data for 0.18 μm is used to construct the case studies. The PTM model for a 0.18 μm CMOS technology is used to estimate the parameters of the interconnects. The resistance, capacitance, and inductance of the interconnects are, respectively, 11 Ω/mm, 150 fF/mm, and 0.72 nH/mm. The output resistance of the clock driver is set to 10 Ω. The decoupling capacitor is designed such that the resonant frequency of the capacitor and resonant inductor is much higher than (typically about ten times) the desired clock frequency. The decoupling capacitor is 15 pF which is large enough not to interfere with the operating clock frequency. The power consumption, signal swing, and area of the *LC* tanks of the proposed method are compared with the methods presented in Refs. [7] and [9]. The inductance of a spiral inductor can be estimated as

$$L = K_1 \cdot \mu_0 \frac{n^2 \cdot d_{avg}}{1 + K_2\rho} \qquad (7)$$

where K_1 and K_2 for square inductors are, respectively, 2.34 and 2.75.[12] The average diameter of a square inductor is $d_{avg} = (d_{out} + d_{in})/2$ where d_{out} and d_{in} are the outer and inner diameters of the inductor and $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$. To approximate the area of the resonant inductors, the ratio between d_{out} and d_{in} is considered to be 3, which is a practical ratio to have a proper magnetic flux[13] and results in $\rho = 0.5$. The area of the inductor can be described as:

$$Area = d_{out}^2 = \left(\frac{3 \cdot L \cdot (1 + 0.5 \cdot K_2)}{2 \cdot K_1\mu_0 n^2}\right)^2 \qquad (8)$$

where n stands for the number of turns and for all of the inductors is considered to be four in this work.

To determine the resonant inductance, for LARCS a library of four inductors; 8 nH, 10 nH, 12 nH, and 15 nH is used where for the method presented in Ref. [7] the first-order estimation is utilized. For the proposed method, the *minPow* and *minArea* approaches are considered as discussed in the previous section. When the resonant inductance is determined, the corresponding spiral inductor with a high quality factor and low area should be designed. There are different simulation tools to design spiral inductors such as COMSOL,[14] ASITIC,[15] and Sonnet.[16]

The transfer function for a sink node of a synthesized tree with 1016 sinks is plotted in Figure 10. As shown in this figure, adding 15 *LC* tanks as determined by the proposed method can deliver a full swing signal to the sink nodes where using the LARCS method results in inadequate clock signal swing although 58 *LC* tanks are employed. The method of Ref. [7], adds 14 *LC* tanks to the clock tree where the amplitude of transfer function is 0.5 and clock buffers should be used to deliver a full swing signal to the sinks. Simulation results show that LARCS is not working properly for clock trees, which is expected since this method has been proposed for clock grids.
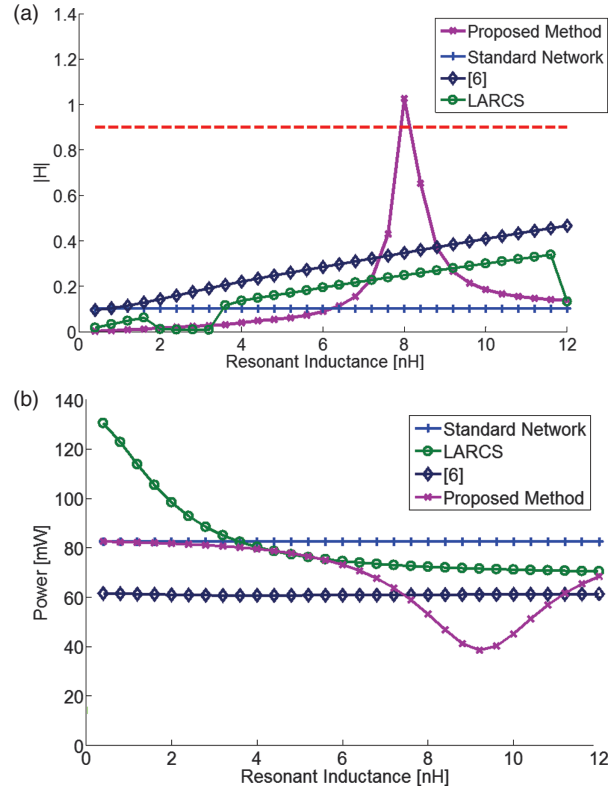

Fig. 10. Comparison of a synthesized tree with 1016 sinks among different design methods where (a) is the transfer function for a sink node and (b) is the power consumption.

Design parameters and simulation results for different clock trees are listed in Tables I and II. Number of *LC* tanks, resonant inductance, and the amplitude of the transfer function for the method proposed in Ref. [7], LARCS, *minPow* and *minArea* are reported in Table I and area overhead, and the power consumed by these methods are listed in Table II. Comparing the two approaches of proposed method shows that the first approach reduces the power consumption up to 14.7% where the second approach reduces the area overhead up to 19%.

The power consumed by the clock distribution network is reduced up to 57% applying the resonant clocking scheme as compared to a standard clock network. The amplitude of the transfer function for Ref. [7] is around 0.5, while the proposed method delivers a full swing signal improving the signal swing up to 80%. The number of *LC* tanks for the proposed method and the method presented in Ref. [7] is comparable where the *minPow* algorithm leads to an inductor area decrease by 51% since the inductors used by the proposed method are smaller than the inductors determined by the first order estimation in Ref. [7]. This situation is because the first-order estimation neglects the inductive parameters of the interconnect and overestimates the resonant inductance. This improvement increases up to 57% for the *minArea*. Simultaneously, the power consumed by the proposed method is decreased up

Table I. Design parameters for different design methodologies.

| | [6] | | LARCKS [7] | | Proposed method | | |
| | | | | | | *minPow* | *minArea* |
# sinks	# *LC* tanks	Res_Ind (nH)	# *LC* tanks	Res_Ind (nH)	# *LC* tanks	Res_Ind (nH)	Res_Ind (nH)
1107	14	11.5	58	10	15	8.3	7.8
2249	27	15	71	12	23	10.8	9.7
1845	20	13	63	10	18	9.6	9
1915	19	20	42	15	18	16.2	14.5
1016	15	18	35	15	13	16	13
1134	17	19.5	29	15	14	15	12.5

Table II. Power consumption and inductor area for different design methodologies.

	[6]			LARCKS [7]			Proposed method					
								minPow		*minArea*		
			Ind Area			Ind Area			Ind Area		Ind Area	Power
# sinks	Power (mW)	|H|	(mm^2)	Power (mW)	|H|	(mm^2)	|H|	Power (mW)	(mm^2)	Power (mW)	(mm^2)	standard (mW)
1107	60	0.5	10.6	70	0.35	47.5	0.9	47	6	55	5.25	113
2249	136	0.43	34.8	184	0.3	58.2	0.9	116	15.4	134	12.4	271
1845	45	0.45	19.4	138	0.4	51.6	0.9	37	9.4	41	8.28	68
1915	36	0.55	43.6	41	0.48	54.2	0.9	29	27.1	33	21.7	59
1016	28	0.57	27.8	35	0.53	45.2	0.9	21	19.1	24	12.6	43
1134	40	0.6	37	54	0.55	37.4	0.9	32	18	37	12.5	61

to 25% and 14% for the *minPow* and *minArea* approach as compared to the method presented in Ref. [7]. Using the proposed method drastically decreases the resonant inductance compared to previous methods. Although the inductor area for *minArea* is 19% less than *minPow*, comparing to the previous methods the area improvement for these two methods is in the same range.

5. CONCLUSIONS

A design method to apply resonant clocking to clock trees is proposed. A "breadth first" tree traversal algorithm is employed and the *LC* tanks are swept from the highest capacitive nodes of the topmost level to the clock sinks to determine the minimum number of *LC* tanks and the size of *LC* tanks. The transfer function of the sink nodes and the power consumption of the clock network for a wide range of resonant inductance are explored to determine the amount of resonant inductance that results in a full swing clock signal at the sink nodes. Two approaches are presented where in the first approach the inductance that minimizes the power is determined as the resonant inductance and, in the second approach, the inductance that results in the least area overhead is determined as the inductance of the *LC* tanks.

The power consumed by the resonant clock tree produced by the new method is significantly lower than the standard clock network. Up to 57% power reduction is achieved in simulated case studies. Comparing the proposed method with previous methods shows up to 80%

improvement in the amplitude of the transfer function at the sink nodes by locating the *LC* tanks in proper nodes of the tree. Using fewer number of *LC* tanks and smaller resonance inductors reduces the area up to 51% as compared to previous methods. Proper allocation of *LC* tanks, using a distributed *RLC* model for the clock network and sweeping the resonant inductance also reduces the power consumption of the proposed method up to 25% as compared to previous methods. Comparing *minPow* and *minArea* approaches shows that the *minPow* reduces the power consumption up to 14.7% where the *minArea* reduces the area overhead up to 19%.

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