Towards Structured ASICs using Polarity-Tunable Si Nanowire Transistors

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Abstract

In addition to scaling semiconductor devices down to their physical limit, novel devices show enhanced functionality compared to conventional CMOS. At advanced technology nodes, many devices exhibit ambipolar behavior, i.e., they show *n*- and *p*-type characteristics simultaneously. This phenomenon can be tamed using double-gate structures. In this paper, we present a complete framework relying on *Double-Gate-all-around Vertically stacked NanoWire FETs* (DG-NWFETs). Such device enables a compact realization of arithmetic logic functions and presents unprecedented interest for structured ASIC applications.

Categories and Subject Descriptors

[Hardware] Emerging technologies – Circuit substrates

General Terms

Design, Performance

Keywords

Nanowire transistors; controllable polarity; regular fabrics; XOR logic synthesis

1. Introduction

During the last four decades, the increase of computing power was achieved by reducing the dimensions of semiconductor devices down to the nanoscale. Today, the semiconductor industry is approaching the ultimate limits of conventional silicon-based *Integrated Circuits* (IC) and researchers are focusing their effort on identifying possible approaches that will enable the continuation of Moore's scaling law. Keeping the trend towards "More Moore", FinFET transistors are successfully replacing planar CMOS transistors at the 22-nm technology node [1]. Further, they are expected to evolve in the next few years to *vertically-stacked Silicon NanoWires Field Effect Transistors* (SiNWFETs) [2]. Indeed, by splitting the 2-D thin film channel in a collection of 1-D *Gate-All-Around* (GAA) structures, the device exhibits higher *Ion/Ioff* ratio and reduced leakage current [3].

In addition to this traditional path, the "More than Moore" approach emerged in the last decade and consists of adding functionality to keep increasing its computation power. Widely used at the system level, this approach is also valid at the device level, where devices can present an enhanced-functionality. In particular, several novel devices demonstrate controllable polarity [4-7]. At advanced technology nodes, an increasingly larger number of devices are affected by Schottky contacts at the source and drain interfaces. Hence, such devices face an ambipolar behavior, i.e., that the devices exhibit *n*- and *p*-type characteristics simultaneously. While technologists aim at suppressing the ambipolar behavior of the devices through additional process steps, the construction of independent double-gate structures can tame it. As a result, the device polarity can be electrostatically programmed to be either *n*- or *p*-type. The functionality of such a device is biconditional on both gate values and enables a compressed realization of XOR-based logic functions, which are not implementable in CMOS in a compact form [8], as well as the realization of ultra-fine grain configurable logic cells [9].

In this paper, we present a complete framework associated with the technology of *Double-Gate* SiNWFET (DG-SiNWFET) from technology to CAD tools. The remainder of the paper is organized as follows. In Section 2, we report on our DG-SiNWFET technology. In Section 3, we present its opportunities for realizing arithmetic logic gates. Section 4 introduces the interests of regular arrangements to mitigate the impact of the additional gate, while Section 5 discusses the opportunities from a CAD perspective. The paper is concluded in Section 6.

1. Vertically-Stacked Double Gate NWFETs

Transistors with controllable polarity consist of double-independent gate FETs having one gate regulating the Schottky barriers on source/drain junctions. In this work, we highlight a top-down fabricated, vertically-stacked SiNW FET, featuring two GAA electrodes (Fig. 1).

Vertically-stacked GAA SiNWs represent a natural evolution of FinFET structures, providing the best electrostatic control over the channel and consequently superior scalability properties [10]. In our device, one gate electrode, the *Control Gate* (CG) acts conventionally by turning *on* and *off* the device. The other electrode, the *Polarity Gate* (PG), acts on the side regions of the device, in proximity of the *Source/Drain* (S/D) Schottky junctions, switching the device polarity dynamically between *n*- and *p*-type (Fig. **Error! Reference source not found.**). The voltage ranges applied to the two gates are comparable, and the input and output voltage levels are compatible, resulting in directly cascadable logic gates.

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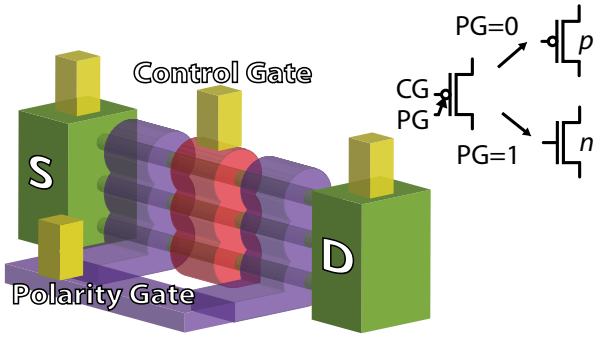

Figure 1. 3D sketch of the SiNWFETs featuring 2 independent gates and its associated symbol.

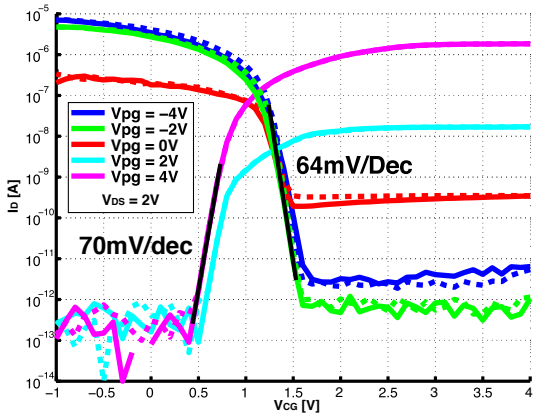

Figure 2. I_{DS}-V_{CG} logarithmic plot of a measured device for serveral V_{PG} voltages. Curves extracted at V_{DS} = 2V [10].

2. Compact Arithmetic Logic Gates

Compared to unipolar transistors, that intrinsically embed the INV function, DG-SiNWFETs can implement natively the XOR operation. Therefore, the realization of arithmetic logic operators can reach a high level of compactness. In particular, with this technology, a full-swing 2-input XOR, reported in Fig. 3a, requires 4 transistors while the traditional full-swing static CMOS implementation uses 8 transistors [11]. Extending the logic design style from static to pass-transistor, the 3-input XOR realization introduced in [12] is obtained, and depicted by Fig. 3b. The same implementation scheme can be used to implement the majority voting operation. Hence, a 4-transistor 3-input majority logic gate is proposed in [13] and reported in Fig. 3c. Note that in static CMOS, the same gate has 10 devices in place of 4 [11]. The compact implementation of both 3-input XOR and 3-input majority function offers an advantageous realization for both the *Sum* and *Carry* functions of *Full-Adder* (FA) gates. Therefore, the FA is competitively realized with 8 devices, input inverters apart, as depicted in Fig. 3d. For comparison, the static (transmission-gate) CMOS counterpart has 28 (14) transistors [11].

3. Towards Stuctured ASICs

Regularity is one of the key features to increase the yield of integrated circuits at advanced technology nodes [14], while keeping the routing complexity under control. The introduced technology presents a unique opportunity to rejuvenate the field. With the electrostatic device configuration, the frontier between *n*- and *p*-branches does not exist anymore. This simplifies the technology realization drastically and enables even more regularity. However, the polarity selection comes at the cost of extra routing. To mitigate this extra-cost, we describe a regular array of elementary logic blocks, called *Sea-of-Tiles* (SoT). This structure, depicted in Fig. 4, was presented as an optimal layout fabric for ambipolar SiNWFET [15].

As introduced in [15], both unate and binate logic functions fit on the regular tile structure reported in Fig. 6a. This structure consists of 4 transistors grouped into pairs. Each pair shares a common source/drain terminal, as well as its polarity gate connection. The connection is done at the polysilicon level to minimize the wiring complexity. The two pairs are aligned in parallel and share their control gates.

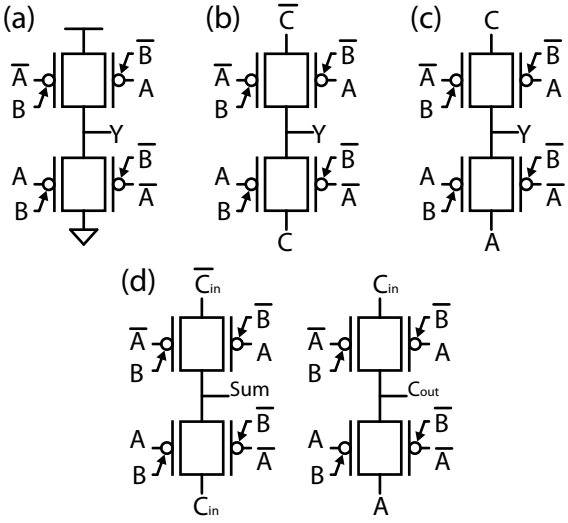

Figure 3. 2-input XOR (a), 3-input XOR (b), 3-input MAJ, 1-bit Full-Adder (d) implementations with DG-SiNWFETs.

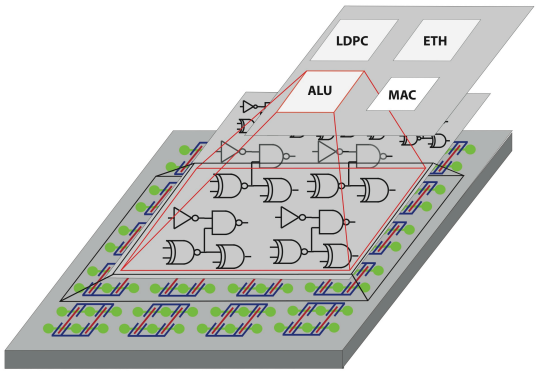

Figure 4. Conceptual representation of a regular *sea-of-tiles*. Tiles are configured to realize logic functions that are part of a complex system [16].

Unate logic functions are obtained by biasing the PGs of the *Pull-Up-Network* (PUN) and *Pull-Down-Network* (PDN) to Gnd and V_{DD} respectively. Hence, all the transistors in the PUN (and PDN) can be grouped together, as shown in Fig. 6b where a 2-input NAND gate example is provided. In the case of binate functions, the polarity gates in the PUN (and PDN) cannot be grouped, leading to extra routing effort. However, the transistor sharing the same polarity gates can be grouped. This is possible, as the

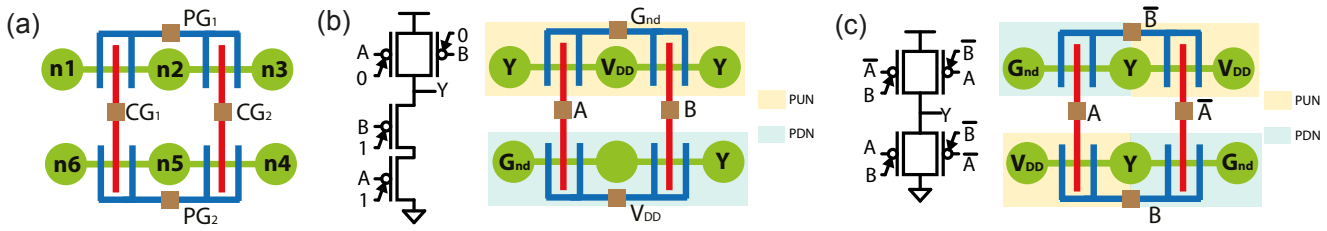

Figure 5. Regular Tile structure sketch from top view (a); Static 2-input NAND gate mapping (b – left: schematic – right: mapped view); Static 2-input XOR gate (c – left: schematic – right: mapped view).

concept of PUN/PDN with segregated *n*- or *p*-type transistors does not hold with the presented technology. An efficient implementation is shown in Fig. 6c with a 2-input XOR gate illustration.

4. CAD Opportunities and Challenges

In this section, we present the novel opportunities and challenges in *Electronic Design Automation* (EDA) targeting logic circuits based on controllable polarity DG-SiNWFETs.

4.1 Logic Synthesis

DG-SiNWFETs intrinsically embed the biconditional (XNOR) logical connective thanks to the on-line re-configuration of the device polarity. Consequently, XOR/XNOR-based logic is remarkably compact and became as efficient as NAND/NOR operations. In order to harness this novel paradigm during automated circuit synthesis, both XOR/XNOR and AND/OR functions must be evidenced and exploited at the same time. A first attempt to achieve effective logic synthesis targeting controllable polarity transistors is MIXSyn [17]. The key feature of MIXSyn is a hybrid logic optimization. A step further in the synthesis of DG-SiNWFETs based circuits is presented in [13] where *Biconditional Binary Decision Diagrams* (BBDDs) are introduced. BBDD is a canonical logic representation form based on the biconditional (XNOR) expansion, which is defined as:

$$f(x,y,..,z) = (x \oplus y) f(y',y,..,z) + (x \overline{\oplus} y) f(y,y,..,z)$$

The one-to-one correspondence between the functionality of DG-SiNWFETs and the core expansion of BBDDs enables an efficient mapping of the devices onto BBDD structures. In this way, the representation compactness of BBDDs is preserved in the final logic circuit.

Recently, it was shown that also majority logic has an efficient implementation with controllable polarity devices [13]. This highlights the interest to extend the capabilities of previous synthesis tools to deal with majority functions, as introduced in [18].

4.2 Physical Synthesis

Despite MIXSyn and BBDDs being efficient means to synthesize logic circuits based on controllable polarity DG-SiNWFETs, they imply challenges at the physical synthesis level. Indeed, both these synthesis flows require on the fly generation of logic cells while currently standard cells are characterized and designed off-line. Regular layout fabrics represent a promising solution to soften this problem. In the context of SoT, direct mapping of logic cells onto a regular array is enabled and therefore supports natively library-free synthesis flows at a limited utilization-efficiency overhead cost.

5. Conclusion

In this paper, we presented a complete design framework of DG-SiNWFET technology involving process, design and automated tools. In particular, we showed how transistors with controllable polarity are interesting from an arithmetic logic perspective and we proposed a credible route for its very large scale integration, through the Sea-of-Tiles organization. Finally, we provided insights on specific CAD research that is motivated by this technology.

6. Acknowledgments

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7. References

[1] C. Auth *et al.*, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," VLSI Tech. Symp., 2012.

[2] S. D. Suk *et al.*, "High performance 5nm radius twin silicon nanowire mosfet (tsnwfet): fabrication on bulk si wafer, characteristics, and reliability," IEDM Tech. Dig., 2005.

[3] S. Bangsaruntip *et al.*, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," IEDM Tech. Dig., 2009.

[4] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter and S. Guha, "Dual-gate silicon nanowire transistors with nickel silicide contacts," IEDM Tech. Dig., 2006.

[5] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick and W. M. Weber, "Reconfigurable Silicon Nanowire Transistors," Nano Letters, vol. 12, pp. 119-124, 2011.

[6] Y.-M. Lin, J. Appenzeller, J. Knoch and P. Avouris "High-Performance Carbon Nanotube Field-Effect Transistor With Tunable Polarities," IEEE Trans. Nanotechnology, vol. 4, pp. 481-489, 2005.

[7] N. Harada, K. Yagi, S. Sato and N. Yokoyama, "A polarity-controllable graphene inverter," Applied Physics Letters, vol. 96, pp. 12102, 2010.

[8] M.H. Ben Jamaa, K. Mohanram and G. De Micheli, "Novel library of logic gates with ambipolar CNTFETs: Opportunities for multi-level logic synthesis," DATE Tech. Dig., 2009.

[9] I. O'Connor *et al.*, "CNTFET modeling and reconfigurable logic-circuit design," IEEE Trans. on CAS, vol. 54, pp. 2365-2379, 2007.

[10] M. De Marchi *et al.*, "Polarity control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs," IEDM Tech. Dig., 2012.

[11] J.M. Rabaey, A.P. Chandrakasan and B. Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentice Hall, 2003

[12] A. Zukovski, Y. Xuebei and K. Mohanram, "Universal logic modules based on double-gate carbon nanotube transistors," DAC. Tech. Dig., 2011.

[13] L. Amarù, P.-E. Gaillardon and G. De Micheli, "Biconditional BDD: A Novel Canonical BDD targeting the Synthesis of XOR-rich Circuits," DATE Tech. Dig., 2013.

[14] T. Jhaveri *et al.*, "Maximization of layout printability/manufacturability by extreme layout regularity," J. of Micro/Nanolith. MEMS, vol.6, 2007.

[15] S. Bobba, M. De Marchi, Y. Leblebici an G. De Micheli, "Physical Synthesis onto a Sea-of-Tiles with Double-Gate Silicon Nanowire Transistors," DAC Tech. Dig., 2012.

[16] P.-E. Gaillardon *et al.*, "Vertically Stacked Double Gate Nanowires FETs with Controllable Polarity: From Devices to Regular ASICs," DATE Tech. Dig., 2013.

[17] L. Amarù, P.-E. Gaillardon and G. De Micheli, "MIXSyn: An Area-Efficient Logic Synthesis Methodology for Mixed XOR-AND/OR Dominated Circuits," ASP-DAC Tech. Dig., 2013.

[18] L. Amarù, P.-E. Gaillardon and G. De Micheli, "BDS-MAJ: A BDD Logic Synthesis Tool Expoliting Majority Logic Decomposition," DAC Tech. Dig., 2013.