# Power-Gated Differential Logic Style Based on Double-Gate Controllable-Polarity Transistors

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***Abstract*—This brief presents a novel power-gating technique for *differential cascade voltage switch logic* (DCVSL) based on *double-gate* (DG) controllable-polarity *field-effect transistors* (FETs). DG controllable-polarity FETs, commonly referred to as ambipolar transistors, are devices whose polarity is *online* reconfigurable by changing the second gate bias. In this brief, we exploit the *online* control of ambipolar device polarity to achieve intrinsically power-gated DCVSL circuits bypassing the use of series sleep transistors. We perform circuit-level simulations and comparisons at 22-nm technology node, considering *silicon nanowire*-based DG controllable-polarity FETs. Experimental results show that ambipolar DCVSL circuits power gated by the proposed technique have on average $6\times$ smaller standby power with only $1.1\times$ timing penalty with respect to their non-power-gated versions. As compared with unipolar FinFET-based realizations, our proposal is capable to reduce up to $1.9\times$ the standby power consumption of a low-standby-power process and, at the same time, increase up to 10% the performance of a high-performance process.**

***Index Terms*— Circuit topology, double-gate FETs, logic gates, power dissipation.**

## I. Introduction

LEAKAGE power is one of the major concerns in contemporary *integrated circuits* [1]. In order to alleviate this issue, technology and design countermeasures are used in conjunction. On the one hand, *low-standby-power* (LSTP) *field-effect-transistor* (FET) technologies enable a marked reduction of the device leakage currents, but they are slower and bigger than their *high-performance* (HP) counterparts. On the other hand, design techniques further minimize the leakage power consumption. Among them, power gating [2]–[5] is an effective and widely used design technique where sleep transistors are employed to disconnect the power supply from the rest of the circuit during idle time. The main drawbacks of power gating are due to the series sleep transistor that: 1) reduces the speed during normal operation; and 2) increases the circuit area.

Emerging nanotechnologies enable new circuit design opportunities that overcome previous limitations of traditional *complementary metal–oxide–semiconductor* (CMOS) technology. In particular, *double-gate* (DG) FETs with controllable polarity, referred here to as ambipolar transistors, are emerging devices that can be online configured to either $n$- or $p$-type via the second gate. Ambipolar transistors have been fabricated in carbon nanotube [6], graphene [7], and *Silicon NanoWire* (SiNW) [8] technologies.

In this brief, we exploit controllable-polarity DG-SiNWFETs to achieve power-gated *differential cascade voltage switch logic* (DCVSL) circuits with no series sleep transistor. We showcase the impact of the proposed approach at 22-nm technology node. Circuit-level electrical simulations show that ambipolar DCVSL circuits power gated by the proposed technique have on average $6\times$ smaller standby power with only $1.1\times$ timing penalty compared with their non-power-gated implementations. With respect to the same implementations based on unipolar FinFETs, our proposal has up to $1.9\times$ smaller standby power than an LSTP process and, at the same time, up to 10% more performance than an HP process.

The remainder of this brief is organized as follows. Section II introduces DG controllable-polarity transistors. Section III presents the proposed power-gating methodology for ambipolar DCVSL circuits. In Sections IV and V, comparison results for power-gated DCVSL logic gates and circuits implemented in ambipolar and FinFET technology are presented. In Section VI, the interest of our proposal is discussed at the light of the experimental results. This brief is concluded in Section VII.

## II. DG Controllable-Polarity Transistors

DG controllable-polarity devices, also called ambipolar devices, are transistors whose polarity is electrically configurable via the second gate. This is in contrast to traditional unipolar devices, where the polarity is determined during fabrication by chemical doping. Ambipolar transistors have been successfully fabricated in carbon nanotube [6], graphene [7], and SiNW [8] technologies. As the natural evolution of FinFET structure, vertically stacked SiNWs are a promising platform for DG controllable-polarity devices due to their high $I_{\rm on}/I_{\rm off}$ ratio and CMOS-compatible fabrication process [8]. Such device, as depicted in Fig. 1(a), consists of three vertically stacked SiNWs and three gated regions. The side regions are tied together to the *polarity gate* (PG), whereas the central region is tied to the *control gate* (CG). The PG tunes the Schottky barriers at the S/D junctions choosing the channel carriers' type ($V_{\rm PG} = V_{dd} \Rightarrow n$ - type, $V_{\rm PG} = V_{ss} \Rightarrow p$ - type), whereas the CG modulates the amount of carriers flowing into the channel. Fig. 1(b) shows the $I$–$V$ characteristic for a 22-nm device simulated using a

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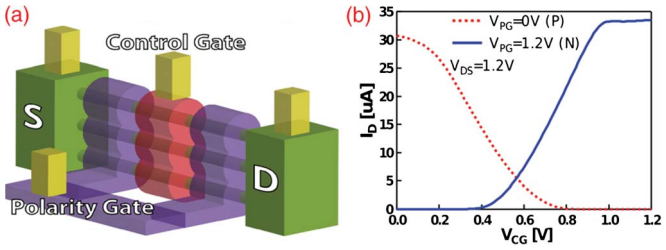


Fig. 1. (a) Conceptual structure of an ambipolar transistor with vertically stacked SiNWs. (b) $I$–$V_{\mathrm{CG}}$ plot of a simulated controllable-polarity DG-SiNWFET for $V_{\mathrm{PG}} = 0$ V and $V_{\mathrm{PG}} = 1.2$ V ($V_{ds} = 1.2$ V) [8].

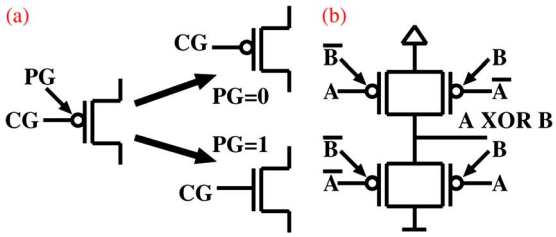


Fig. 2. (a) Ambipolar transistor polarity (re)configuration. (b) Full-swing XOR-2 gate with four ambipolar devices.

TCAD model fitted onto experimental devices [8]. We refer the interested reader to [8] for more details about the physics of DG-SiNWFETs.

The online configuration of $n$- or $p$-type polarity in ambipolar transistors is depicted in Fig. 2(a). Such enhanced functionality makes it possible to implement XOR-based logic gates with fewer resources, as compared with traditional unipolar devices. Fig. 2(b) depicts an XOR-2 logic gate implemented with only four ambipolar devices [9]. The standard CMOS counterpart uses 2× more devices, input inverters apart [10].

## III. Power-Gated Ambipolar DCVSL

This section first introduces ambipolar DCVSL circuits and then describes the proposed power-gating technique for ambipolar DCVSL style.

### A. Ambipolar DCVSL

DCVSL is a general logic style that implements a logic function and its complement simultaneously [11]. A DCVSL logic gate consists of two mutually exclusive *pull-down* (PD) networks driving two *pull-up* (PU) devices intertwined in a positive feedback. While traditionally realized with unipolar transistors, DCVSL style is naturally extended to DG ambipolar devices. Fig. 3(a) depicts an XOR/XNOR-2 logic gate realized in DCVSL style with ambipolar transistors.

PU devices behave as $p$-type having their PGs fixed to logic zero. PD networks implement the XOR/XNOR functions with fewer devices, as compared with unipolar counterparts due to the enhanced capabilities of ambipolar transistors. Note that we assume that an ambipolar DCVSL logic gate/cell is composed by only ambipolar transistors. If unipolar behavior is needed, or preferable, in some part of the circuit, it is emulated by fixing the voltage at the PG.

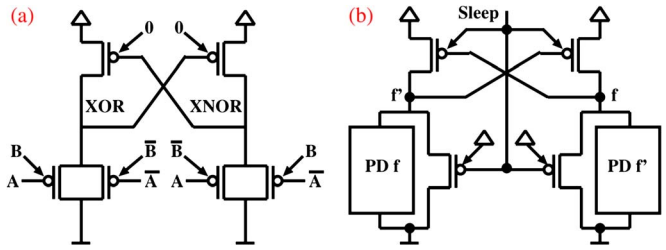


Fig. 3. (a) Ambipolar DCVSL XOR/XNOR-2 gate with no power gating. (b) Ambipolar DCVSL style with the proposed embedded power gating.

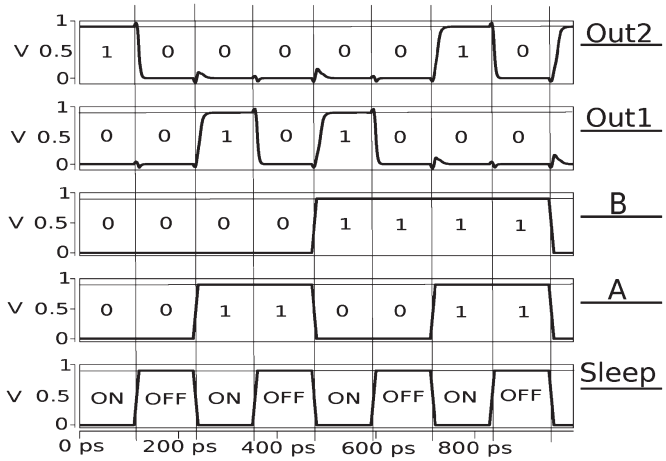


Fig. 4. Simulation waveforms for the proposed power gating of ambipolar DCVSL XOR/XNOR-2 gate.

### B. Ambipolar DCVSL Style With Embedded Power Gating

DCVSL ambipolar gates are promising to implement compact logic due to the controllable-polarity feature. On top of the logic compactness achievable, ambipolar devices enable also new efficient power-gating opportunities. In contrast to traditional sleep transistor-based approaches, ambipolar DCVSL gates can be power gated with no additional series device, thereby avoiding major performance degradation. This concept is reported in Fig. 3(b) and explained hereafter.

In the proposed power-gating method, PU ambipolar devices are not fixed to behave as $p$-type but their polarity is online modulated by the *Sleep* signal, which is connected to the PGs. Together with floating output countermeasures (two $n$-type devices in parallel to the PD networks), the PU polarity control automatically provides the demanded disconnection from the power supply during standby mode. A detailed study of the circuit behavior for each operation mode is as follows.

*1) Standby Operation Mode:* In the standby mode ($Sleep = 1$), the ambipolar PU devices are switched to $n$-type through the PGs. The CGs are tied to logic 0 by the two additional $n$-type devices. Therefore, during the standby mode, both ambipolar PU devices are in the *off*-state since $\mathrm{PG} = 1$ and $\mathrm{CG} = 0$ ($\mathrm{PG} \overline{\oplus} \mathrm{CG} = 0$). This provides the desired disconnection from the power supply.

*2) Active Operation Mode:* In the active operation mode ($Sleep = 0$), the ambipolar PU devices are configured as $p$-type. The CGs (connected to the gate outputs) are not anymore tied to logic 0 since the two additional $n$-type devices are in the *off*-state. The PD networks are now enabled to drive the outputs and close the standard feedback in DCVSL gates via the

TABLE I
HSPICE SIMULATIONS FOR VARIOUS LOGIC GATES IN DCVSL STYLE

| Circuit type | PoWer-Gate (PW-G) | FinFET HP | | FinFET LSTP | | Ambipolar SiNWFET | | |
|---|---|---|---|---|---|---|---|---|
| | | PW-G Standard | No PW-G | PW-G Standard | No PW-G | PW-G Standard | PW-G Proposed | No PW-G |
| XOR/XNOR-2 | Sleep Power ($pW$) | 4417.88 | 1.57e04 | 4.28 | 14.43 | **1.18** | 2.18 | **13.70** |
| | Dynamic Power @1 $GHz$ ($\mu W$) | 0.21 | 0.12 | 8.67 | 3.24 | 0.42 | **0.12** | **0.09** |
| | Delay *worst case* ($ps$) | 88.29 | **50.44** | 666.42 | 455.90 | 319.05 | **80.14** | 71.18 |
| | Wake-up time ($ps$) | **20.71** | - | 29.41 | - | 296.90 | 52.87 | - |
| | PDP ($aJ$) | 213.66 | 109.45 | 8.67e03 | 3.24e03 | 421.14 | **119.40** | **94.66** |
| | SPDP ($yJ$) | 3.90e05 | 7.91e05 | 2.85e03 | 6.57e03 | 376.47 | **174.70** | **975.16** |
| | Area ($\mu m^2$) | 0.95 | 0.69 | 1.28 | 0.93 | 0.99 | **0.88** | **0.66** |
| AND/NAND-2 (OR/NOR-2) | Sleep Power ($pW$) | 4418.00 | 1.00e04 | 4.28 | 9.31 | **1.19** | 2.05 | **8.90** |
| | Dynamic Power @1 $GHz$ ($\mu W$) | **0.10** | **0.05** | 2.74 | 1.21 | 0.34 | 0.22 | 0.18 |
| | Delay *worst case* ($ps$) | **82.66** | **46.33** | 646.10 | 406.10 | 426.28 | 218.30 | 196.50 |
| | Wake-up time ($ps$) | **18.75** | - | 27.02 | - | 318.35 | 55.43 | - |
| | PDP ($aJ$) | **186.81** | **90.80** | 5.490e03 | 2.41e03 | 682.04 | 445.33 | 363.52 |
| | SPDP ($yJ$) | 3.65e05 | 4.63e05 | 2.76e03 | 3.78e03 | 507.27 | **447.51** | **1.74e03** |
| | Area ($\mu m^2$) | **1.12** | **0.86** | 1.51 | 1.16 | 1.43 | 1.32 | 1.10 |
| Generalized AOI/OAI | Sleep Power ($pW$) | 6176.09 | 1.62e04 | 8.55 | 15.23 | **3.20** | 5.04 | **11.36** |
| | Dynamic Power @1 $GHz$ ($\mu W$) | **0.12** | **0.07** | 4.18 | 2.34 | 0.39 | 0.24 | 0.20 |
| | Delay *worst case* ($ps$) | **92.82** | **53.07** | 701.76 | 569.10 | 466.70 | 228.75 | 203.21 |
| | Wake-up time ($ps$) | **20.74** | - | 30.51 | - | 342.92 | 53.65 | - |
| | PDP ($aJ$) | **247.82** | **124.66** | 8.37e03 | 4.69e03 | 779.39 | 491.81 | 406.42 |
| | SPDP ($yJ$) | 5.73e05 | 8.59e05 | 6.00e03 | 8.67e03 | 1.49e03 | **1.15e03** | **2.31e03** |
| | Area ($\mu m^2$) | 1.30 | 1.04 | 1.75 | 1.40 | 1.21 | **1.10** | **0.88** |
| Multiplexer 2:1 | Sleep Power ($pW$) | 4417.55 | 1.57e04 | 4.28 | 14.44 | **2.04** | 3.74 | **12.50** |
| | Dynamic Power @1 $GHz$ ($\mu W$) | **0.09** | **0.04** | 3.90 | 1.45 | 0.40 | 0.25 | 0.19 |
| | Delay *worst case* ($ps$) | **87.75** | **52.91** | 659.62 | 491.03 | 446.33 | 217.65 | 198.14 |
| | Wake-up time ($ps$) | **20.74** | - | 29.10 | - | 329.81 | 51.55 | - |
| | PDP ($aJ$) | **95.55** | **51.66** | 3.86e03 | 1.57e03 | 745.37 | 444.06 | 366.56 |
| | SPDP ($yJ$) | 3.87e05 | 8.30e05 | 2.82e03 | 7.09e03 | 910.51 | **814.01** | **2.47e03** |
| | Area ($\mu m^2$) | **0.95** | **0.69** | 1.28 | 0.93 | 1.21 | 1.10 | 0.88 |

PU devices. Note that, during active operation mode, the circuit is the same as its non-power-gated versions' exception made for the two parallel $n$-type devices . The equivalent slowdown due to power gating is here only dependent on the additional drain capacitance carried by the extra parallel $n$-type device. Instead, in traditional power gating, the slowdown is more marked due to the extra series sleep transistor.

## IV. DCVSL GATE SIMULATION

In this section, we first validate the correctness of the proposed power-gating technique in 22-nm SiNW ambipolar technology. Then, we simulate several SiNW ambipolar DCVSL cells employing our power-gating method, and we compare them to traditional power-gating solution. FinFETs are considered as state-of-art unipolar technology reference.

### A. Correctness of the Proposed Power Gating

The correctness of the proposed power-gating technique is evaluated with vertically stacked SiNWs at 22-nm technology node using electrical circuit-level simulations. The ambipolar transistor (four vertically stacked SiNWs, three gated regions) is characterized using Synopsys Sentaurus, and the obtained results are employed to create a SPICE-compatible table model. Then, this model is run in the HSPICE simulator engine. Fig. 4 shows the simulated waveforms for a power-gated XOR/XNOR-2 ambipolar DCVSL cell. The correct behavior of the XOR/XNOR-2 function is noted when $Sleep = 0$ (active mode), whereas when $Sleep = 1$ (standby mode), both outputs assume the logic 0 value regardless of the other inputs. Note that the wake-up time is comparable with the regular logic gate delay permitting a fast standby to active mode transition.

### B. Simulation Setup

Simulations in ambipolar SiNW technology are run with the same setup described above. FinFET technology is considered as state-of-art unipolar reference. FinFET HP and LSTP 22-nm SPICE-compatible models are taken from [12]. The power supply voltage is set to 0.9 V for both FinFETs and SiNWFETs according to the 22-nm technology node typical working point [1]. Traditional power gating uses a series header sleep transistor and parallel $n$-type devices at PD networks to avoid floating outputs during standby mode. The logic functions designed are XOR/XNOR-2, AND/NAND-2, OR/NOR-2, generalized AOI/OAI [9], and MUX 2:1. In the simulation environment, DCVSL gates are loaded at each output with 0.5 $f$F. For dynamic power measurement purposes, the input signals switch at 1-GHz frequency.

### C. Results

Table I presents the full set of results, including performance, power consumption, and area for various DCVSL gate implementations. The area is computed considering the physical occupation of DG ambipolar SiNWFETs, as shown in Fig. 1(a); LSTP FinFETs; and HP FinFETs at the 22-nm technology node. PU/PD devices in DCVSL gates are sized to guarantee the correct functionality of the logic circuit, i.e., the PD networks are made stronger than the PU devices. The *power-delay product* (PDP) and the *sleep PDP* (SPDP) are used as comparison metrics. The best results for each power-gated DCVSL cell are highlighted in blue in Table I. The best results for the non-power-gated versions are evidenced in red. Note that, in the proposed approach, the sleep power consumption is slightly increased with respect to traditional power-gated ambipolar

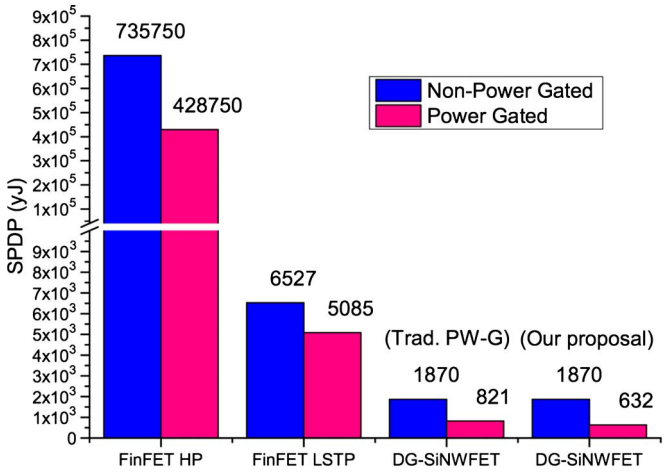


Fig. 5. Average SPDP metric for the DCVSL gates.

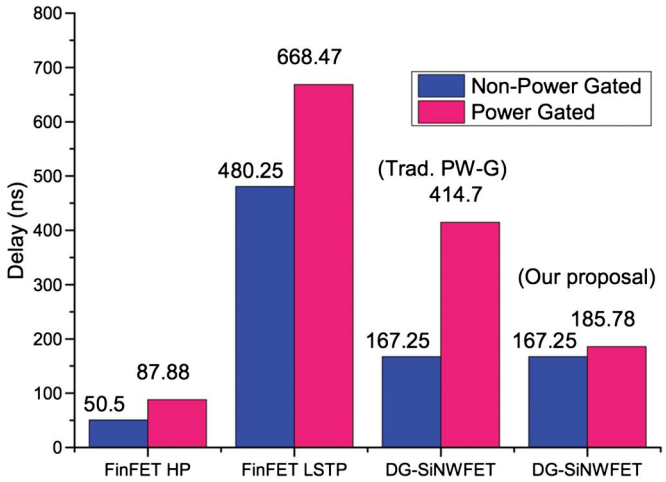


Fig. 6. Average delay for the simulated DCVSL gates.

SiNW DCVSL circuits. This is because of the additional series device that, on the one hand, can further reduce the sleep power but, on the other hand, generates major penalties for the performance. The SPDP metric provides information about the sleep power/performance tradeoff.

*1) SPDP Metric:* The SPDP measures the tradeoff between leakage reduction and performance loss. As for the standard PDP metric, low values of SPDP are desirable. Power gating is a design technique that aims to reduce the SPDP metric, therefore introducing more leakage suppression than delay penalties. Fig. 5 shows average SPDP results for the simulated DCVSL gates. In ambipolar DCVSL gates, traditional power gating (header sleep transistor) is able to decrease the SPDP from 1870 to 821 $y$J corresponding to a 56.1% reduction. Our proposed power-gating technique further lowers the SPDP to 632 $y$J, which is 23.0% smaller than traditional power-gated counterpart and 66.2% smaller than non-power-gated version. The marked SPDP reduction, or increase in power-gating efficiency, derives from the absence of sleep transistors that represent the major source of inefficiency in power gating.

Considering unipolar FinFET technology, non-power-gated HP and LSTP achieve SPDPs equal to 735 750 and 6527 $y$J, respectively. The HP process has more than two orders of magnitude larger SPDP than the LSTP process. Indeed, FinFET HP is not convenient for LSTP designs. The impact of power gating in FinFET HP and LSTP is an SPDP reduction of 41.7% and 22.1%, respectively.

Ambipolar SiNW technology is capable to reach lower absolute SPDP values than FinFET technology due to its superior electrostatic control [8]. With respect to relative SPDP reduction figures, the ambipolar sleep-transistor-less power gating presents the highest percentage (66.2%) evidencing the net advantage of the proposed method.

*2) Delay:* The major drawback of traditional power gating is the increased delay due to the series sleep transistor. Fig. 6 shows the average delay results for both power-gated and non-power-gated DCVSL logic gates. In ambipolar SiNW technology, traditional power gating slows down the DCVSL gate about $2.5\times$ compared with the standard (non-power-gated) version. Instead, the proposed power-gating technique implies a delay overhead of just 9.5%, resulting in minor global performance penalties. Moreover, the wake-up time in the proposed power gating is reduced by $6.2\times$ with respect to the traditional method.

In unipolar FinFET technology, traditional power gating still implies a marked speed reduction of $1.7\times$ in an HP process and $1.4\times$ in an LSTP process.

Considering absolute delay values, FinFET HP provides the fastest power-gated implementation. However, the delay increase in the proposed ambipolar power-gated design, with respect to the fastest FinFET HP, is only $2.1\times$, whereas in traditional ambipolar power gating, it is $4.7\times$, and in FinFET LSTP, it is $7.6\times$.

Again, the promising characteristics shown by DCVSL gates designed by the proposed technique are enabled by the enhanced flexibility of controllable-polarity devices.

## V. Arithmetic Circuit Design and Simulation

In order to demonstrate the interest of the proposed method for practical applications, we have designed and simulated: 1) an 8-input parity check circuit; and 2) a 3-bit full adder DCVSL circuit, which are widely used in digital designs.

### A. Eight-Bit Parity Circuit

An 8-bit parity circuit implements function $f = a_0 \oplus a_1 \oplus \ldots \oplus a_7$. We design such circuit using a three-level binary tree of XOR/XNOR-2 DCVSL gates.

Simulation results for the 8-bit parity circuit are shown in Table II. The simulation setup is the same as in Section IV. Among the power-gated implementations, our proposed approach for ambipolar technology achieves the best delay, PDP, SPDP, and area. FinFET technology produces globally worse results for the 8-bit parity power-gated circuit. Indeed, for XOR-rich circuits, ambipolar technology offers a very compact logic implementation that further evidences the advantage of the sleep-transistor-less power-gating method proposed. As compared with its non-power-gated version, our ambipolar design has only 13% more delay but $6.6\times$ less static power.

TABLE II
HSPICE SIMULATIONS FOR COMPOSED CIRCUITS IN DCVSL STYLE

| Inputs | Circuit type | PoWer-Gate (PW-G) | FinFET HP | | FinFET LSTP | | Ambipolar SiNWFET | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | PW-G Standard | No PW-G | PW-G Standard | No PW-G | PW-G Standard | PW-G Proposed | No PW-G |
| 8 | Parity Check | Sleep Power ($pW$) | 2.74e04 | 1.11e05 | 43.49 | 167.64 | **13.84** | 25.78 | **164.89** |
| | | Dynamic Power @ 0.4 $GHz$ ($\mu W$) | 0.76 | **0.32** | 47.63 | 17.11 | 2.85 | **0.70** | 0.48 |
| | | Delay *worst case* ($ps$) | 162.23 | **108.95** | 2.25e03 | 1.64e03 | 685.70 | **126.89** | 111.89 |
| | | PDP ($aJ$) | 1.89e03 | **555.64** | 1.19e05 | 4.27e04 | 7.13e03 | **1.76e03** | 1.20e03 |
| | | SPDP ($yJ$) | 4.44e06 | 1.20e07 | 9.78e04 | 2.74e05 | 9.49e03 | **3.27e03** | **1.85e04** |
| | | Area ($\mu m^2$) | 6.15 | 4.85 | 8.31 | 6.54 | 6.31 | **5.75** | **4.65** |
| 3 | Full Adder | Sleep Power ($pW$) | 1.32e04 | 5.22e04 | 12.86 | 71.30 | **3.56** | 5.91 | **49.27** |
| | | Dynamic Power @ 0.7 $GHz$ ($\mu W$) | 0.95 | **0.36** | 16.35 | 9.89 | 2.09 | **0.87** | 0.56 |
| | | Delay *worst case* ($ps$) | **156.20** | **91.97** | 1.42e03 | 1.10e03 | 295.80 | 171.18 | 159.78 |
| | | PDP ($aJ$) | 1.49e03 | **565.61** | 2.32e04 | 1.38e04 | 3.06e03 | **1.26e03** | 893.17 |
| | | SPDP ($yJ$) | 2.06e06 | 4.80e06 | 1.82e04 | 7.84e04 | 1.05e03 | **1.01e03** | **7.87e03** |
| | | Area ($\mu m^2$) | 2.87 | **2.08** | 3.86 | 2.80 | 3.21 | **2.86** | 2.21 |

### B. Full Adder Circuit

A full adder circuit implements functions $Sum = a \oplus b \oplus c$ and $C_{\text{out}} = Majority(a, b, c)$. The sum function can be directly implemented by two cascaded XOR/XNOR-2 DCVSL gates respectively for $x = a \oplus b$ and $Sum = x \oplus c$. Exploiting the intermediate function $x$, $C_{\text{out}}$ can be implemented using a MUX 2:1 DCVSL gate as $C_{\text{out}} = MUX(Sel = x, I_0 = b, I_1 = c)$. Such implementation requires two XOR/XNOR-2 gates and one MUX 2:1 DCVSL gate.

Simulation results for the full adder circuit are shown in Table II. The ambipolar full adder power gated by the proposed method presents the best PDP, SPDP, and area compared with traditional power-gating techniques in ambipolar and FinFET technologies. The best delay, with power gating, is achieved by FinFET HP with 156.20 ps being only 8.7% smaller than our proposal. For our ambipolar power-gating proposal, the delay overhead with respect to non-power-gated version is only 6.8% and the static power is $8.3\times$ smaller.

## VI. DISCUSSION

A major drawback of power gating is the timing penalty due to the series sleeping transistor. Indeed, when high speed is a fundamental requirement in designs, power gating is generally not applied. In FinFET 22-nm technology, traditional power gating reduces DCVSL cells' speed by $1.4\times$ in the LSTP process and by $1.7\times$ in the HP process. On the other hand, the leakage power suppression derived from power gating accounts for about $4\times$ in FinFET HP and for about $5\times$ in FinFET LSTP. Consequently, power gating enables a leakage suppression larger than its delay penalty. However, such performance loss is still quite marked, therefore limiting a broad application of traditional power-gating technique in current technologies. Exploiting instead the emerging DG controllable-polarity (ambipolar) devices, our proposed power-gating technique is capable to overcome previous performance limitations. Achieving a leakage power reduction of about $6\times$, our ambipolar power-gating proposal produces DCVSL cells only 9.5% slower compared with their non-power-gated versions. This promising feature opens up the opportunity to extend power gating to a wider class of designs, achieving superior low-leakage/HP circuits.

## VII. CONCLUSION

In this brief, we have presented a novel power-gating technique for DCVSL cells based on DG controllable-polarity (ambipolar) FETs. The proposed technique enables power gating of DCVSL cells, based on ambipolar devices, at almost no timing penalty. In 22-nm SiNW ambipolar transistor technology, simulation results show that DCVSL circuits power gated by the proposed technique have on average $6\times$ smaller standby power with only $1.1\times$ timing penalty with respect to their non-power-gated versions. Compared with FinFET 22-nm technology, the simulated power-gated ambipolar DCVSL circuits are up to 10% faster than an HP process and, at the same time, have up to $1.9\times$ smaller standby power consumption than an LSTP process.

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