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Vertically-stacked gate-all-around polysilicon nanowire FETs with sub-μm gates patterned by nanostencil lithography

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ABSTRACT

We report on the top-down fabrication of vertically-stacked polysilicon nanowire (NW) gate-all-around (GAA) field-effect-transistors (FET) by means of Inductively Coupled Plasma (ICP) etching and nanostencil lithography. The nanostencil is used to form sub-μm GAA gates over polysilicon NW array channels with high aspect ratio, considerably simplifying the lithographic steps above regions with deep 3D topography and non-planar surface features. This process lead to fabrication yields larger than 70% and authors envisage even larger yields of $\geqslant 85\%$ with optimized mask design. Electrical measurements confirm the results obtained from similar devices fabricated with a standard lithography method while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling.

1. Introduction

Future technological innovations enabling ever higher circuit densities predicted by Moore's law will most likely be concentrated on novel materials, innovative device structures, and significant modifications of the planar transistor design [1,2]. Considering novel device structures, multiple-gated transistors have been proved of better electrostatic control and larger drive current with respect to the traditional planar transistor design [3]. These features are particularly attractive as enablers for further device scaling. In fact, double-gate and finFET structures are the first non-planar 3D gate constructions being successfully employed into commercial products. Nowadays, growing research efforts are spent with gate-all-around constructions with sub-10 nm diameter nanowire (NW) channels. Nevertheless, as the dimensions reduce and 3D structures are introduced, major difficulties arises due to the need of scaling while keeping large fabrication yields.

We report on a fully CMOS-compatible top-downfabrication flow of polysilicon channel finFETs and vertically-stacked polysilicon NW gate-all-around (GAA) FETs by means of an optimized Bosch process [4] and nanostencil lithography [5]. In a previous work, the authors envisaged stencil lithography [6] as a key enabler for gate patterning on 3D structures, such as vertically-stacked Si NW transistors [4]. In this work, nanostencil lithography is used to deposit the Al mask used to pattern sub-μm GAA polysilicon gates deposited with LPCVD as alternative solution for patterning nanoscaled features having high aspect ratio, which is a non trivial issue in photo-resist lithography. Moreover, a simple method to form vertically-stacked Si NWs on bulk-Si substrates [7] has been adapted to form vertically-stacked NWs onto polycristalline Si substrates. Preliminary electrical characterizations performed before the metal contact formation demonstrate functional memristive FET operation and confirming the behavior of previously reported devices fabricated with standard processing technology and μm-scale gate lengths [8]. The finFETs and the vertically-stacked polysilicon NW GAA devices are fabricated with yields larger than 70%, demonstrating a promising new method for 3D transistor fabrication with sub-μm nanostencil lithography.

In Section 2.1 we describe the structure of both finFETs and vertically-stacked GAA SiNW FETs. Then in Section 2.2 the fabrication flow for the devices is explained in detail, whereas the fabricated structures and discussion on the nano-fabrication results are provided in Section 3. Hence, the electrical measurement results are reported Section 4, with discussion among the difference in performance achieved by finFETs and vertically-stacked polysilicon NW GAA FETs. Finally, in Section 5 we draw the conclusions.

2. Device Fabrication

2.1. Device Description

The devices built can be grouped into two categories: finFETs and vertically-stacked SiNW FETs. In the first case, FETs or inverters having either 1 to 11 fins channels and tri-gate construction are built (in Fig. 1(a), a finFET with 3 fins is depicted). In the second

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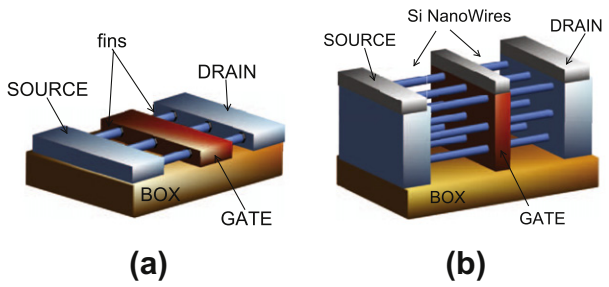

Fig. 1. Non-planar device topologies considered: (a) finFET with tri-gate construction.(b) Vertically-stacked SiNW FET with GAA construction.

case, FETs or inverters with 1 to 11 parallel strands consisting of 3 vertically-stacked SiNWs and GAA construction are built (in Fig. 1(b), a 3 times 3 SiNW matrix with GAA construction is shown). Apart from the fabrication of non-planar channels in such devices, the lithography definition of tri-gate or all-around gate structures above 3D channel regions is considered to be a significant challenge [1].

2.2. Process Flow

The fabrication starts with the substrate preparation for the two separate wafer batches. Bulk-Si wafers are oxidized in wet atmosphere to form 500 nm thermal oxide. Then either 50 nm or 350 nm thick LPCVD polysilicon is deposited as the device layer to build finFETs or vertically-stacked SiNW FETs, respectively. Individual or arrays of lines of widths of 50 nm and length of 8 μm are patterned with diluted *hydrogen silsesquioxane (HSQ)* using it e-beam lithography (EBL) (see Fig. 2(a)). The HSQ is then used as hard mask for the fins and the vertically-stacked SiNWs etching (Fig. 2(b)). For the fin formation, a Cl2 based plasma etching is used to obtain vertical sidewalls, whereas for the vertically-stacked SiNWs the etching consists of 3 cycles of passivation and etching steps, alternating low frequency pulses of C_4F_8 and SF_6 plasmas. The etching technique used for the stacked SiNW formation has been calibrated from the recipes previously described by the authors for the formation of vertically-stacked SiNWs in crystalline Si substrates [7]. Next, a 10 nm dry oxidation followed by a 100 nm LPCVD polysilicon deposition form the gate stack (see Fig. 2(c)). At the same time a low stress SiN nanostencil mask has been patterned with the gate design. The fabrication details of the nanostencil are described by the authors in a different publication [5]. In this work, the nanostencil is made of 100 nm thick LPCVD low stress Si_xN_y. The gate and contact pads are defined by EBL, followed by consecutive etching steps to open the apertures and back side windows. Then the nanostencil mask is aligned with a dedicated optical alignment tool and mechanically clamped with the device substrates. After loading the substrates with the nanostencil into a commercial e-beam evaporator, 40 nm Al are deposited, leaving an Al hard mask reproducing the gate design on top of the polysilicon layer (Fig. 2(d)). The Al mask gives better selectivity than SiO_2 hard maks for dry Si etching, thus enabling the patterning of higher aspect ratio structure. Hence, polysilicon gates are etched and Si_xN_y spacers are formed to provide good isolation barrier between the gate and the source/drain regions (Fig. 2(e)). This step is thus used to form pad areas for electrical characterization as well as polysilicon gates with lengths between 100 nm and 500 nm. Finally, a 30 nm thick Ni layer is deposited on the substrates, and a thermal annealing process at 400°C is utilized to form a stoichiometric 1:1 NiSi phase on top of the gates and to metallized source/drain regions. The unreacted Ni that was lying either on top of SiO_2 BOX layer or onto the spacers has been removed with a selective Piranha solution.

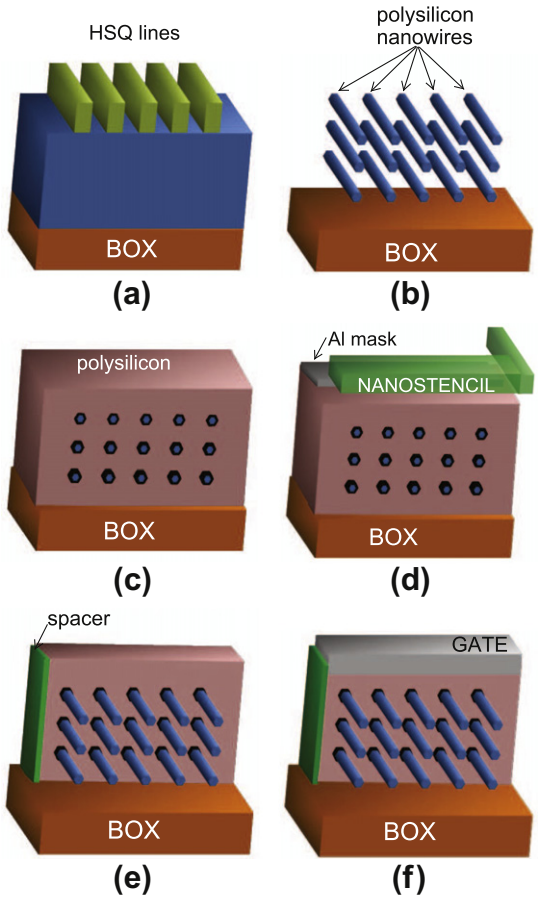

Fig. 2. Fabrication flow of the vertically-stacked GAA FETs. (a) HSQ lines are patterned with EBL. (b) A DRIE etching process is tuned to form 3 levels of stacked SiNWs. The nanowires are attached to polysilicon pillars at their extremes (not shown). (c) 10 nm dry oxide and 100 nm LPCVD polysilicon are deposited to form the gate stack. (d) A nanostencil mask is aligned and mechanically clamped with the substrate, serving as evaporation mask for Al deposition. The Al is then used as mask to pattern the gate.(e) After gate patterning a Si_xN_y spacer is formed on vertical sidewalls. (f) After Ni blanket deposition and a thermal annealing at 400°C, a Piranha wet etching is used to remove unreacted Ni from either BOX and spacer regions, thus forming self-aligned NiSi source/drain and gate areas.

Thanks to the self-alignment of the Si_xN_y spacers with the gates, self-aligned source/drain regions are formed and the devices are ready for electrical characterization.

3. Fabricated Devices

The fabricated devices included FETs or inverters designed with different number of channels, having either 1 to 11 parallel SiNWs for the finFETs. For the vertically-stacked SiNWs the same design is used, nevertheless, thanks to stacking 3 levels, the same devices have 3 to 33 parallel SiNW channels. Another difference among finFETs and vertically-stacked FETs is notably the gate structure, which are tri-gates and GAA, respectively. In Fig. 3, a finFET with 11 parallel SiNWs and tri-gate construction is shown. The SiNWs are interconnected every 500nm in order to improve the mechanical stiffness and so to avoid bending. In Fig. 4, a vertically-stacked FET with 3 stacked SiNWs of 30 nm diameter and GAA construction is shown. In the inset, conformal coverage of 10nm thick SiO_2 dielectric and LPCVD polysilicon gate is shown.

In all substrates, the design included 150 FETs and 150 inverters, for which the fabrication yield has been checked. In Table 1 fabrication yields larger than 70% are reported, showing excellent reproducibility, considering the experimental nature of the

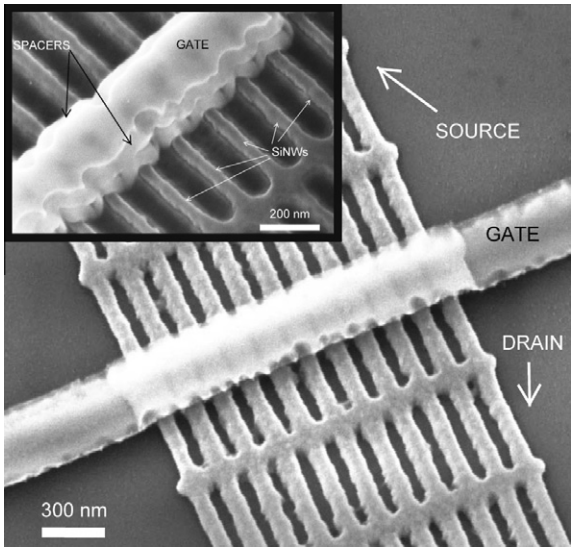

Fig. 3. Si nanowire FET with 11 channels with 50 nm times 50 nm channel cross-section, 350 nm long polysilicon gate. The nanowires are connected at regular intervals of 500nm in order to improve the stiffness of the structure. In the inset a magnified and tilted SEM view shows the nitride spacers and the SiNWs around the gate structure.

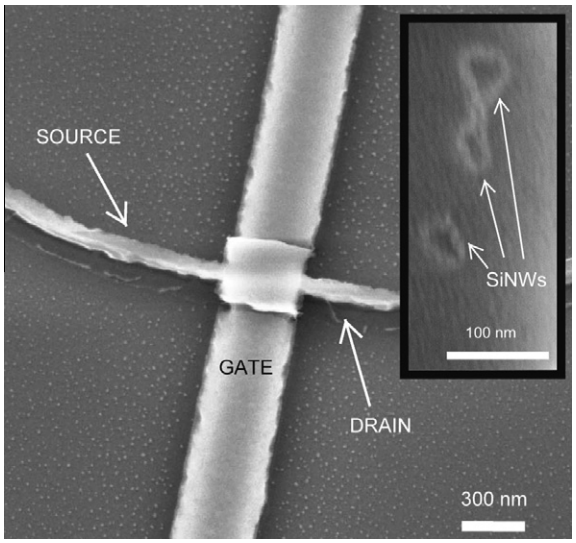

Fig. 4. Si nanowire FET with 3 vertically stacked single-stranded 30 nm diameter channels. In the inset, a Focused Ion Beam cross-section of the gate shows 3 SiNWs surrounded by 10 nm SiO_2 dielectric and 100 nm LPCVD polysilicon. Gate length is 350 nm.

process. Moreover, the failing sites have been observed the same for all the substrates, regardless of the process flow. This is the reason for the very similar yield reported for finFETs and vertically-stacked FETs. It is worth noticing that failing devices are mainly related with defects in the mask design, and that this aspect of the work has not been optimized. Thus, the main limitation on the fabrication yield is related with systematic errors in the design.

Table 1
Fabrication Yield measured for the 4 device types.

Yield	finFETs	vertically-stacked FETs
FETs	70%	70%
Inverters	85%	84%

For instance, one of the major fabrication issues is the mechanical stability of the nanostencil, whose robusteness is crucial for the correct patterning of the Al mask. If we consider the device subset of finFET inverters, the the larger yield of 85% is mainly attributed to the lower number of defective nanostencil patterns. Using a smaller size for the nanostencil, which would be a natural consequence when fabricating more scaled devices, improves stability and, at the same time, reduces the frequency of defective patterns. Hence, there is indication that fabrication yields larger than 85% with this process flow is possible with relatively little effort in the mask design.

4. Electrical Measurements

Electrical characterization is carried out with a manual probe station connected to a Agilent B1500 semiconductor parameter

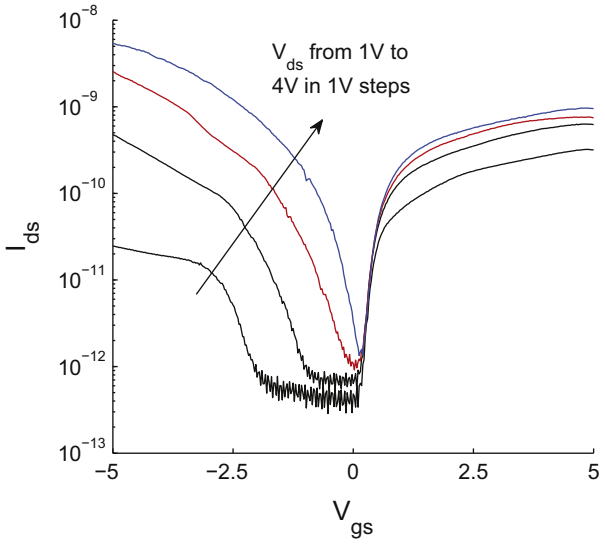

Fig. 5. $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 stacked channels. Measured minimum inverse subthreshold slopes for electrons (n-branch) and holes (p-branch) are $300mV/dec$ and $1300mV/dec$ at V_{ds}=4V.

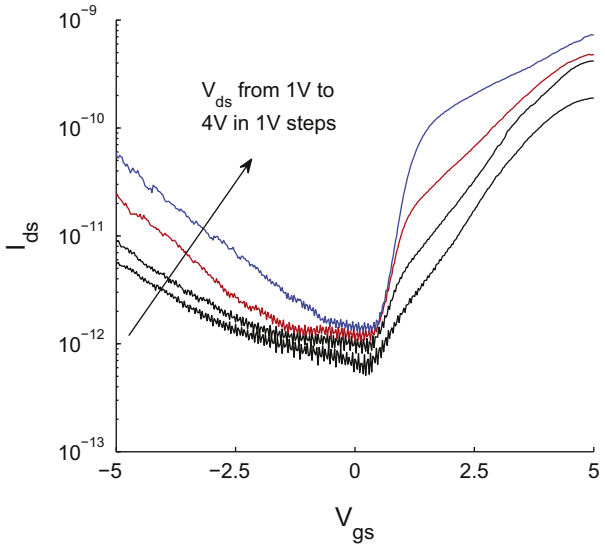

Fig. 6. $I_{ds} - V_{gs}$ curve for vertically-stacked SiNW GAA FET with 3 times 11 channels. Measured minimum inverse subthreshold slope for electrons is $350mV/dec$. Notice that the holes conduction is effectively suppressed due to the 3D nanowire mesh.

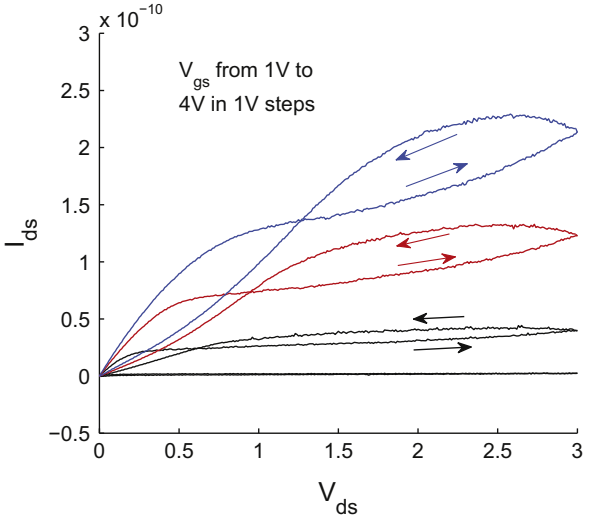

Fig. 7. $I_{ds} - V_{ds}$ memristive/hysteresis curve for vertically-stacked SiNW GAA FET with 3 stacked channels. The hysteresis lead to different saturation threshold due to the dynamics of charges with interface states at either the Shottky junctions or at the polysilicon grain boundaries.

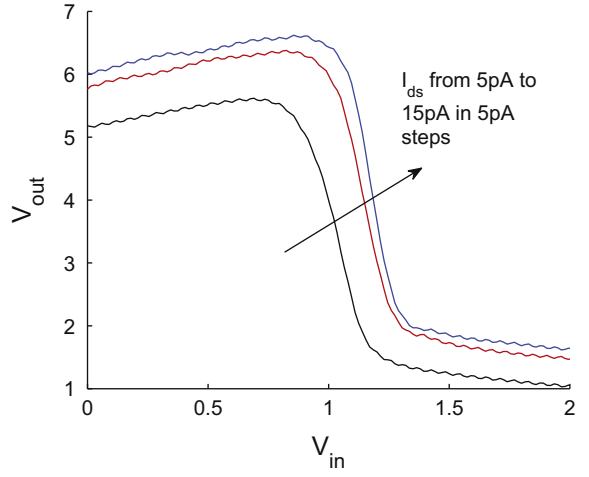

Fig. 8. Inverter operation obtained by biasing a FET with constant current. The $V_{out} - V_{in}$ characteristics switched from high to low V_{out} at $V_{in} \approx 1$ V.

analyzer. Tungsten tips are put in contact with the polysilicon source/drain pads and on the Al/polysilicon gate pad. Typical $I_{ds} - V_{gs}$ curves are first measured for finFETs which show large inverse subthreshold slopes of about $1500mV/dec$ and average $I_{ON} - I_{OFF}$ ratio of 3 orders of magnitude. These results are then compared with the electrical performance measured for the vertically-stacked GAA NW FETs. The $I_{ds} - V_{gs}$ curves (Fig. 5) for the vertically-stacked FETs with 3 stacked SiNWs show typical device ambipolarity with inverse subthreshold slopes for n- and p-branches up to $300mV/dec$ and up to $1300mV/dec$, respectively. Notice the strong dependence of the p-branch with applied V_{ds}. This undesired behavior is largely compensated for, in the devices with 3 times 11 parallel fingers, as shown in Fig. 6. The apparent robustness with respect to short channel effects is attributed to the different geometry of the 3D mesh with respect to the single stranded stacked SiNWs.

Another interesting result is the hysteresis observed for $I_{ds} - V_{ds}$ curves (see Fig. 7). The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward V_{ds} sweep is not identical to the same curve for backward V_{ds} sweep. This behavior can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [9]. More detailed explanation of the memristive electrical behavior can be found for similar, previously reported devices [8].

V_1[V]	V_2[V]	V_{out}[V]
0 (logic 0)	0 (logic 0)	≈ 4 (logic 1)
0 (logic 0)	2 (logic 1)	≈ 3 (logic 1)
2 (logic 1)	0 (logic 0)	≈ 5 (logic 1)
2 (logic 1)	2 (logic 1)	≈ 0.5 (logic 0)

Finally, inverter and logic NAND operation have been performed using a current biasing scheme. In Fig. 8, a current bias from 5 pA to 15 pA in 5 pA steps has been utilized. As shown in the graph, the inversion voltage saturates at $V_{in} \approx 1.2$V with a gain $\Delta V_{out} / \Delta V_{in} \approx 14$. Moreover, by using two vertically-stacked FETs in series connection, NAND functionality can be achieved by measuring the voltage drop across while sweeping the gate voltages of the two devices. With this method, typical NAND functionality is obtained, as shown in Table 1.

5. Conclusions

In conclusion, we demonstrated for the first time vertically-stacked Si nanowire FETs with polysilicon GAA having gate lengths down to 100 nm and yield larger than 70%. Moreover, the reported ambipolar behavior for vertically-stacked FETs achieves I_{ON}/I_{OFF} ratio up to 4 orders of magnitude and inverse subthreshold slopes (SS) up to $300mV/dec$, effectively improving the SS of $1500mV/dec$ obtained for finFETs. The method provide excellent step coverage on either finFETs and vertically-stacked SiNW FETs with strongly non-planar topography, thanks to the use of an Al etch mask deposited with nanostencil. The electrical behavior confirms the results obtained from similar devices fabricated with a standard lithography approach while achieving higher density, larger reproducibility and yield, maintaining the performance improvement related with scaling. Finally, functional inverter and logic NAND operations are obtained, confirming the discussed fabrication flow as valuable tool to build logic circuits.

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