Low-cost, CMOS compatible, Ta_2O_5-based hemi-memristor for neuromorphic circuits

E. Kyriakides, S. Carrara, G. De Micheli and J. Georgiou

In the past, tantalum oxide devices have been used to create non-volatile digital memories, whilst neglecting the analogue memristive characteristics of such devices. In this Letter, it is shown that these devices can provide a low-cost, low-power solution for hemi-memristive devices, when used in their pre-formed, memristive region, whilst being fully CMOS compatible. Furthermore, measurements are presented from the devices that have been fabricated and it is shown that these devices do not require electroforming. Electroforming circuitry takes up valuable chip space at the transistor layers and significantly increases fabrication cost, since voltages as high as 12 V are required, which in turn requires extra masks to form high voltage devices and distribution circuits.

Introduction: Memristors were initially postulated by Leon Chua in 1971 [1] based on theoretical arguments in order to complete the symmetry of passive electronic devices. Their practical implementation in 2008 [2] sparked renewed interest, given their wide range of applications in digital and analogue circuits. Although the bulk of the application direction has been towards non-volatile memories, we believe that memristors will have a greater impact if used in biomimetic computer architectures. A successful shift in the traditional computing paradigm using neuromorphic components may bridge the performance gap between current electronics and biological circuits [3].

Previously, it was assumed that the device in question required a forming step for the initial filament formation to behave like a hemi-memristor. We show that it can also be used at below-forming voltages as a bipolar hemi-memristor with hysteretic behaviour, without compromising the functionality required in biomimetic circuits. We therefore do away with area-consuming circuitry needed for forming, in addition to the requirement of an expensive, high-voltage technology.

The fabricated devices are hereby presented and their pre-forming and post-forming behaviour discussed.

Ta_2O_5-based memristors: Various implementations of memristive devices have been presented in the References Section. A subset of them follows a similar structure, employing two metal electrodes enfolding a transition metal oxide. However, their principle of operation can be altogether different. For example, the $Pt/TiO_2/Pt$ structure presented by Hewlett-Packard, owes its behaviour to the moving oxygen vacancies in an insulating layer of TiO_2, resulting in conductive oxygen-deficient locales of TiO_{2-x} [4]. In contrast, $Cu/Ta_2O_5/Pt$ devices rely on a filament formation to vary conductivity. Cu^+ cations diffuse into the insulating Ta_2O_5 layer creating a conductive bridge. The forming and dissolution of this conductive path results in the hemi-memristive behaviour observed [5, 6].

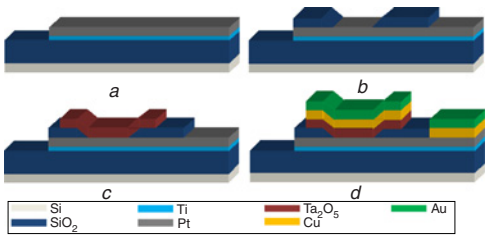

Fig. 1 *Fabrication steps*

a Bottom electrode
b Interlayer dielectric
c Ta_2O_5 active layer
d Top electrode

Device fabrication: Starting with a thermal oxide layer, bottom 50 nm Pt electrodes were formed using a Ti adhesion layer and patterned using lift-off. To define the active device region through an interlayer dielectric, SiO_2 was sputtered and patterned into various geometries. Ta was subsequently reactively sputtered to form a Ta_2O_5 layer of 15 nm thickness. Dry etching was used for the Ta_2O_5 patterning. Afterwards, a 50 nm Cu layer was formed through evaporation, operating both as the cation source and the top electrode. Finally, Au was added on top of the Cu electrode to prevent the oxidation of Cu. Lift-off was again used for the Au/Cu layer patterning. The major process flow steps can be seen in Fig. 1.

A cross-section of the device as captured through a scanning electron microscope can be seen in Fig. 2. The image is captured at a sample inclination of 52° following a cross-section created using a focused ion beam gun.

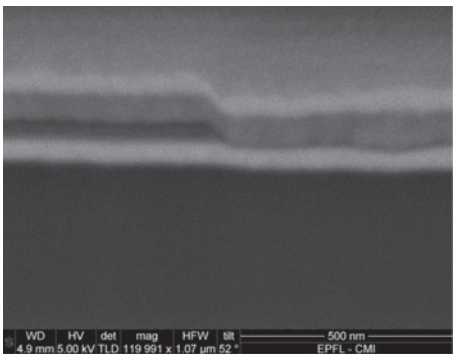

Fig. 2 *SEM image of device cross-section*
SiO_2 step can be seen defining active device area (right) from inactive area (left)

Forming and classical operation: The device forming procedure involves the application of a large voltage to form the conductive filament within the dielectric sheet. Cu^+ cations diffuse into the insulating Ta_2O_5 layer under the applied electric field, aided by the solubility of Cu^+ ions in Ta_2O_5 and limited by the diffusion coefficient of Cu^+ ions in Ta_2O_5 [5]. A high concentration of Cu^+ cations at the Ta_2O_5/Pt interface causes nucleation through a reduction reaction, which in turn leads to the formation of a conductive filament of Cu atoms extending between the two electrodes.

The forming process involves a large voltage being applied to the top electrode to generate the electric field required for the Cu^+ cation diffusion. The voltage required for the forming of our devices can be as much as 12 V, a value that entails a high voltage supply. If this step is to be carried out without using external sources on a 'learning chip', substantial additional circuitry will be required on-chip, in addition to the requirement of a costly high voltage technology. Thus, the forming process is commercially unattractive.

Once formed, the devices under investigation exhibit hemi-memristive characteristics. Voltage sweeps reveal the pinched hysteresis loop (Fig. 3). However, the interesting aspect of pre-forming hysteretic behaviour has so far been overlooked.

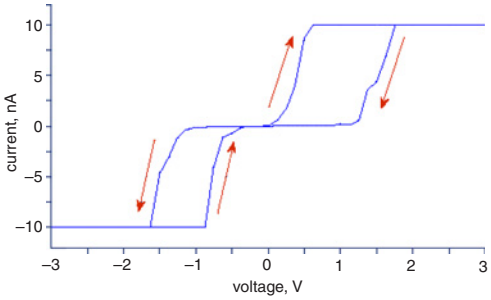

Fig. 3 *Post-forming I-V characteristics showing pinched bow-tie loop*

Proposed pre-forming operation: Adhering to the 3.3 V as a low voltage operation region, the devices were taken through voltage sweeps of ±3.3 V, well below the forming threshold (Fig. 4). The hysteresis effect is very consistent, through a variety of device geometries with very high repeatability.

To probe into the mechanisms causing the hysteretic behaviour, some devices were manufactured that omitted the Cu layer. The resistivity of the Ta_2O_5/Pt heterostructure did not exhibit any memristive behaviour. This led us to deduce that the observed behaviour of the full device is based on Cu^+ ionic diffusion. To investigate further, cyclic voltammetry experiments with varying triangular voltage sweep rates (0.05 – 0.1Hz) were conducted. Frequency measurements clearly show a dependence of peak conductivity and hysteresis on frequency, as shown in Fig. 5,

however these show an opposite trend to an idealised memristor, hence we use the term 'hemi-memristor'. Furthermore, increasing sweep rates yield increasing peak currents. More specifically, the Cottrell equation is verified in peak current against sweep time.

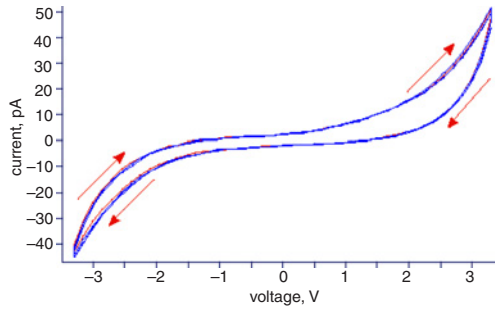

Fig. 4 *Pre-forming I-V hysteresis loop comprising four sweeps*

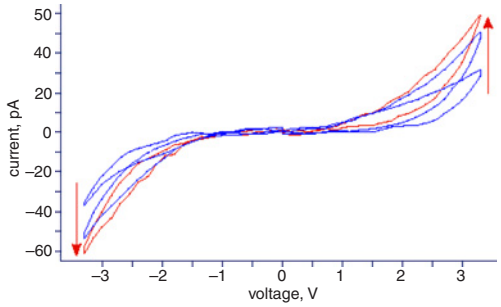

Fig. 5 *Sweep frequency variation*
Red arrows indicate increasing frequency, ranging from 0.05 to 0.1Hz

Taking the above into account, along with the lack of current peaks in the voltage sweeps at the Cu standard redox potentials (0.153 V, 0.521 V), it is evident that no redox reactions take place [7]. Moreover, the slightly asymmetric *I-V* curve further attests to diffusion between dissimilar electrodes. Hence, the low currents, limited by the tantalum oxide dielectric, ensure the electrochemical reaction at the Pt bottom electrode does not occur [5], thereby preventing the subsequent Cu^{+} nucleation and filament creation from taking place. Therefore, in this region of operation we observe only the Cu^{+} ion migration mechanism through the solid electrolyte layer. This matches the expected behaviour at below-forming voltages and could account for the nonzero current at 0 V, which is being looked into.

Neuromorphic computing: Ta_2O_5-based hemi-memristors provide characteristics useful for biomimetic circuit design. Although the frequency dependence of the pre-forming hysteretic response is not compliant with the strict memristor definition [2], these devices can be employed as synapses in Hebbian learning neural circuits or STDP synapses [8, 9].

Conclusion: We have presented a class of devices that can be used as electronic synapses in neuromorphic circuits. The devices are fully CMOS compliant and can be used without the extra circuitry and costs relating to forming solid electrolyte memristors. Their low voltage/current operation lends itself nicely to low power biomimetic architecture circuits.

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One or more of the Figures in this Letter are available in colour online.

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