Ambipolar Gate-Controllable SiNW FETs for Configurable Logic Circuits With Improved Expressive Capability

Davide Sacchetto, Yusuf Leblebici, and Giovanni De Micheli

***Abstract*—In this letter, we report on the fabrication and characterization of ambipolar silicon-nanowire (SiNW) field-effect transistors (FETs) with a double-independent-gate (DIG) structure for polarity control. Several structures are fabricated, showing the effectiveness of local back gate to enable switchable ambipolar functionality. Moreover, AND, NAND, NOR, XOR, and XNOR binary logic functions can be obtained with a single gate, depending on the encoding values used for the input signals. Repeatable behaviors of DIG SiNW FETs are considered as enablers for ambipolar-controlled logic, with all the benefits related to the maturity of the silicon technology.**

***Index Terms*—Ambipolar control, field-effect transistor (FET), nanowire, Schottky barrier.**

I. Introduction

THE CONTINUING pursuit for extending Moore's law to future device families also fuels the intensifying research on new device functionality for implementing next-generation circuits. New computational paradigms based on the control of alternative state variables [1] are being investigated along with novel structures, such as double-gate and gate-all-around nanowire devices [2], or new materials, such as higher κ dielectrics and metal gates, or different device concepts, such as modified Schottky-barrier field-effect transistors (FETs). Most of these paradigms require physics different from the physics of CMOS. For instance, computation has been demonstrated with devices based on the laws of photonics [3], spintronics [4], or nanoionics [5].

Nevertheless, alternative solutions that require a less dramatic impact on technological development would be preferable for practical applications. Regarding the different solutions, the ambipolar-controlled logic gates are among the most promising ones, owing to the higher expressive logic power due to the polarity control as state variable [6]. The polarity control can be achieved in ambipolar devices by using a double-independent-gate (DIG) structure. A few examples can be found for DIG FETs based on carbon nanotubes [7], [8], graphene [9], semiconducting polymers, and silicon nanowires (SiNWs) [10]. Nevertheless, very limited research has been done in terms of integrating ambipolar-controlled devices with CMOS-compatible top-down Si fabrication flow, which is crucial for large-scale system integration.

In this work, ambipolar SiNW FETs with a DIG structure enable the use of polarity control signals as a method toward Si circuits with increased logic expressive power. Moreover, the use of polarity control leads to improved performance in terms of $I_{\mathrm{ON}}-I_{\mathrm{OFF}}$ ratios and inverse subthreshold slopes with respect to the ambipolar behavior.

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II. Device Description

The device consists of a 20-μm-long crystalline SiNW attached between two Si pillars on an SOI wafer [see Fig. 1(a)]. The SiNW is then covered by two independent n^{++} polysilicon gates with this scheme: a main central gate (gate 1) of 7.5-μm length and a second gate (gate 2) that is used to control the SiNW portions between the main gate and the source and drain regions, respectively.

A. Fabrication

First, a low-doping p-type ($N_A \approx 10^{15}$ atoms/cm^2) SOI wafer with a 1.5-μm device layer is spin coated. The photoresist is then patterned in 1.5-μm-wide lines [see Fig. 1(b)] and used as a mask for a next isotropic Si etching. A Si plasma etching recipe is tuned to form a triangular 75-nm-wide SiNW lying on top of the buried oxide layer [Fig. 1(c)]. Then, a 30-nm-thick gate oxide and a 150-nm polysilicon layer are deposited with low-pressure chemical vapor deposition (LPCVD) method to form a main gate with 7.5-μm length [gate 1 in Fig. 1(d)]. The main gate is then isolated by a 300-nm LPCVD low-temperature oxide (LTO). A second 500-nm polysilicon layer is then deposited. Then, a thick photoresist is spun over the wafer and planarized using a chemical mechanical polishing procedure similar to the one previously described by the authors in [11]. This method leaves a protective polymer layer that is used to etch a second polysilicon gate self-aligned within the cavity due to the topography [see gate 2 in Fig. 1(e)]. After standard cleaning steps, one additional patterning of gate 2

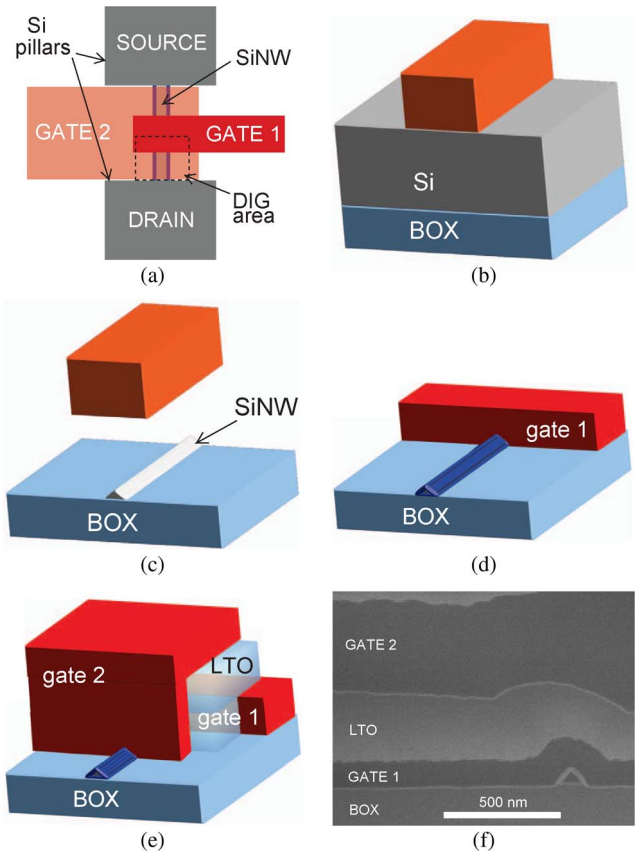

Fig. 1. Fabrication flow. (a) Top view of the dual-gate device. The next steps focus on the DIG area construction. (b) Photoresist mask is patterned. (c) After isotropic etching of Si, a triangular-shaped SiNW is formed. (d) Gate oxide and LPCVD polysilicon are deposited and patterned to form the main central gate stack. (e) LTO interpoly dielectric is deposited, and a second polysilicon gate is made self-aligned with the nanowire. (f) Focused ion beam cross section showing a triangular SiNW channel with two 75-nm sides and a 100-nm base. Gate 1, gate 2, and the LTO interpoly dielectric have 150-, 500-, and 300-nm thicknesses, respectively. The gate-1 dielectric is 30 nm thick.

is performed to remove the unnecessary polysilicon and to form areas for the contacts [see the top view of the device in Fig. 1(a)]. In Fig. 1(f), a focused ion beam cross section of the triangular SiNW channel with the DIG stack is shown. Then, source/drain contacts are formed by means of NiSi silicidation in a horizontal wall furnace in forming gas at 400 °C. Finally, Al metal lines and a pad area are defined for the electrical characterization.

B. Device Operation

The source/drain regions after NiSi silicidation have a midgap Schottky-barrier contact with the SiNW; thus, both electrons and holes can contribute to the current flow. The use of the two gates enables the selection of which carrier species shall prevail in the conduction. In the following discussions, the voltage applied to gate 1 is defined as $V_{\rm gs}$, while the voltage applied to gate 2 is defined as $V_{\rm bg}$. This scheme was proposed by Lin *et al.* [7] for the control of polarity of carbon-nanotube FETs. As shown in Fig. 2(a), a positive back-gate voltage $V_{\rm bg}$ enables electron flow, while the hole current is blocked. Similarly [Fig. 2(b)], a negative $V_{\rm bg}$ makes the opposite selection: The hole current is enabled while the electron flow is blocked.

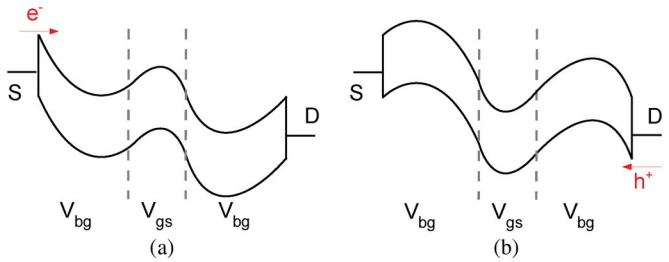

Fig. 2. (a) Conceptual band diagram for n-type operation. A positive $V_{\rm bg}$ is used to block the flow of holes from the drain. (b) Conceptual band diagram for p-type operation. A negative $V_{\rm bg}$ is used to block the flow of electrons from the source.

TABLE I
OBTAINED ELECTRICAL BEHAVIOR FOR DIFFERENT $V_{\rm bg}$ VOLTAGES

$V_{\rm bg}$[V]	$\frac{I^{h+}_{ON}}{I_{OFF}}$	$\frac{I^{e-}_{ON}}{I_{OFF}}$	SS^{h+}[mV/dec]	SS^{e-}[mv/dec]
+10	50	250	1000	600
+7.5	N/A	2000	N/A	250
+5	N/A	1000	N/A	250
+2.5	N/A	1000	N/A	325
0	1000	600	475	750
-2.5	1000	N/A	375	N/A
-5	5000	N/A	250	N/A
-7.5	10000	N/A	300	N/A
-10	30000	N/A	300	N/A

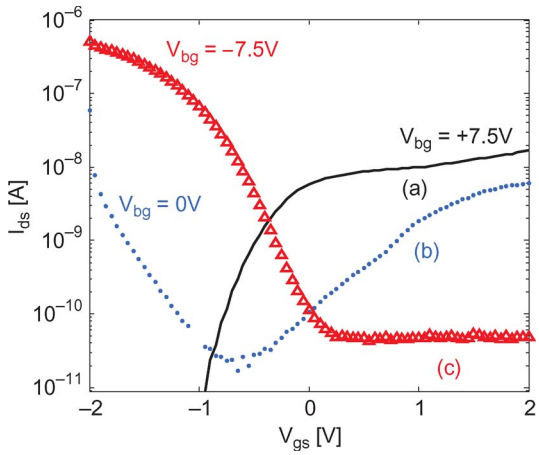

Fig. 3. Controlled ambipolar $I_{\rm ds}$–$V_{\rm gs}$ characteristics at different $V_{\rm bg}$ back-gate voltages. (a) Positive $V_{\rm bg} = +7.5$ V is used to obtain an n-type characteristic. (b) $V_{\rm bg} = 0$ V gives ambipolar $I_{\rm ds}$–$V_{\rm gs}$. (c) Negative $V_{\rm bg} = -7.5$ V is used to obtain a p-type characteristic.

III. Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer in dark at room temperature. In Table I, the effect of $V_{\rm bg}$ on the inverse subthreshold slopes (SS^{h+} and SS^{e-}) for hole and electron conduction branches depicts a trend for improved SS^{h+} and SS^{e-} when increasing $V_{\rm bg}$ voltages of negative and positive polarities are applied, respectively. Similarly, improved $I_{\rm ON}-I_{\rm OFF}$ ratios ($I^{h+}_{\rm ON}/I_{\rm OFF}$ and $I^{e-}_{\rm ON}/I_{\rm OFF}$) are observed when larger $V_{\rm bg}$ voltages are applied. The improved performance is related to a reduced $I_{\rm OFF}$ current due to the screening of one of the two types of carriers for the conduction. As better shown in Fig. 3, positive or negative $V_{\rm bg}$ voltages can be used to obtain n-type or p-type

TABLE II
BINARY LOGIC VOLTAGE SIGNALS CODING FOR XOR, NAND, AND, AND NOR OPERATIONS

CODE	XOR		NAND		AND		NOR	
	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]	V_{gs} [V]	V_{bg} [V]
logic 0	+1	-7.5	-0.5	+7.5	0	0	0	+7.5
logic 1	-1	+7.5	+1	-7.5	-1	-7.5	-1	0

TABLE III
OUTPUT CURRENT LEVELS FOR THE FOUR LOGIC OPERATIONS: XOR, NAND, AND, AND NOR

logic values		XOR	NAND	AND	NOR
gate 1	gate 2	I_{OUT}[A]	I_{OUT}[A]	I_{OUT}[A]	I_{OUT}[A]
0	0	$4 \cdot 10^{-11}$	$2 \cdot 10^{-9}$	10^{-10}	$6 \cdot 10^{-9}$
0	1	10^{-8}	$2 \cdot 10^{-9}$	10^{-10}	10^{-10}
1	0	$7 \cdot 10^{-8}$	10^{-8}	10^{-11}	10^{-11}
1	1	10^{-11}	$4 \cdot 10^{-11}$	10^{-7}	$5 \cdot 10^{-11}$

I_{ds}–V_{gs}. Moreover, a symmetrical ambipolar I_{ds}–V_{gs} is obtained for $V_{bg} = 0$ V. This functionality allows for increased expressive logic power with a single FET. For instance, the two voltage signals V_{gs} and V_{bg} can be coded to make logic XOR operation with the device in Fig. 3, an operation that would require more transistors in standard CMOS technology. In Table II, V_{gs} and V_{bg} voltage values are encoded into logic levels 0 and 1 to map into four binary logic operations, namely, XOR, NAND, AND, and NOR, while using the data plot in Fig. 3. The results of the logic operations are summarized in Table III. Logic 0 and logic 1 outputs are represented by light and dark gray, respectively. Another solution that can be envisaged can use the same logic levels for both gates in order to save space for external encoding circuits. This solution will become the most desirable one by optimizing the thickness of the two gate dielectrics, which, in the current implementation, leads to a more effective electric field density for gate 1 than for gate 2. In future designs, this technological issue might be overcome by optimizing the dielectric thickness for the two gates and/or in combination with dopant segregation techniques to balance the Schottky-barrier heights for holes and electrons. Moreover, gate work-function engineering can be used to code the threshold voltage of the device, thus addressing the different logic 0/1 voltages needed for a specific logic function. Owing to these technological options, dense arrays of ambipolar DIG FETs can be envisaged as basic building blocks to map complex logic circuits. The ac characteristic of the proposed device concerning delay and power will depend, among other factors, on the capacitive coupling between the two gate electrodes. However, this parasitic coupling is estimated to be of the same order of magnitude of the source/drain-to-gate capacitance, and given the fact that the fabricated device performs a more expressive logic functionality, this additional coupling is not expected to be a limiting factor.

IV. CONCLUSION

In this study, a new device structure exploiting a DIG configuration with SiNW and top-down fabrication flow has been demonstrated as a useful building block for ambipolar-controlled logic operation. All the I_{ds}–V_{gs} characteristics, defining n-type, p-type, and ambipolar behavior, have been obtained with good $I_{ON}-I_{OFF}$ ratios of up to four orders of magnitude and with inverse subthreshold slopes close to those of state-of-the-art Schottky-barrier FETs. In addition, a single device can be used to perform any of the XOR, XNOR, NAND, AND, and NOR binary logic operations depending on the input signals encoding. The proposed integration scheme is envisaged for logic circuits exploiting the improved logic expressive power of ambipolar-controlled SiNW devices, which is enabled by the reliability of Si fabrication technology.

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