INVITED PAPER

Multiterminal Memristive Nanowire Devices for Logic and Memory Applications: A Review

The authors of this paper introduce multiterminal memristive nanowire devices in memory applications.

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ABSTRACT | Memristive devices have the potential for a complete renewal of the electron devices landscape, including memory, logic, and sensing applications. This is especially true when considering that the memristive functionality is not limited to two-terminal devices, whose practical realization has been demonstrated within a broad range of different technologies. For electron devices, the memristive functionality can be generally attributed to a material state modification, whose dynamics can be engineered to target a specific application. In this review paper, we show that trap charging dynamics can explain some of the memristive effects previously reported for Schottky-barrier field-effect Si nanowire transistors (SB SiNW FETs). Moreover, the SB SiNW FETs do show additional memristive functionality due to trap charging at the metal/semiconductor surface. The combination of these two memristive effects into multiterminal metal–oxide–semiconductor field-effect transistor (MOSFET) devices gives rise to new opportunities for both memory and logic applications as well as new sensors based on the physical mechanism that originate memristance. In the special case of four-terminal memristive Si nanowire devices, which are presented for the first time in this paper, enhanced functionality is demonstrated. Finally, the multiterminal memristive devices presented here have the potential of a very high integration density, and they are suitable for hybrid complementary metal–oxide–semiconductor (CMOS) cofabrication with a CMOS-compatible process.

KEYWORDS | Ambipolar; memristor; nanowire; Schottky barrier; transistor

I. INTRODUCTION

The main source of the complementary metal–oxide–semiconductor (CMOS) success lies in the exponential increase of device density that the silicon industry kept true for more than 40 years reducing the unit cost of integrated circuits. Recently, the pace of scaling has been slowed down due to approaching fundamental limits at the device level. While the paradigm of scaling is still alive, researchers are striving to follow Moore's law by focusing on new materials, new device structures, and new state variables. The basic building block for circuits has always been the four-terminal planar transistor but new versions of the metal–oxide–semiconductor field-effect transistor (MOSFET) structure such as the double-gate FET, the FinFET, the gate-all-around nanowire FET can be found in commercial products.

Due to the natural limitations of materials, future deeply scaled circuits will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages an end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. A long list of fundamental state variables other than charge includes the spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states [1]. Technologies using new state variables would have to be implemented within a completely new technological

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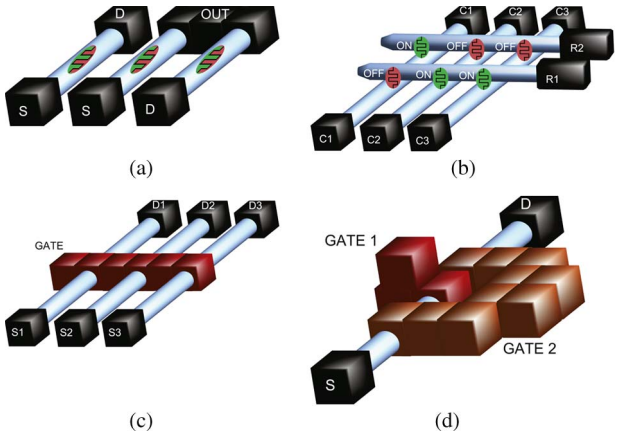

Fig. 1. ***(a) Parallel nanowire two-terminal memristive devices. (b) Crossbar array consisting of memristive cross points (two terminal). (c) Gate controlled three-terminal nanowire memristive device. (d) Double-gate four-terminal nanowire memristive devices.***

platform, and cannot be seen as CMOS-compatible alternatives.

The recent realization of devices by Strukov *et al.* [2] gave new push to solid state research for logic and memory applications. For instance, ultradense crossbar memristive memory arrays can be made thanks to the compactness of the two-terminal junction. Complementary logic based on two-terminal memristive devices [see Fig. 1(a)] or ultradense crossbar arrays with memristive cross points [see Fig. 1(b)] can dramatically improve device density up to 10^{11} b/cm^2 [3]. Moreover, the use of memristive effects as new state variables for computation can be exploited to build new types of functional devices with three or four terminals [see Fig. 1(c) and (d), respectively].

The physical realization of the memristor, whose behavior was postulated by Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6]. It is worth noting that a generalized model for memristive systems can be implemented under direct current (dc), small signal, and sinusoidal excitation [5]. The implications of such modeling are linked with the observation of memristive functionalities over a broad range of technologies based on nanoelectronics and nanoionics behaviors.

In this paper, a short review (see [7] and [8] for a more complete list) of two-terminal memristive devices is reported, while more space is given to multiterminal memristive devices that for their nature are readily implementable with front-end CMOS processes. Particular emphasis is given to devices based on the *gate-all-around (GAA) Schottky-barrier field-effect transistor (SB FET)* concept with *Si nanowire (SiNW)* channels on bulk-Si or silicon-on-insulator (SOI) wafers. The new concept of four-terminal memristive devices is presented in this paper for the first time and enhanced functionality is demonstrated. The coexistence of memristive functionality at both gate and drain electrodes with ambipolar conductance make these devices unique and capable of very high expressive power. The electrical characteristics can be attributed to the coexistence of different physical phenomena, such as device ambipolarity (both holes and electrons are responsible for conduction), Schottky barrier modulation induced by interface trap charging, and charge trapping at the gate oxide interface. It is highlighted that the unique properties of the emerging nanowire devices combine memristive functionality with ambipolar conductance, thus giving rise to novel conductance properties. We confirm some of these statements with previously reported *poly-crystalline Si nanowires (poly-SiNWs)* [9], which show a similar memristive behavior.

The memristive functionality is not a unique property of two-terminal passive devices but mainly a memory effect related to internal state variable changes. For instance, the memristive functionality can also arise from a delayed switching response of a Zener diode [10]. In the next sections, we review some of the two-terminal passive devices that can be modeled as memristive. The memristive functionality is seen as arising from different physical mechanism for different device classes. Thus, three- and four-terminal devices that show memristive functionality can be used for electrical control signals (either voltage or current). It is important to remember that a device showing a "pure" flux-charge relationship has not been found yet. Conversely, internal state variables can provide a stimulus response that can be modeled as memristive, thus adding more degrees of freedom for circuits designers.

This review paper is organized as follows. In Section II, two-terminal memristive devices are quickly surveyed. Then, in Section III, the electrical behavior of three-terminal memristive devices is discussed. Section IV will discuss on various fabrication methods for Si nanowire memristive devices. Hence, four-terminal memristive devices based on Si nanowires are discussed in Section V. Finally, possible applications for multiterminal memristive devices are discussed in Section VI.

II. TWO-TERMINAL MEMRISTIVE DEVICES

Two-terminal memristive devices can be based on metal/oxide switches, such as for SiO_2, HfO_2 [11], CuO [12], NiO [13], ZnO [14], Al_2O_3 [15], VO_2 [16], and $SrTiO_3$ [17]. These devices behave as solid-state electrochemical switches, whose resistance is defined by a metallic filament formation mechanism related to the solid-state redox reactions stimulated by the polarity of the applied electric field [18]. One example is the CuO-based ReRAM of Dong *et al.* [12] that shows repeatable resistive switching at very low voltages.

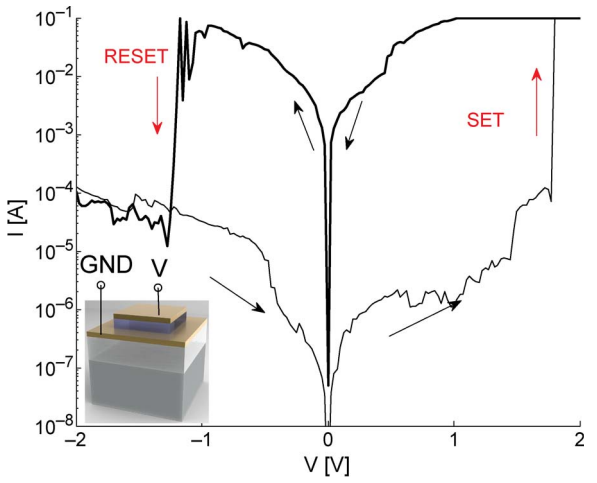

Fig. 2. *Resistive switching through I-V sweeps for planar Pt/TiO_2/Pt [21]. The inset shows the Pt/TiO_2/Pt ReRAM sandwich layer on top of an insulated substate with the two-terminal electrical contacts.*

The well-known TiO_2-based ReRAM [19], [20] seems to be based on a different mechanism, which is attributed to the vacancy/dopant diffusion in the oxide layer. The redistribution of oxygen vacancies into the TiO_2 depends on the polarity of the applied voltage, and it causes the switching between a semiconductor state into a metallic one. Typical ReRAM functionality of the TiO_2-based ReRAM is shown in Fig. 2 [21].

Another type of two-terminal memristive device is the phase change (PC) RAM [22]. The main switching mechanism is based on phase transition between an amorphous and a crystalline type due to Joule heating effects controlled by a voltage pulse. For instance, Si nanowires can be engineered such that melting and solidification processes can be iterated, thus giving rise to alternate restates [23].

Another class is based on polymers [24]. Several memristive switches can be built by interposing a biomolecule layer with properties ranging from molecule-dependent switching, such as rotaxanes [3], or more in general on interlocked molecules [25] but also on molecule-independent switching, where a filament formation mechanism through the molecular layer is involved [26].

A fifth class belongs to spintronics [27]. The spin-transfer-induced domain wall motion in a spin valve structure is by nature a memristive effect and is confirmed by some recently published results [28]. Moreover, Pershin *et al.* demonstrated that electron-spin polarization controlled by the external voltage applied to a spintronic device acts as a state variable that can be modeled as memristance [29].

In all these devices the amplitude and frequency of the input signal contribute in the formation of a so-called pinched hysteresis loop, whose salient feature is its zero crossing property [5], which is critical for ultralow power operation.

III. THREE-TERMINAL MEMRISTIVE DEVICES

The new concept of three-terminal memristive device is presented in terms of memristive functionality for logic and memory applications.

Examples of three-terminal memristive devices are the electrochemical organic memristor [31], the solid-electrolyte nanometer switch [32], the ferroelectric FET [33], and the ambipolar Si nanowire Schottky barrier FET [9], [34].

A classification of three-terminal memristive devices can be based from the general concept of the FET structure [see Fig. 3(a)] in which memristive functionality can be inserted either by engineering the gate dielectric or by gating a memristive channel. For instance, trap charging dielectric layers inserted between the channel and the gate fall into the category of FET with capacitive memory storage [Fig. 3(b)]. Examples of devices falling into this category can be the flash memory for which the trap charging into the gate dielectric influences the transconductance state of the channel. Thus, a first category that exploits the operation of writing/erasing cycles into the gate dielectric will be a generalization of the flash memory concept, for which volatility of the charges that are injected into the trap charging layer can be tuned accordingly to a desired frequency response.

A second category is the one of the gated memristor [Fig. 3(c)]. A few examples are the electrochemical organic memristor [31], the biomemristive nanowire [30], and the solid-electrolyte nanometer switch [32]. In the electrochemical organic memristor, the gate potential is represented by the potential of the bath, which is used to transfer positively charged Rb^+ ions into a polyaniline

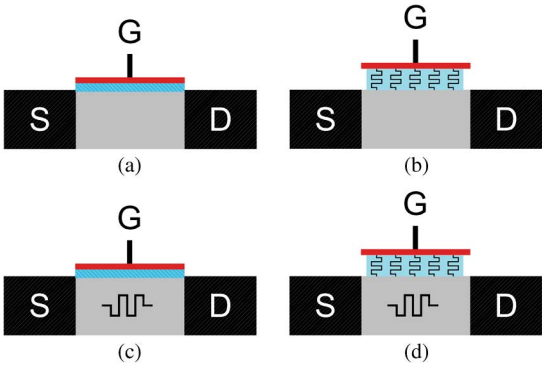

Fig. 3. *Categorization of FETs with memristive functionalities: (a) Conventional FET. (b) FET with memristive gate dielectric. (c) Gated memristor (memristive channel). (d) Gated memristor with memristive dielectric.*

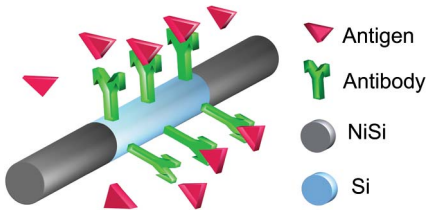

Fig. 4. *Suspended functionalized Si nanowire with NiSi extremities. The functionalized layer is capable of trapping antigen molecules which in turn affects the memristive hysteresis behavior, giving a new method for biosensing [30].*

(PANI) layer. The conductivity change can be iterated by switching the polarity of the bath potential, thus giving rise to a unipolar I_{ds}–V_{ds} curve that can be modeled as a memristor. In this case, the device can be set into either memristive or diode functionality. Similarly, a novel method for biosensing that has been recently proposed exploits the memristive effect to detect low concentration of biomolecules [30]. The device consisting of a NiSi/Si/NiSi nanowire structure coated with antibody layer (see Fig. 4) shows memristive behavior. The hysteresis loop of this device has been demonstrated for detection of low concentrations of biomolecules (antigen) in a dry environment (see Fig. 5). Conversely, the three-terminal solid-state electrolyte nanometer switch shows a typical bistable resistance state but using 100 times less current than standard two terminal operation [35]. This device is based on controlling the filament formation mechanism using the voltage of a gate terminal.

The ambipolar SB FET with SiNW channel reported in [36] [see Fig. 3(d)] falls in both categories of gated memristor and trap charging dielectric, as it shows dynamic trap charging mechanisms at the Schottky junctions and in the gate dielectric insulator. The result depicted in Fig. 6 shows a hysteretic behavior that is reminiscent of a two-terminal monolithic memristive device [37]. The hysteresis reflects the fact that the I_{ds}–V_{ds} curve for forward V_{ds} sweep is not identical to the same curve for backwards V_{ds} sweep. It can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [38]. First, two-terminal measurements are performed. The drain/source current I_{ds} is measured versus the drain/source voltage V_{ds} at constant $V_{gs} = 5$ V. The device is equivalent to two back-to-back Schottky diodes. The two diodes operate in opposite regimes: for negative V_{ds}, the source-to-channel diode is reversely biased while the drain-to-channel diode is forward biased. For positive V_{ds} both diodes invert their respective bias conditions. In either case, I_{ds} is limited by the current flowing in the reverse-biased diode. The reverse current of a metal/insulator/semiconductor diode has been observed to be very sensitive to charge trapping at the metal/semiconductor interface [15]. The large current value in the range of mA is most likely due to the large parallel parasitic structure in the bulk. In an ideal Schottky diode, the current is given by

$$I = I_S \cdot e^{-\phi_B q/kT}\left(e^{Vq/kT} - 1\right) \tag{1}$$

with I and V the diode current and voltage, respectively, ϕ_B the Schottky barrier, k the Boltzmann constant, q the

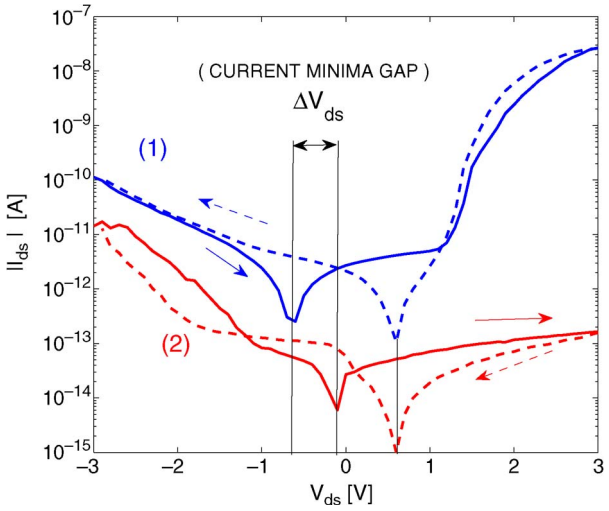

Fig. 5. *A typical memristive hysteresis is observed; the blue curve (1) is measured after drying the sample from deionized water. The red curve (2) is measured after dipping in 5-pM antigen solution and drying. The measured V_{ds} is proportional to the concentration of antigen [30].*

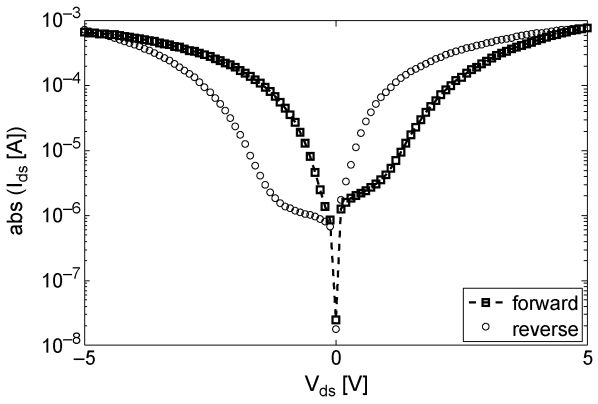

Fig. 6. *I_{ds}–V_{ds} characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 SiNW in parallel. The forward sweep curve has a symmetrical correspondence with the reverse sweep curve, showing the respective Schottky barrier modulation. A current ratio of about 50 is found at either $V_{ds} = \pm 1$ V. This behavior is typical of two-terminal memristive devices for ReRAM applications.*

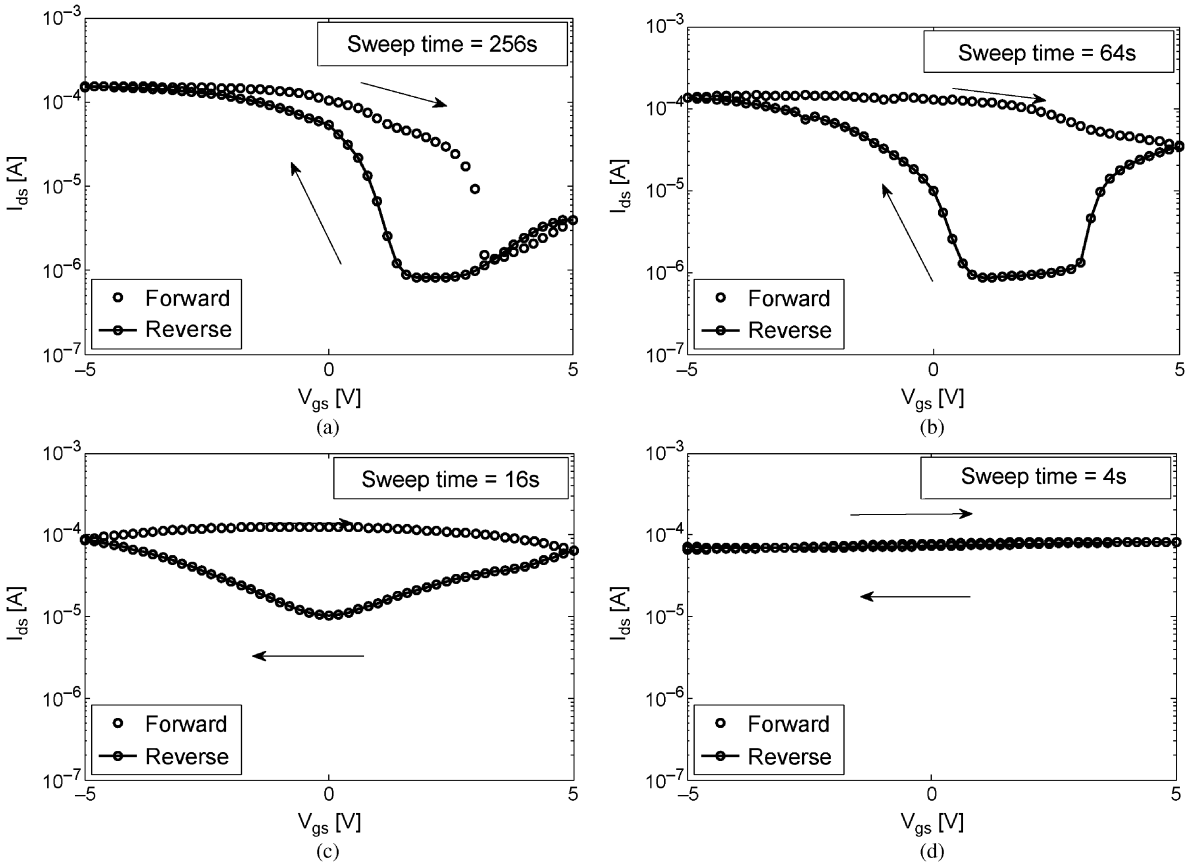

Fig. 7. ***Hysteretic dependence with the measurement (sweep time) duration; the hysteresis window closes by reducing the measurement time: (a) 256 s; (b) 64 s; (c) 16 s; and (d) 4 s.***

elementary charge, and T the absolute temperature. From the measured hysteretic behavior, it seems that the diode curve is modified as follows:

$$I = I_S \cdot e^{-\phi_B q/kT}\left(e^{(V-V_0(V))q/kT} - 1\right) \qquad (2)$$

with V_0 a built-in voltage at the Schottky contact that is positive for a positive V sweep and negative for a negative V sweep.

Another memristive functionality is linked with charging/decharging mechanisms into the gate dielectric. We measure I_{ds} for constant $V_{ds} = 1$ V while sweeping V_{gs} back and forth between -5 and $+5$ V [see Fig. 7(d)]. The devices are not annealed, and the source is connected to the substrate. This measurement is repeated for different integration times, which is a parameter of the measurement setup that can be set by the operator; and it represents the time over which the measurement is repeated and averaged. The I_{ds}–V_{gs} curves show an ambipolar behavior, meaning a large current conductance under either high or low gate bias. This is mainly due to the utilization of a silicide (NiSi) having a work function value that falls within the silicon bandgap, and to the utilization of a lightly doped silicon. On the other hand, the I_{ds}–V_{gs} curves have a hysteretic behavior that suggests the hypothesis of charge trapping at the semiconductor/oxide interface of the MOS capacitor, as well as the existence of interface states at the metal/semiconductor junction. Both ambipolarity and hysteresis depend on the integration time (see Fig. 7). When V_{gs} reaches $+5$ V in forward mode, the electrons experience a maximum probability of charges being trapped in the gate oxide, which is enhanced when the integration time is longer. Due to the electron trapping at the gate oxide, the channel operates in accumulation mode, with a lower conductance state for positive V_{gs}, than in the inversion mode for negative V_{gs}. Sweeping V_{gs} back to negative values reduces the amount of electrons trapped and the device operates in inversion mode, which restores the higher conductance state.

The threshold at which this high conductance state is reached depends on the integration time. The hysteresis window is larger when the integration time is shorter, because the charges have less time to be trapped and

detrapped. In the case of a very short integration time, the charges cannot be completely trapped and the lower conductance state is not reached (see Fig. 7).

IV. Si NANOWIRE MEMRISTIVE DEVICE FABRICATION METHODS

This section summarizes the main fabrication steps for multiterminal memristive devices based on CMOS-compatible Si nanowire technology. More details about the process flow can be found in [9], [36], and [39] for crystalline-Si (c-Si), polycrystalline-Si (poly-Si), and amorphous-Si (α-Si) nanowire channels. All the techniques yield nanowires with a subphotolithographic thickness. The general scheme is the one of the SB SiNW FET with midgap source/drain junctions. The use of a NiSi/poly-Si or NiSi/Si with undoped or lightly doped channel gives rise to a midgap Schottky barrier responsible for ambipolar conductance (see Fig. 8). The ambipolar nature of the midgap Schottky barrier field effect transistor (SBFET) can be qualitatively understood by the equal probability of either electron or hole injection, which is related to the midgap Schottky barriers. Both devices confirm the existence of an ambipolar conduction with a hysteretic behavior due to either charge trapping or modulation of the Schottky barrier through current flow. The following section surveys the fabrication details for three types of device.

A. Gate-All-Around Si Nanowire FETs

Bulk-Si wafers with low boron concentration ($N_A \sim 10^{15}$ atoms/cm^3) have been used as a substrate for the fabricated devices. Vertical stacks of Si nanowires are defined on the substrate by optical lithography [see Fig. 9(a)] without any constraint on the resolution limit (1 μm). The photoresist is then used as a mask for a deep reactive ion etching (DRIE) [Fig. 9(b)]. The optimized DRIE technique, which alternates plasma etching with passivation steps, defines scalloped trenches attached to Si pillars with high reproducibility. The enhanced scalloping effect produces vertical modulation of the trench width. A

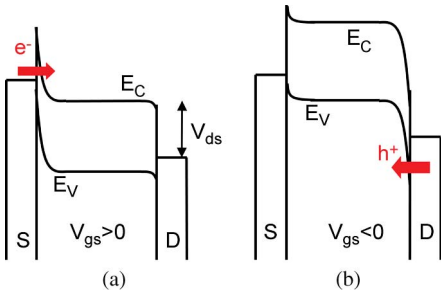

Fig. 8. *Band diagram explaining ambipolarity: (a) positive V_{gs} reduces the width of the Schottky barriers for electrons; (b) negative V_{gs} reduces the width of Schottky barrier for holes.*

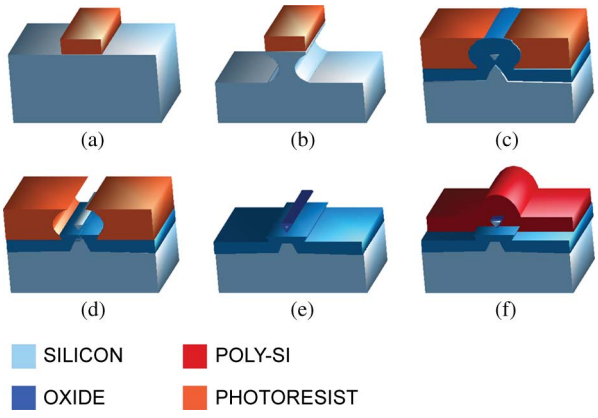

Fig. 9. *GAA SiNW SBFET process flow. (a) A photoresist line determines the nanowire position. (b) DRIE etching forms a scalloped trench. (c) After wet oxidation, the Si trench reduces to a suspended nanowire. The caves are filled with photoresist and planarized with CMP. (d) Buffered HF oxide etch releases the SiNWs. (e) Gate oxidation. (f) Polysilicon is deposited and patterned to form the gate.*

sacrificial oxidation is then carried out with the double purpose of eliminating the Si where the trench is thin, and also to reduce the surface roughness induced by the etching [Fig. 9(c)]. A combination of chemical mechanical polishing (CMP) and buffered HF (BHF) dip leaves vertically stacked nanowires suspended on a thick layer of insulating oxide [Fig. 9(d)]. The gate oxide is grown in a horizontal furnace with a dry atmosphere [Fig. 9(e)]. The gate polysilicon is conformally deposited and doped with phosphorous by means of a diffusion process and then patterned with a combination of isotropic and anisotropic plasma etching steps [Fig. 9(f)]. The fabrication of SBFETs requires the use of metallic source and drain contacts, meaning source-to-body and drain-to-body Schottky junctions. We pattern a Cr/Ni bilayers (10 nm/50 nm) on top of the Si pillars, partially covering the SiNW at the anchor points (see Fig. 10). This leads to the silicidation of the nanowire channel from the Cr/Ni bilayer toward the gated region of the nanowire. The process presented here is compatible with the one presented in [34] for dense SiNW FET arrays. An example of 3-D crossbar construction with 1 GAA poly-Si gate and 4 $\times$ 4 SiNW channels is shown in Fig. 11.

B. Poly-Si Nanowire FETs

The spacer technique is a promising approach to define subphotolithographic dimensions by using standard photolithography and CMOS steps [9]. The process flow is illustrated in Fig. 12. First, a sacrificial layer of SiO_2 is defined on a Si substrate followed by the deposition of a thin conformal layer of poly-Si [Fig. 12(a)]. Next, the poly-Si is etched by a reactive ion etching (RIE) technique, in order to remove the lateral layer and keep the sidewalls as a spacer [Fig. 12(b)]. Then a second low temperature

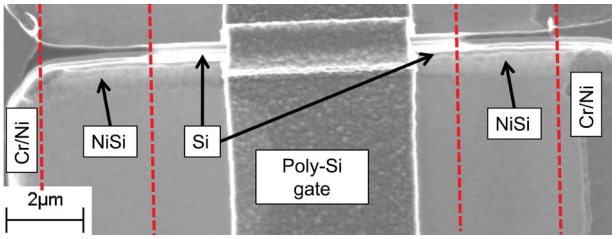

Fig. 10. *GAA SiNW SBFET with Cr/Ni source/drain after the liftoff process. The change in contrast on the NW channel is attributed to a difference between Si and silicided regions.*

oxide (LTO) spacer is defined next to the poly-Si in order to isolate the first poly-Si spacer [Fig. 12(c)]. The spacers form the nanowires with thicknesses ranging between 20 and 60 nm. The contact regions of the undoped poly-Si nanowire are defined by the electron-beam evaporation of 10-nm Cr and 50-nm nichrome ($Ni_{0.8}Cr_{0.2}$) and liftoff [Fig. 12(d)]. The Cr enhances the adhesion and thermal stability of Ni to oxidation during the following two-step annealing process. The substrate is used as a back-gate with a thick dry oxide as insulator (up to 400 nm thick). A scanning electron microscope (SEM) image of the obtained structure with an additional top gate defined on the poly-SiNW is shown in Fig. 13. This process has been reported for the construction of dense poly-SiNW crossbar arrays [40]. A small crossbar with one upper poly-SiNW and four lower poly-SiNW is shown in Fig. 14.

C. Low-Temperature Fabrication of α-Si Nanowires FETs

The fabrication process starts with the formation of isolation and active layers on a bulk-Si substrate. The isolation is composed of a 500-nm-thick wet oxide and a 100-nm LTO layer. Then, a 100-nm α-Si film is deposited as the active layer. A 70-nm-thick dilution of hydrogen-silsesquioxane (HSQ) is spin coated and patterned with e-beam lithography. Lines having widths ranging from

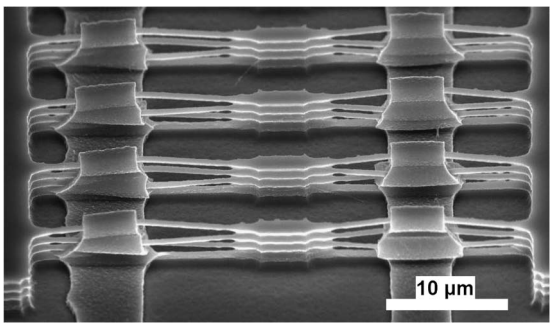

Fig. 11. *A 4 × 4 SiNW array with 2 poly-Si gate-all-around construction. The image is taken from [34].*

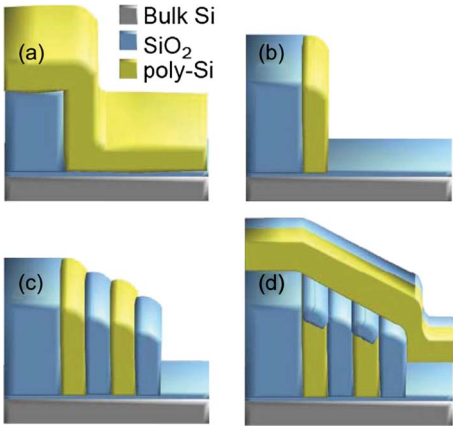

Fig. 12. *Nanowire arrays constructed using multi-spacer patterning technique [36]. (a) Conformal deposition of poly-Si. (b) RIE etch. (c) Definition of a SiO_2 spacer and iteration of previous steps. (d) Contacts formation.*

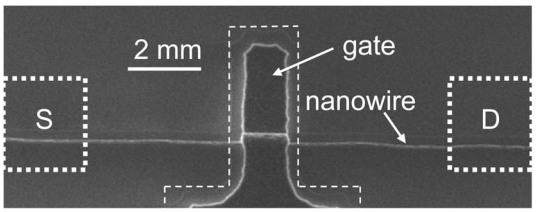

Fig. 13. *SEM image of a poly-SiNW with a top gate and $Cr/Ni_{0.8}Cr_{0.2}$*

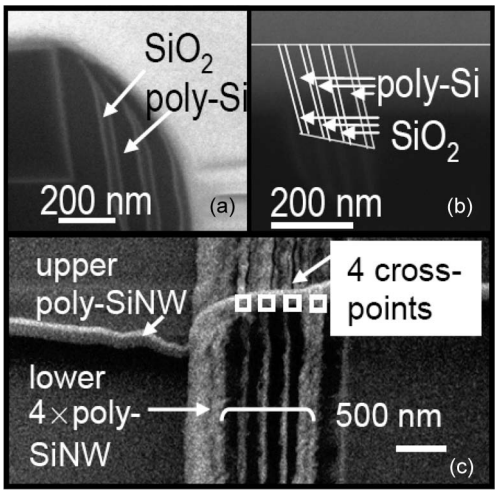

Fig. 14. *(a) Poly-Si NWs cross-section. (b) Poly-Si and SiO_2 spacers. (c) SEM image of a small crossbar with 1 upper and 4 lower poly-Si spacers [40].*

70 to 250 nm have been used as mask for Si dry etching. An LTO under etch and HSQ strip has been performed by a dip BHF step. The obtained α-Si nanowires are then covered by a 40-nm dry oxide and a 50-nm LPCVD poly-Si

layers. Large 100 μm $\times$ 100 μm poly-Si pads and gates are etched with an anisotropic SF_6 plasma etching recipe. Thus, poly-Si Ω-gated FinFETs with gate lengths between 1 and 10 μm are obtained.

Then, a bilayer of 20-nm Ti/55-nm Ni is patterned with liftoff to form electrical contacts between the Si nanowires and the pads. A 400 °C furnace annealing step forms Ni_xSi_y silicide source and drain Schottky junctions at the metal/Si interface. The Ti layer serves as cap layer to prevent Ni oxidation. Ni silicide process has been chosen for its midgap work function and for its use in α-Si metal induced recrystallization process [41]. The fabrication flow is completed by the patterning of Al-gated devices by means of a stencil deposition approach. The full wafer stencil mask contains 100-nm-thick SiN membranes with apertures having widths between 100 nm and 1 μm [42]. Through these, material for the transistor gates is deposited. The stencil is manually aligned to the substrate with 2-μm [42] accuracy using a customized SUSS MA/BA6 mask aligner [43]. The clamped substrate-stencil setup is placed in an evaporator where 100-nm-thick Al gates are deposited. FinFETs and inverters with up to 62-μm nanowire length were fabricated. An example of a 2-μm-long poly-Si gate FinFET having 100 nm $\times$ 65 nm Si nanowire channel is shown in the SEM tilted view of Fig. 15(a). In Fig. 15(b), a Si nanowire transistor with 130 nm $\times$ 65 nm channel [see Fig. 16(d)] cross section and 700-nm large stenciled Al gate is shown. Focused ion beam (FIB) cross sections [see Fig. 16(a)–(c)] demonstrate nanowire channels sections having widths between 65 and 130 nm. The total Si thickness is reduced from the initial value of 100 to 65 nm due to processing. Narrower nanowires (the expected nanowire size was around 35 nm) detached from the isolation layer due to LTO under etch caused by the dip BHF step.

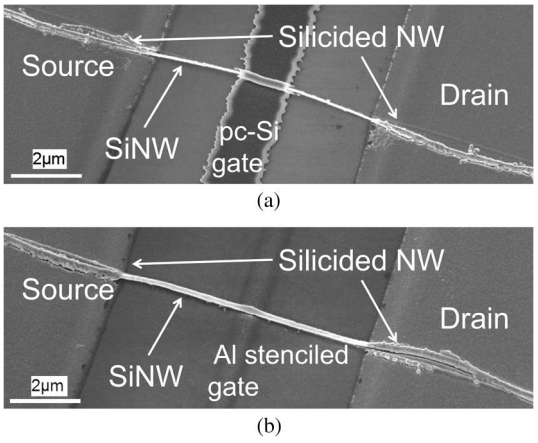

Fig. 15. *FinFETs with silicided nanowire portions at source/drain contacts: (a) poly-Si FinFET having 2-μm-long gate and 60 nm $\times$ 65 nm channel cross section. (b) Al stenciled FinFET having 700-nm gate length and 60 nm $\times$ 140 nm channel cross section.*

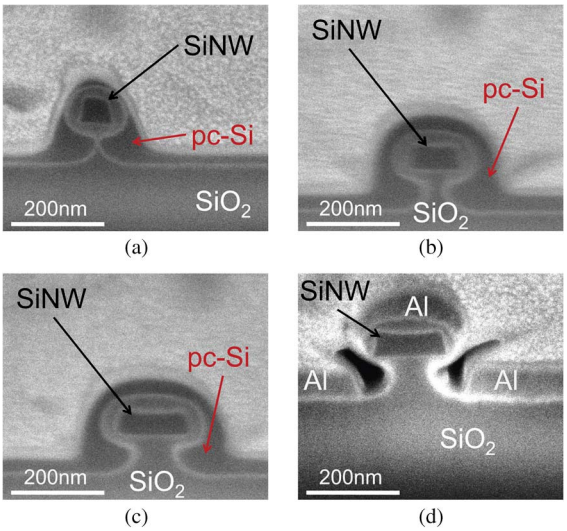

Fig. 16. *FIB cross sections showing the nanowire channels embedded in 40-nm oxide and gate materials: (a) poly-Si -gate FinFET with 60 nm $\times$ 65 nm section; (b) poly-Si -gate FinFET with 60 nm $\times$ 110 nm section; (c) poly-Si -gate FinFET with 60 nm $\times$ 140 nm section; (d) Al stenciled-gate FinFET with 60 nm $\times$ 140 nm section.*

V. FOUR-TERMINAL MEMRISTIVE DEVICES

Memristive functionality can be seen as state variable that can be used for more expressive logic gates [6]. The memristive behavior reported in Section III for the SB SiNW FETs can be tuned by operating on the polarity of the gate voltage. This type of behavior is linked with the

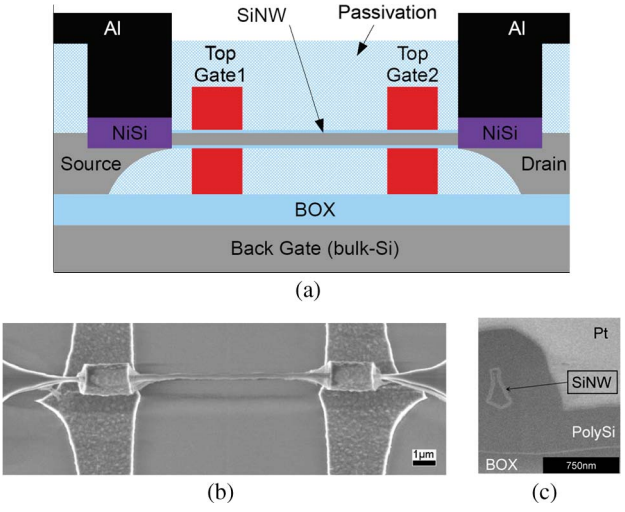

Fig. 17. *(a) Schematic cross section of a dual-gate device with NiSi source and drain regions on SOI substrate. (b) A 20-μm-long SiNW with two parallel GAA polysilicon gates having 4-μm gate lengths. (c) A FIB cut cross-section image showing the SiNW channel surrounded by a 500-nm polysilicon top gate.*

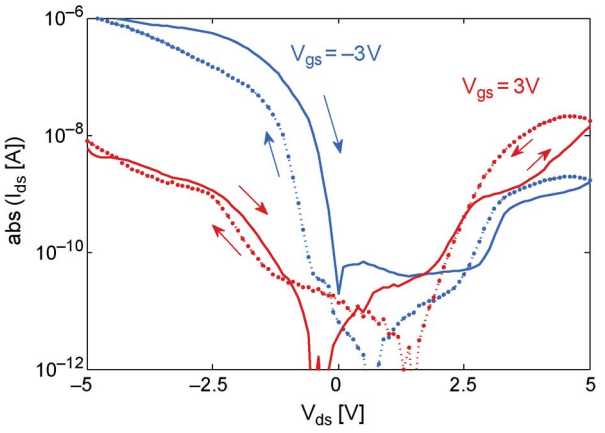

Fig. 18. ***Controlled memristance for fixed top and back gate voltages $V_{bf} = -5$ V.***

double conductance, for holes and electrons. As described in [44] for SB carbon-nanotube (CNT) FETS, the ambipolarity can be controlled by using an additional control gate, such that it blocks one type of carrier conductance. Following this principle, four-terminal memristive SB SiNW FETs can be built (see Fig. 17). In the following, two modes of operation are reported, depending on the nature of the controlling signal applied at the Si nanowire channel.

A. Voltage-Controlled Four-Terminal Memristive Device

A voltage-controlled four-terminal memristive Schottky barrier SiNW FET is obtained by using a dual-gate configuration such that one of the two gates is controlling a portion of the channel that is between the source/drain contacts and the main gate. This configuration is exploited to control the ambipolarity imbalance, such as for CNT FETs [44]. Since the back-gate voltage

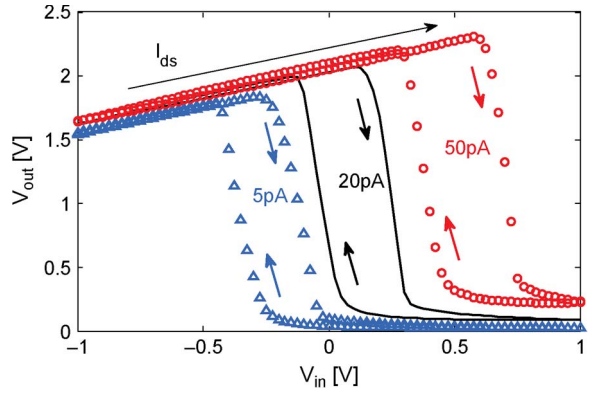

Fig. 19. ***Current-controlled memristive Schottky barrier SiNW FET hysteresis loop.***

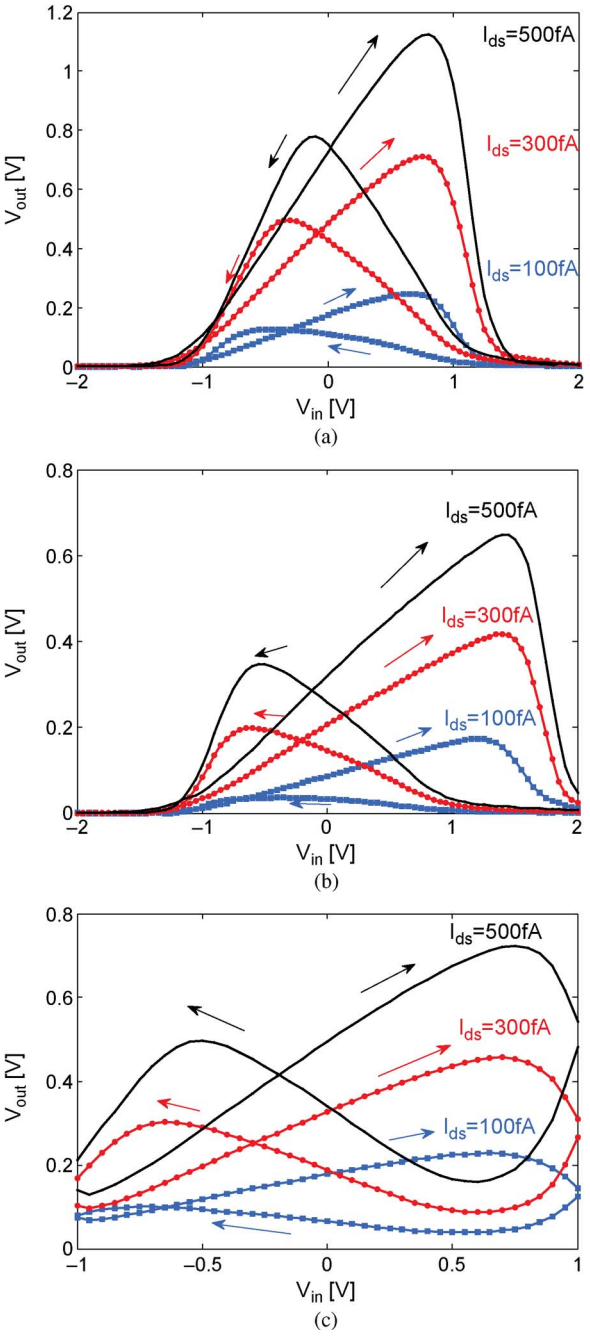

Fig. 20. ***V_{out} voltages for increasing with I_{ds} current bias. In all the figures I_{ds} bias values are 100, 300, and 500 fA. Notice the output voltage hysteresis narrows for increasing frequency sweep: (a) 24 s; (b) 6 s; and (c) 0.5 s.***

modifies the ambipolar conductance, this fact can be used in ambipolar memristive devices to limit the current levels for one of the carriers. A fixed back-gate voltage $V_{bg} = 0$ V leads to imbalanced bistable hysteresis loops under different V_{gs} voltages. By applying a negative $V_{bg} = -5$ V this imbalance is toggled for the negative side of the characteristics, giving a complementary effect (Fig. 18).

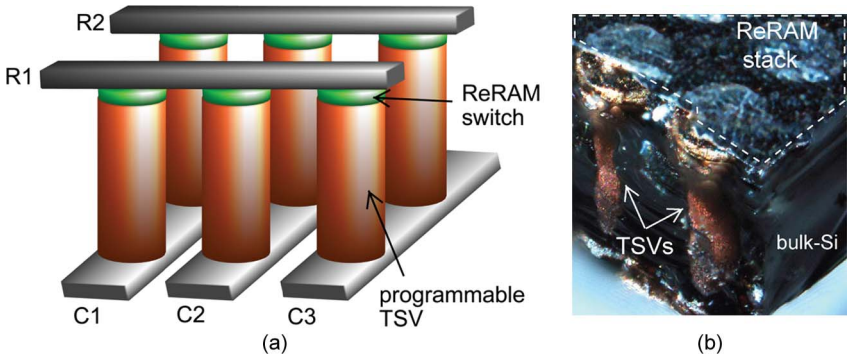

Fig. 21. *(a) A crossbar architecture with programmable TSVs made of ReRAM stacks [21]. (b) Reconstructed 3-D photograph of the TSV-ReRAM stack. The die is cleaved in order to reveal the TSV and the ReRAM layer deposited on top.*

Finally, a $V_{bg} = +5$ V levels off the conductances of electrons and holes, giving a pretty symmetric hysteresis.

B. Current-Controlled Four-Terminal Memristive Devices

A current-controlled version of the four-terminal memristive Schottky barrier SiNW FET is obtained by using a current I_{ds} bias instead of a V_{ds}. The output voltage is then compared with V_{gs} (Fig. 19). The obtained hysteresis can be used as a latch device, whose position in the $V_{out} - V_{in}$ plane can be adjusted by using a different value of the current bias. A similar behavior has been exploited with three-terminal Schottky-barrier polysilicon nanowire FETs circuits to build a new logic family based on precharge and evaluation scheme [45]. Moreover, a similar scheme has been demonstrated for DRAM type of memory [46] and for pA current and temperature detection [47]. Similarly, SB Si nanowire transistors fabricated with a low thermal budget process and biased in current-controlled mode shows a similar hysteresis. Moreover, polycrystalline SiNWs SB FETs can give a hysteretic transfer characteristic (Fig. 20) very similar to the one reported for crystilline SiNW SB FETs fabricated with a low thermal budget process [39]. As is shown in Fig. 20, the maximum output voltage in the transfer characteristics increases with the I_{ds} bias current. From Fig. 20(a)–(c), the sweep time is reduced. Similarly to what was discussed for the three-terminal SB SiNW FET memristive device, the sweeping time impacts on the amount of charge that traps at the gate oxide/channel interface, thus influencing the conductance state of the nanowire channel. A faster sweeping time outbalances the charge trapping/detrapping mechanism, resulting in lower output voltages [see Fig. 20(a) and (b) compared with Fig. 20(c)].

VI. APPLICATIONS

Very different applications belonging to signal processing, memory, and sensing are envisaged for multiterminal memristive devices. The possibility to build very dense crossbar arrays of two-terminal memristive devices is often seen as a disruptive technology for ultradense ReRAM or write at once (WORM) nonvolatile memory storage [48]. In this concern, all the nonvolatile two-terminal memristive technologies are suitable candidates to replace flash memory in the future, given their higher density storage per cost. This feature is especially interesting because it can be utilized to stack nonvolatile memory elements in the back-end-of-the-line, increasing both density and access speed among logic and memory layers. Good examples are the recently proposed hybrid semiconductor/nanowire/molecular (CMOL) integrated circuits [49], as well as 3-D field-programmable gate array (FPGA) architectures with programmable through silicon vias (TSVs) [21] (see Fig. 21). The two-terminal memristive crossbars can also be integrated into programmable logic array architectures to compute Boolean logic functions. The memristive crossbar architecture can be exploited to reprogram itself. For instance, in [50], a very dense nanowire crossbar with TiO_2 memristive junctions was used to perform logic functions and to store the result into another portion of the same crossbar. Moreover, memristive switches can be used to perform material implication function[1] and exploited to build latches that use resistance in place of voltage or charges as physical state variable [6]. Another application that can exploit the memristive functionality is related to the design of cellular neural networks [8]. The Hodgkin–Huxley model for the synapse was one of the earlier examples reported by Chua and Kang [5] of systems that can be modeled with the memristor. Recently, the use of two-terminal memristive devices in combination with digital-to-analog converters demonstrated a way of reproducing the associative memory of animals [51]. The modification of the memristive characteristic to environmental condition can also be utilized for different types of

[1]Here for material implication it is meant a fundamental Boolean logic operation on two variables "p" and "q" such that pIMPq is equivalent to (NOTp)ORq.

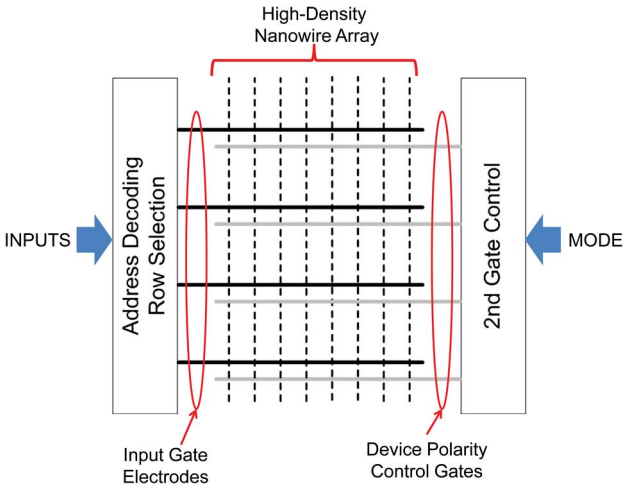

Fig. 22. ***A crossbar architecture with polarity control and address decoding made with high-density four-terminal memristive SiNW arrays.***

sensing. For instance, functionalization of nanowires with redox active molecules give rise to the typical memristive pinched hysteresis loop [52]. Another example can be the sensing of temperature with spintronic memristor [53]. The temperature change can cause a variation of the domain-wall mobility that in turn is sensed thanks to a positive feedback loop electronics. This type of sensor has been reported to be very compact ($\leq 1\ \mu m^2$ cell size) and to operate with very low power.

Multiterminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [32] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for biomolecule detection in dry environment [30]. More specifically, in [30], the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authors [47]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [45]. For instance, in [45], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR, and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing a hysteretical negative differential resistance [46]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel. In Section IV, it is shown that a similar hysteresis can also be obtained independently on the phase state of the Si nanowire channel. Similarly, the same structure can exploit the functionality of an additional gate to tune the polarity of an SB SiNW FET, thus giving even more functionality (Section IV). A very high expressive power architecture can be made of four-terminal memristive devices arranged in a crossbar implementation that exploits the high density of the SiNW arrays (Fig. 22).

VII. CONCLUSION

A general overview on multiterminal memristive devices is reported. The functionality of the devices can be used for logic, memory and sensing applications. Ultradense memristive ReRAMs crossbar arrays can be used for ultradense nonvolatile memory storage. It was shown that three- and four-terminal memristive devices can be used for both logic and memory applications. In particular, Schottky-barrier silicon nanowire FETs are very interesting devices due to their CMOS compatibility and ease of fabrication. Disruptive applications exploiting the high expressive power of four-terminal memristive devices arranged in crossbar arrays are foreseen as a significant advance in the electronic computation. ■

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