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RESEARCH ARTICLE

Silicon Nanowire Arrays and Crossbars: Top-Down Fabrication Techniques and Circuit Applications

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Several nanowire technologies have emerged recently, providing a way to continue the scaling down of *complementary metal-oxide-semiconductor (CMOS)* technology. The opportunities offered at the level of logic circuit design depend on the technology properties, and some applications seem to be suitable for specific technologies. In this paper, we survey three nanowire technologies that yield nanowire arrays. All of them depend on the photolithography limit but they differ with respect to the processing and the device properties. We show the ability of the spacer technique to yield nanowires with a pitch below the photolithography limit. We introduce the nanowire crossbars in a pure CMOS process and extract the parasitics that affect nanowire crossbar circuits. Vertically stacked nanowires are also demonstrated with the *deep reactive ion etching (DRIE)* process. We link the surveyed processes to specific circuit architectures that are optimized for the considered technologies. A nanowire decoder for sub-lithographic nanowires is demonstrated with the smallest size compared to other competing technologies. Then an optimized crossbar multiplexer is presented, which takes into account the presence of parasitics. Finally, a general library of logic gates based on vertically stacked nanowires is evaluated showing a smaller area and a better performance than CMOS.

Keywords: Silicon Nanowires, Spacer Technique, Deep Reactive Ion Etching, Memory, Reconfigurable Logic, Crossbar.

1. INTRODUCTION

The further scaling of *complementary metal-oxide-semiconductor (CMOS)* technology is enabled by *silicon nanowires (SiNWs)*. Such devices are promising not for the 1-dimensional nature *per se*, but mainly due to their inherent cost effectiveness, when they are embedded as the channel of *field effect transistors (FETs)*. As a matter of fact, the increasing photolithography constraints can be addressed by a regular organization of SiNWs into arrays. The obtained structures are compatible with the technology booster techniques described in the ITRS chapters,[1] including strained silicon channel, silicide contacts, 3-dimensional device architectures, etc. Different approaches have been suggested for the fabrication of *nanowire (NW)* arrays. While some of them are based on the growth of nanowires form a silicon-based seed, which are commonly called *bottom-up* techniques, the others are based on photolithography and yield regular arrays of nanowires. These approaches are called *top-down* techniques.

The bottom-up approaches are generally based on the growth of silicon nanowires on a silicon substrate. The growth position, dimensions and doping concentration are controlled *in situ* within a certain variability range that depends on the maturity of the considered process. Following the growth process, the obtained SiNWs are collected from the seed substrate and dispersed onto the target substrate using fluidic techniques.[2,3] These techniques yield very small nanowires and compete with lithography-based top-down technique. However, if the accuracy of the alignment is of highest interest, the top-down approaches are more promising candidates, allowing for the arrangement of nanowire layers with a pitch down to a few tens of nanometers.[4]

In this work, we survey three top-down nanowire fabrication techniques which can be optimized according to specific applications. While they all share their dependency on the lithographic dimensions in a certain way, some of them offer the opportunity to reduce either the nanowire dimension, the pitch or both beyond this limit. Moreover, 2-dimensional and 3-dimensional definition of nanowire arrays are addressed. Our interest in this paper is not only

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on the technology but also on the electronic application. We particularly focus on the link between the considered fabrication technique and the optimal applications in the field of logic design.

This paper is organized as follows. We first survey the existing literature on nanowire array fabrication and design approaches in Section 2. Then we introduce in Section 3 three top-down techniques for the fabrication of nanowire arrays, covering the spacer technique, the pure lithography and the *deep reactive ion etching (DRIE)* technique. Following the survey of the technology options, we explain in Section 4 the baseline architecture that will be investigated within the frame of the presented technologies. In Section 5, we present different electronic application for which those techniques may be suited, including dense nanowire decoders, multiplexers and 3-dimensional logic gates. Then, we summarize the different approaches and discuss their limitations in Section 6. We conclude the paper with Section 7.

2. BACKGROUND AND RELATED WORK

This section surveys previous research works related to the emerging nanowire techniques. It includes both bottom-up and top-down approaches and highlights the reported results in terms of device quality and array density. Following this technology survey, we look into the reported applications of nanowire arrays, which range from interconnect crossbars, to memories and full computational units.

2.1. Nanowire Technologies

Bottom-up techniques are based on the growth of nanowires on a silicon substrate from catalyst seeds. The as-grown nanowires are then collected in a solution and dispersed on top of the substrate to be functionalized. In Ref. [2], the control of the nanowire thickness down to 4 to 5 nm and a length of several micrometers is reported. The orientation of the as-obtained nanowires could be controlled by tuning the growth process parameters. In Ref. [3], the nanowire deposition is performed in large arrays with controlled pitch in the range of the nm to μm scale using the fluidic technique called *Langmuir-Blodgett technique*.

When it comes to lithographic approaches, the spacer technique has been presented as a possible way to overcome the limitations of photolithography 5, 6. It is based on the iteration of the definition of successive spacers that can be either used as the active device area, or as a mold to pattern the active device area on the target substrate.[7, 8] This technique has been applied in order to fabricate *fin field effect transistors (Fin FETs)* with shorter gate length and higher performance than lithographically defined *metal-oxide-semiconductor field effect transistors (MOS FETs)*.[9] The iteration of the spacer definition following an *additive* or a *multiplicative road* is reported in Refs. [10, 11]. Another technique based on the definition of nanoridges by means of successive wet etching and oxidation is reported in Ref. [4].

Using standard photolithography techniques, it could be demonstrated that 3-dimensional vertical stacks of nanowires can be achieved. A possible method was presented in Refs. [12, 13], which is based on the alternation of etching and passivation steps in a similar way to the DRIE technique. This method yields scalloping edges, that can be thinned out through self-limited oxidation and controlled wet etch, resulting in vertical stacks of suspended nanowires. A fully different technique[14] uses alternating epitaxial Si and Ge layers; then, a selective etching of the Ge layers releases the thin suspended Si layers, which can be transformed into suspended Si nanowire stacks by accurately controlling their lateral etch.

2.2. Nanowire Circuits

In a crossbar circuit,[15] parallel nanowires are organized in two perpendicular layers crossing each other at the *crosspoints*, thus providing a large improvement in terms of area and a higher regularity compared to CMOS.[15] Crossbars are useful to build ultra-dense reconfigurable circuits with emerging devices. The NWs can be used to carry signals locally; it is also possible to perform computation and information storage by functionalizing the crosspoints, which consists in defining active or passive elements at the crosspoints. The elements that have been suggested range from $p-n$ junctions[16] to FETs[17] and molecular programmable switches/diodes.[18]

In Ref. [18], molecular diode-switches at the crossbar intersections are demonstrated and the structure is used in a diode logic in order to implement a *programmable logic array (PLA)*. A more convenient solution, which avoid the level restoration required by the diode logic consists in using FET logic as introduced in Ref. [19]. The same concept is extended in Ref. [20] by creating a double-stage combinational logic on FET crossbars. This structure is used as a general fabric to implement a nanoprocessor. In Ref. [21], very dense interconnect networks using nanowire arrays are suggested within a hybrid CMOS circuit.

3. TOP-DOWN NANOWIRE TECHNOLOGIES

This section surveys different lithography-based nanowire technologies. The first technique uses lithography in order to define the active area, however the nanowire definition is lithography-independent, which offers the opportunity to control the nanowire dimensions and pitch below the lithography limit and to organize the nanowires in a crossbar. The second technique is based on photolithography on a SOI wafer with a thin active layer. This is a standard CMOS process, which gives us an insight into the

parasitics affecting the performance of nanowire crossbars. The third technique uses lithography in order to define the nanowire footprint, which is then thinned out by means of controlled etching and oxidation. This technique offers the advantage of controlling the nanowire dimension below the lithography limit and stacking them vertically. In the following we explain the details of these techniques.

3.1. Spacer-Based Nanowire Arrays

The fabrication process of a single nanowire layer is shown in Figure 1 and was described in Ref. [22]. The process is based on the iterative definition of thin spacers with alternating semiconducting and insulating materials. The resulting thin parallel layers are used as semiconducting and insulating nanowires. The process starts with the definition of a 1-μm SiO_2 layer on a Boron-doped Si substrate covered by a wet oxide. A first sacrificial layer is defined (step 1) in the wet oxide. Then, a thin conformal layer of poly-Si is deposited by *low pressure chemical vapor deposition (LPCVD)* with a thickness of a few tens of nanometer (step 2). Subsequently, we etch this layer with a *reactive ion etching (RIE)* equipment using Cl_2 plasma. This physical etch removes the horizontal layer while keeping the sidewall as a spacer (step 3); and the poly-Si spacer is densified at 700 °C for 1 h. Then, the poly-Si spacer is partially oxidized and the successive poly-Si spacers are thereby insulated. Another option consists in depositing a conformal insulating layer of *low temperature oxide (LTO)* obtained by LPCVD, which is thereafter densified for 45 min, and then etched in a RIE etchant using a fluorine plasma in order to remove the horizontal layer and keep the vertical LTO spacer. These operations of poly-Si and SiO_2 spacer definition are repeated a number of times resulting in a multi-spacer alternating poly-Si and SiO_2 nanowires (step 4).

It is also possible to repeat the definition of the nanowire spacer on top of an existing nanowire layer, perpendicularly to it, resulting in nanowire crossbars. The bottom multi-spacer is fabricated as explained previously, then a thin insulating dry oxide is grown and the top sacrificial layer is defined with LTO perpendicularly to the direction of the bottom sacrificial layer. Then a poly-Si spacer is defined at the edge of the top sacrificial layer in a similar way to the bottom poly-Si spacers. The operations mentioned previously can be iterated in order to define alternating poly-Si/oxide spacers. To visualize the structure, the separation dry oxide and both sacrificial layers can be removed in a buffered HF solution showing the resulting poly-Si nanowire crossbar.

In order to access the sub-lithographic nanowire array through the lithographic CMOS circuit, a fabrication flow that includes the decoder in a spacer-based nanowire process has been proposed in Ref. [23] and it represents an extension inserted between steps 3 and 4 in Figure 1, while other steps remain unchanged. The purpose of these steps is to pattern the nanowires differently in order to identify them. The additional steps are lithography patterning and light doping after every spacer definition step, using *p*-type (*n*-type) doping to increase (decrease) the total doping level. Specific regions from every poly-Si nanowire are defined and doped in this way. The total doping level of a specific region is the sum of all (positive and negative) doping levels accumulated in this region throughout the definition of the whole array. An optimized choice of the lithography/doping sequences and the light doping doses may result in the desired nanowire pattern.

Figure 2(a) shows a SEM image of 3 poly-SiNW separated by LTO NWs with a poly-SiNWs thickness of 54 nm. The height of the first poly-SiNW is about the height of the sacrificial layer and it has a rounded corner due to the conformal poly-Si deposition and the following etching procedure. We can see a decrease of the poly-SiNW height with the number of nanowires in the multi-spacer. Figure 2(b) shows poly-SiNW have a width of 20 nm obtained by the deposition of thinner poly-Si. For the device in this

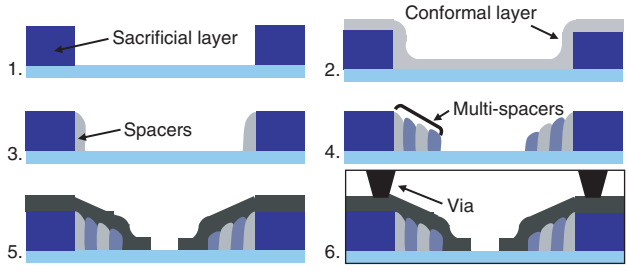

Fig. 1. Main process steps:[22] (1) Definition of sacrificial layers (2) Conformal deposition of poly-Si. (3) RIE etch. (4) Alternation of poly-Si/SiO_2 spacers. (5) Definition of the gate stack. (6) Passivation and metallization.

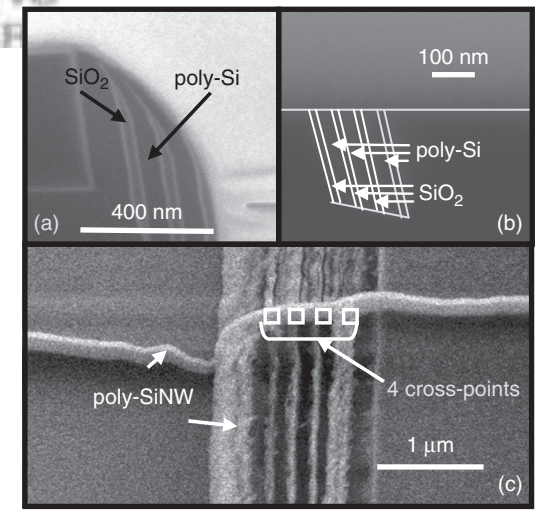

Fig. 2. SEM images of multi-spacers and a small crossbar.[22] (a) Alternating 54 nm thin poly-Si and LTO spacers. (b) Scaling down to 20 nm thin poly-Si. (c) Small 4 × 1 crossbar with 1 upper and 4 lower poly-Si spacers.

SEM image, the multi-spacer was planarized using *chemical mechanical polishing (CMP)* in order to remove the rounded-corner effect reported in Figure 2(a). The possible use of the MSPT for the fabrication of two perpendicular layers of crossing NWs is illustrated in Figure 2(c) with one poly-SiNW crossing 4 poly-SiNWs underneath it.

3.2. FDSOI-Based Nanowire Arrays

Using a *fully-depleted silicon-on-insulator (FDSOI)* process, wires can be manufactured with ultra regular lines as demonstrated in Ref. [24]. In this section, we conceptually complete the already established process for a single layer of parallel nanowires, with a perpendicular top layer of parallel nanowires. In the proposed process, the bottommost nanowires are defined using photo-lithography at the lithographic pitch, and their dimensions could be controlled through oxidation and etching below the lithographic limit down to 15 nm.[25] Thereby, both *n*- and *p*-type doping are allowed. This technique reduces the nanowire width without any impact on their pitch or density. On the other hand, the topmost lines are defined as polycrystalline silicon (poly-Si) stripes at the lithographic scale. These two perpendicular layers of parallel lines form a crossbar whereby the intersections represent the crosspoints. In such a crossbar, the top lines can electrostatically control the nanowires underneath them at the crosspoints in a FET fashion when the ladders are covered by a gate oxide. Moreover, the top nanowires can form an ohmic contact to those lying underneath them when a via is defined at crosspoint.

Figure 3 shows the associated process flow. A *p*-type SOI substrate is patterned by lithography to form parallel ridges that are subsequently etched into nanowires. *Plasma doping (PLAD)* is used to softly define *n*-type wires.[26] Then, the nanowires are passivated in oxide and planarized (Fig. 3(a)). Following this step, the passive regions, i.e., the parts of the nanowires connecting every series FETs, are defined by *n*- and *p*-type PLAD on the *p*- and *n*-type nanowires respectively (Fig. 3(b)). It is worth noting that the implantation step is performed softly because of the small dimensions of the nanowires. Thus, dopants do not migrate too far. Moreover, these are separated by an oxide, which limits further the diffusion of dopants. This reduces the requirements on spacing, which are generally included in the design rules. This allows to reach the smallest lithographic dimensions for all operations of patterning and doping. Then, the gate stack is defined by depositing the gate insulator, followed by the poly-silicon gate deposition and etch (Fig. 3(c)). The poly-silicon lines carrying the gates are defined with regular parallel lines. At this level, the active devices are defined and the east–west connections between them are established through the passive parts of the nanowires, operating as resistances.

The north–south connections are performed with the poly-silicon lines and require the definition of vias between them and the nanowires underneath them. The vias are defined by etching the poly-silicon lines and filling it with a metal. In order to decrease the resistance of the north–south poly-silicon lines and the passive parts of the east–west silicon NW lines, it is possible to sputter a thin layer of nickel (or platinum) over the whole structure. An annealing process is then used to control the growth of a low resistance silicide phase at the metal/silicon interface (Fig. 3(d)). Thereby, it is important to first etch the oxide covering the passive regions before sputtering the metal. The unreacted metal after the diffusion can be selectively removed by wet etching. Finally, the contacts between the crossbar and the outer circuit are performed through conventional metallization steps (Fig. 3(e)).

3.3. DRIE-Based Nanowire Arrays

A process flow for the fabrication of the Schottky barrier SiNW FETs has been reported earlier.[12] Here we summarize some of the critical steps. A slightly *p*-doped *silicon on insulator (SOI)* wafer is used as the substrate. Then a DRIE step is carried out to form horizontal strands of suspended Si nanoribbons over the *buried oxide (BOX)*. The wide Si nanoribbons anchored to two Si pillars are smoothed and thinned down to a 100 nm diameter

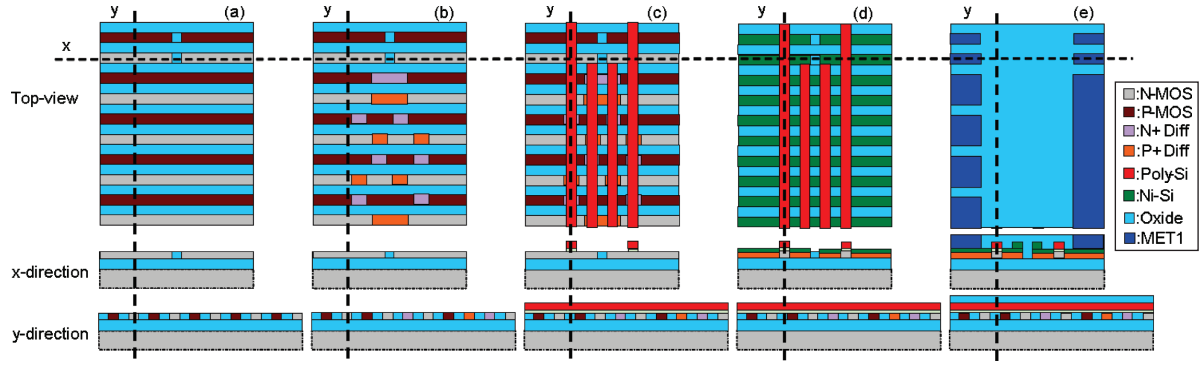

Fig. 3. Manufacturing process to build a FDSOI crossbar: (a) grating patterning and active regions doping, (b) passive regions definition, (c) gate deposition, (d) passive regions finalization and salicidation, (e) metallization to contact passive regions.

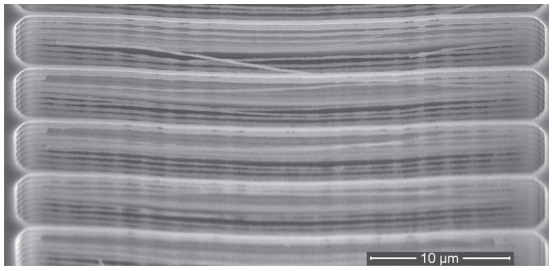

Fig. 4. High density array produced with the DRIE technique[12] consisting of multiple parallel strands of vertically-stacked SiNWs, each with a diameter of less than 100 nm. The structure is suitable for ultra-high dense 3D crossbar arrays of logic/memory elements.

cross-section by means of a 500-nm deep sacrificial oxidation step. After oxide removal, thinned Si nanowire arrays are obtained (see Fig. 4). Then a 20 nm dry oxidation is performed followed by a 500 nm LPCVD poly-Si layer. The patterning enables a device construction having two parallel poly-Si gates over 20 μm long SiNWs. A 1 μm high passivation layer of sputtered SiO_2 is deposited and used as hard mask for the metallization phase. Contact openings are patterned with lift-off. The self-alignment of the via openings with the lift-off is then exploited for the definition of 50 nm thick contact areas at the anchor points of the devices. This first metallization layer consists of a 50 nm Ni underneath 10 nm Al deposited by a standard e-beam evaporation tool. The Al is used as a cap layer to prevent Ni oxidation during the salicidation steps and to provide a good interface with the final metallization. Then a dual step salicidation annealing has been performed in a standard horizontal wall furnace to form NiSi source/drain regions. Finally, a 1-μm thick Al layer is patterned for electrical characterizations.

4. BASELINE ARCHITECTURE

The nanowire crossbar paradigm has appeared as a possible architecture for post-CMOS technologies[27, 28, 21] because it requires a simple processing and it can be used to implement configurable logic circuits. The baseline organization of a nanowire array is depicted in Figure 5.

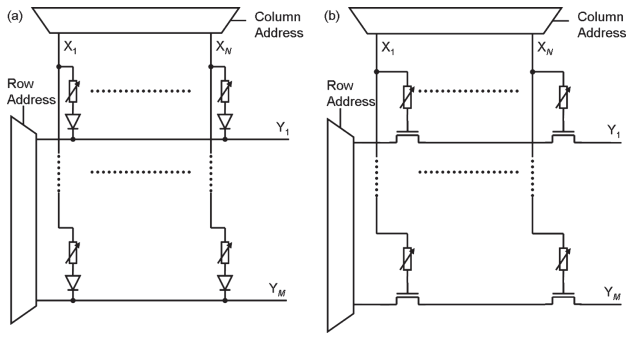

Fig. 5. Baseline nanowire array architecture: (a) using passive elements, (b) using active elements.

In the following, we consider the logic and decoder parts of the circuit.

4.1. Logic Core

An arrangement of two orthogonal layers of parallel nanowires defines a regular grid of intersections called crosspoints. The logic operation is realized with resistive memories deposited between the two nanowire layers. In Figure 5(a) only passive elements are used, consisting of a variable resistance and a diode. Both elements can be a single monolithic device.[29] This configuration can be implemented using the technique suggested in Section 3.1. The obtained circuit implements a resistor/diode logic.

For the nanowire crossbar architecture shown in Figure 5(b), each cross-point junction is made of a FET and a non-volatile memory element. This architecture has been suggested in Ref. [28] and it consists of defining FETs along the nanowires of the bottommost level. The effectiveness of the FET control signal, i.e., the gate voltage, depends on the resistance state of the memory element. On the one hand, a high resistance state makes the FET insensitive to the applied input voltage. On the other hand, the correct FET functionality is obtained as long as the memory element is at its low resistance state. The higher writing/erase voltages required to program the resistive element are compatible with the standard FET operation. This type of architecture requires a specific circuit organization which is explained in Section 3.2. For the sake of simplicity, the circuit organization of Section 3.2 the resistive elements are mimicked by the presence or absence of transistors, which is equivalent to a hard configuration of the circuit.

4.2. Programmable Part

The arrangement of the orthogonal layers of parallel nanowires does not operated as a logic circuit unless the programmable part is defined. It consists of a layer of *resistive random access memories (ReRAMs)* that is deposited between the crossing nanowires in order to enable the programmable logic operation between them. ReRAMs are two-terminal memories that store the information in their resistivity. Several types of resistive memories have been developped recently, and different physical phenomena inducing the resistance change have been identified. They include *phase-change memories (PCRAM)*, *oxide memories (OxRAM)* and *conductive-bridge memories (CBRAM)*, as well as redox-based resistance switching elements and molecular switches.

PCRAMs are formed by a thin film chalcogenide resistor, whose resistance can be tuned through suitable electrical pulses leading to a reversible phase change.[30] The chalcogenide material can exist in two different phases: a low-resistive, ordered, polycrystalline configuration and a high-resistive, disordered, amorphous configuration.[31]

Intermediate states also exist, allowing for a multi-valued logic information storage. Different variations of this technology have been demonstrated. For instance, in Ref. [29], a diode has been embedded in the resistive memory element in oder to introduce a rectifying behavior. In Ref. [32], the phase-change resistive layer consists of molecular elements that change their resistance according to a redox reaction. When it comes to OxRAMs, those devices have a metal-insulator-metal structure. Depending on the combination of the oxide and the metal electrodes, the device can exhibit a resistivity switching behavior.[33] Finally, CBRAMs consists of a bottom electrode made of an inert material, which acts as the cathode. A layer of solid electrolyte material (chalcogenide or oxide) is deposited on top of the inert electrode, followed by a layer of anode (Ag and Cu). The resistance change is brought about by the formation and dissolution of a metallic filament between the anode and cathode.

The redox reactions driving resistive switching elements have been surveyed in Ref. [34]. Such elements are based on an insulating layer sandwiched between two metal layers. Different chemical phenomena have been identified as responsible for the switching behavior. The first mechanism is the bipolar electrochemical metallization. By applying a voltage at the metal electrodes, highly mobile cations drift from one metal layer into the insulating layer, where they discharge and lead to the growth of a conducting dendrite or filament, representing the on-state. The dendite can be dissolved by applying an oppposite voltage. The second mechanisme, the valence change, is described by the migration of anions and a subsequent change of the stoichiometry, leading to a redox reaction whose direction can be modulated by changing the voltage pulse duration. The third mechanism relies on thermochemisty, whereby the current-induced temperature increase leads to a change of the stoichiometry.

The molecular switches have attracted a large attention because of their small size, easy processing and expected high on-to-off-resistance ratio. In Ref. [35], it has been demonstrated that molecular switches are suited for terascale integration and beyond thanks to their dimensions ranging from 0.3 to 3 nm. The molecules can be grafted at the silicon stripes during a step that is between the front- and the back-end of line steps. The link between the nano-scale molecules and the larger CMOS circuit could be addressed by using adapded decoders. It is suggested that a sequence of alternating single and double bond in a π-conjugated molecule may be broken by oxidation, and several conduction mechanisms and CMOS-compatible etching and grafting procedures are proposed. The modelling of memories and reconfigurable circuits based on molecular switches have been addressed in Refs. [36 and 37] respectively, demonstrating the impact of the rectifying behavior of the molecular switches on the circuit performance.

4.3. Array Decoder

In any implementation of the nanowire array, a decoder is utilized in order to make every nanowire within this set uniquely addressable by the outer circuit (Fig. 5). Given the small nanowire pitch, usual decoders may be too bulky and may have a high cost in terms of silicon area. Different decoders have been suggested for nanowire arrays. Their design depends on the nanowire fabrication technology. Nanowires fabricated with a bottom-up approach can be addressed with an axial or radial decoder.[38, 39] These decoders are based on a random dispersion of nanowires whose pattern is defined by *in-situ* doping. Mask-based decoders[40] are proposed for nanowires fabricated with a top-down approach, whose pattern is deterministically defined by using a conventional mask. Random-contact decoders[41] use stochastic contact areas in order to address top-down nanowires. For other top-down techniques with a large pitch, a gate-all-around decoder is suggested in Ref. [42]. A conceptual approach to fabricate and design a specific decoder with the spacer technique is presented in Ref. [23].

5. NANOWIRE-BASED LOGIC CIRCUITS

This section introduces different logic circuits implemented using nanowire arrays. We fist focus on the access to the nanowire layers, which is carried out using nanowire decoders. Then, we look into the implementation of *multiplexers (MUXs)* with nanowire crossbars, which represent the basic blocs for *field-programmable gate arrays (FPGAs)*. Based on those MUXs, we quantify the performance and discuss the limiting technology factors. In the last part of this section, we look into regular *application-specific integrated circuits (ASICs)* implemented using vertical stacks of nanowire arrays.

5.1. Nanowire Decoders

A decoder is utilized in order to make every nanowire uniquely addressable by the outer circuit. It is formed by a series of transistors along the nanowire body, controlled by the poly-Si lines and having different threshold voltages.[43] Depending on the distribution of threshold voltages (V_T's) of the series transistors along the nanowires and on the sequence of applied voltages in the decoder (V_A's), one single nanowire in the array can be made conductive, which is required for a correct addressing operation.

Several decoders have been suggested, including stochastic[38, 39, 41] and deterministic approaches.[40, 23] A possible metrics that can be used to compare decoders is their size given by M, the required number of poly-Si lines needed to address N nanowires. Using light nanowires doped with different doses and the same type (either n or p), the minimal cost is given by $M = 2 \cdot \lceil \log_2(N) \rceil$.[43] With ultimately scaled nanowires, the dopant fluctuation

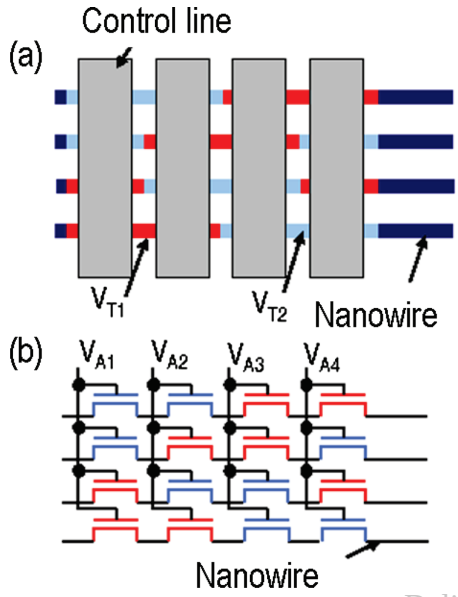

Fig. 6. Decoder circuit showing transistor threshold voltages V_T and applied voltages V_A: (a) layout view, (b) circuit schematic.

may be an issue; this will be addressed later. The minimal cost is just the half of this values, when a complementary logic (using both *n*- and *p*-type) is used; nevertheless, for technological reasons, this is not expected to be the case for nanowire decoders.[43] The randomness of stochastic approaches[38, 39, 41] results in a large overhead in M. Even the deterministic approach in Ref. [40] needs a certain overhead due to the dimension mismatch between the nanowires and the poly-Si lines. The cost M for these approaches is summarized in Table I.

In Ref. [23] a technology cost T has been defined as the number of additional process steps and a variability cost V as the sum of the variances of all doping regions. The following multi-linear mapping between these costs and the encoding scheme of the nanowires has been established:

$$T = \sum_{i=0}^{N-2} \tau_i + k_1$$

$$V = \left(\sum_{i=0}^{N-2} (i+1) \cdot \tau_i + k_2 \right) \cdot \sigma_0^2$$

with: τ_i the *Hamming distance* between code words i and $i+1$ of two successive nanowires, k_1 and k_2 constant numbers that depend on the pattern of the first nanowire, N the number of nanowires and σ_0^2 the unit variance of the threshold voltage induced by one single doping step.

By minimizing these costs, we interestingly find that the *Gray codes* represent the optimal encoding scheme for the nanowires. The spacer-based decoder is expected to yield the lowest possible cost in terms of M when the optimal Gray code is used (Table I).

5.2. Multiplexers

The array structure explained in Section 3.2 can be used to physically implement any logic circuit by folding the complementary branches around the contact pad. We investigate in this section the proposed approach based on the example of a *multiplexer (MUX)*. The choice of multiplexers is motivated by their intensive utilization in regular architectures such as FPGAs.

The proposed patterning style consists in alternating *p*- and *n*-type regions. This is particularly suited to build pass-gates between two contact pads. In Figure 7, we a show a multiplexer, which is based on pass-gates that are placed between its inputs and outputs. The addressing is realized using poly-Si lines, which are controlling all transistors. Control inputs are available with both polarities by using a primary inverter stage. It is worth noting that, alternatively, it is possible to group the *p*- and *n*-type regions separately, which is reminiscent to the traditional representation of CMOS circuits.

Several parasitic devices should be considered in the crossbar layout. We distinguish between two types of crosspoints with respect to their parasitic model: the active crosspoints operating as transistors, with a poly-Si line electrostatically controlling the Si line underneath it; and the passive crosspoints that are formed by a poly-Si line crossing a passivated highly doped Si line, without forming any FET. In the considered process, the passive crosspoints are formed by a highly-doped conductive Si wire crossing a salicide poly-Si line. The two lines are just separated by a thin layer of gate dielectric. Thus, the areas under the poly-Si lines, which are not used as a FET channel, result in an important parasitic capacitance between the two wires. Moreover, the parasitic resistance through the doped conductive areas and the electrostatic inter-wire capacitive coupling are modelled.

The optimization of the circuit and its underlying technology under the consideration of the parasitics requires the optimal oxide thickness of 6 nm (Fig. 8). Below this value, the parasitics of the passive crosspoints are dominating, and beyond this value, the FETs defined at the active crosspoints have a bad electrostatic control and they

Table I. Survey of reported digital nanowire decoders.

Reference	[38]	[39]	[41]	[40]	[23]
NW technique	Fluidic Assembly	Fluidic Assembly	Any Top-Down	NIL/SNAP	Spacer
NW decoder	Axial Decoder	Radial Decoder	Random Contact Decoder	Mask-Based Decoder	Spacer Decoder
Decoder type	Stochastic	Stochastic	Stochastic	Deterministic	Deterministic
M (Decoder size)	$\lceil 2.2 \cdot \log_2(N) \rceil + 11$	$\lceil 2.2 \cdot \log_2(N) \rceil + 11$	$\lceil 4.8 \cdot \log_2(N) \rceil + \mathcal{O}(1)$	$2.0 \cdot \lceil \log_2(N) \rceil + \mathcal{O}(1)$	$2.0 \cdot \lceil \log_2(N) \rceil$

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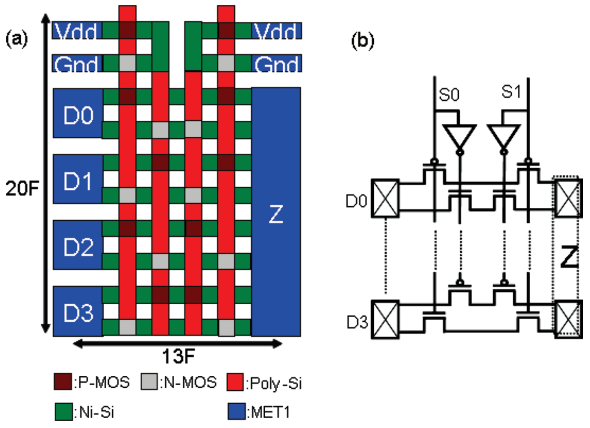

Fig. 7. A crossbar implementation of a 4:1 MUX for FPGAs: (a) layout view, (b) circuit schematic.

dominate the delay. Under these optimized conditions, we compared the performance of the crossbar MUX with the equivalent circuit in a 65-nm CMOS process. The performance of the crossbar MUX is poor in terms of the intrinsic delay (3.4× higher) because of the included parasitics, and it is better in terms of power consumption (1.5× lower) and area (6× lower) thanks to the compact crossbar.

5.3. General-Purpose Logic Gates

A new approach based on vertical SiNW crossbar arrays fabricated with the DRIE technique adds one more degree of freedom to circuit designers, which is the vertical silicon depth in bulk silicon technology. For instance, the large surface to volume ratio of SiNW arrays can be exploited to adjust the width of a device by tuning the number of channels. Besides that, due to the one dimensionality of the channels, specific technology boosters such as strain can be envisaged to enhance the performance compared with planar technology. Moreover, the SiNW channels are compatible with the atomic layer deposition of any of the high-κ, high-μ materials used to improve the performance of standard planar FETs. In the following, we investigate the design opportunity and we leverage impact of the technology boosters. We first introduce the design approach, then we perfom logic synthesis with the considered logic gates.

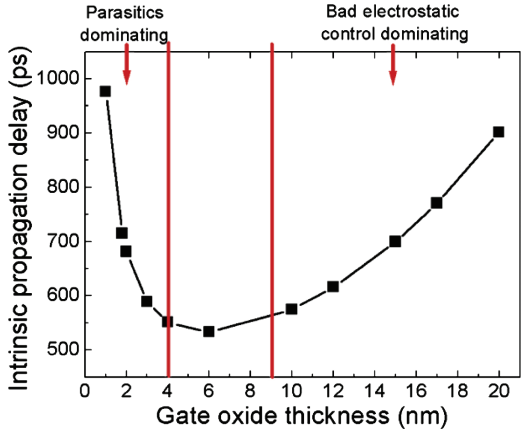

Fig. 8. Influence of gate oxide thickness on the MUX propagation delay (lithography half-pitch: 60 nm).

5.3.1. Logic Design with Vertically Stacked NWs

We illustrate the approach of vertically-stacked nanowire logic gates with a standard CMOS inverter. As depicted in Figure 9 either the pull-up or the pull-down networks are made of SiNW transistors anchored to source/drain pillars. The imbalance between hole and electron conductivities requires different transistor widths, which can be addressed by using a different number of vertical nanowire channels, depending on the current drive requirements for the specific gate. Ideally it is possible to increase the driving strength of a transistor without consuming the silicon estate.

In the proposed implementation, the source/drain access resistance to the nanowire stack is an important factor, which strongly depends on the engineering of the source/drain contacts to nanowires.[44] Another factor that limits the circuit performance is the additional parasitic capacitance due to the 3D structure. A way to solve this issue can be the integration of internal spacers between the gate and the source/drain pillars to drastically reduce parasitic capacitive coupling.[24]

In order to investigate the proposed approach, a set of combinational logic gates are evaluated in terms of delay, area and input capacitance from the current drive requirements. These values can be computed according to both design and technology parameters. In Ref. [45], 14 libraries have been obtained by varying two technology parameters: the access resistance (represented by R_s) and the strain (represented by the actual channel resistance, and a design parameter: the number of nanowire stacks). Based on this, a set of logic gates, including inverters, multiplexers, NAND and NOR gates, have been designed in every library using the linear switch model, which assumes that every logic gate is driving the same current as a unit inverter when it switches. This gives an insight into the

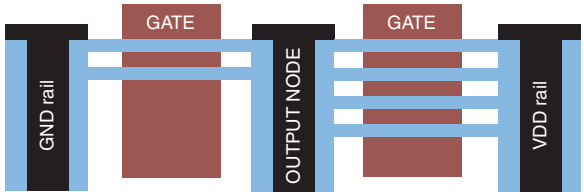

Fig. 9. Vertically-stacked inverter structure with SiNW channels anchored to Si pillars with a gate-all-around configuration. The number of vertically-stacked nanowires is adjusted to balance the mobility ratio between the PMOS and the NMOS sections.

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area and delay. The latter was estimated as the *fanout-of-four (FO4)* delay, i.e., assuming that every gate drives its own intrinsic delay and a load of 4 instances of itself.

5.3.2. Logic Synthesis with Vertically Stacked NWs

The logic gate libraries summarized in Section 5.3.1 can be generated by considering several combinations of technology and design parameters. A cost function depending on the number of vertical nanowires can be used to take into account the impact of parasitics on the performance. In particular, in Ref. [45] the technological parameters considered a strong degradation of the contact access resistance. The impact of the cost function on the performance can be relaxed by using a design choice that is in between a pure vertically-stacked nanowire solution and a planar solution, such as in FinFET technologies. The generic gate libraries can be used to synthesize any combinatorial logic circuit and to compare area and delay for different parameters. For instance, in Ref. [45], different *carry look-ahead adders CLA* were synthesized and compared for 14 libraries. It has been shown how the choice of a double stacking (design parameter) combined with a moderate level of strain booster (a technology parameter) for a 64-bit CLA can effectively re-balance the negative impact of 300% channel resistance increase while giving improved area and delays with respect to a planar solution (see Figure 10). Conversely, libraries designed for minimum area (i.e., smaller gate footprint but higher number of NWs in vertical stacks) always show an increased delay compared with the planar solutions because of the stack capacitance. Nevertheless, a reduction of the active area occupancy of up to 49% can be achieved without forcing the tool to map the circuits with the smallest gates, which represents a better trade-off with respect to delay. The delay can be further improved by taking into account the positive impact of strain. When we compare the SiNW implementation with a standard planar CMOS implementation, we notice that the technology and design boosters promise a better performance of the SiNW implementation with respect to planar CMOS by up to 30%.

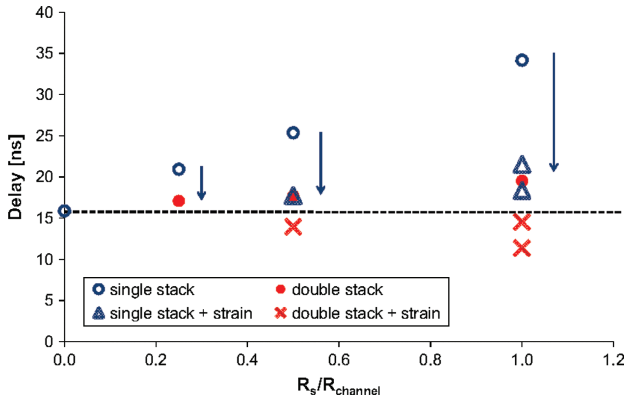

Fig. 10. Effect of strain on delay of a 64-bit carry look-ahead adder. Dashed horizontal line represent delay of planar technology. The plot shows that either using double stacks and/or strain improve delay. Notice that strained nanowires with double stacking outperform planar Si technology.

6. SUMMARY AND DISCUSSIONS

The three fabrication techniques for nanowire arrays presented in the paper offers an exclusive utilization of CMOS materials and the opportunity to organize logic circuits in a regular way, which enables a significant cost reduction and an enhancement of the technology abilities.

For what concern the spacer technique, it has the advantage of yielding a lithography-independent nanowire pitch. This raised the question of interfacing the sub-lithographic pitch with the lithography-dependent CMOS circuit. We showed the possibility of enhancing the process in order to design and optimize the nanowire decoder so that it has the minimum cost in terms of size with respect to other competing technologies. The co-optimization of the process and the decoder design leads to minimizing the variability and the number of process steps.

On the other hand, the FDSOI-based nanowires are suitable for hard reconfiguration of generic logic gates in a crossbar organization. Thanks to their regularity and straight-forward connectivity to the rest of the CMOS chip, they can be used in regular architectures such as FPGA. The circuits implemented with this technology is a multiplexer, which is the basic bloc in a FPGA. It shows an interesting gain in terms of area and power consumption due to the compact crossbar design. A co-optimization of the process and the design allows for a significant improvement of the delay.

The vertically-stacked nanowires formed with the DRIE technique provide a compact solution for regular gate array design, since the driving requirements are met by exploiting the depth of the silicon. Three-dimensional logic gates that are based on this design paradigm show interesting trade-offs between the technology options. The considered circuits show a saving in terms of area and delay of logic gates compared with planar technology. Moreover, the DRIE Si nanowires can be envisaged for 3D crossbar design, for which the poly-Si wordlines are placed along the vertical direction.

7. CONCLUSIONS

We surveyed in this paper three different photolithography-based technologies that yield nanowire arrays. The spacer technique is useful for the fabrication of nanowires with a pitch below the photolithography limit. A pure FDSOI CMOS process enables the fabrication of arrays and the extraction of the parasitics affecting the nanowires. The DRIE-based nanowires offer the opportunity to vertically stack nanowires and thus reduce the device footprint.

We showed fabrication and simulation results related to these technologies. Then we highlighted the benefits of logic circuits designed specifically for these technologies. The spacer-based nanowire decoder offers for instance the densest size with respect to competing technologies. FDSOI-based crossbar multiplexers can be optimized with respect to the nanowire parasitics and offer a 1.4× lower power consumption and 6× lower area with respect to the CMOS implementation. By using DRIE-based nanowires, it is possible to vertically fold the physical implementation of logic gates, which reduces the delay by 8 to 26% with respect to the CMOS implementation.

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